

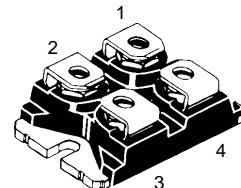
High Current Power MOSFET

N-Channel Enhancement Mode

	V_{DSS}	I_{D25}	$R_{DS(on)}$
IXFN 58N50	500V	58A	85 mΩ
IXFN 61N50	500V	61A	75 mΩ

Symbol	Test Conditions	Maximum Ratings		
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	500	V	
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1.0 \text{ M}\Omega$	500	V	
V_{GS}	Continuous	± 20	V	
V_{GSM}	Transient	± 30	V	
I_{D25}	$T_c = 25^\circ\text{C}$	IXFN 58N50 IXFN 61N50	58 61	A
I_{DM}	$T_c = 25^\circ\text{C}$ (1)	IXFN 58N50 IXFN 61N50	232 244	A
P_D	$T_c = 25^\circ\text{C}$	625	W	
T_J		-40 ... +150	$^\circ\text{C}$	
T_{JM}		150	$^\circ\text{C}$	
T_{stg}		-40 ... +150	$^\circ\text{C}$	
V_{ISOL}	50/60 Hz, RMS	$t = 1 \text{ minute}$	2500	V~
		$t = 1\text{s}$	3000	V~
M_d	Mounting torque	1.5/13	Nm/lb.in.	
	Terminal connection torque (M4)	1.5/13	Nm/lb.in.	
Weight		30	g	
E_{AR}		75	mJ	

Symbol	Test Conditions	Characteristic Values		
		($T_J = 25^\circ\text{C}$ unless otherwise specified)		
		Min.	Typ.	Max.
V_{DSS}	$V_{GS} = 0 \text{ V}$, $I_D = 5 \text{ mA}$	500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 12 \text{ mA}$	1.7	4.0	V
I_{GSS}	$V_{GS} = \pm 20 \text{ V DC}$, $V_{DS} = 0$		± 200	nA
I_{DSS}	$V_{DS} = 0.8 V_{DSS}$ $V_{GS} = 0 \text{ V}$	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$	500 2	μA mA
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$, $I_D = 0.5 I_{D25}$	58N50 61N50		85 mΩ 75 mΩ
	Pulse test, $t \leq 300 \mu\text{s}$, duty cycle $\leq 2 \%$			

miniBLOC, SOT-227 B

1 = Source 2 = Gate
3 = Drain 4 = Source

Features

- International standard package
- Isolation voltage 3000V (RMS)
- Low $R_{DS(on)}$ HDMOS™ process¹
- Rugged polysilicon gate cell structure
- Low drain-to-case capacitance (<60 pF)
 - reduced RFI
- Low package inductance (< 10 nH)
 - easy to drive and to protect
- Aluminium Nitride Isolation
 - increased current ratings

Applications

- DC choppers
- AC motor speed controls
- DC servo and robot drives
- Uninterruptible power supplies (UPS)
- Switched mode and resonant mode power supplies

Advantages

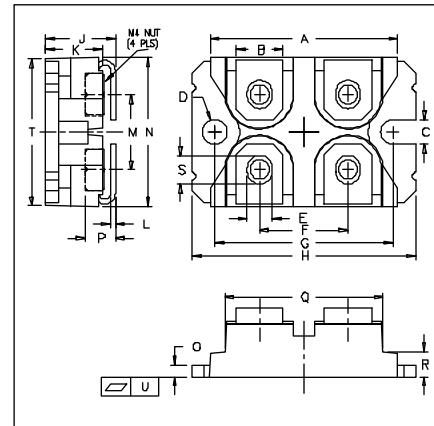
- Easy to mount
- Space savings
- High power density

Symbol	Test Conditions	Characteristic Values			
		($T_J = 25^\circ\text{C}$ unless otherwise specified)	Min.	Typ.	Max.
g_{fs}	$V_{DS} = 10 \text{ V}; I_D = 0.5 I_{D25}$, pulse test	20	30	S	
C_{iss}	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$	11		nF	
C_{oss}		1550		pF	
C_{rss}		225		pF	
$t_{d(on)}$	$V_{GS} = 10 \text{ V}, V_{DS} = 0.5 V_{DSS}, I_D = 50 \text{ A}$	30		ns	
t_r	$R_G = 1 \Omega$ (External)	60		ns	
$t_{d(off)}$		100		ns	
t_f		50		ns	
Q_g	$V_{GS} = 10 \text{ V}, V_{DS} = 0.5 V_{DSS}, I_D = I_{D25}$	420		nC	
Q_{gs}		55		nC	
Q_{gd}		160		nC	
R_{thJC}			0.20	K/W	
R_{thCK}		0.05		K/W	

Source-Drain Diode**Ratings and Characteristics**
($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Test Conditions	Min.	Typ.	Max.	INCHES		MILLIMETERS	
					MIN.	MAX.	MIN.	MAX.
I_s	$V_{GS} = 0$		61	A				
I_{SM}	Repetitive; pulse width limited by T_{JM}		244	A				
V_{SD}	$I_F = I_s, V_{GS} = 0 \text{ V}$, Pulse test, $t \leq 300 \mu\text{s}$, duty cycle $\leq 2 \%$		1.5	V				
t_{rr}	$I_F = 50 \text{ A}, di/dt = -100 \text{ A}/\mu\text{s}, V_R = 100 \text{ V}$		250	ns				

Notes: 1. Pulse width limited by max T_J .
 2. $I_F \leq I_{DM}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$, $R_G = 2\Omega$.

Package Outline

SYM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	1.240	1.255	31.50	31.88
B	.307	.323	7.80	8.20
C	.161	.169	4.09	4.29
D	.161	.169	4.09	4.29
E	.161	.169	4.09	4.29
F	.587	.595	14.91	15.11
G	1.186	1.193	30.12	30.30
H	1.496	1.505	38.00	38.23
J	.460	.481	11.68	12.22
K	.351	.378	8.92	9.60
L	.030	.033	0.76	0.84
M	.496	.506	12.60	12.85
N	.990	1.001	25.15	25.42
O	.078	.084	1.98	2.13
P	.195	.235	4.95	5.97
Q	1.045	1.059	26.54	26.90
R	.155	.174	3.94	4.42
S	.186	.191	4.72	4.85
T	.968	.987	24.59	25.07
U	-.002	.004	-0.05	0.1

The data supplied herein reflects the pre-production objective specification and characterization from engineering lots.
 IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,881,106	5,017,508	5,049,961	5,187,117	5,486,715
4,850,072	4,931,844	5,034,796	5,063,307	5,237,481	5,381,025