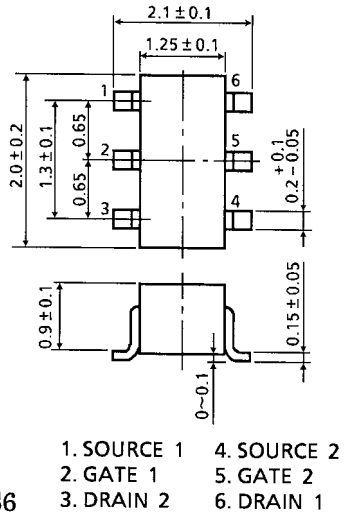
TOSHIBA Field Effect Transistor Silicon N·P Channel MOS Type

HN1L03FU

High Speed Switching Applications
Analog Switch Applications

Unit in mm



JEDEC	—
EIAJ	—
TOSHIBA	2-2J1C

Weight: 6.8mg

Q1, Q2 common

- Low threshold voltage
  Q1: V_{th} = 0.8~2.5V Q2: V_{th} = −0.5~−1.5V
- High speed
- Small package

Q1 Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Drain-Source voltage	V_{DS}	50	V
Gate-Source voltage	V_{GSS}	10	V
Drain current	I_D	50	mA

Q2 Maximum Ratings (Ta = 25°C)

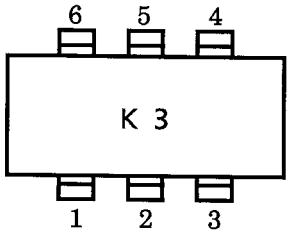
Characteristic	Symbol	Rating	Unit
Drain-Source voltage	V_{DS}	−20	V
Gate-Source voltage	V_{GSS}	−7	V
Drain current	I_D	−50	mA

Maximum Ratings (Q1, Q2 Common) (Ta = 25°C)

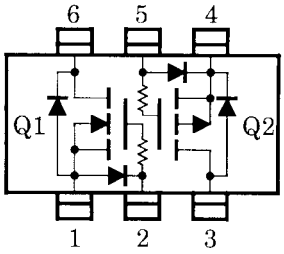
Characteristic	Symbol	Rating	Unit
Drain power dissipation	P_{D*}	200	mW
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	−55~150	°C

* Total rating

Marking



Equivalent Circuit (Top View)



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Q1 Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = 10V, V_{DS} = 0	—	—	1	μA
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 100μA, V_{GS} = 0	50	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = 50V, V_{GS} = 0	—	—	1	μA
Gate threshold voltage		V_{th}	V_{DS} = 5V, I_D = 0.1mA	0.8	—	2.5	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 5V, I_D = 10mA	20	—	—	mS
Drain-Source ON resistance		$R_{DS\ (ON)}$	I_D = 10mA, V_{GS} = 4.0V	—	20	50	Ω
Input capacitance		C_{iss}	V_{DS} = 5V, V_{GS} = 0, f = 1MHz	—	6.3	—	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = 5V, V_{GS} = 0, f = 1MHz	—	1.3	—	pF
Output capacitance		C_{oss}	V_{DS} = 5V, V_{GS} = 0, f = 1MHz	—	5.7	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = 5V, I_D = 10mA, V_{GS} = 0~4.0V	—	0.11	—	μs
	Turn-off time	t_{off}	V_{DD} = 5V, I_D = 10mA, V_{GS} = 0~4.0V	—	0.15	—	μs

Q2 Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = −7V, V_{DS} = 0	—	—	−1	μA
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −100μA, V_{GS} = 0	−20	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = −20V, V_{GS} = 0	—	—	−1	μA
Gate threshold voltage		V_{th}	V_{DS} = −3V, I_D = −0.1mA	−0.5	—	−1.5	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −3V, I_D = −10mA	15	—	—	mS
Drain-Source ON resistance		$R_{DS\ (ON)}$	I_D = −10mA, V_{GS} = −2.5V	—	20	40	Ω
Input capacitance		C_{iss}	V_{DS} = −3V, V_{GS} = 0, f = 1MHz	—	10.4	—	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = −3V, V_{GS} = 0, f = 1MHz	—	2.8	—	pF
Output capacitance		C_{oss}	V_{DS} = −3V, V_{GS} = 0, f = 1MHz	—	8.4	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = −3V, I_D = −10mA, V_{GS} = 0~−2.5V	—	0.15	—	μs
	Turn-off time	t_{off}	V_{DD} = −3V, I_D = −10mA, V_{GS} = 0~−2.5V	—	0.13	—	μs

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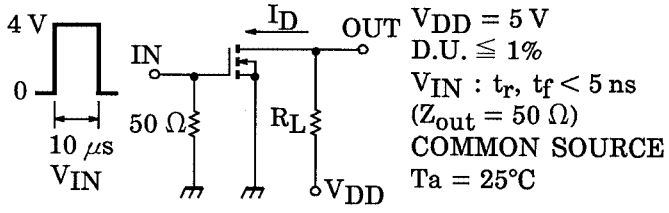
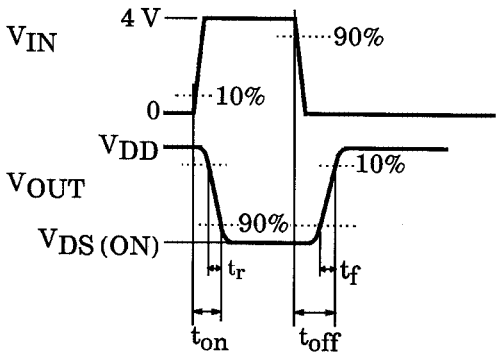
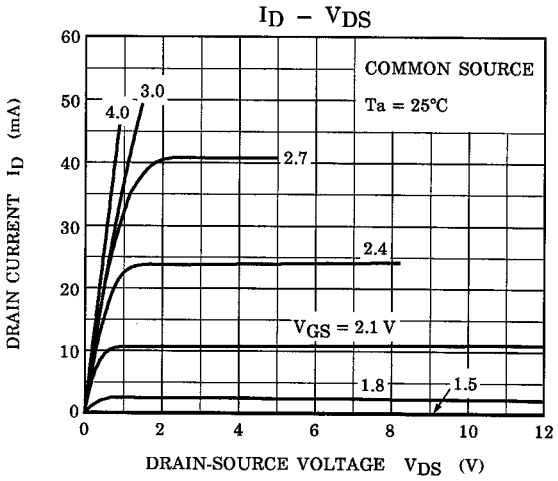
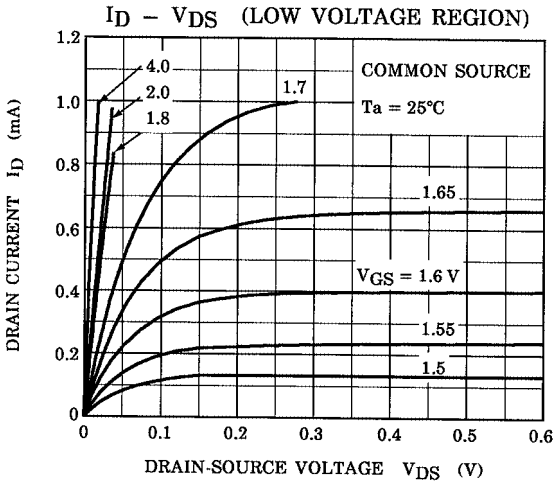
Q1 (Nch MOS FET)

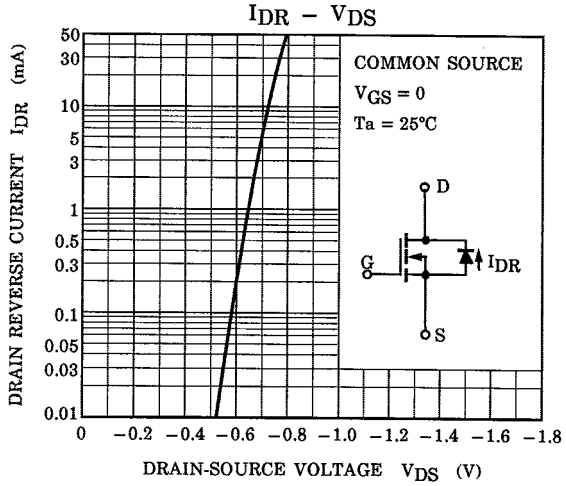
Switching Time Test Circuit

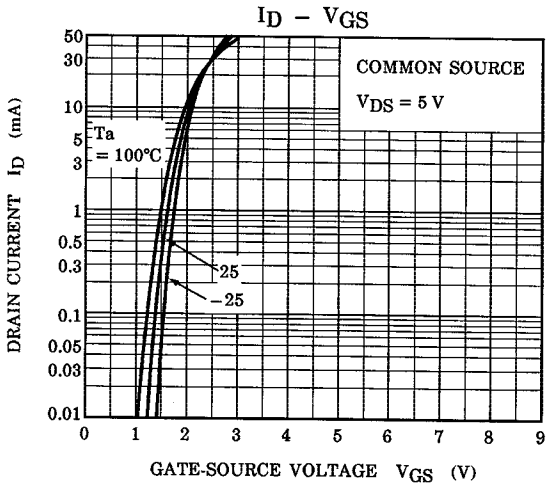






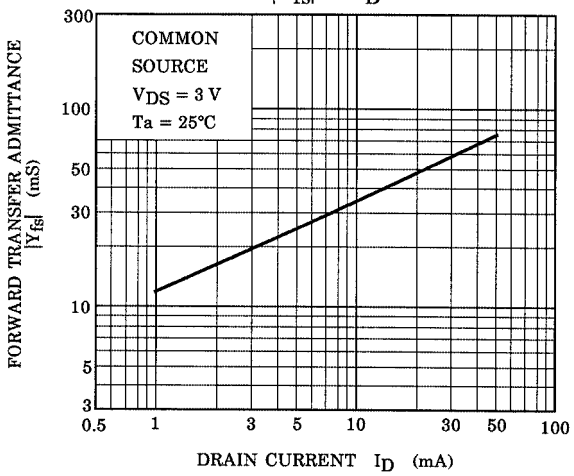




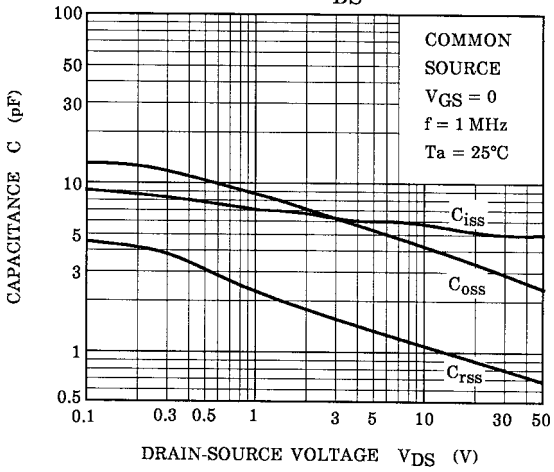


Q1 (Nch MOS FET)

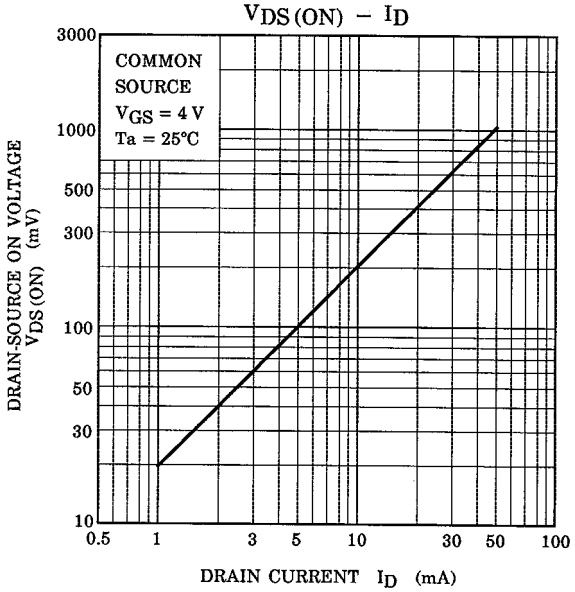
$|Y_{fs}|$ – I_D



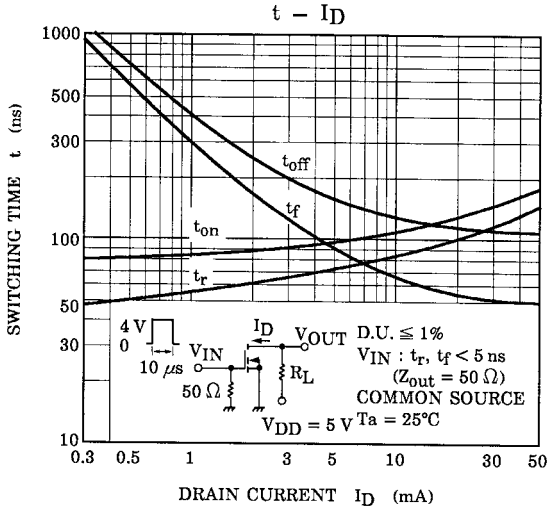
C – V_{DS}



$V_{DS\,(ON)}$ – I_D

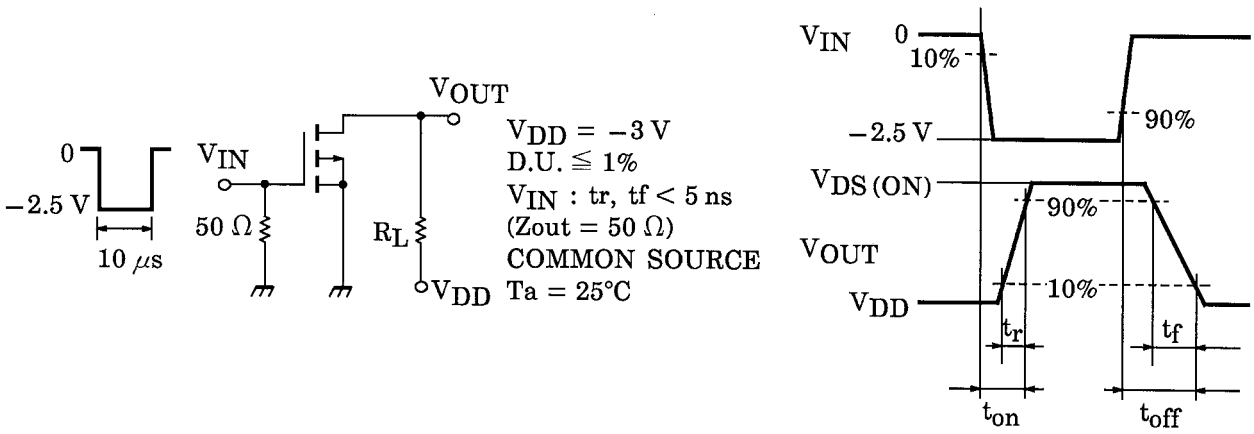


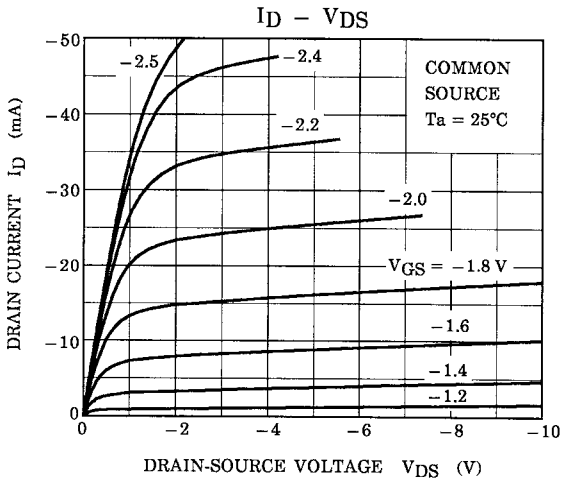
t – I_D

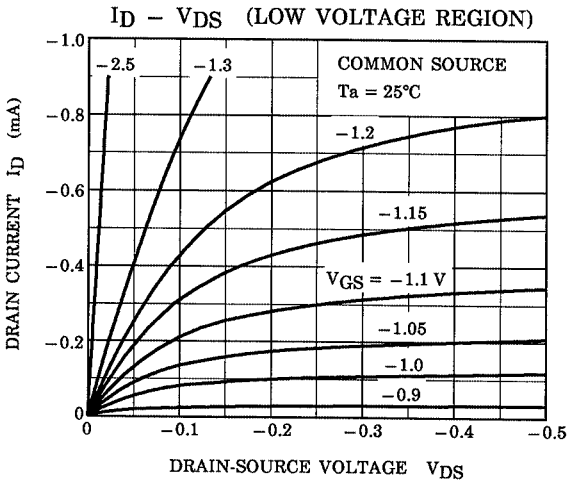


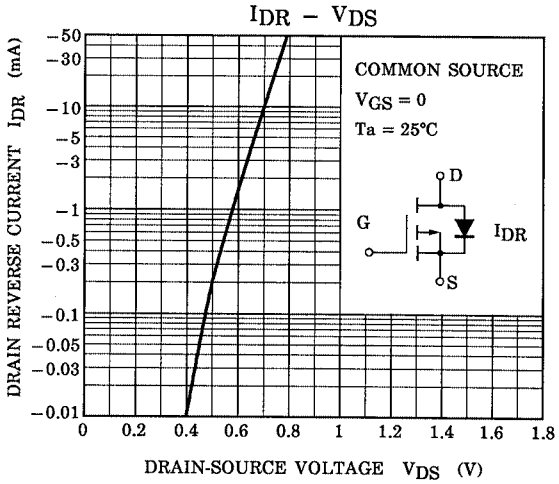
Q2 (Pch MOS FET)

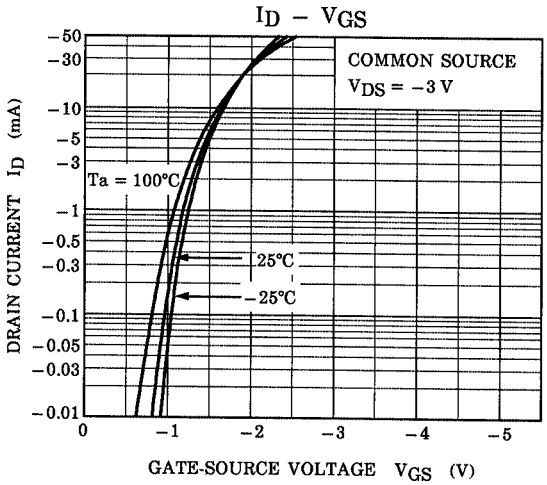
Switching Time Test Circuit





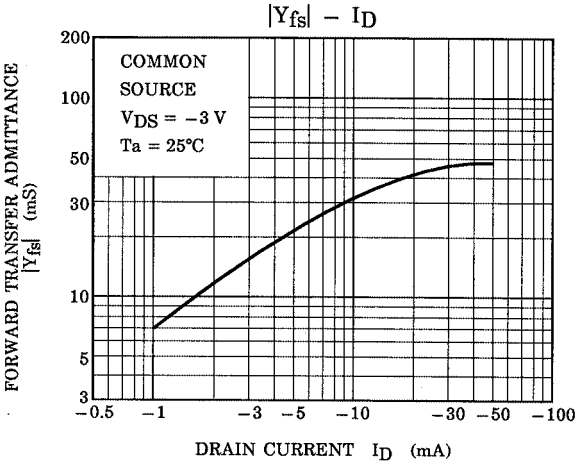




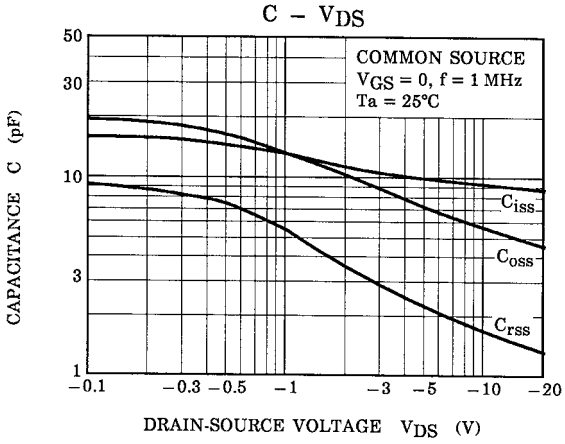


Q2 (Pch MOS FET)

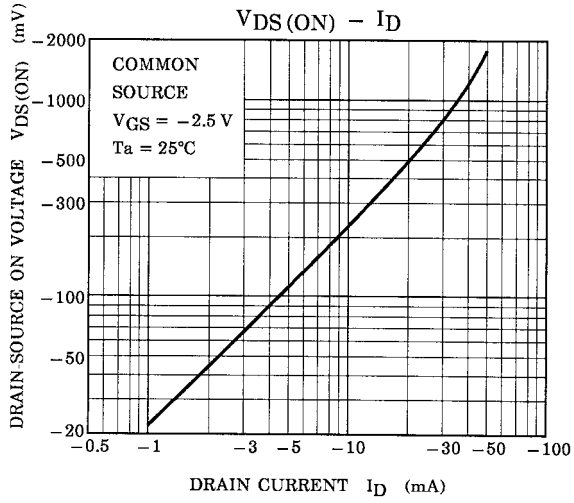
$|Y_{fs}| - I_D$



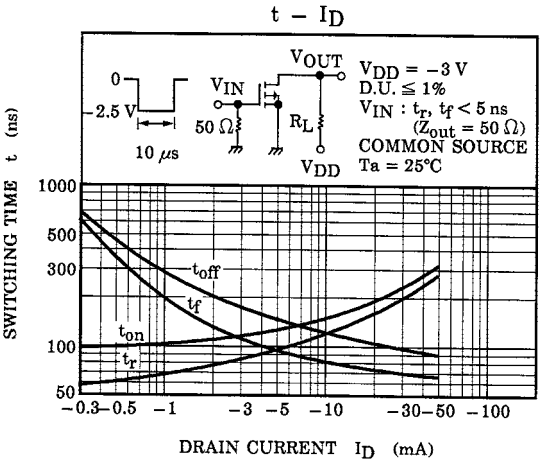
$C - V_{DS}$



$V_{DS(ON)} - I_D$

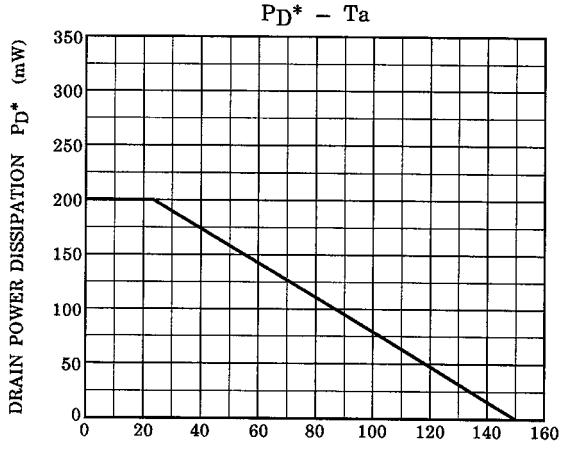


$t - I_D$



(Q1, Q2 common)

$P_D^* - Ta$



* : Total Rating