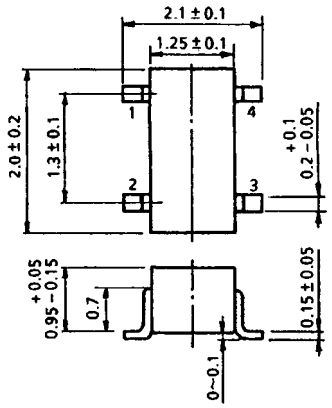
TOSHIBA Field Effect Transistor Silicon N Channel Dual Gate MOS Type

3SK256

TV Tuner, UHF RF Amplifier Applications

- Superior cross modulation performance.
- Low reverse transfer capacitance: C_{rss} = 0.015 pF (typ.)
- Low noise figure: NF = 1.9dB (typ.)

Unit: mm



1. GATE 1
2. GATE 2
3. DRAIN
4. SOURCE

USQ

JEDEC	—
JEITA	—
TOSHIBA	2-2K1B

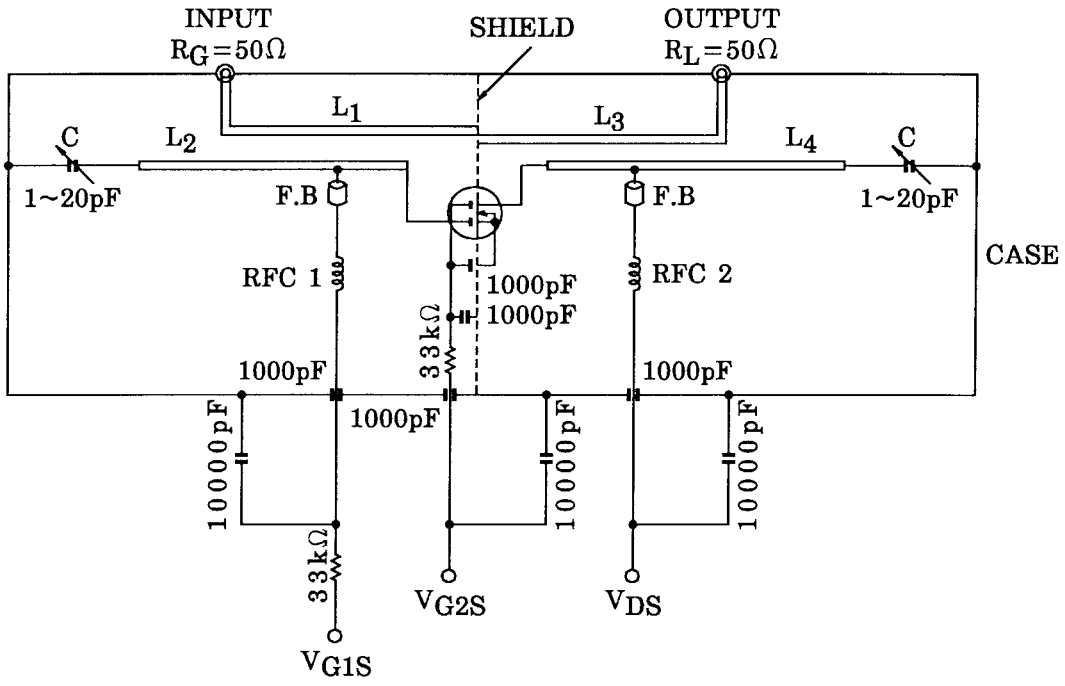
Weight: 0.006 g (typ.)

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DS}	13.5	V
Gate 1-source voltage	V_{G1S}	±8	V
Gate 2-source voltage	V_{G2S}	±8	V
Drain current	I_D	30	mA
Drain power dissipation	P_D	100	mW
Channel temperature	T_{ch}	125	°C
Storage temperature range	T_{stg}	−55~125	°C

Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate 1 leakage current	I_{G1SS}	V_{DS} = 0, V_{G1S} = ±6 V, V_{G2S} = 0	—	—	±50	nA
Gate 2 leakage current	I_{G2SS}	V_{DS} = 0, V_{G1S} = 0, V_{G2S} = ±6 V	—	—	±50	nA
Drain-source voltage	$V_{(BR)\ DSX}$	V_{G1S} = −1 V, V_{G2S} = −1 V I_D = 100 μA	13.5	—	—	V
Drain current	I_{DSS}	V_{DS} = 6 V, V_{G1S} = 0, V_{G2S} = 4.5 V	0	—	0.1	mA
Gate 1-source cut-off voltage	$V_{G1S\ (OFF)}$	V_{DS} = 6 V, V_{G2S} = 4.5 V, I_D = 100 μA	0	—	1.0	V
Gate 2-source cut-off voltage	$V_{G2S\ (OFF)}$	V_{DS} = 6 V, V_{G1S} = 4 V, I_D = 100 μA	0.5	1.0	1.5	V
Forward transfer admittance	$\lvert Y_{fs} \rvert$	V_{DS} = 6 V, V_{G2S} = 4.5 V I_D = 10 mA, f = 1 kHz	—	21.5	—	mS
Input capacitance	C_{iss}	V_{DS} = 6 V, V_{G2S} = 4.5 V I_D = 10 mA, f = 1 MHz	1.0	1.6	2.4	pF
Reverse transfer capacitance	C_{rss}		—	0.015	0.03	pF
Power gain	G_{ps}	V_{DS} = 6 V, V_{G2S} = 4.5 V I_D = 10 mA, f = 800 MHz	18	19.5	—	dB
Noise figure	NF		—	1.9	3.0	dB



L_1~L_4: ϕ0.8 mm silver plated copper wire

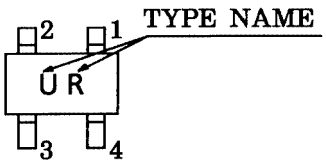
C: Air trimmer TTA25A200A (MURATA Manufacturing, Co., Ltd.)

RFC 1: ϕ0.35 mm copper wire 3 mm ID, 7 T

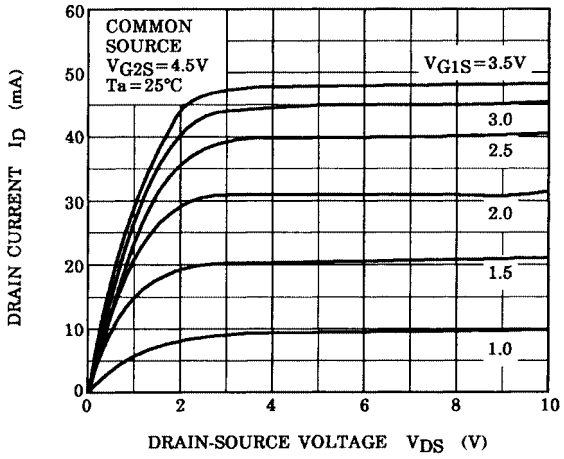
RFC 2: ϕ0.35 mm copper wire 3 mm ID, 10 T

Figure 1 G_{PS}, NF Test Circuit

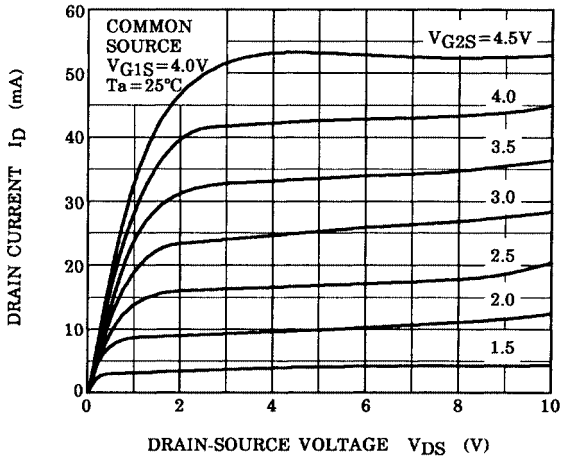
Marking



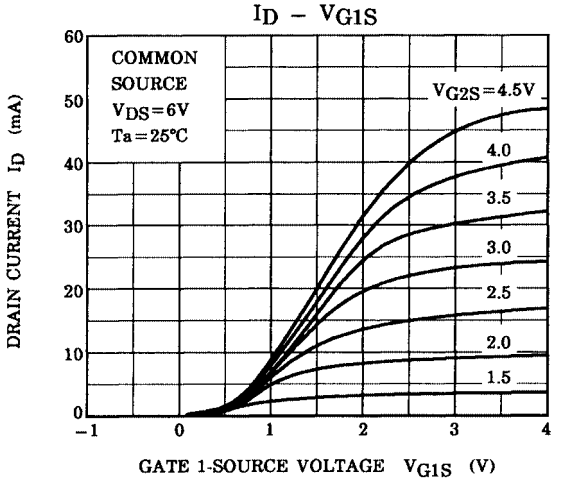
I_D – V_{DS}



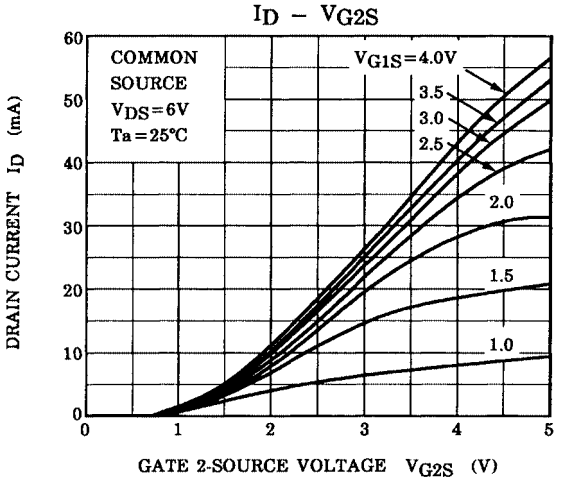
I_D – V_{DS}



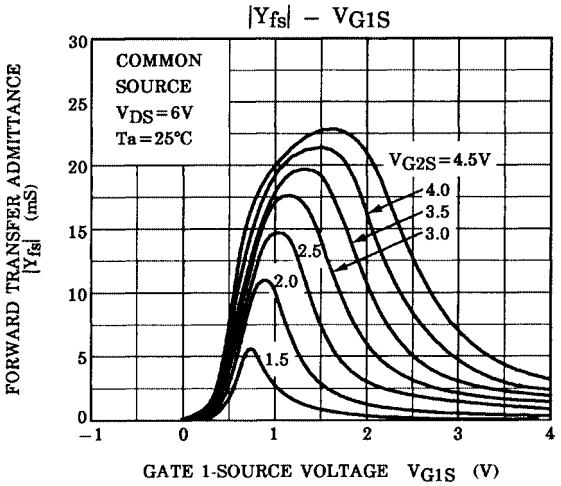
I_D – V_{G1S}



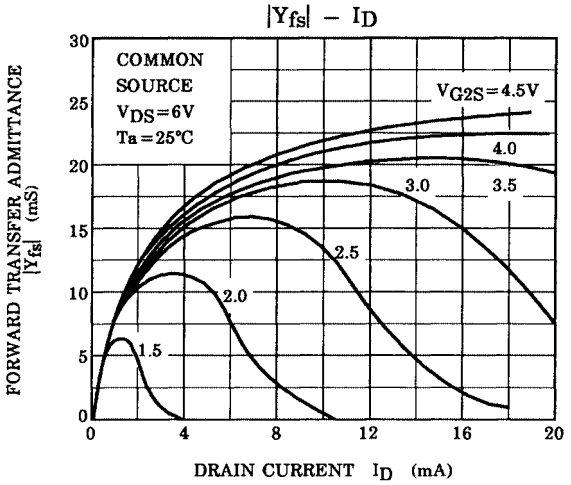
I_D – V_{G2S}



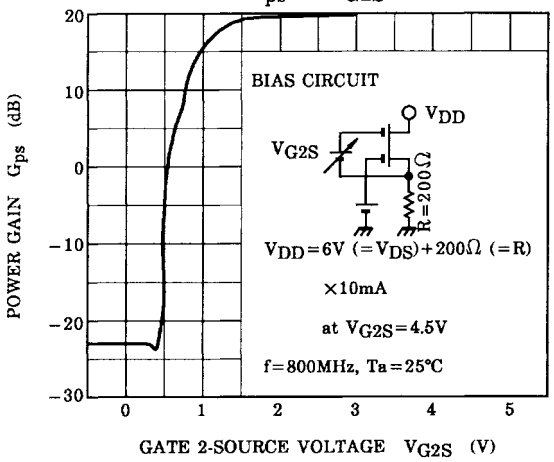
$|Y_{fs}|$ – V_{G1S}



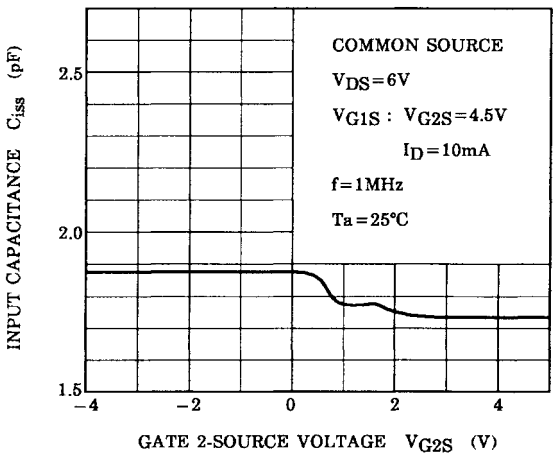
$|Y_{fs}|$ – I_D



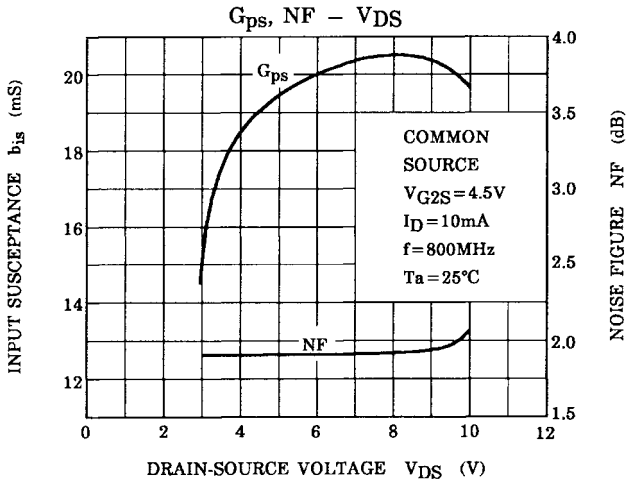
G_{ps} – V_{G2S}



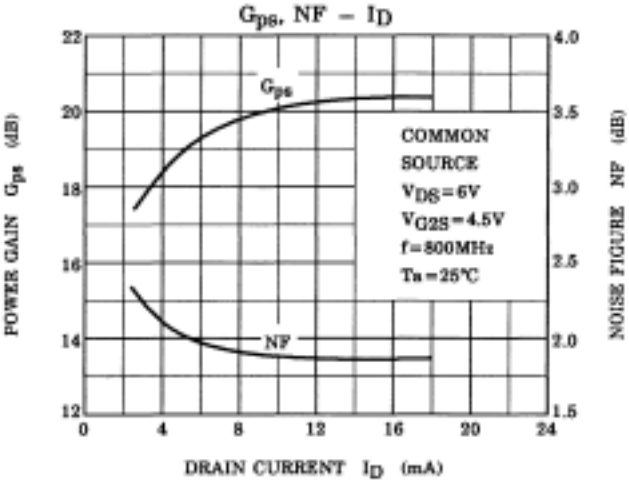
C_{iss} – V_{G2S}



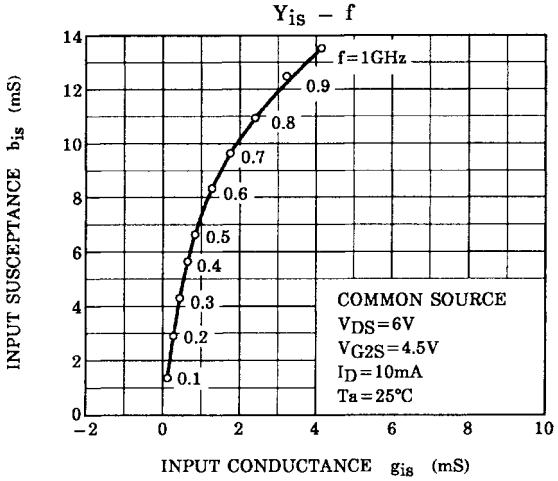
G_{ps}, NF – V_{DS}



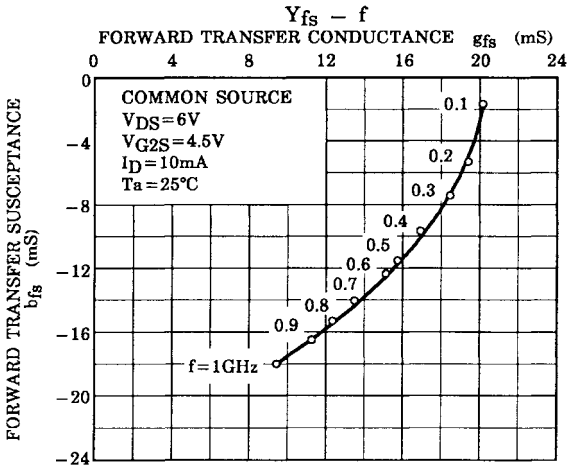
G_{ps}, NF – I_D



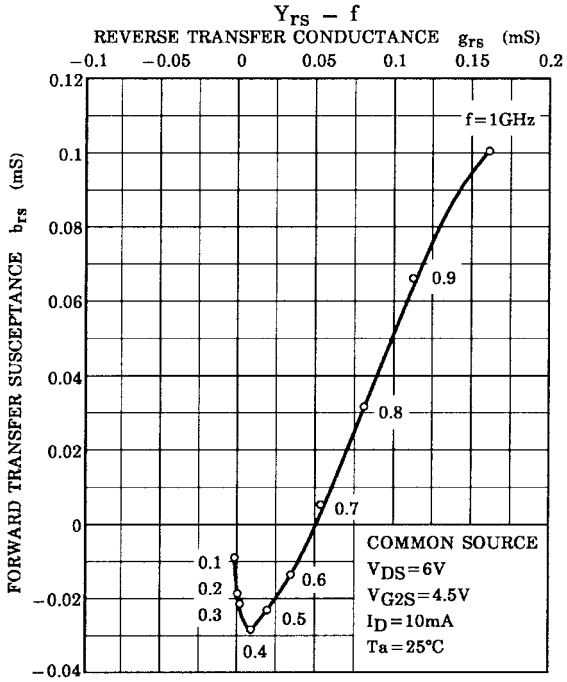
Y_{is} – f



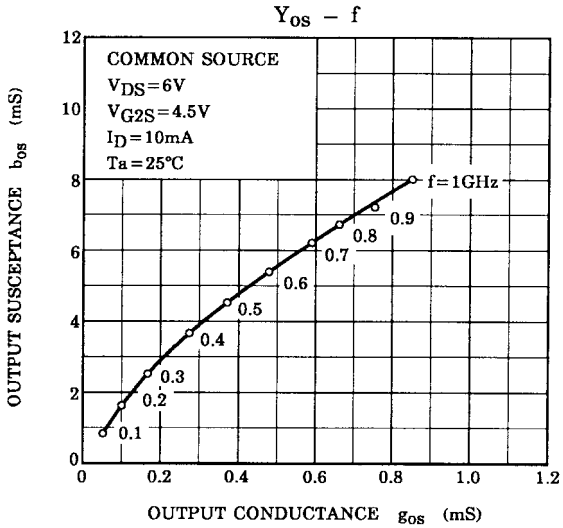
Y_{fs} – f



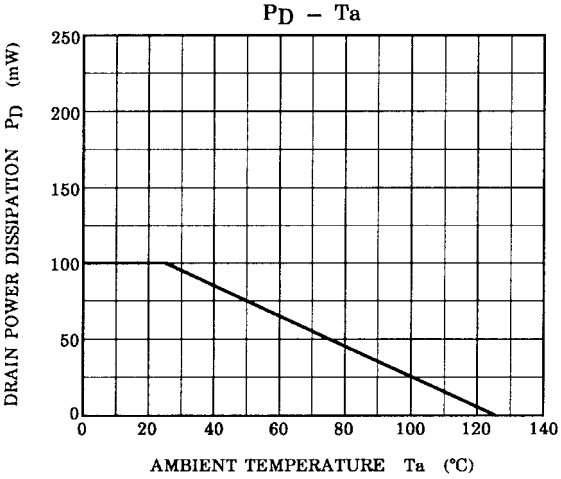
Y_{rs} – f



Y_{os} – f



P_D – Ta



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