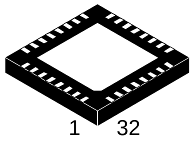
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

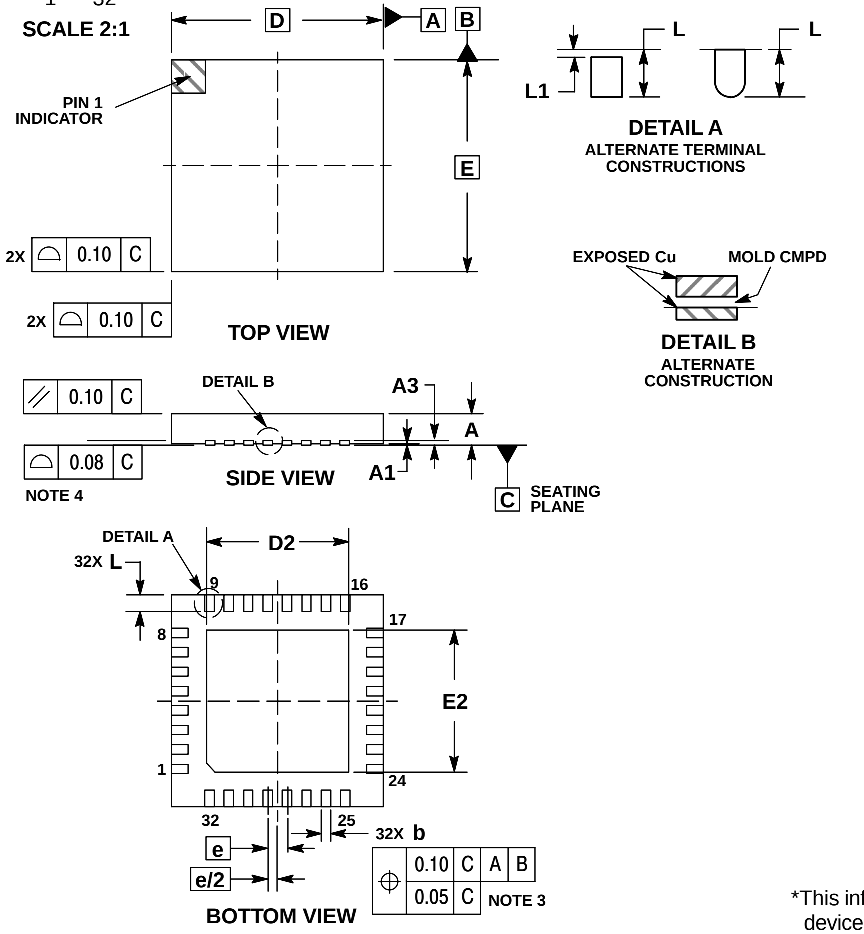
ON Semiconductor®



SCALE 2:1

QFN32 7x7, 0.65P
CASE 485ED
ISSUE A

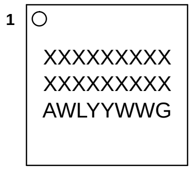
DATE 09 JUL 2015



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	0.90
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	7.00 BSC	
D2	4.60	4.80
E	7.00 BSC	
E2	4.60	4.80
e	0.65 BSC	
L	0.45	0.65
L1	0.00	0.15

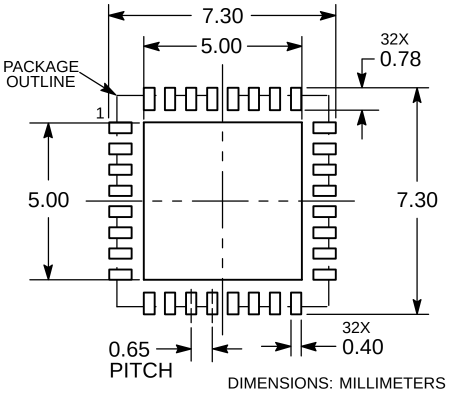
GENERIC MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

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STATUS:	**ON SEMICONDUCTOR STANDARD**	
NEW STANDARD:		
DESCRIPTION:	**QFN32 7X7, 0.65MM PITCH**	**PAGE 1 OF 2**

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY D. TRUHITTE.	29 JUN 2013
A	REDREW TO ON SEMICONDUCTOR AND JEDEC STANDARDS. REQ. BY B. BLAUER.	09 JUL 2015

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