BURR - BROWN®

VSP2101

SpeedPLUS™ CCD SIGNAL PROCESSOR For Digital Cameras

FEATURES

- **CCD SIGNAL PROCESSING:**
  Correlated Double Sampling
  Black Level Clamping
  –2 to +34dB Gain Ranging
  High SNR: 53dB
- **10-BIT A/D CONVERSION:**
  Up to 27MHz Conversion Rate
  No Missing Codes
- **PORTABLE OPERATION:**
  Low Voltage: 2.7V to 3.6V
  Low Power: 190mW at 3.0V
- **LOW POWER: 160mW at 2.7V**
- **POWER-DOWN MODE: 18mW**

APPLICATIONS

- **VIDEO CAMERAS**
- **DIGITAL STILL CAMERAS**
- **PC CAMERAS**
- **SECURITY CAMERAS**

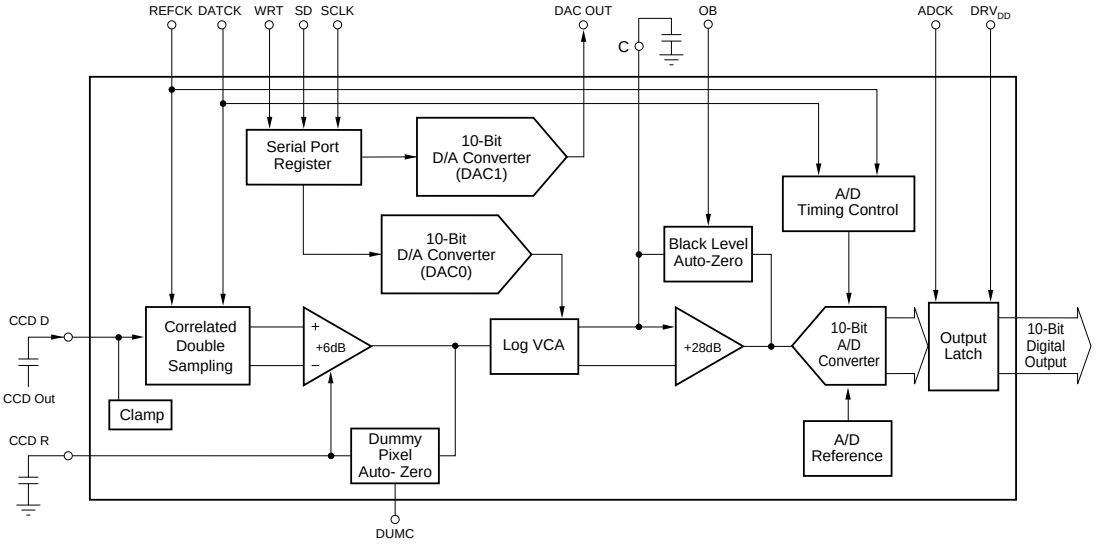
DESCRIPTION

The VSP2101Y is a complete digital camera IC, providing signal conditioning and 10-bit analog-to-digital conversion for the output of a CCD array.

The primary CCD channel provides correlated double sampling to extract the video information from the pixels, –2dB to +34dB gain ranging with digital control for varying illumination conditions, and black level clamping for an accurate black reference.

Input signal clamping and offset correction of the CDS is also performed. The stable gain control is linear in dB. Additionally, the black level is quickly recovered after gain change. An on-chip general purpose 10-bit digital-to-analog converter allows you to obtain analog control voltage for iris control.

The VSP2101Y is available in a 48-lead LQFP package and operates from a single +3V supply.



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SPECIFICATIONS

At T_A = +25°C, all power supply voltages = +3.0V, and conversion rate = 18MHz, unless otherwise specified.

PARAMETER	CONDITIONS	VSP2101Y			UNITS
		MIN	TYP	MAX	
RESOLUTION			10		Bits
DIGITAL INPUT					
Logic Family			CMOS		
Logic Levels	Logic HI	2.5			V
	Logic LO			+0.4	V
Logic Currents	Logic HI, V_{IN} = +3V			10	µA
	Logic LO, V_{IN} = 0V			10	µA
A/D Clock Duty Cycle			50		%
Input Capacitance			5		pF
DIGITAL OUTPUT					
Logic Family			CMOS		
Logic Levels	Logic HI, C_L = 10pF	2.5			V
	Logic LO, C_L = 10pF			+0.4	V
ANALOG OUTPUT					
General Purpose D/A Converter Output					
Minimum Output Voltage	Control Data = 1023		0.3		V
Maximum Output Voltage	Control Data = 0		2.4		V
DAC Settling TIme			1.0		µs
TRANSFER CHARACTERISTICS					
Differential Non-Linearity			±0.5		LSB
Integral Non-Linearity			2.0		LSB
No Missing Codes			Guaranteed		
Signal Settling Time	Black to Full-Scale Change to 1/4 LSB into A/D			110	ns
Conversion Rate		500kHz		27	MHz
Data Latency			5.5		Clocks
Signal-to-Noise Ratio[1]	Grounded Input Cap, Maximum Gain		53		dB
CCD Offset Correction Range			±150		mV
Black Clamp Level			32		LSB
CDS					
Data Settling Time to ±0.1% for FS Change with R_S = 40	From Leading Edge of DATCK		11		ns
Input Signal Level for FS Out	Minimum Gain	600			mV
Input Capacitance	DATCK LOW		20		pF
Input Time Constant			300		ps
INPUT CLAMP					
Clamp-On Resistance			3.3		kΩ
Clamp Level			1.2		V
GAIN CONTROL CHARACTERISTICS					
Gain, max	Control Data = 0	32	34		dB
Gain, min	Control Data = 1023		–2		dB
Gain Control Linearity			±1.0		dB
Gain Control Settling Time			10		µs
POWER SUPPLY					
Rated Voltage		+2.7	+3.0	+3.6	V
Quiescent Current			63		mA
Power Dissipation			190		mW
Power-Down Mode			18		mW
TEMPERATURE RANGE					
Specified Range	Ambient	–25		+85	°C
Thermal Resistance, θ_{JA}					
48-Lead LQFP			100		°C/W

NOTE: (1) SNR = 20log (full-scale voltage/rms noise).

ABSOLUTE MAXIMUM RATINGS

Power Supply ($+V_S$)	+6V
Analog Input	–0.3V to ($+V_S$ +0.3V)
Logic Input	–0.3V to ($+V_S$ +0.3V)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	–40°C to +150°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

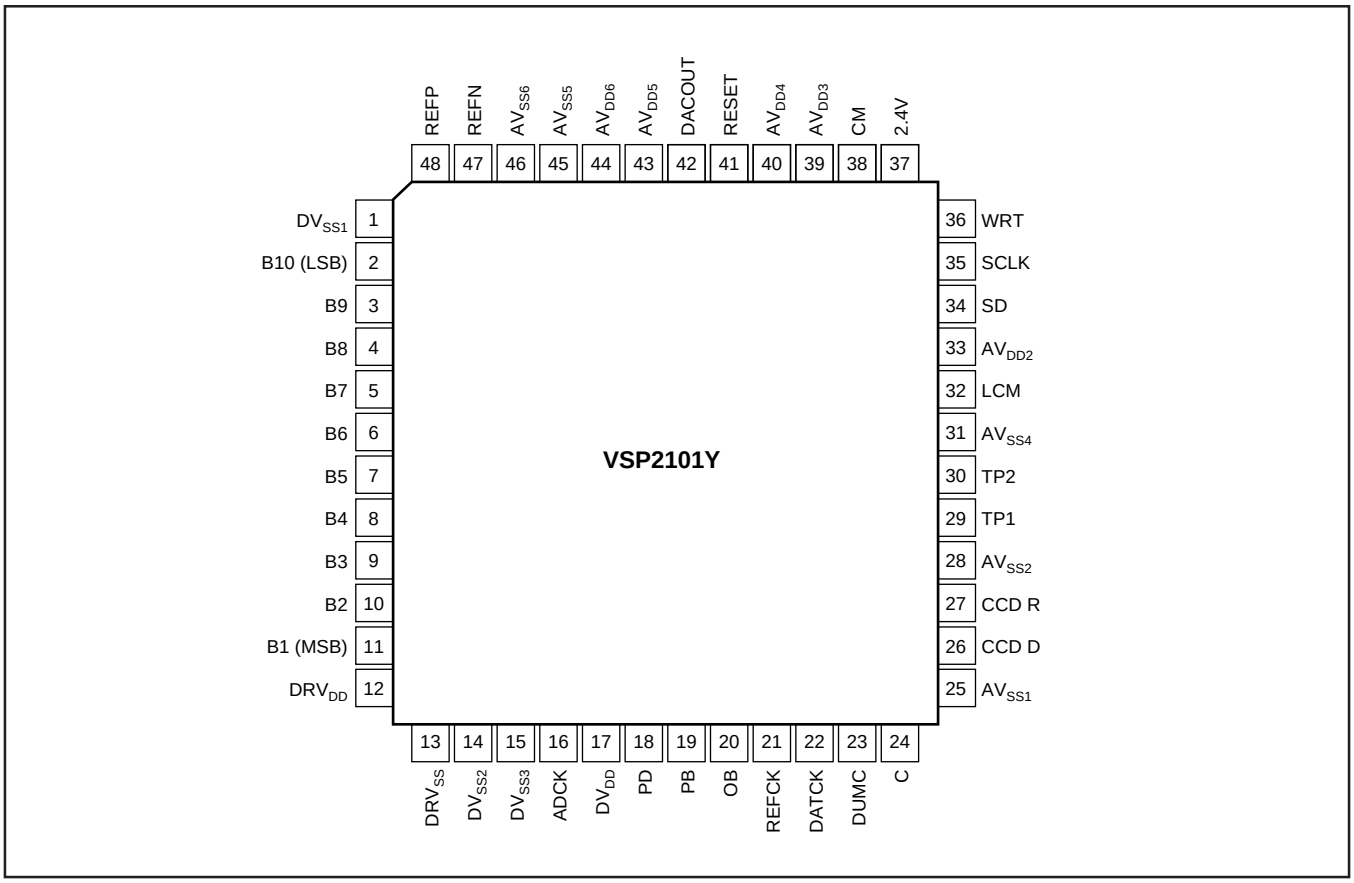
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(2)	TRANSPORT MEDIA
VSP2101Y	48-Lead LQFP	340	–25°C to +85°C	VSP2101Y	VSP2101Y	50-Piece Tray
"	"	"	"	"	VSP2101Y/2K	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of "VSP2101Y/2K" will get a single 1000-piece Tape and Reel.

PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION	PIN	DESIGNATOR	DESCRIPTION
1	DV_{SS1}	Digital Ground	24	C	Capacitor for Optical Feedback Loop
2	B10 (LSB)	Bit 10, ADC Output, Least Significant Bit	25	AV_{SS1}	Analog Ground
3	B9	Bit 9, ADC Output	26	CCD D	CCD Signal Input
4	B8	Bit 8, ADC Output	27	CCD R	Capacitor for Dummy Feedback Loop
5	B7	Bit 7, ADC Output	28	AV_{SS2}	Analog Ground
6	B6	Bit 6, ADC Output	29	TP1	Test Pin 1, Open
7	B5	Bit 5, ADC Output	30	TP2	Test Pin 2, Open
8	B4	Bit 4, ADC Output	31	AV_{SS4}	Analog Ground
9	B3	Bit 3, ADC Output	32	LCM	Attenuator Common-Mode Bypass
10	B2	Bit 2, ADC Output	33	AV_{DD2}	Analog Power Supply
11	B1 (MSB)	Bit 1, ADC Output, Most Significant Bit	34	SD	Serial Data Input for D/A Converters
12	DRV_{DD}	Digital Power Supply for Digital Outputs (B1-B10)	35	SCLK	Clock for Serial Data Input
13	DRV_{SS}	Digital Ground for Digital Outputs (B1-B10)	36	WRT	Write Pulse for Serial Data Input, Rising Edge Trigger
14	DV_{SS2}	Digital Ground	37	2.4V	Attenuator Ladder Bypass
15	DV_{SS3}	Digital Ground	38	CM	ADC Common-Mode Voltage
16	ADCK	Clock for Digital Data Output Latch	39	AV_{DD3}	Analog Power Supply
17	DV_{DD}	Digital Power Supply	40	AV_{DD4}	Analog Power Supply
18	PD	Power Down: LOW = Normal Operation	41	RESET	Resets DAC Registers, Active LOW
		HIGH = Reduced Power (digital	42	DACOUT	D/A Converter (DAC1) Output
		output= 0000000000)	43	AV_{DD5}	Analog Power Supply
19	PB	Preblanking: LOW = ADC Output: –FS +32LSB	44	AV_{DD6}	Analog Power Supply
		HIGH = ADC Output: Normal	45	AV_{SS5}	Analog Ground
20	OB	Optical Black Clamp Pulse, Active LOW	46	AV_{SS6}	Analog Ground
21	REFCK	CDS Reference Sampling Pulse, Active LOW	47	REFN	ADC Negative Reference, Bypass to Ground
22	DATCK	CDS Data Sampling Pulse, Active LOW	48	REFP	ADC Positive Reference, Bypass to Ground
23	DUMC	Dummy Clamp, Active LOW			

SERIAL CONTROL DATA FORMAT FOR DAC0/DAC1

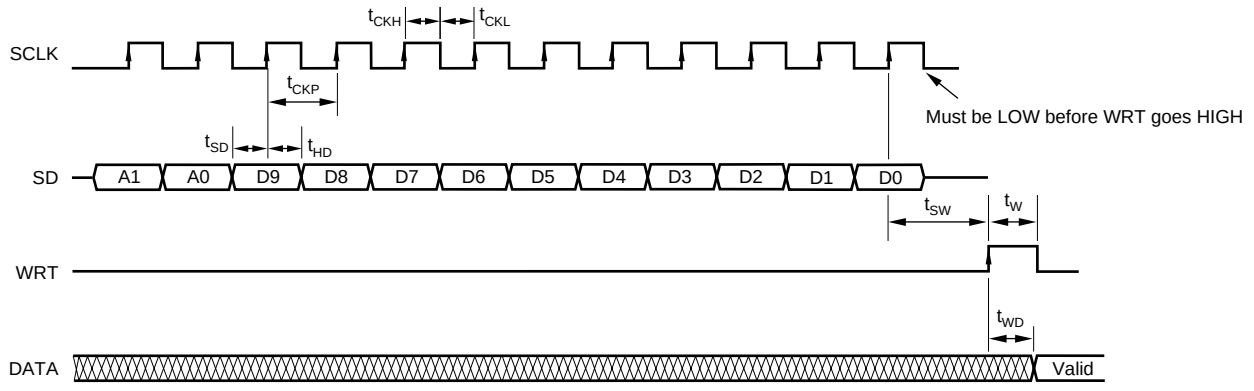
BIT NO.	DESIGNATOR	DESCRIPTION
1	A1	Start Bit. Either HIGH or LOW will be acceptable.
2	A0	Address Bit. Selects internal DACs. LOW = DAC0, VGA control DAC HIGH = DAC1, general purpose DAC
3	D9	Digital Input Data for DAC, Bit 10 (MSB)
4	D8	Digital Input Data for DAC, Bit 9
5	D7	Digital Input Data for DAC, Bit 8
6	D6	Digital Input Data for DAC, Bit 7
7	D5	Digital Input Data for DAC, Bit 6
8	D4	Digital Input Data for DAC, Bit 5
9	D3	Digital Input Data for DAC, Bit 4
10	D2	Digital Input Data for DAC, Bit 3
11	D1	Digital Input Data for DAC, Bit 2
12	D0	Digital Input Data for DAC, Bit 1 (LSB)

TIMING SPECIFICATIONS FOR SERIAL REGISTERS

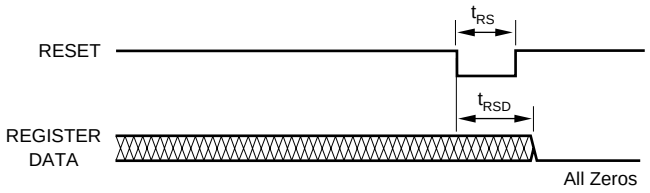
Timing Specifications = t_{MIN} to t_{MAX} with +3V power supply.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{CKP}	Serial Clock Period	100			ns
t_{CKL}	Serial Clock Pulse Width LOW	50			ns
t_{CKH}	Serial Clock Pulse Width HIGH	50			ns
t_{SD}	Data Setup Time	50			ns
t_{HD}	Data Hold Time	25			ns
t_{SW}	Write Pulse Setup Time	100			ns
t_W	Write Pulse Width	50			ns
t_{WD}	Data Valid Delay Time	50			ns
t_{RS}	Register Reset Pulse Width	50			ns
t_{RSD}	Register Reset Delay Time	50			ns

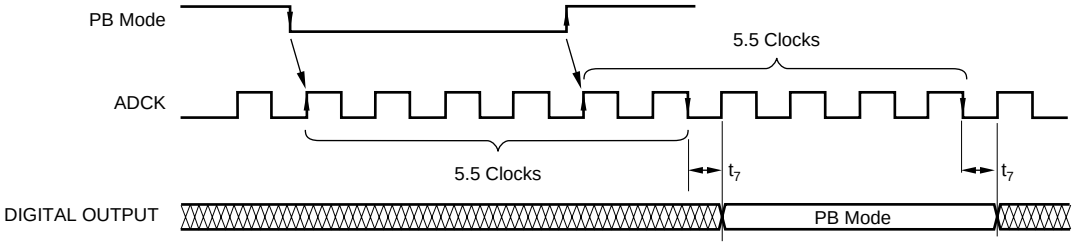
TIMING FOR SERIAL PORT WRITING



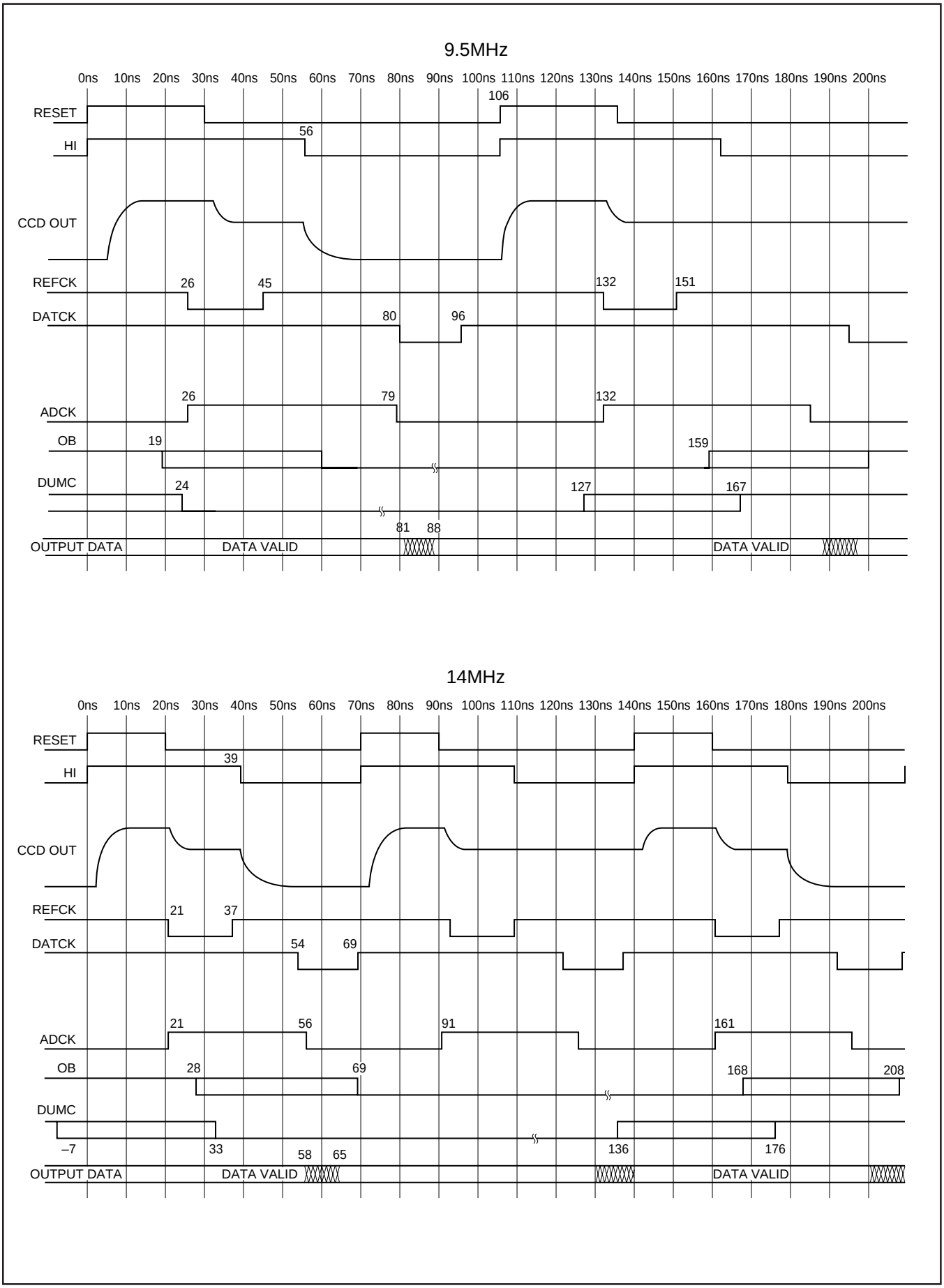
TIMING FOR REGISTER RESET



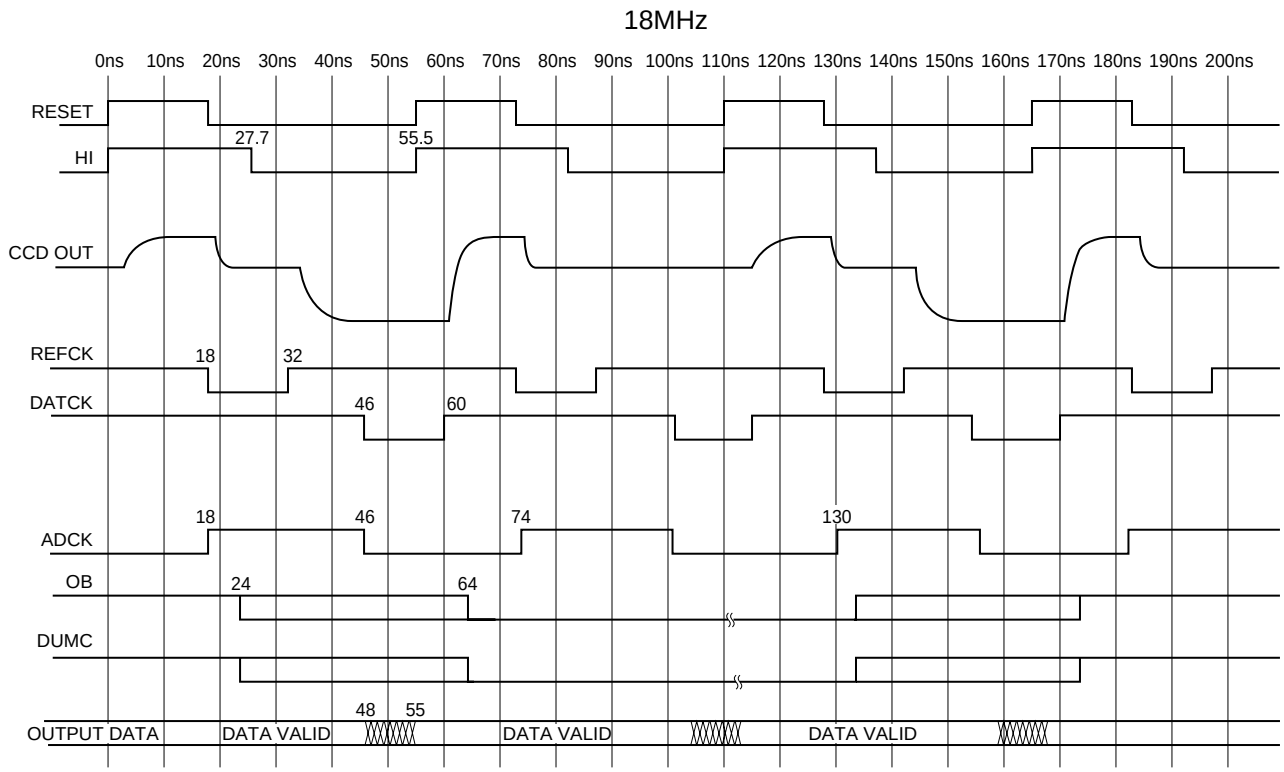
TIMING FOR PREBLANKING



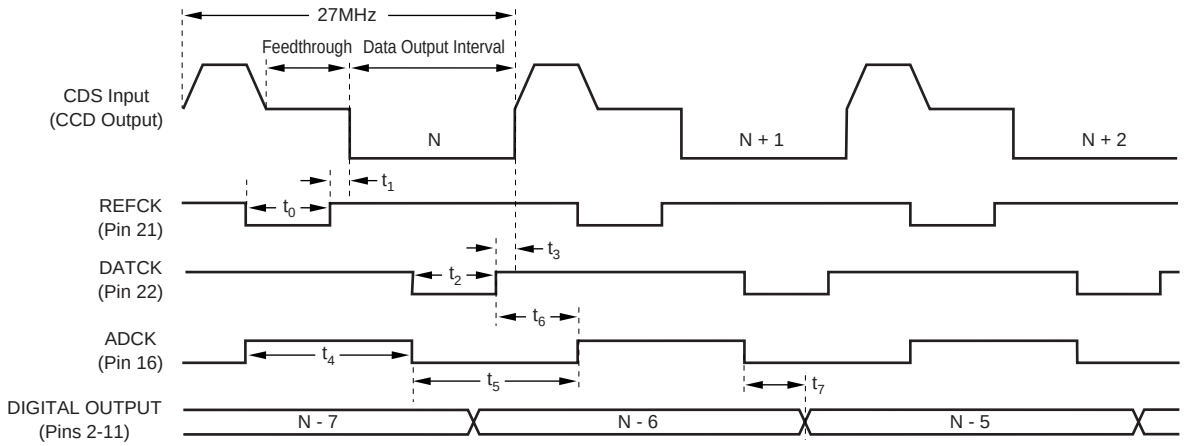
TIMING DIAGRAMS



TIMING DIAGRAMS (CONT)



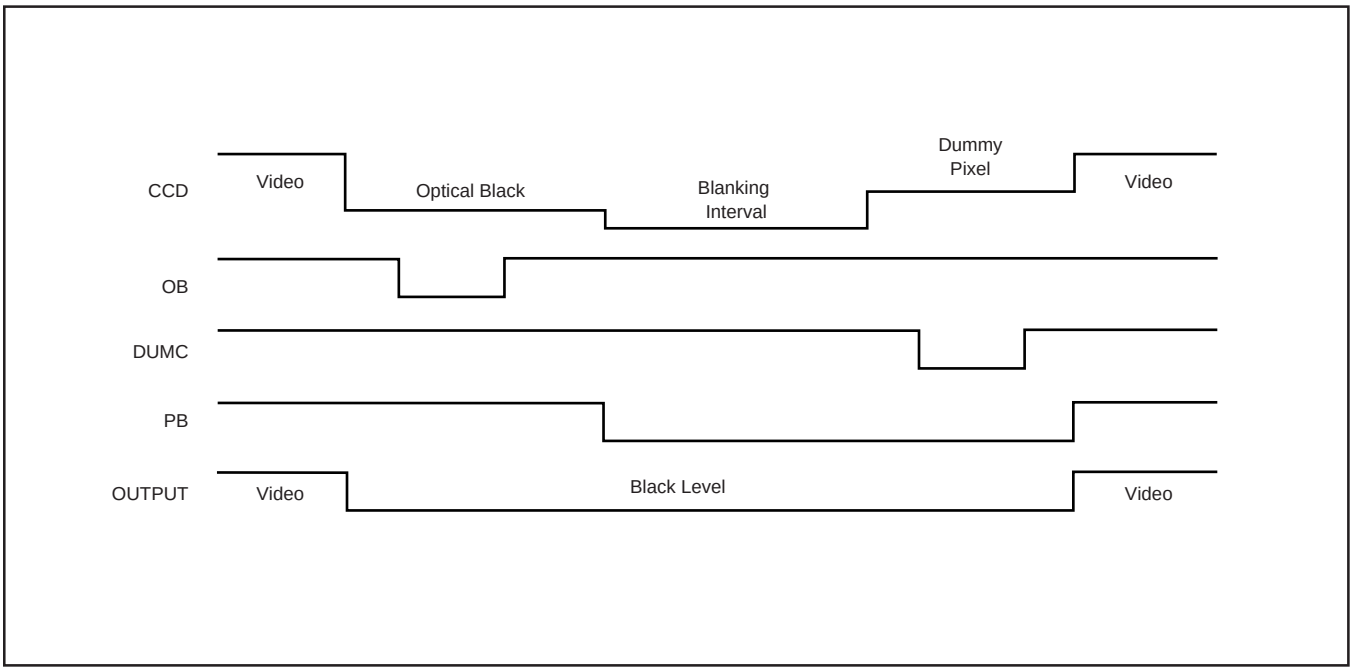
CDS/ADC TIMING DIAGRAM



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_0	REFCK Pulse Width	11	14		ns
t_1	REFCK Samling Delay	1.5	2		ns
t_2	DATCK Pulse Width	11	14		ns
t_3	DATCK Sampling Delay	1.5	2		ns
t_4, t_5	ADCK Pulse Width	18.5	27		ns
t_6	ADCK Delay	0	13	26	ns
t_7	Output Data Delay(1)	7.1	8.3	9.5	ns

NOTE: (1) C_{LOAD} = 5pF.

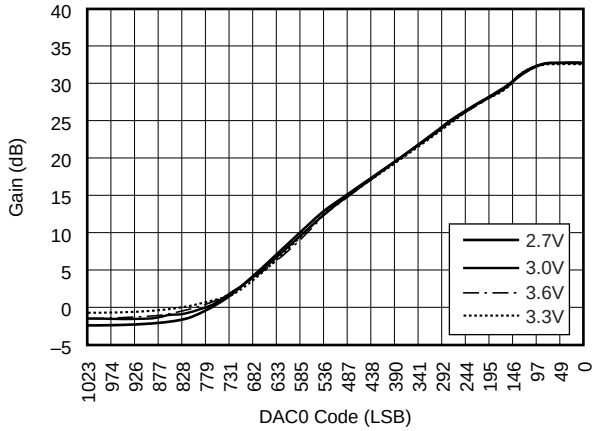
TYPICAL HORIZONTAL INTERVAL TIMING



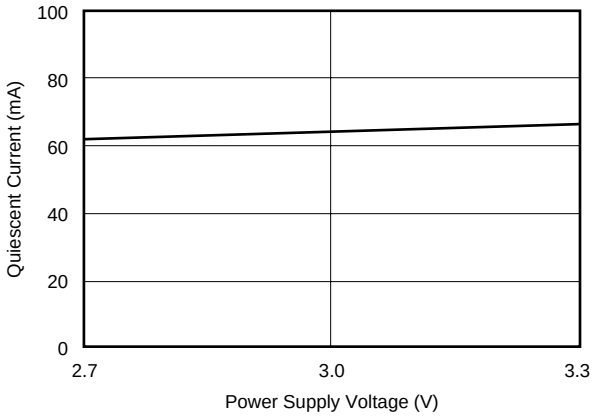
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, all power supply voltages = +3.0V, and conversion rate = 18MHz, unless otherwise specified.

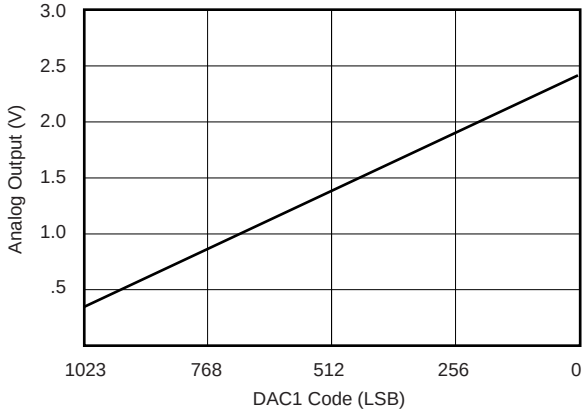
VCA CHARACTERISTICS



QUIESCENT CURRENT vs POWER SUPPLY



DAC1 ANALOG OUTPUT



THEORY OF OPERATION

The VSP2101 is an integrated circuit that contains many of the key features associated with the processing of analog signals in a video camera or a digital-still camera. Figure 1 shows a simplified block diagram of the VSP2101.

The output from the CCD array is first sent to a Correlated Double Sampler (CDS), then a voltage-controlled attenuator with a logarithmic control characteristic, and an output amplifier prior to being applied to the input of a 10-bit A/D converter.

Two calibration cycles are employed to reduce the offset variation of the VSP2101. During the dummy pixel time, an input auto-zero circuit is activated that eliminates the offset of the correlated double sampler. During the optical black timing interval, another auto-zero circuit is employed to eliminate the offset associated with the output amplifier and the remaining offset from the CDS.

CORRELATED DOUBLE SAMPLER (CDS)

The CDS removes low frequency noise from the output of the image sensor. Refer to Figure 2 which shows a block diagram of the CDS. The output from the CCD array is sampled during the reference interval as well as during the data interval. Noise that is present at the input and is of a period greater than the pixel interval will be eliminated by subtraction.

The VSP2101 employs a three track/hold correlated double sampler architecture. Track/Hold 2 is sampled during the reference interval by the REFCK signal. Track/Hold 3 is resampled at the same time that the data Track/Hold 1 is sampled by the DATCK signal. This is done to remove large transients from Track/Hold 2 that results from a portion of the reset transient being present during the acquisition time of this track and hold. The output of Track/Hold 2 is buffered by a voltage follower.

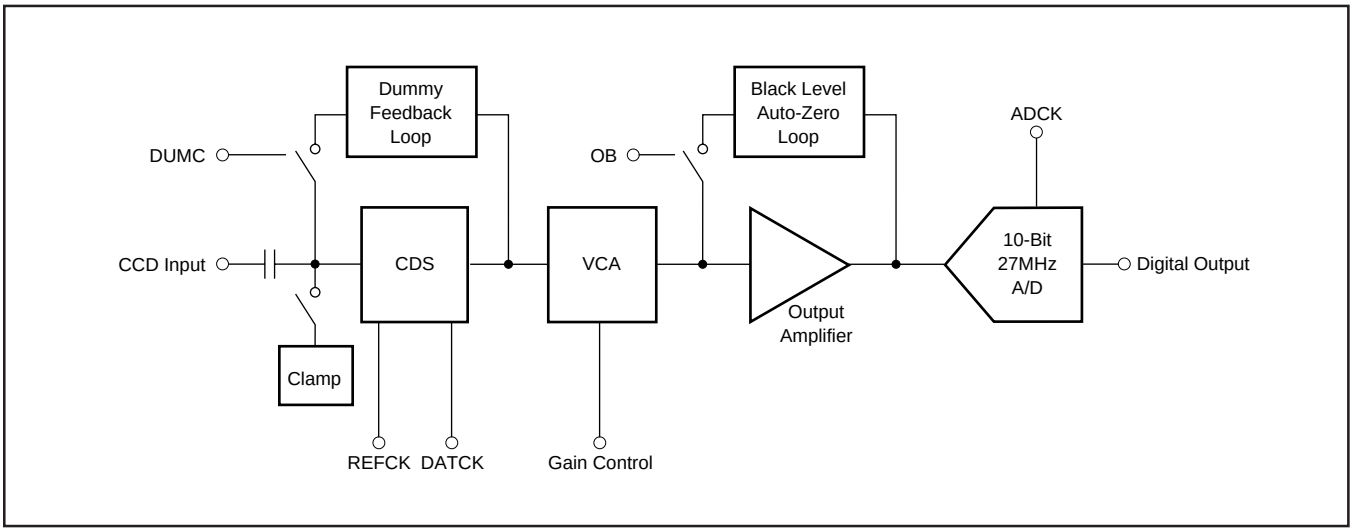


FIGURE 1. Simplified Block Diagram of VSP2101.

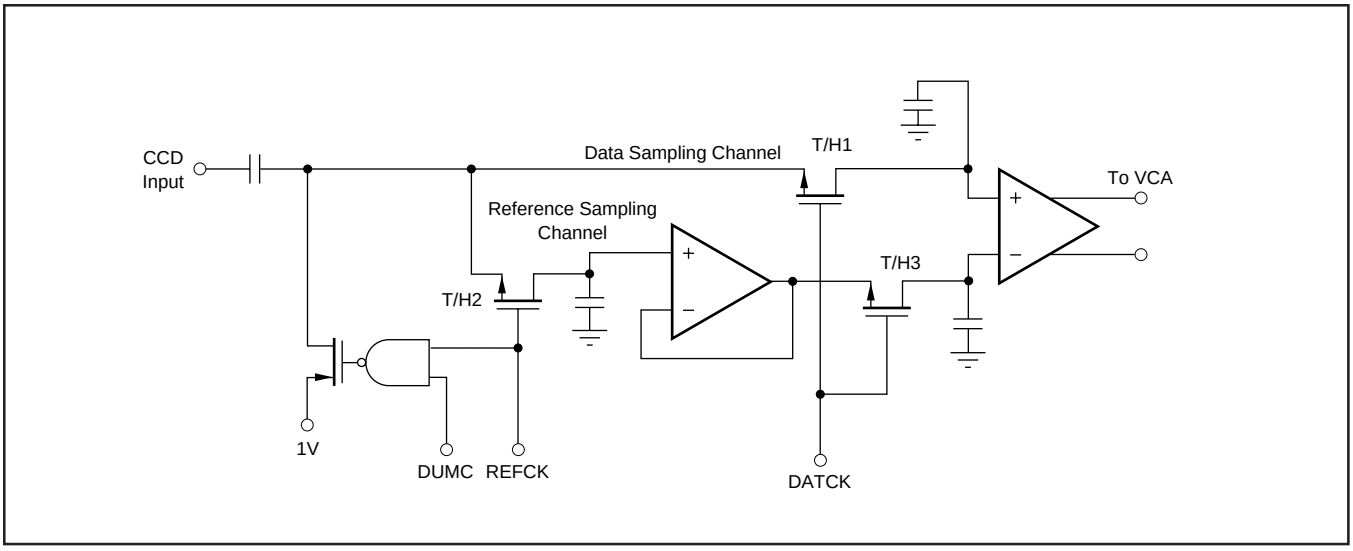


FIGURE 2. Block Diagram of Correlated Double Sampler.

DIFFERENCE AMPLIFIER

The correlated double sampler function is completed when the output of the data and reference channel are sent to the difference amplifier where the signals are subtracted. In addition to providing the difference function, the difference amplifier amplifies the signal by a factor of 2 which helps to improve the overall signal-to-noise ratio. The difference amplifier also generates a differential signal to drive the voltage-controlled attenuator.

INPUT CLAMP

The output from the CCD array is capacitively coupled to the VSP2101. To prevent shifts in the DC level from taking place due to varying input duty cycles, the input capacitor is clamped during the dummy pixel interval by the REFCK signal and the DUMC signal. A P-channel transistor is used for this input clamp switch to allow a 2V negative change at the input that would bring the signal below ground by 1. Under typical conditions, the bias at the input to the VSP2101 is at 1V.

DUMMY PIXEL AUTO-ZERO LOOP

The output from the data and reference channel is processed by the previously mentioned difference amplifier. The differential output from the difference amplifier is sent to both the voltage-controlled logarithmic attenuator and to an error amplifier. The error amplifier amplifies and feeds a signal to the difference amplifier to drive the offset measured at the output of the difference amplifier to zero. A block diagram of this circuit is shown in Figure 3. This error amplifier serves the purpose of reducing the offset of the CDS to avoid a large offset from being amplified by the output amplifier.

The effective time constant of this loop is given by:

$$T = \frac{RC}{AD}$$

where R is 10kΩ, C is an external capacitor connected to pin 27 (CCD R), A is the gain of the error amplifier with a value of 50, and D is the duty cycle of the time that the dummy pixel auto-zero loop is in operation. The duty cycle (D) must be considered as the loop operates in a sampled mode. Operation of the dummy auto-zero loop is activated by the DUMC signal that happens once during each horizontal line interval.

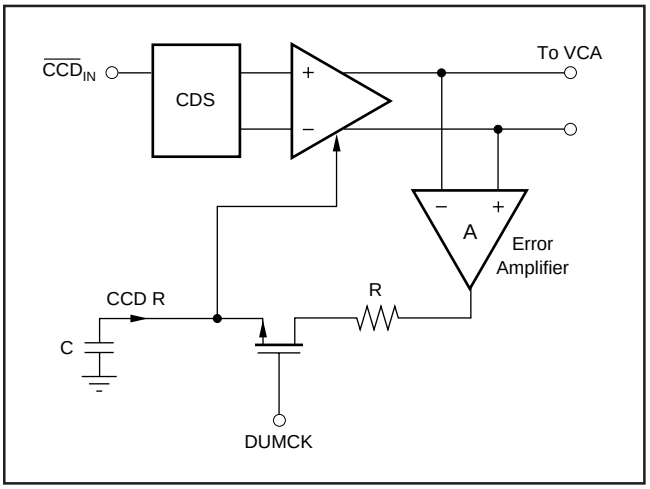


FIGURE 3. Block Diagram of Dummy Pixel Loop.

TIMING

The REFCK and DATCK signals are used to operate the CDS as previously explained. These same two signals are also used by internal timing circuitry to create the necessary timing signals for the A/D. The output from the A/D is read out to external circuitry by the ADCK signal. DUMC is used to activate the dummy pixel auto-zero loop and OB is used to activate the black level auto-zero loop. The input digital timing signals REFCK, DATCK, DUMC and OB are capable of being driven from either 3V or 5V logic levels.

VOLTAGE-CONTROLLED ATTENUATOR

To maximize the dynamic range of the VSP2101, a voltage-controlled attenuator is included with a control range from 0dB to –34dB. The gain control has a logarithmic relationship between the control voltage and the attenuation. The attenuator processes a differential signal from the difference amplifier to improve linearity and to reject both power supply and common-mode noise. The output from the attenuator is amplified by 28dB prior to being applied to the A/D. A typical gain control characteristic of the VSP2101 is shown in the typical performance curve, "VCA Characteristics".

BLACK LEVEL AUTO-ZERO LOOP

The black level auto-zero loop amplifies the difference between the output of the output amplifier and a reference signal during the optical black timing interval. This difference signal is amplified and fed back into the output amplifier to correct the offset. In doing so, the output level of the entire CCD channel can be controlled to be approximately –FS + 32LSBs under zero input signal conditions. The black level auto-zero loop is activated by the OB timing signal.

Figure 4 shows a block diagram of the black level auto-zero loop. The loop time constant is given by:

$$T = \frac{C}{(G_M)\,(D)}$$

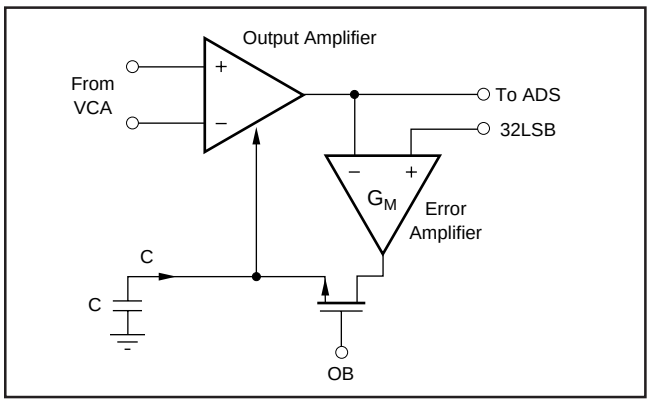


FIGURE 4. Black Level Auto-Zero Loop.

where C is the external filter capacitance applied to pin 24 (C), G_M is .001Ω and D is the duty cycle of the time that the black level auto-zero loop is in operation. The duty cycle (D) must be considered as the loop operates in a sampled mode. Operation of the black level auto-zero loop is activated by the OB signal that happens once during each horizontal line interval.

A/D CONVERTER

The A/D converter utilizes a pipline architecture. The fully differential topology and digital error correction guarantee 10-bit resolution. The A/D converter circuitry includes a reference circuit that provides bias voltages for the entire system.

SERIAL INTERFACE AND DACs

The VSP2101 incorporates two identical 10-bit DACs (DAC0 and DAC1). DAC0 is for controlling the amount of attenuation of the log Voltage Controlled Attenuator (VCA) and DAC1 is for user-defineable options such as iris control.

The input data for these DACs are set by the written data through the serial interface. The serial port has an 12-bit register which is controlled by four signals (SD, SCLK, WRT, RESET). SD is the serial data input, SCLK is the clock for the serial data, WRT pulse takes the serial register data into another internal parallel register at the rising edge, RESET resets all the registers' data to zeros asynchronously when RESET = LOW. The serial register uses master-slave dual flip-flops and the master flip-flop receives the input data at the rising edge of SCLK and transmits this data into the slave at the falling edge of SCLK. Therefore, the clock SCLK must be normally LOW.

When the DAC input data is all zeros, this corresponds to a maximum output voltage of 2.4V. In a similar manner, all ones correspond to a DAC output voltage of 0.3V. The VCA attenuation is at a minimum—which is the same as the channel gain being a maximum—when the DAC voltage is at 2.4V.

The serial data format and the related signal timing are shown page 5. When the input serial data is longer than 12 bits, the last 12 bits become effective and the former bits are erased.

When the registers are reset, the user should be careful that the channel gain setting becomes maximum and DAC1 output voltage goes to maximum.

DECOUPLING AND GROUNDING CONSIDERATIONS

The VSP2101 has several supply pins, one of which is dedicated to supply only the digital output driver (pin 12, DRV_{DD}). The remaining supply pins are not, as is often the case, divided into analog and digital supply pins since they are internally connected on the chip. For this reason, it is recommended that the VSP2101 be treated as an analog component and be powered from the analog supply only. Digital supply lines often carry high levels of wide band noise which can couple back into the VSP2101 and limit performance.

Figure 5 shows the recommended decoupling scheme for the VSP2101. In most cases, 0.1µF ceramic chip capacitors are adequate to keep the impedance low over a wide frequency range. Their effectiveness largely depends on the proximity to the individual pin. Therefore, they should be located as close as possible to the pins. In addition, one larger capacitor (1µF to 22µF) should be placed on the PC board in proximity of the VSP2101.

OTHER RECOMMENDATIONS

DRV_{DD} is a power supply used exclusively for the digital output driver and should not be connected to AV_{DD} and DV_{DD}, even if the power supply voltage is the same. The voltage level difference between DRV_{DD}, AV_{DD}, and DV_{DD} should be kept less than 0.3V.

If your PC board has analog and digital ground, AV_{SS}, DV_{SS}, and DRV_{SS} should be connected to analog ground.

DEMONSTRATION BOARD

A demonstration board, DEM-VSP2101, is available to assist in the inital evaluation of the circuit performance using the VSP2101. The schematic of the DEM-VSP2101 is shown in Figure 5.

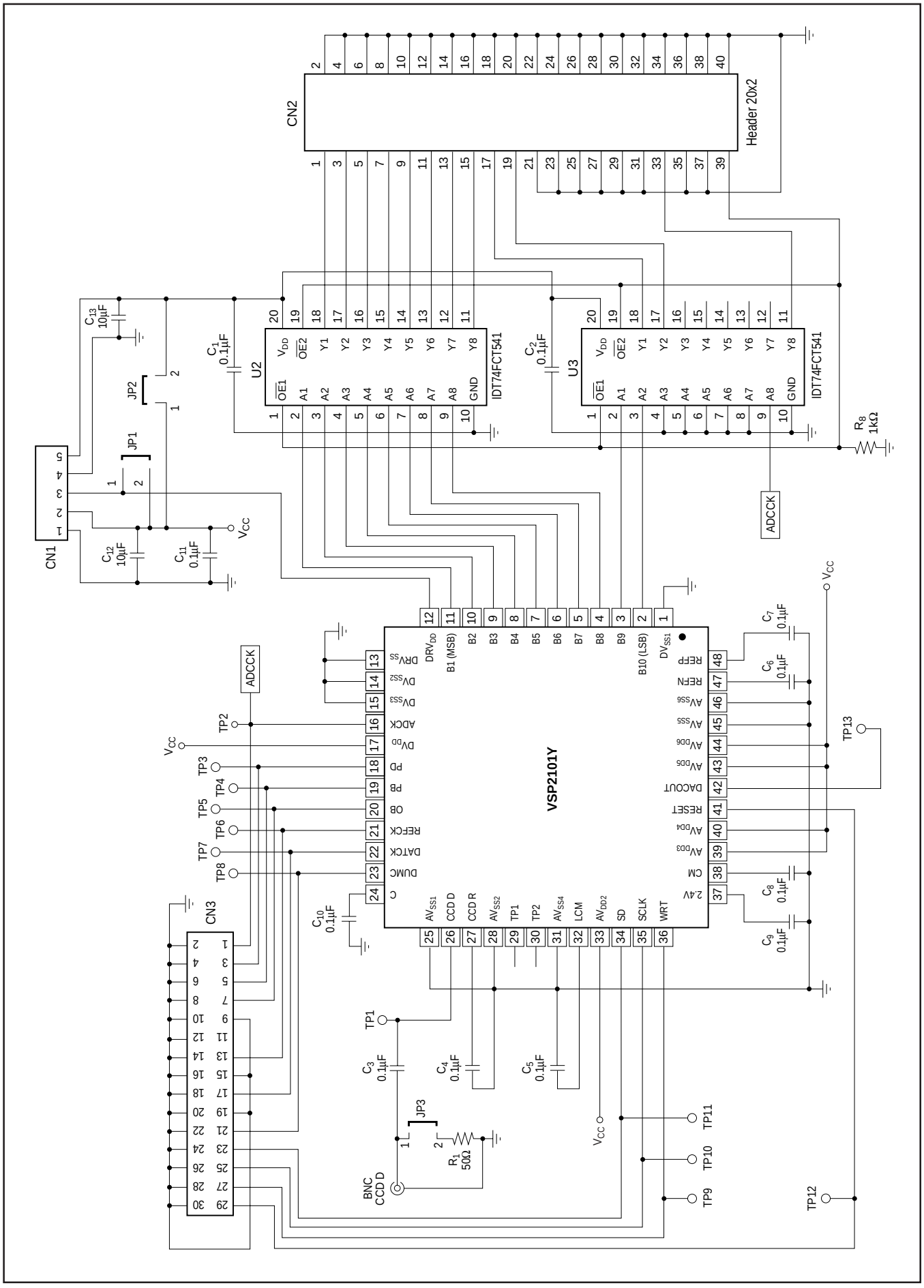


FIGURE 5. DEM-VSP2101Y Schematic.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
VSP2101Y	NRND	LQFP	PT	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
VSP2101YG4	NRND	LQFP	PT	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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