



VPS10

CRT Display Video Output Amplifier: High-Voltage, Wideband Amplification

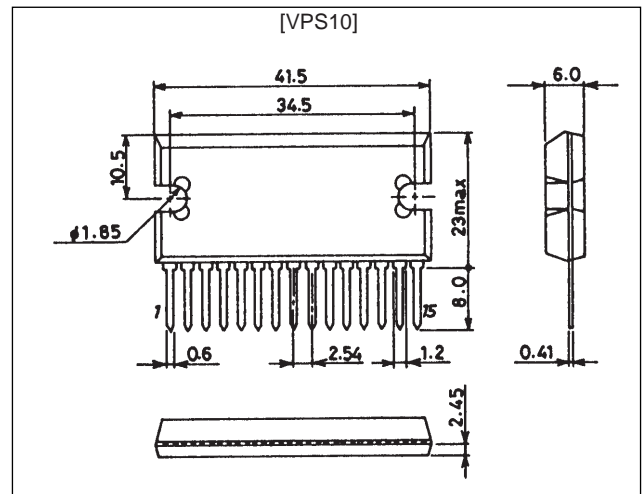
Features

- High output voltage and wide bandwidth make the VPS10 optimal for use in f_H (horizontal deflection frequency) = 85 kHz class color monitors.
($f = 100$ MHz -3 dB at $V_{OUT} = 50$ Vp-p)
- SIP molded 15-pin package with three channels in a single package.

Package Dimensions

unit: mm

2127



Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		120	V
	V_{BB} max		15	V
Allowable power dissipation	P_d max	$T_c = 25^\circ\text{C}$ with an ideal heat sink	25	W
Junction temperature	T_j max		150	$^\circ\text{C}$
Case temperature	T_c max		100	$^\circ\text{C}$
Storage temperature	T_{stg}		-20 to +110	$^\circ\text{C}$

Operating Conditions at $T_a = 25^\circ\text{C}$

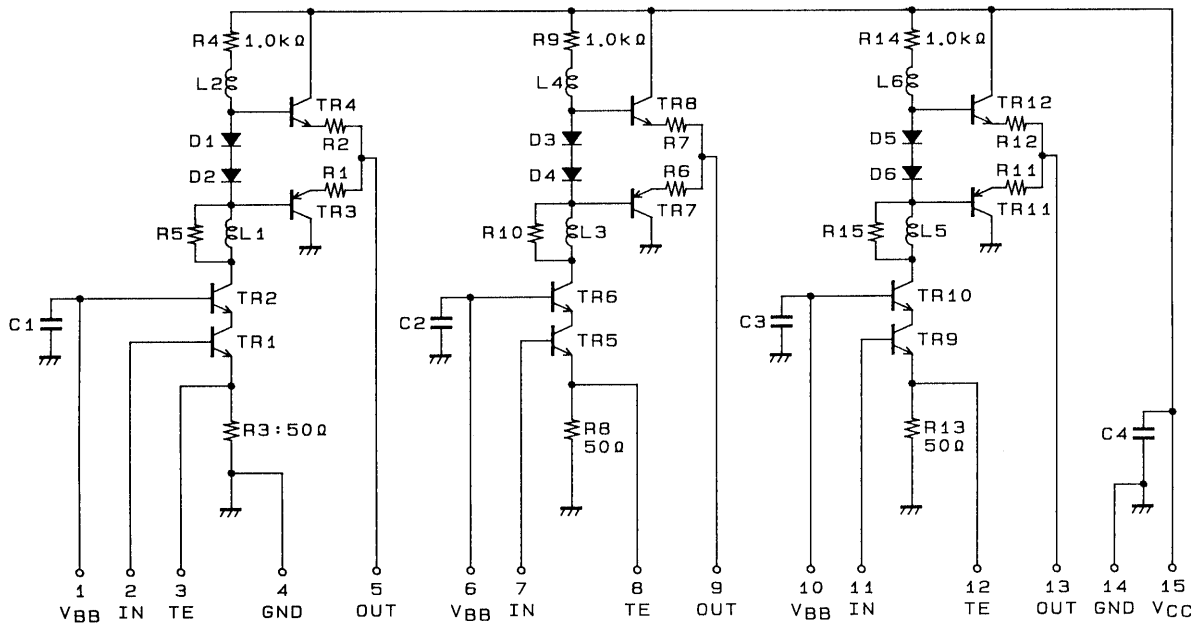
Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage I	V_{CC}		80	V
	V_{BB}		10	V
Recommended supply voltage II	V_{CC}		90	V
	V_{BB}		10	V

VPS10

Electrical Characteristics at $T_a = 25^\circ\text{C}$ (for a single channel)

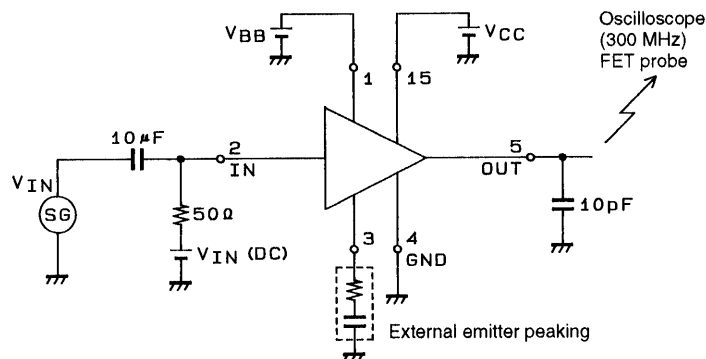
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Frequency band I (-3 dB)	f_c	$V_{CC} = 80\text{ V}$, $V_{BB} = 10\text{ V}$, $C_L = 10\text{ pF}$, $V_{IN}(\text{DC}) = 2.7\text{ V}$, $V_{OUT}(\text{p-p}) = 40\text{ V}$		100		MHz
Frequency band II	f_c	$V_{CC} = 90\text{ V}$, $V_{BB} = 10\text{ V}$, $C_L = 10\text{ pF}$, $V_{IN}(\text{DC}) = 3.0\text{ V}$, $V_{OUT}(\text{p-p}) = 50\text{ V}$		100		MHz
Pulse response characteristics	t_r	$V_{CC} = 80\text{ V}$, $V_{BB} = 10\text{ V}$, $C_L = 10\text{ pF}$, $V_{IN}(\text{DC}) = 2.7\text{ V}$, $V_{OUT}(\text{p-p}) = 40\text{ V}$		5.0		ns
	t_f			3.5		ns
Voltage gain	GV (DC)		17	19	21	times
Current drain I	I_{CC1}	$V_{CC} = 80\text{ V}$, $V_{BB} = 10\text{ V}$, $C_L = 10\text{ pF}$, $V_{IN}(\text{DC}) = 2.5\text{ V}$, $V_{OUT}(\text{p-p}) = 40\text{ V}$, $f = 10\text{ MHz}$ clock		43		mA
	I_{CC2}	$V_{CC} = 80\text{ V}$, $V_{BB} = 10\text{ V}$, $C_L = 10\text{ pF}$, $V_{IN}(\text{DC}) = 2.5\text{ V}$, $V_{OUT}(\text{p-p}) = 40\text{ V}$, $f = 100\text{ MHz}$ clock		60		mA
Current drain II	I_{CC1}	$V_{CC} = 90\text{ V}$, $V_{BB} = 10\text{ V}$, $C_L = 10\text{ pF}$, $V_{IN}(\text{DC}) = 2.8\text{ V}$, $V_{OUT}(\text{p-p}) = 50\text{ V}$, $f = 10\text{ MHz}$ clock		50		mA
	I_{CC2}	$V_{CC} = 90\text{ V}$, $V_{BB} = 10\text{ V}$, $C_L = 10\text{ pF}$, $V_{IN}(\text{DC}) = 2.8\text{ V}$, $V_{OUT}(\text{p-p}) = 50\text{ V}$, $f = 100\text{ MHz}$ clock		75		mA

Internal Equivalent Circuit

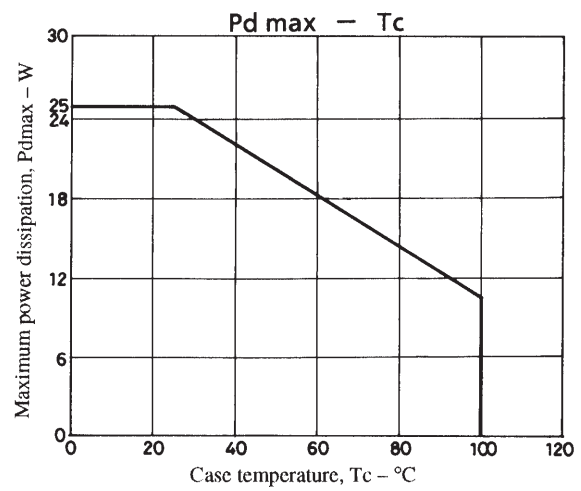
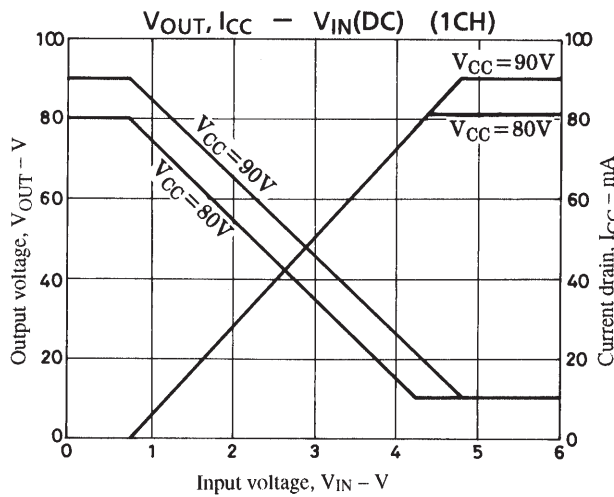
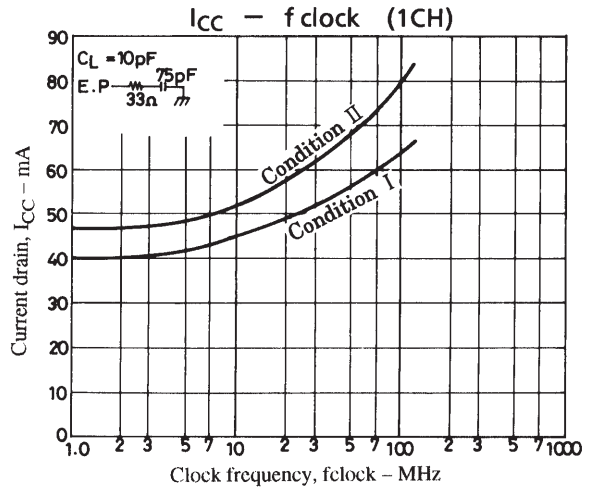
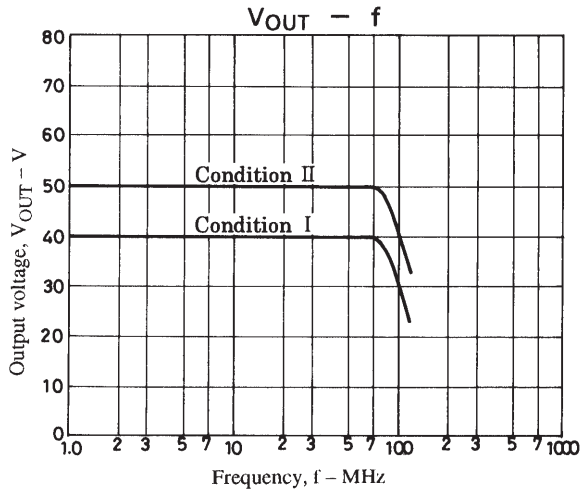


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Test Circuit (for a single channel)



A04374



Thermal Design

Since the VPS10 includes three channels as shown in the internal equivalent circuit diagram, we first consider a single channel. The chip temperature of each transistor under actual operating conditions is determined using the following formula.

$$T_j (TR_i) = \theta_{j-c} (TR_i) \times P_C (TR_i) + \Delta T_c + T_a \text{ (}^\circ\text{C)} \dots\dots\dots (1)$$

$\theta_{j-c} (TR_i)$: Thermal resistance of an individual transistor

$P_C (TR_i)$: Collector loss for an individual transistor

ΔT_c : Case temperature rise

T_a : Ambient temperature

The $\theta_{j-c} (TR_i)$ for each chip is:

$$\theta_{j-c} (TR_1) \text{ to } (TR_4) = 30^\circ\text{C/W} \dots\dots\dots (2)$$

Although the loss for each transistor in a video pack varies with frequency and is not uniform, if we assume operation at the maximum operating frequency, $f = 100 \text{ MHz}$ (clock), then the chips with the largest loss will be the emitter-follower stage transistors (TR3 and TR4) and that loss will be about 20% of the total loss. Thus from the Pd (shown in the figure) for a single channel we have:

$$P_C (E \text{ and } F \text{ stages})_{f=100 \text{ MHz}} = Pd (1ch)_{f=100 \text{ MHz}} \times 0.20 \text{ [W]} \dots\dots\dots (3)$$

Here, we must select a heat sink with a capacity θ_h such that the T_j of these transistors does not exceed 150°C . Equation (4) below gives the relationship between θ_h and ΔT_c .

$$\Delta T_c = Pd (TOTAL) \times \theta_h \dots\dots\dots (4)$$

The required θ_h is calculated using this equation and equation (1).

VPS10 Thermal Design Example

Conditions: Using an $f_H = 85$ kHz class monitor, $f_V = 100$ MHz (clock)

$$V_{CC} = 90 \text{ V}, V_{BB} = 10 \text{ V}, V_{OUT} = 50 \text{ Vp-p} (C_L = 10 \text{ pF})$$

Consider the case where the maximum clock frequency is 100 MHz, taking into account the fact that this class of monitor can be operated at ambient temperatures up to $T_a = 60^\circ\text{C}$.

As mentioned previously, the chips with the largest loss are the transistors in the emitter-follower stage. Determining those values gives:

$$P_C (\text{E and F stages}) = 7.2 \times 0.20 = 1.44 \text{ [W]} \dots\dots\dots (5)$$

We determine ΔT_j by substituting the value for θ_{j-c} in equation (5).

$$\Delta T_j = 1.44 \times 30 = 43.2 \text{ [}^\circ\text{C]}$$

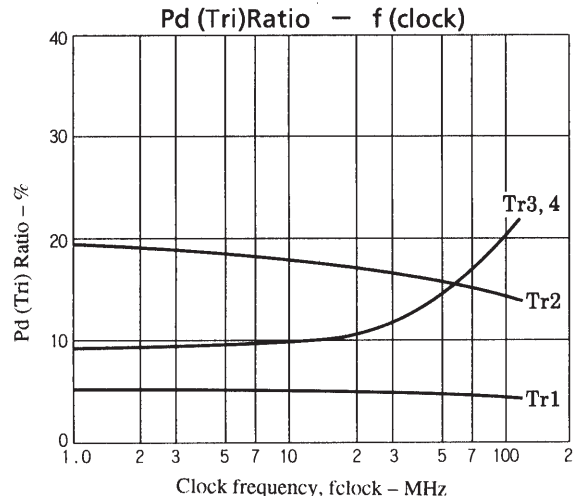
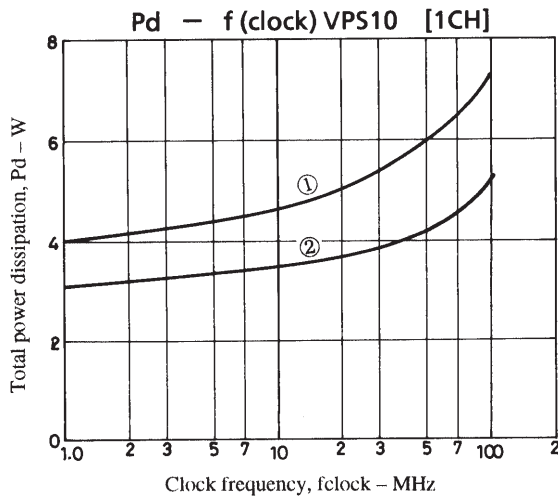
Therefore, T_j (max) will be $43.2 + T_c$ (max) = $43.2 + 100$. Since this will be under 100°C , it suffices to design a heat sink that guarantees that T_c will be under 100°C .

Therefore, a heat sink such that $T_c < 100^\circ\text{C}$ will have the following thermal resistance:

$$\theta_h = \Delta T_c \div P_d (\text{TOTAL}) = (T_c - T_a) \div [P_d (1ch) \times 3] = 40 \div (7.2 \times 3) = 1.85^\circ\text{C/W}$$

Thus the thermal resistance in this case is $\theta_h = 1.8^\circ\text{C/W}$.

In actual practice, the ambient temperature and operating conditions will allow a heat sink smaller than that indicated by this calculation to be used. Therefore, design optimization taking the actual conditions into account is also required.



Item	V _{CC} (V)	V _{BB} (V)	V _{OUT} (V)	V _O (center)
1	90	10	50	50
2	80	10	40	45

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