Ordering number : EN5209

Wide-Bandwidth Output Module (video pack)

VPS10

CRT Display Video Output Amplifier: High-Voltage, Wideband Amplification

Features

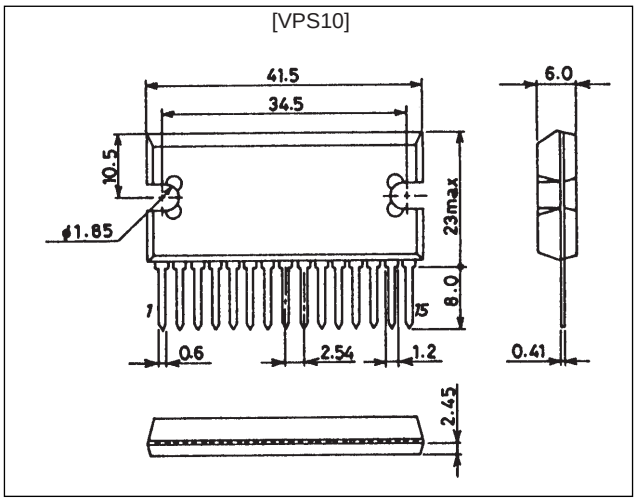
- High output voltage and wide bandwidth make the VPS10 optimal for use in f_H (horizontal deflection frequency) = 85 kHz class color monitors.
  (f = 100 MHz –3 dB at V_{OUT} = 50 Vp-p)
- SIP molded 15-pin package with three channels in a single package.

Package Dimensions

unit: mm

2127

[VPS10]



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		120	V
	V_{BB} max		15	V
Allowable power dissipation	Pd max	Tc = 25°C with an ideal heat sink	25	W
Junction temperature	Tj max		150	°C
Case temperature	Tc max		100	°C
Storage temperature	Tstg		–20 to +110	°C

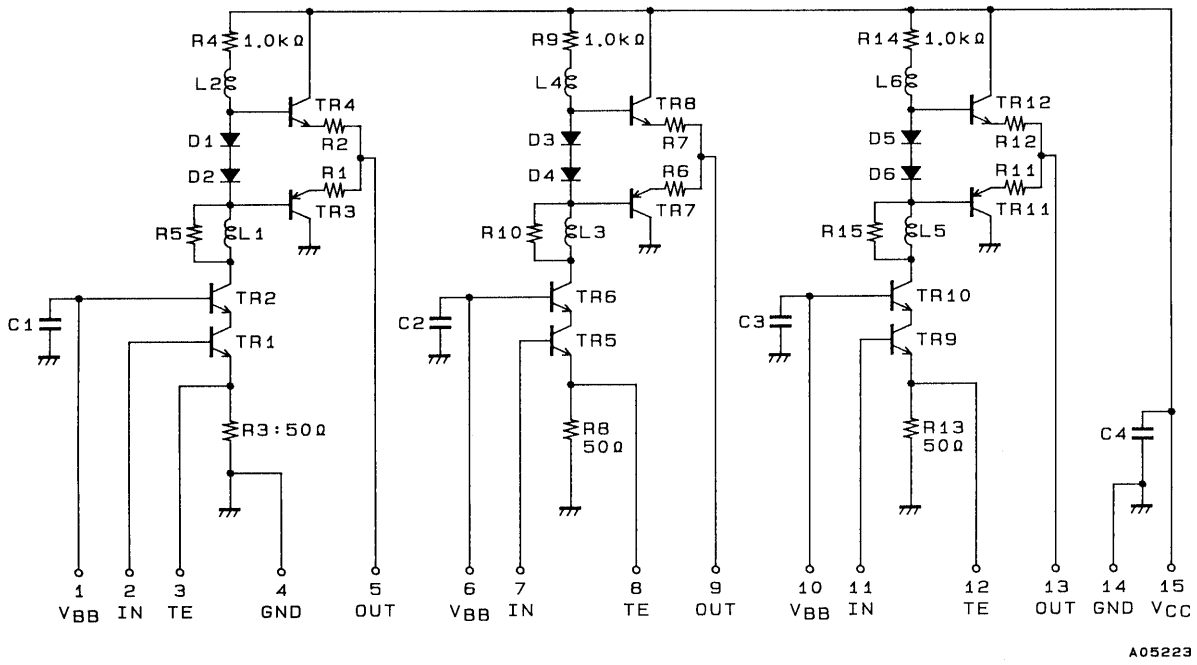
Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage I	V_{CC}		80	V
	V_{BB}		10	V
Recommended supply voltage II	V_{CC}		90	V
	V_{BB}		10	V

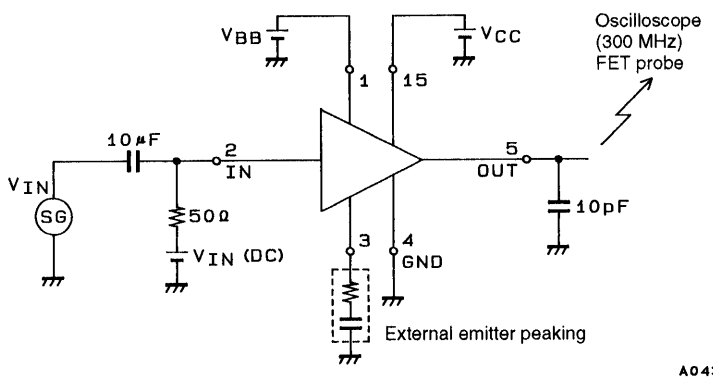
Electrical Characteristics at Ta = 25°C (for a single channel)

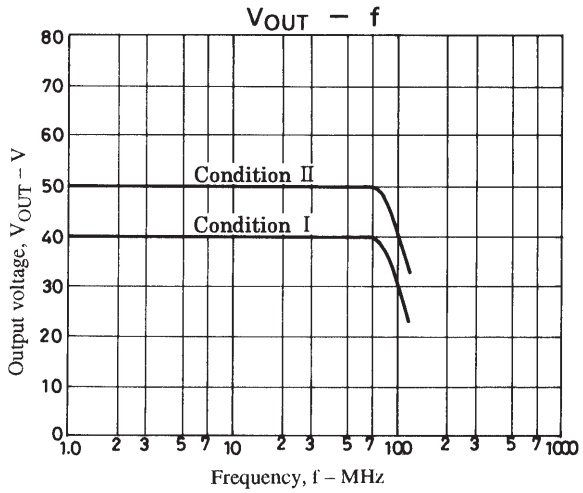
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Frequency band I (–3 dB)	f_c	V_{CC} = 80 V, V_{BB} = 10 V, C_L = 10 pF, V_{IN} (DC) = 2.7 V, V_{OUT} (p-p) = 40 V		100		MHz
Frequency band II	t_c	V_{CC} = 90 V, V_{BB} = 10 V, C_L = 10 pF, V_{IN} (DC) = 3.0 V, V_{OUT} (p-p) = 50 V		100		MHz
Pulse response characteristics	t_r	V_{CC} = 80 V, V_{BB} = 10 V, C_L = 10 pF, V_{IN} (DC) = 2.7 V, V_{OUT} (p-p) = 40 V		5.0		ns
	t_f			3.5		ns
Voltage gain	GV (DC)		17	19	21	times
Current drain I	$I_{CC}1$	V_{CC} = 80 V, V_{BB} = 10 V, C_L = 10 pF, V_{IN} (DC) = 2.5 V, V_{OUT} (p-p) = 40 V, f = 10 MHz clock		43		mA
	$I_{CC}2$	V_{CC} = 80 V, V_{BB} = 10 V, C_L = 10 pF, V_{IN} (DC) = 2.5 V, V_{OUT} (p-p) = 40 V, f = 100 MHz clock		60		mA
Current drain II	$I_{CC}1$	V_{CC} = 90 V, V_{BB} = 10 V, C_L = 10 pF, V_{IN} (DC) = 2.8 V, V_{OUT} (p-p) = 50 V, f = 10 MHz clock		50		mA
	$I_{CC}2$	V_{CC} = 90 V, V_{BB} = 10 V, C_L = 10 pF, V_{IN} (DC) = 2.8 V, V_{OUT} (p-p) = 50 V, f = 100 MHz clock		75		mA

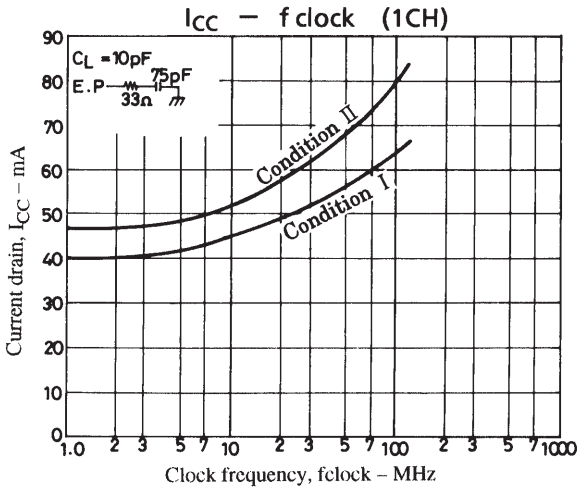
Internal Equivalent Circuit

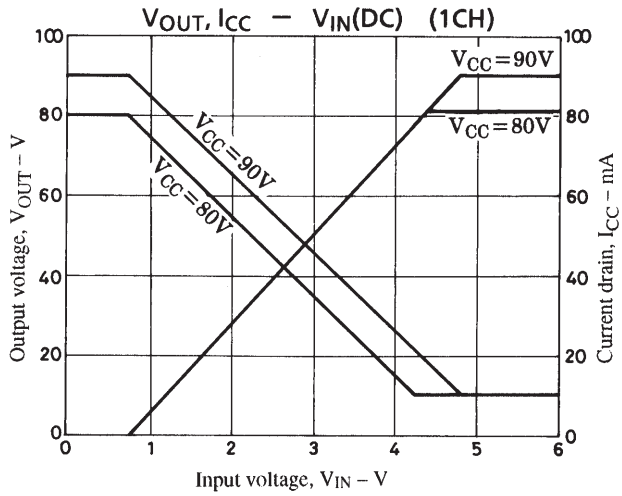


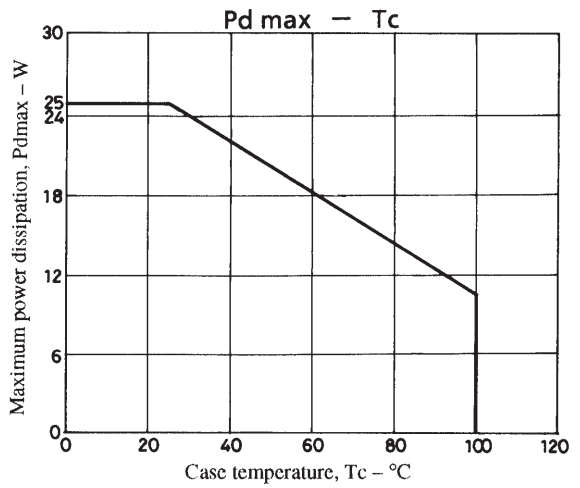
Test Circuit (for a single channel)











Thermal Design

Since the VPS10 includes three channels as shown in the internal equivalent circuit diagram, we first consider a single channel. The chip temperature of each transistor under actual operating conditions is determined using the following formula.

T_j (TRi) = $\theta_{j\text{-}c}$ (TRi) × P_C (TRi) + ΔTc + Ta (°C) ..... (1)

$\theta_{j\text{-}c}$ (Tri): Thermal resistance of an individual transistor

P_C (Tri): Collector loss for an individual transistor

ΔTc: Case temperature rise

Ta: Ambient temperature

The $\theta_{j\text{-}c}$ (Tri) for each chip is:

$\theta_{j\text{-}c}$ (TR1) to (TR4) = 30°C/W..... (2)

Although the loss for each transistor in a video pack varies with frequency and is not uniform, if we assume operation at the maximum operating frequency, f = 100 MHz (clock), then the chips with the largest loss will be the emitter-follower stage transistors (TR3 and TR4) and that loss will be about 20% of the total loss. Thus from the Pd (shown in the figure) for a single channel we have:

P_C (E and F stages)$_{f = 100\ MHz}$ = Pd (1ch)$_{f = 100\ MHz}$ × 0.20 [W] ..... (3)

Here, we must select a heat sink with a capacity θh such that the Tj of these transistors does not exceed 150°C. Equation (4) below gives the relationship between θh and ΔTc.

ΔTc = Pd (TOTAL) × θh..... (4)

The required θh is calculated using this equation and equation (1).

VPS10 Thermal Design Example

Conditions: Using an f_H = 85 kHz class monitor, f_V = 100 MHz (clock)

V_{CC} = 90 V, V_{BB} = 10 V, V_{OUT} = 50 Vp-p (C_L = 10 pF)

Consider the case where the maximum clock frequency is 100 MHz, taking into account the fact that this class of monitor can be operated at ambient temperatures up to Ta = 60°C.

As mentioned previously, the chips with the largest loss are the transistors in the emitter-follower stage. Determining those values gives:

P_C (E and F stages) = $7.2 \times 0.20 = 1.44$ [W]..... (5)

We determine ΔTj by substituting the value for $\theta j\text{-}c$ in equation (5).

$\Delta Tj = 1.44 \times 30 = 43.2$ [°C]

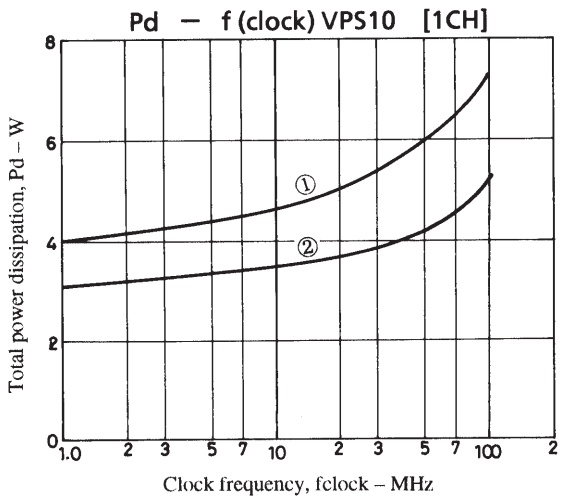
Therefore, Tj (max) will be 43.2 + Tc (max) = 43.2 + 100. Since this will be under 100°C, it suffices to design a heat sink that guarantees that Tc will be under 100°C.

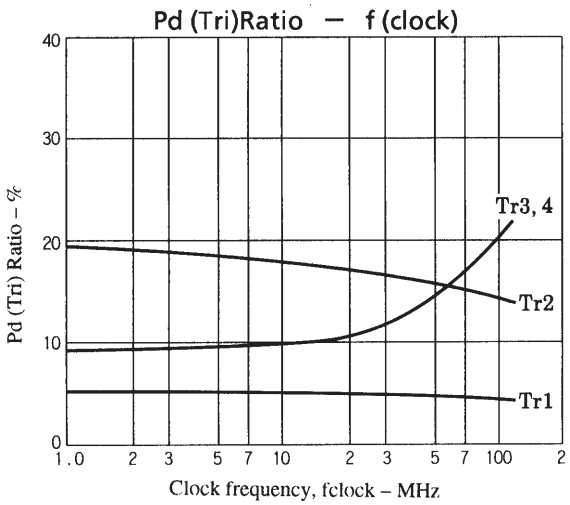
Therefore, a heat sink such that Tc < 100°C will have the following thermal resistance:

$\theta h = \Delta Tc \div Pd\ (TOTAL) = (Tc - Ta) \div [Pd\ (1ch) \times 3] = 40 \div (7.2 \times 3) = 1.85$°C/W

Thus the thermal resistance in this case is θh = 1.8°C/W.

In actual practice, the ambient temperature and operating conditions will allow a heat sink smaller than that indicated by this calculation to be used. Therefore, design optimization taking the actual conditions into account is also required.





Item	V_{CC} (V)	V_{BB} (V)	V_{OUT} (V)	V_O (center)
1	90	10	50	50
2	80	10	40	45