NEC

MOS INTEGRATED CIRCUIT

μPD78P312A

16-/8- BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

μPD78P312A is a 16-/8-bit single-chip microcomputer having the same functions as μPD78312A, except that the internal mask ROM of μPD78312A is replaced with one-time ROM or EPROM. Allowing data to be written only once, the one-time EPROM product is suited for small-scale production of various types of products, or early development of the application system. The EPROM version allows programs to be written more than once and is ideal for system evaluation.

A detailed functional description is provided in the following user's manual. Be sure to read this manual when designing your system.

μPD78312A User's Manual: IEM-5086

FEATURES

- Compatible with μPD78312A
  - Can be replaced with μPD78312A, which integrates mask ROM, when the application system is mass-produced
- Internal PROM: 8,192 x 8 bits
  - Data can be written only once (one-time PROM product without window)
  - Erasable by ultraviolet ray. Electrically rewritten (EPROM product with window)
- PROM programming characteristics: Compatible with μPD27C256A
- Available as QTOP™ microcomputer ★

Remarks: QTOP microcomputer is the generic name for the NEC built-in PROM single-chip micro computer providing total support of program writing, printing, screening, and verifying.

ORDERING INFORMATION

Part Number	Package	Internal ROM
μPD78P312ACW	64-pin plastic shrink DIP (750 mil)	One-time PROM
μPD78P312AGF-3BE	64-pin plastic QFP (14 x 20 mm)	ditto
μPD78P312AGQ-36	64-pin plastic QUIP	ditto
μPD78P312AL	68-pin plastic QFJ (□ 950 mil)	ditto
μPD78P312ADW	64-pin shrink DIP with ceramic window (750 mil)	EPROM
μPD78P312AR	64-pin QUIP with ceramic window	ditto

QUALITY GRADE

Standard

Please refer to "Quality Grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and their recommended

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Date Published November 1993 P
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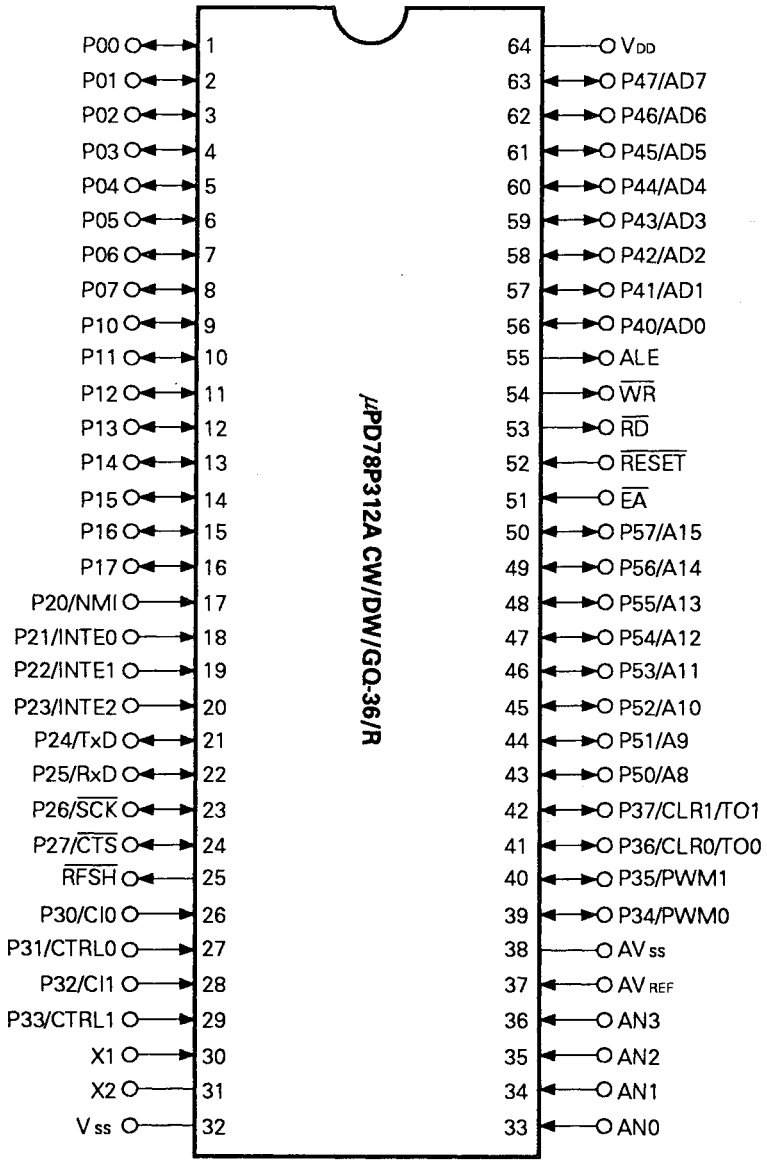
The mark ★ shows the major revised points.

PIN CONFIGURATION (Top View)

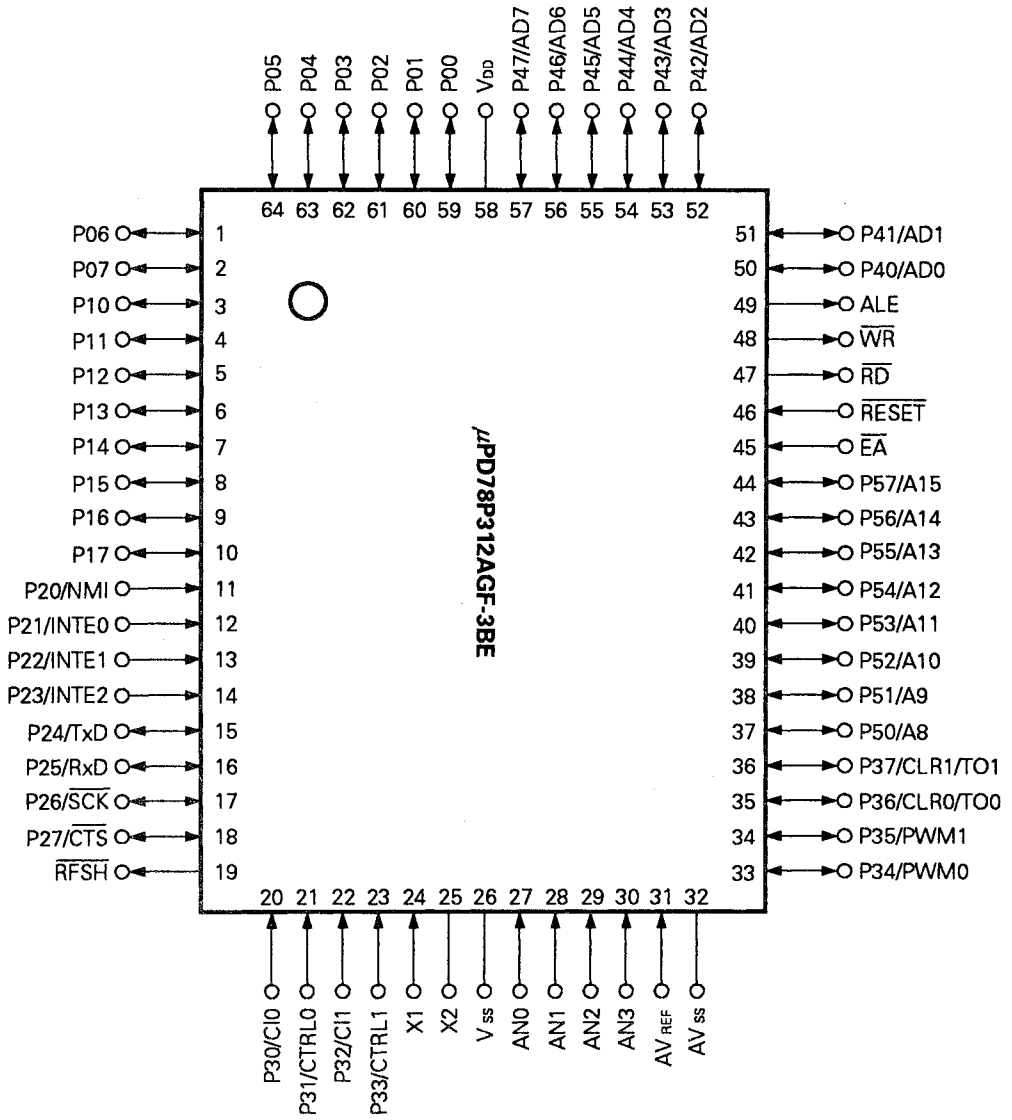
(1) Normal operation mode

(a) 64-pin plastic shrink DIP/QUIP
64-pin shrink DIP/QUIP with ceramic window

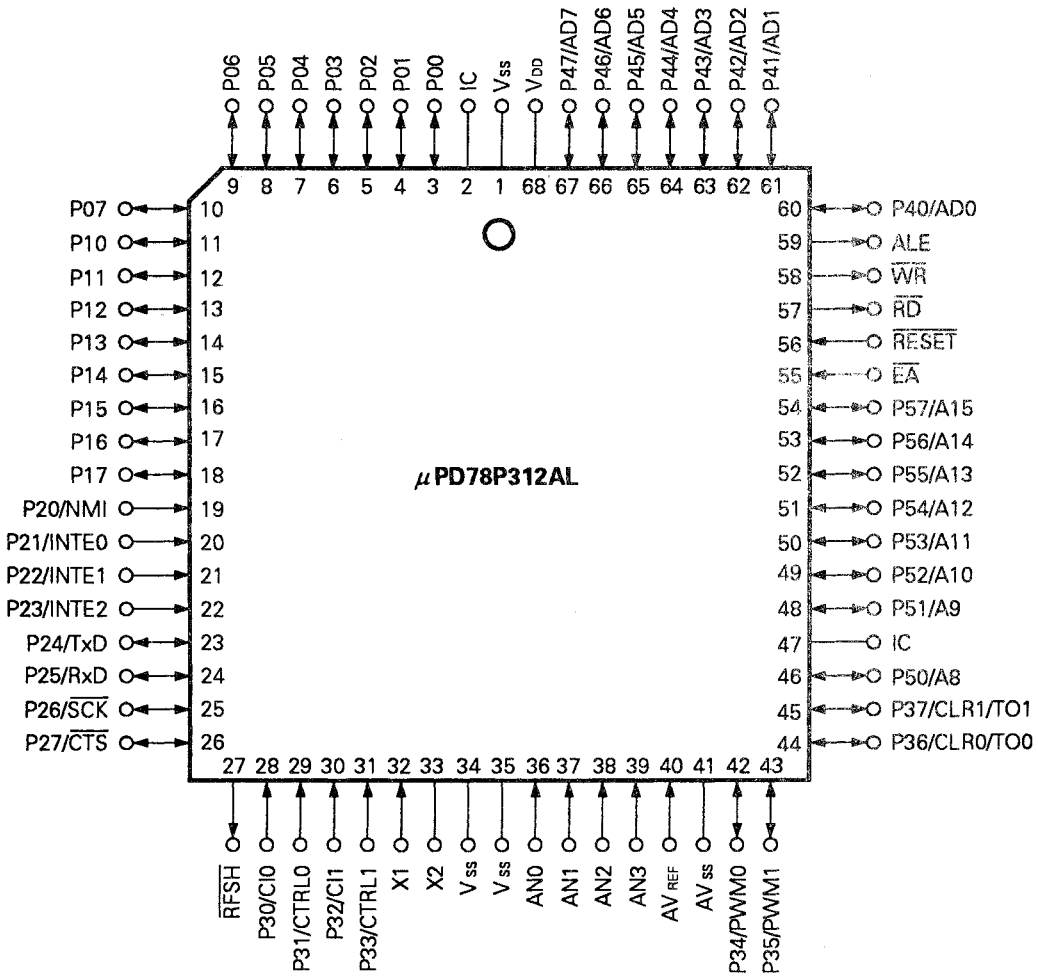


P00-P07	:	Port0	ALE	:	Address Latch Enable	NMI	:	Nonmaskable Interrupt
P10-P17	:	Port1	RFSH	:	Refresh	INTE0-INTE2	:	Interrupt From Externals
P20-P27	:	Port2	X1, X2	:	Crystal	AN0-AN3	:	Analog Input
P30-P37	:	Port3	RESET	:	Reset	AVREF	:	Reference Voltage
P40-P47	:	Port4	EA	:	External Access	AVss	:	Analog Vss
P50-P57	:	Port5	CI0, CI1	:	Count Pulse Input	RxD	:	Receive Serial Data
AD0-AD7	:	Address/Data	CTRL0, CTRL1	:	Control Pulse Input	TxD	:	Transfer Serial Data
A8-A15	:	Address	CLR0, CLR1	:	Timer Clear Input	SCK	:	Serial Clock
RD	:	Read Strobe	PWM0, PWM1	:	Pulse Width Modulation Output	CTS	:	Clear To Send
WR	:	Write Strobe	TO0, TO1	:	Timer Output	IC	:	Internally Connected

(b) 64-pin plastic QFP (14 x 20 mm)

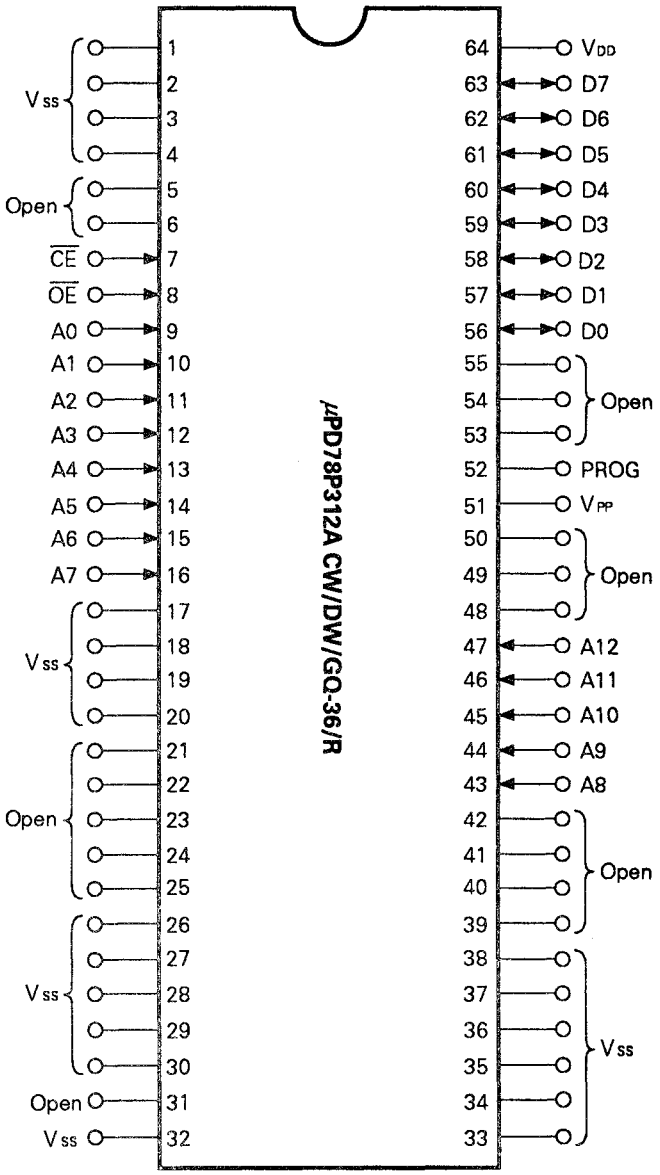


(c) 68-pin plastic QFJ (□ 950 mil)



(2) PROM programming mode

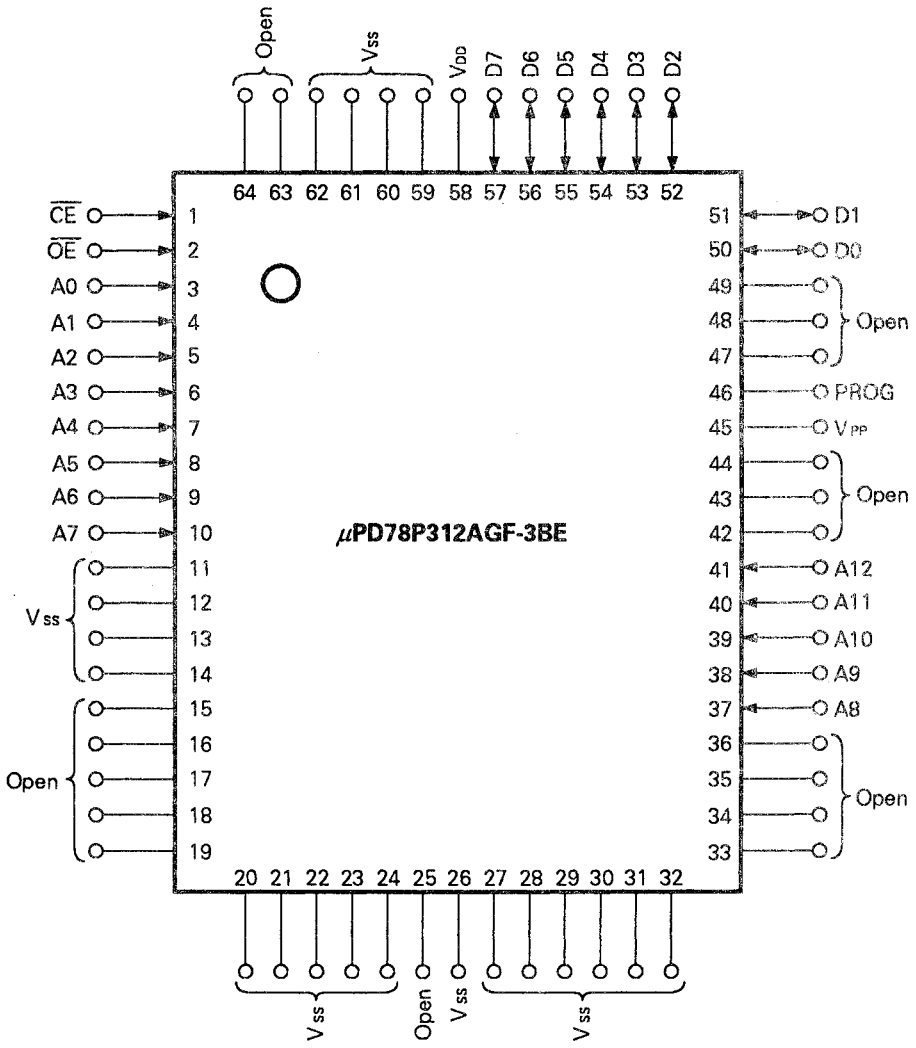
(a) 64-pin plastic shrink DIP/QUIP
64-pin shrink DIP/QUIP ceramic window



Note: **1.** V_{SS} : Ground this pin.
2. Open : Do not connect this pin.

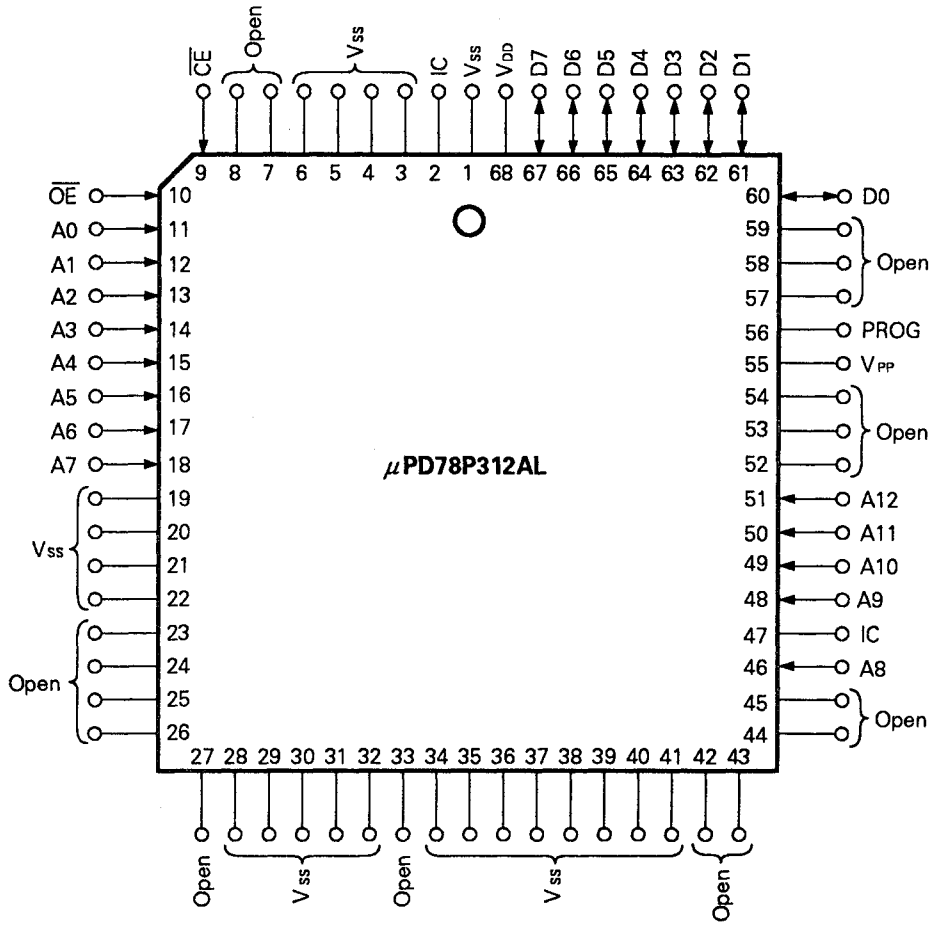
A0-A12 : Address Bus
D0-D7 : Data Bus
PROG : Program
$\overline{CE}$: Chip Enable
$\overline{OE}$: Output Enable
V_{PP} : Program Power Supply

(b) 64-pin plastic QFP (14 x 20 mm)



Note: **1.** V_{SS} : Ground this pin.
2. Open : Do not connect this pin.

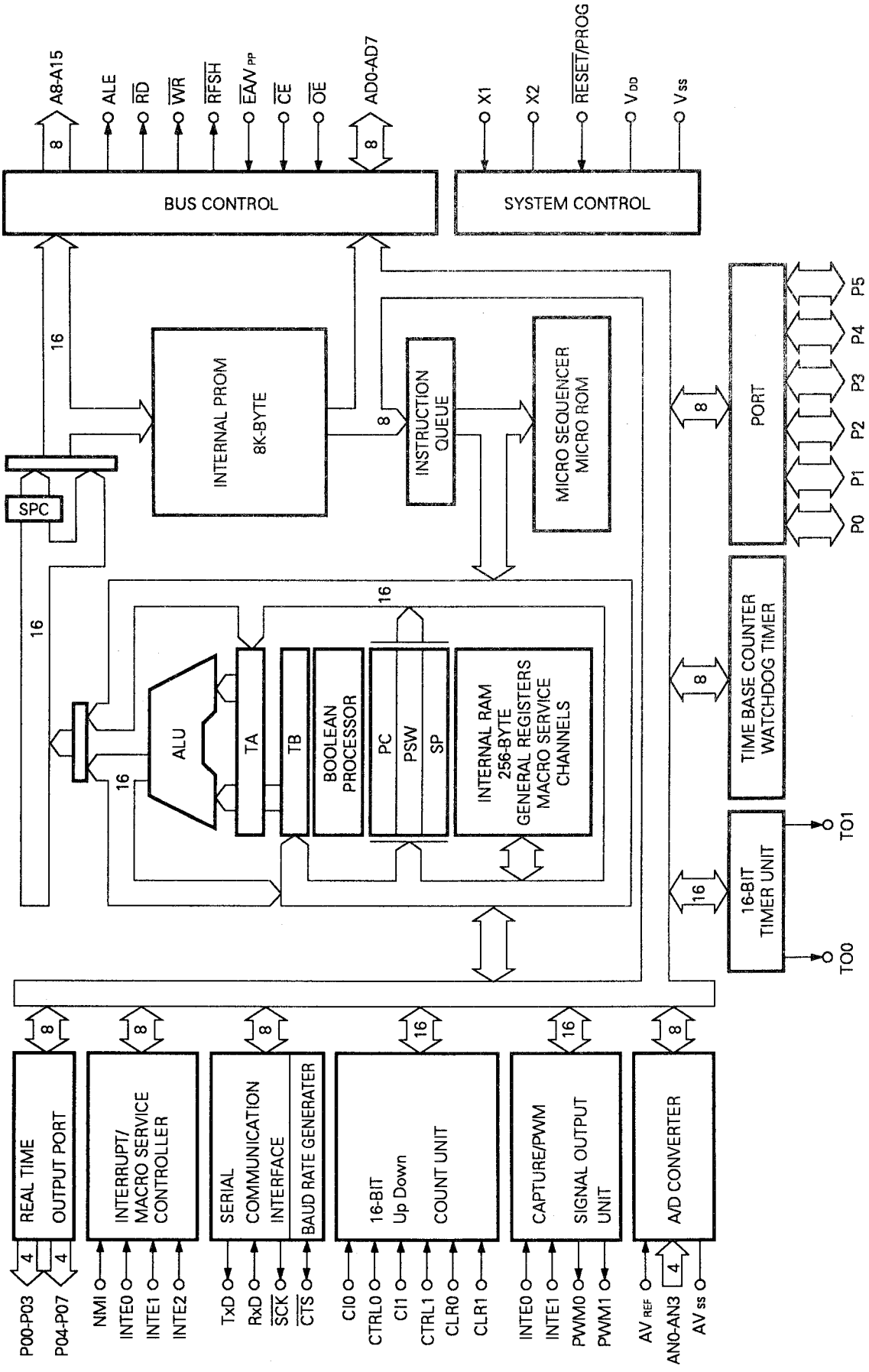
(c) 68-pin plastic QFJ (□ 950 mil)



Note: **1.** V_{SS} : Ground this pin.

2. Open : Do not connect this pin.

BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

1.1 PORT PINS

Pin Name	Input/ Output	Shared Pin *	Function
P00-P05	Input/ output, real-time output	–	(Port 0) • This is an 8-bit input/output port that can be specified for input or output in bit units. • This port can be used as two independent 4-bit real-time output ports (channels)
P06		($\overline{CE}$)	
P07		($\overline{OE}$)	
P10-P17	Input/ Output	(A0-A7)	(Port 1) This is an 8-bit input/output port that can be specified for input or output in bit units.
P20	Input	NMI	(Port 2) P20 to P23 are input port pins. P24 to P27 are input/output port pins each of which can be independently specified for input or output.
P21		INTE0	
P22		INTE1	
P23		INTE2	
P24	Input/ output	TxD	
P25		RxD	
P26		$\overline{SCK}$	
P27		$\overline{CTS}$	
P30	Input	CI0	(Port 3) P30 to P33 are input port pins. P34 to P37 are input/output port pins each of which can be independently specified for input or output.
P31		CTRL0	
P32		CI1	
P33		CTRL1	
P34	Input/ output	PWM0	
P35		PWM1	
P36		TO0-CLR0	
P37		TO1-CLR1	
P40-P47	Input/ output	AD0-AD7 (D0-D7)	(Port 4) This is an 8-bit input/output port that can be specified for input or output in 8-bit units.
P50-P54	Input/ output	A8-A12 (A8-A12)	(Port 5) This is an 8-bit input/output port that can be specified for input or output in bit units.
P55-P57		A13-A15	

*: Parentheses indicate the pin name shared in the PROM programming mode.

1.2 ALL OTHER PINS (IN NORMAL OPERATION MODE)

(1/2)

Pin Name	Input/ Output	Shared Pin*	Function
NMI	Input	P20	Non-maskable interrupt request pin
INTE0	Input	P21	External interrupt request input pin
INTE1		P22	
INTE2		P23	
TxD	Output	P24	Serial data output pin
RxD	Input	P25	Serial data input pin
$\overline{SCK}$	Output	P26	Serial clock output pin
$\overline{CTS}$	Input/ Output	P27	• In the asynchronous mode, this pin serves as the transmit enable control pin. • In the I/O interface mode, this pin inputs/outputs the serial clock.
CI0	Input	P30	These pins input the external count clock for the count unit.
CI1		P32	
CTRL0	Input	P31	These pins input the count operation selection control signal for the count unit.
CTRL1		P33	
CLR0	Input	P36/TO0	Count unit clear signal input pin
CLR1		P37/TO1	
PWM0	Output	P34	PWM output pin
PWM1		P35	
TO0	Output	P36/CLR0	Timer unit pulse output pin
TO1		P37/CLR1	
AD0-AD7	Input/ Output	P40-P47 (D0-D7)	Multiplexed address/data but pins used when the external memory space is expanded.
A8-A12	Output	P50-P54 (A8-A12)	Address bus pins when the external memory space is expanded.
A13-A15		P55-P57	
$\overline{WR}$	Output	–	External memory write signal output pin
$\overline{RD}$	Output	–	External memory read signal output pin
ALE	Output	–	This pin outputs the timing signal used to externally latch the address output when accessing the external memory.
AN0-AN3	Input	–	A/D converter analog input pin
AV_{REF}	Input	–	A/D converter reference voltage input pin
AV_{SS}	–	–	A/D converter GND pin

*: Parentheses indicate the pin name shared in the PROM programming mode.

(2/2)

Pin Name	Input/ Output	Shared Pin*	Function
X1	Input	–	The system clock crystal is connected across these pins. When using an external clock, the X1 pin inputs the external clock.
X2	–		
$\overline{RFSH}$	Output	–	This pin outputs the refresh pulse to the externally connected pseudo-static memory.
$\overline{RESET}$	Input	(PROG)	System reset pin
V_{DD}	–	–	Positive power supply pin
V_{SS}	–	–	GND
$\overline{EA}$	Input	(V_{PP})	This pin is usually connected to V_{DD}. When this pin is connected to V_{SS}, the ROM-less mode is set in which the external memory can be accessed. The level of this pin cannot be changed during operation.
IC	–	–	Internally connected. Leave this pin open.

*: Parentheses indicate the pin name shared in the PROM programming mode.

1.3 ALL OTHER PINS (ON PROM PROGRAMMING MODE)

Pin Name	Input/ Output	Shared Pin	Function
A0-A7	Input	P10-P17	Address input pins
A8-A12		P50-P54/ A8-A12	
D0-D7	Input/ output	P40-P47/ AD0-AD7	Data input/output pins
$\overline{CE}$	Input	P06	Chip-enable input pin/program pulse input pin
$\overline{OE}$	Input	P07	Output-enable input pin
PROG	–	$\overline{RESET}$	PROM programming mode set pin
V_{PP}	–	$\overline{EA}$	Program write/verify high voltage application pin
V_{DD}	–	–	Positive power supply pin
V_{SS}	–	–	GND

1.4 PIN INPUT/OUTPUT CIRCUITS

Table 1-1 and Fig. 1-1 describe each pin input/output circuit in a simplified manner.

Table 1-1 Input/Output Circuit Type for Each Pin

Pin*	Input/output circuit type	Pin*	Input/output circuit type
P00-P05	5	P34/PWM0	5
P06/($\overline{CE}$)		P35/PWM1	
P07/($\overline{OE}$)		P36/TO0/CLR0	6
P10-P17/(A0-A7)	5	P37/TO1/CLR1	
P20/NMI	2	P40-P47/AD0-AD7/(D0-D7)	5
P21/INTE0	1	P50-P54/A8-A12/(A8-A12)	5
P22/INTE1		P55-P57/A13-A15	
P23/INTE2		$\overline{WR}$	3
P24/TxD	5	$\overline{RD}$	
P25/RxD		ALE	
P26/$\overline{SCK}$		$\overline{EA}$	1
P27/$\overline{CTS}$		AN0-AN3	7
P30/CIO	1	$\overline{RFSH}$	3
P31/CTRL0		$\overline{RESET}$/(PROG)	2
P32/CI1			
P33/CTRL1			

*: Parentheses indicate pin used for PROM programming.

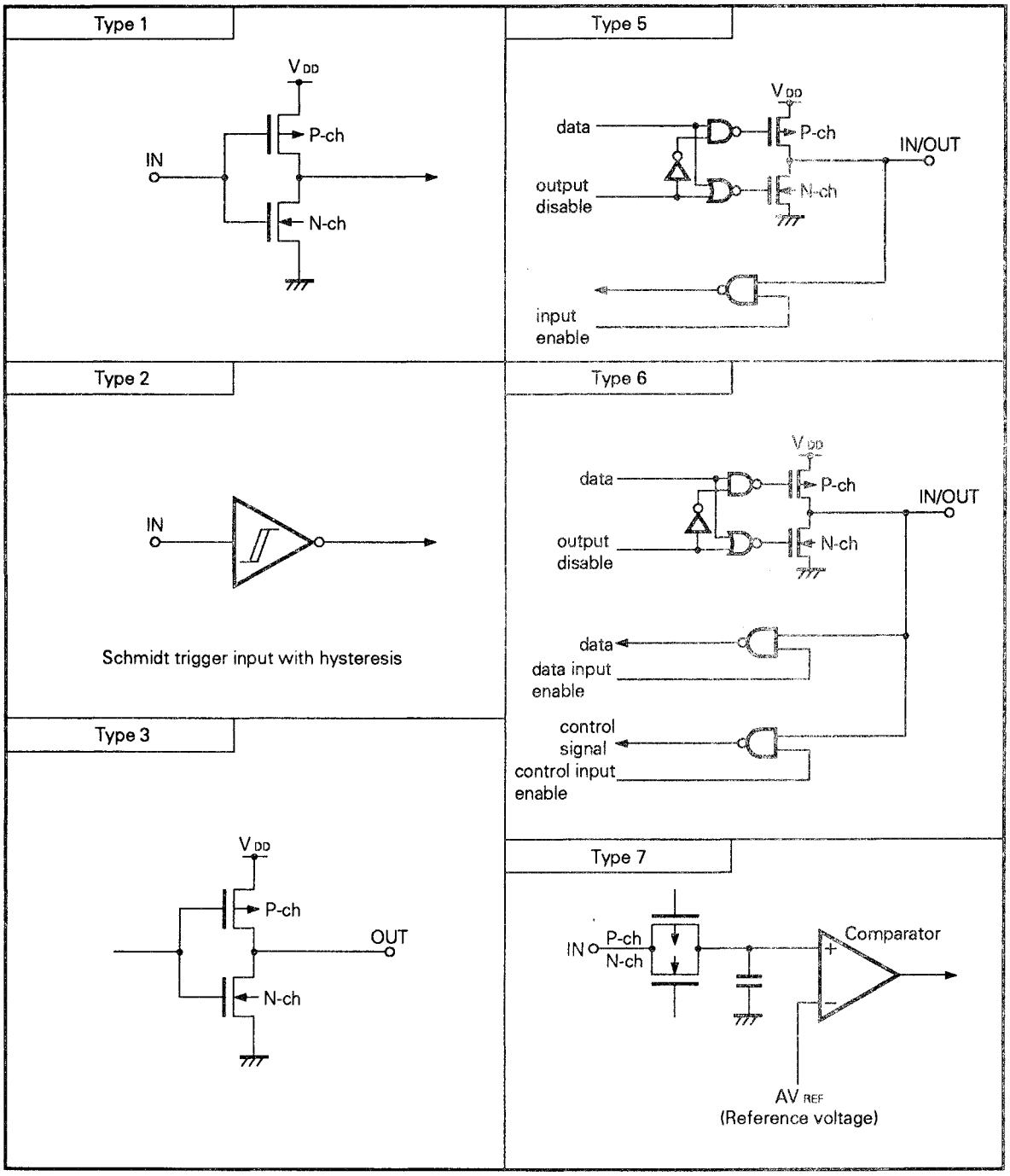


Fig. 1-1 Pin Input/Output Circuits

1.5 RECOMMENDED CONDITIONS FOR UNUSED PINS

Pin	Recommended connection
P00-P07 P10-P17	Input mode: Connect to V_{DD} through a pull-up resistor Output mode: Open
P20-P23	Connect to Vss
P30-P33	Connect to either Vss or V_{DD}
P24-P27 P34-P37 P40-P47 P50-P57	Input mode: Connect to V_{DD} through a pull-up resistor Output mode: Open
$\overline{WR}$ $\overline{RD}$ ALE $\overline{RFSH}$	Open
AN0-AN3	Connect to either Vss or V_{DD}
AV_{REF} AVss	Connect to Vss

2. COMPARISON OF FAMILY PRODUCTS

The μPD78P312A is a version of the μPD78312A in which the internal mask ROM is replaced with an one-time PROM or EPROM. The μPD78P312A is an upgraded version of the μPD78P312. Table 2-1 shows a comparison of the μPD78P312A, μPD78312A, and μPD78310A. Table 2-2 shows a comparison of the μPD78P312A and μPD78P312. Except where noted, these products are identical with respect to function.

Refer to the documents provided for the μPD78312A and μPD78310A for details concerning the internal hardware such as CPU functions.

Table 2-1 Comparison of μPD78P312A, μPD78312A, and μPD78310A

Item		μPD78P312A	μPD78312A	μPD78310A
Program memory		• PROM • 8,192 x 8 bits	• Mask ROM • 8,192 x 8 bits	• Not internally provided
Pin function	PROM programming mode	Provided	None	
	Ports 4, 5	Provided	Provided	None (These ports always serve as the address bus, data bus)
	$\overline{EA}$	Provided		Provided (However, must be operated with this pin set to low)
External memory access		External memory can be expanded in steps by 256 bytes, 4K bytes, 16K bytes, or 56K bytes, using the memory expansion mode register (MM).		Always accesses 64K bytes of the external memory (regardless of the setting in the memory expansion mode register (MM).
Package	Without window	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QUIP • 64-pin plastic QFP (14 x 20 mm) • 68-pin plastic QFJ (□ 950 mil)		
	With window	• 64-pin ceramic shrink DIP with window (750 mil) • 64-pin ceramic QUIP with window	None	

Table 2-2 Difference Between μPD78P312A and μPD78P312

Item	μPD78P312A	μPD78P312
Mode 4 in count unit (4 x multiplication mode)	Provided	Not provided
Count start triggered by external pulse of interval timer	Provided	Not provided
16 bit data transfer instruction used between memory and a pair register • MOVW rp1, !addr 16 instruction • MOVW !addr 16, rp1 instruction	Provided	Not provided

3. PROM PROGRAMMING

The ROM contained in μPD78P312A is an electrically erasable PROM with 8,192 x 8 bit configuration. The pins listed in the table below are used to program the PROM.

When used in the normal operation mode, 5 V ±10% is applied to the V_{DD} and V_{PP} pins. A voltage higher than V_{DD} should not be applied to other pins.

The programming characteristics of the μPD78P312A are identical to those of the μPD27C256A.

Pin Name	Function
V_{PP}	High voltage input (write/verify mode), high level input (read mode)
PROG	High voltage input (write/verify mode, read mode)
A0-A7	Address input (lower 8 bits)
A8-A12	Address input (upper 8 bits)
D0-D7	Data input (write mode), data output (verify mode)
$\overline{CE}$	Program pulse input
$\overline{OE}$	Output enable input
V_{DD}	Power supply pin

Note: 1. Attach a light baffle film to μPD78P312A with an erase window to protect the EPROM from being erased accidentally.

2. The one-time PROM product, μPD78P312A, cannot be erased by ultraviolet rays, because it is not provided with a window.

3.1 PROM PROGRAMMING MODE

When +6 V is applied to the V_{DD} pin and +12.5 V is applied to the PROG pin and V_{PP} pin, the μPD78P312A enters the program write/verify mode. Operation in this mode is determined according to the setting of $\overline{CE}$ and $\overline{OE}$ pins as indicated in the table below. Additionally, when set to the read mode, the μPD78P312A can read the contents of PROM.

Operation mode specification					Operation mode	
V_{PP}	V_{DD}	$\overline{CE}$	$\overline{OE}$	PROG		
+12.5 V	+6 V	L	H	+12.5 V	Write mode	
		H	L		Verify mode	
		H	H		Program inhibit mode	
$V_{PP}=V_{DD}$=+5 V		L/H	L		Read mode	Data is output from the D0-D7 pins
			H			D0-D7 are high impedance

Remarks: H indicates high level; L indicates low level.

Note: When +12.5 V is applied to V_{PP} and +6 V is applied to V_{DD}, both $\overline{CE}$ and $\overline{OE}$ must not be set to low level (L) simultaneously.

3.2 PROM WRITE PROCEDURE

Data can be written to the PROM using the following procedure. High speed data write operation is possible.

(1) Process the pins not used in accordance with the description in Pin Configuration, and supply +6 V to the V_{DD} pin and +12.5 V to the V_{PP} pin.
(2) Provide the initial address.
(3) Provide write data.
(4) Provide a 1 ms program pulse (active low) to the $\overline{CE}$ pin.
(5) Verify mode. If the data has been written, proceed to (7), if not, repeat steps (3) to (5). If the data cannot be correctly written in 25 attempts, go to step (6).
(6) Classify the PROM as defective and cease write operation.
(7) Provide write data and supply (for additional writing) program pulses for 3 ms times the number of repeats performed between steps (3) to (5).
(8) Increment the address.
(9) Repeat steps (3) to (8) until the end address is reached.

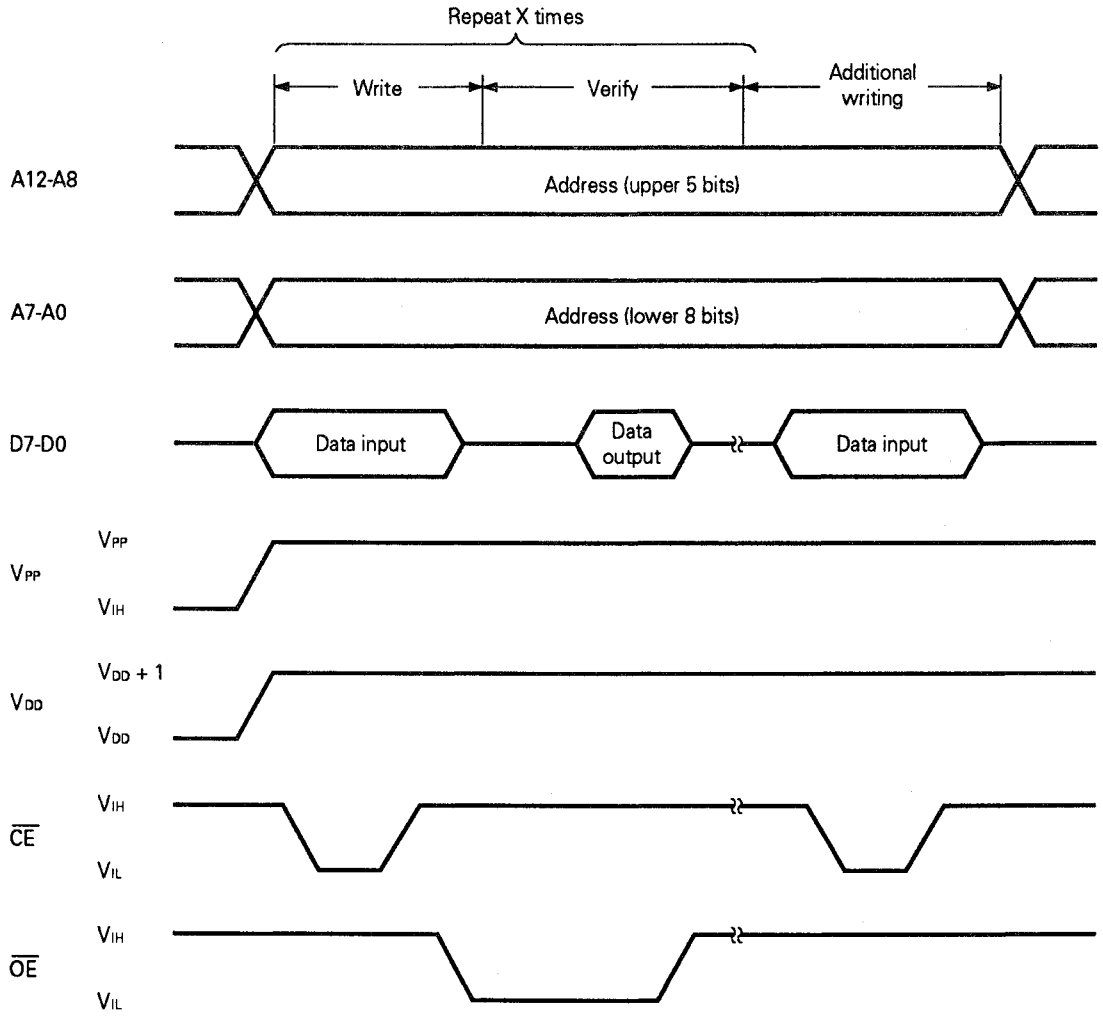


Fig. 3-1 PROM Write/Verify Timing

3.3 PROM READ PROCEDURE

The contents of the PROM can be read out to the external data bus (D0-D7) using the following procedure.

(1) Process the unused pins in accordance with the description in Pin Configuration.
(2) Supply +5 V to the V_{DD} pin and V_{PP} pin, and +12.5 V to the PROG pin.
(3) Input the address of the data to be read to the A0 to A12 pins.
(4) Read mode.
(5) Data is output to the D0 to D7 pins.

Fig. 3-2 shows the timing for this sequence from steps (2) to (5).

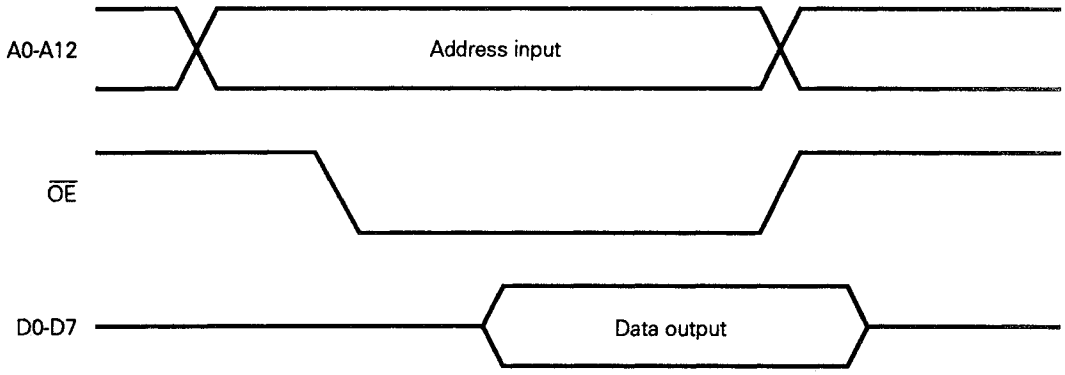


Fig. 3-2 PROM Read Timing

3.4 ERASING PROCEDURE (EPROM PRODUCT ONLY)

Data on the μPD78P312ADW/R EPROM can be erased by exposing the EPROM to light with a wavelength shorter than 400 nm. Therefore, if the EPROM is exposed to direct sunlight or the light of a fluorescent lamp for a long time, the data on the EPROM may be erased. To protect the data, mask the EPROM window with a light baffle film, which is attached as an accessory.

Usually, cast a 254 nm ultraviolet ray onto the window of the EPROM to erase the memory contents. To completely erase the EPROM contents, a minimum of 15 W·s/cm^2 (strength of the ultraviolet light x erase time) of exposure is necessary. This means that, when a 12,000 μW/cm^2 ultraviolet lamp is used, about 15 to 20 minutes are required to completely erase the EPROM contents. The time required to erase the EPROM contents, however, may be lengthened if the file of the ultraviolet lamp used is ending, or if the window of the EPROM is soiled. The distance between the ultraviolet lamp and the window should be 2.5 cm or shorter.

3.5 SCREENING OF ONE-TIME PROM PRODUCTS ★

One-time PROM products (μPD78P312ACW, 78P312AGF-3BE, 78P312AGQ-36, and 78P312AL) cannot be completely tested by NEC before shipment. It is recommended that screening be implemented under the folowing conditions to verify the PROM after the necessary data has been written:

Storage Temperature	Storage Time
125°C	24 hours

NEC offers changed services including writing, printing, screening, and verifying one-time PROMs by the device called a QTOP microcomputer. For details, consult NEC.

4. ELECTRICAL CHARACTERISTICS

Absolute Maximum Rating (Ta = 25°C)

Item	Symbol	Conditions	Rating	Units
Power supply voltage	V_{DD}		-0.5 to +7.0	V
	AV_{REF}		-0.5 to V_{DD}+0.3	V
	AV_{SS}		-0.5 to +0.5	V
	V_{PP}		-0.5 to +13.5	V
Input voltage	V_{I1}	Other than $\overline{RESET}$	-0.5 to V_{DD}+0.5	V
	V_{I2}	$\overline{RESET}$	-0.5 to +13.5	V
Output voltage	V_O		-0.5 to V_{DD}+0.5	V
Low level output current	I_{OL}	Single pin	4.0	mA
		All output pins total	60	mA
High level output current	I_{OH}	Single pin	-2	mA
		All output pins total	-15	mA
Operating temperature	T_{opt}		-10 to +70	°C
Storage temperature	T_{stg}		-65 to +150	°C

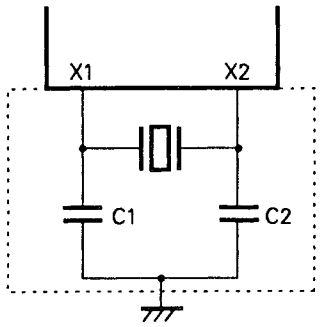
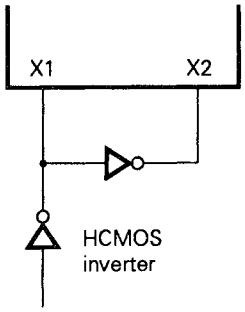
Operating Condition

Item / Oscillation frequency	Ta	V_{DD}
4 MHz ≤ fxx ≤ 12 MHz	-10 to +70°C	+5.0 V ±10%

Capacitance (Ta = 25°C, V_{DD} = V_{SS} = 0 V)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Input capacitance	C_I	f = 1 MHz Pin not used for measurement is 0 V			10	pF
Output capacitance	C_O				20	pF
Input/Output capacitance	C_{IO}				20	pF

Oscillator Characteristics (Ta = -10 to +70°C, V_{DD} = +5.0 V ±10%, V_{SS} = AV_{SS} = 0 V, 4 V ≤ AV_{REF} ≤ V_{DD})

Oscillator	Recommended circuit	Item	MIN.	MAX.	Units
Ceramic oscillator or crystal resonator		Oscillation frequency (fxx)	4	12	MHz
External clock		X1 input frequency (fx)	4	12	MHz
		X1 input rise, fall time (t_{XR}, t_{XF})	0	30	ns
		X1 input high/low level width (t_{WXH}, t_{WXL})	30	130	ns

Notes 1: Oscillator circuit must be located as close as possible to the X1 and X2 pins.

2: To prevent noise from affecting operation, avoid locating other signal lines within portion enclosed in dotted line.

Recommended Oscillator Circuit Constants

Ceramic oscillator

Manufacturer	Product name	Frequency [MHz]	External capacitance [pF]	
			C1	C2
Murata Mfg.	CSA8.00MT CSA10.0MT CSA12.0MT	8.0 10.0 12.0	30	30
	CST8.00MT CST10.0MT CST12.0MT	8.0 10.0 12.0	Internal	Internal
Kyocera	KBR-8.0M KBR-10.0M KBR-12.0M	8.0 10.0 12.0	33	33
TDK	FCR10.0MC FCR12.0MC	10.0 12.0	Internal	Internal

Crystal resonator

Manufacturer	Product name	Frequency [MHz]	External capacitance [pF]	
			C1	C2
Kinseki	HC-49U	8.0 10.0 12.0	22	22

DC Characteristics (Ta = -10°C to +70°C, V_{DD} = +5.0 V ±10%, Vss = 0 V)

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Units
Low level input voltage	V_{IL1}	Other than $\overline{EA}$		0		0.8	V
	V_{IL2}	$\overline{EA}$		0		0.5	V
High level input voltage	V_{IH1}	Except the P20/NMI, X1, X2, $\overline{RESET}$ pins		2.2		V_{DD}	V
	V_{IH2}	P20/NMI, X1, X2 $\overline{RESET}$ pins		3.8		V_{DD}	V
Low level output voltage	V_{OL}	I_{OL} = 2.0 mA				0.45	V
High level output voltage	V_{OH}	I_{OH} = -1.0 mA		V_{DD}-1.0			V
Input current	I_{I1}	P20/NMI, $\overline{RESET}$ 0.45 V < V_I < V_{DD}				±10	μA
Input leakage current	I_{LI}					±10	μA
Input/output leakage current	I_{LO}					±10	μA
AV_{REF} current	AI_{REF}	f_{CLK} = 6 MHz			1.5	5	mA
V_{DD} power supply current	I_{DD1}	Operating mode, f_{CLK} = 6 MHz			30	60	mA
	I_{DD2}	HALT mode, f_{CLK} = 6 MHz			5	15	mA
Data retention voltage	V_{DDDR}	STOP mode		2.5			V
Data retention current	I_{DDDR}	STOP mode	V_{DDDR} = 2.5 V		3	15	μA
			V_{DDDR} = 5.0 V ±10%		10	50	μA

AC Characteristics

Read/Write operation (Ta =-10°C to +70°C, V_{DD} = +5 V ±10%, V_{SS} = 0 V)

Item	Symbol	Conditions	MIN.	MAX.	Units
Internal system clock cycle time *1	t_{CYK}		166	1000	ns
Address set up time (vs. ALE ↓)	t_{SAL}		150		ns
Address hold time (vs. ALE ↓)	t_{HLA}		30		ns
Address → $\overline{RD}$ ↓ delay time	t_{DAR}		233		ns
$\overline{RD}$ ↓ → address float time	t_{FRA}			0	ns
Address → data input time	t_{DAID}			413	ns
ALE ↓ → data input time	t_{DLID}			233	ns
$\overline{RD}$ ↓ → data input time	t_{DRID}			180	ns
ALE ↓ → $\overline{RD}$ ↓ delay time	t_{DLR}		63		ns
Data hold time (vs. $\overline{RD}$ ↑)	t_{HRID}		0		ns
$\overline{RD}$ ↑ → address active time	t_{DRA}		53		ns
$\overline{RD}$ ↑ → ALE ↑ delay time	t_{DRL}		116		ns
$\overline{RD}$ low level width	t_{WRL}		200		ns
ALE high level width	t_{WLH}		126		ns
Address → $\overline{WR}$ ↓ delay time	t_{DAW}		233		ns
ALE ↓ → data output time	t_{DLOD}			193	ns
$\overline{WR}$ ↓ → data output time	t_{DWOD}			100	ns
ALE ↓ → $\overline{WR}$ ↓ delay time *2	t_{DLW}		63		ns
		Refresh mode	116		ns
Data set up time (vs. $\overline{WR}$ ↑)	t_{SODWR}		150		ns
Data set up time (vs. $\overline{WR}$ ↓) *3	t_{SODWF}	Refresh mode	33		ns
Data hold time (vs. $\overline{WR}$ ↑)	t_{HWOD}		20		ns
$\overline{WR}$ ↑ → ALE ↑ delay time	t_{DWL}		116		ns
$\overline{WR}$ low level width	t_{WWL}		200		ns

***1:** The internal system clock (f_{CLK}) is the oscillation clock (f_{XX}) divided by 2 or 8, depending on the STBC register specification. The value in this table is indicated as f_{XX} = 12 MHz and $f_{CLK} = f_{XX}/2$.

***2:** During pulse refresh operation, the falling edge of the $\overline{WR}$ signal is delayed by a half clock. Therefore, the value in the lower row is used as the value of t_{DLW}.

***3:** When accessing a pseudo-static RAM (μPD428128 etc.) from which the data is clocked in at the falling edge of the $\overline{WR}$ signal, the data set up time is not t_{SODWR}, but t_{SODWF}.

Remarks: This table shows the characteristics when the number of weight cycles is 0.

Serial Operation (Ta = -10°C to +70°C, V_{DD} = +5.0 V ±10%, V_{SS} = 0 V)

Item	Symbol	Conditions			MIN.	MAX.	Units
Serial clock cycle time	t_{CYSK}	Output	$\overline{SCK}$	*1	1.33		μs
			$\overline{CTS}$	*2	1.33		μs
		Input	$\overline{CTS}$	*3	1		μs
Serial clock low level width	t_{WSKL}	Output	$\overline{SCK}$	*1	580		ns
			$\overline{CTS}$	*2	580		ns
		Input	$\overline{CTS}$	*3	420		ns
Serial clock high level width	t_{WSKH}	Output	$\overline{SCK}$	*1	580		ns
			$\overline{CTS}$	*2	580		ns
		Input	$\overline{CTS}$	*3	420		ns
$\overline{CTS}$ high, low level width	t_{WCSH}, t_{WCSL}			*4	3		t_{CYK}
RxD set up time (vs. $\overline{CTS}$ ↑)	t_{SRXSK}				80		ns
RxD hold time (vs. $\overline{CTS}$ ↑)	t_{HSKRX}				80		ns
$\overline{SCK}$ ↓ → TxD delay time	t_{DSKTX}					210	ns

*1: When transmitting at 750 kbps in the I/O interface mode.
*2: When receiving at 750 kbps in the I/O interface mode.
*3: When receiving at 1 Mbps in the I/O interface mode.
*4: In the asynchronous mode.

A/D Converter Characteristics (Ta = -10°C to +70°C, V_{DD} = +5 V ±10%, 4 V ≤ AV_{REF} ≤ V_{DD}, AVss = V_{SS} = 0 V)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Resolution			8			bit
Over all error *		4.0 V ≤ AV_{REF} ≤ V_{DD}, 166 ns ≤ t_{CYK} ≤ 500 ns			0.4	%
Quantified error					±1/2	LSB
Conversion time	t_{CONV}	166 ns ≤ t_{CYK} ≤ 250 ns	180			t_{CYK}
		250 ns ≤ t_{CYK} ≤ 500 ns	120			t_{CYK}
Sampling time	t_{SAMP}	166 ns ≤ t_{CYK} ≤ 250 ns	36			t_{CYK}
		250 ns ≤ t_{CYK} ≤ 500 ns	24			t_{CYK}
Analog input	V_{IAN}		-0.3		AV_{REF}+0.3	V
Analog input impedance	R_{AN}			1000		MΩ
Reference voltage	AV_{REF}		4		V_{DD}	V
AV_{REF} current	AI_{REF}	f_{CLK} = 6 MHz		1.5	5.0	mA

*: Not including any quantified errors. Expressed as a percentage of the full-scale value.

Count Unit Operation (Ta = -10°C to +70°C, V_{DD} = +5.0 V ±10%, V_{SS} = 0 V)

Item	Symbol	Conditions	MIN.	MAX.	Units
CI0, CI1 high, low level width	t_{WCIH}, t_{WCIL}		3		t_{CYK}
CTRL0, CTRL1 high, low level width	t_{WCTH}, t_{WCTL}		3		t_{CYK}
CTRL0, CTRL1 set up time (vs. CI ↑)	t_{SCTCI}	When the operation mode of the count unit is specified as mode 3, and the CI pin input to the rising edge is effective	2		t_{CYK}
CTRL0, CTRL1 hold time (vs. CI ↑)	t_{HCICT}	When the operation mode of the count unit is specified as mode 3, and the CI pin input to the rising edge is effective	5		t_{CYK}
CLR0, CLR1 high, low level width	t_{WCRH}, t_{WCRL}		3		t_{CYK}
CI0, CI1 set up time (vs. CI ↑)	t_{S4CTCI}	With the operation mode of the count unit is specified as mode 4	6		t_{CYK}
CI0, CI1 hold time (vs. CI ↑)	t_{H4CICT}	With the operation mode of the count unit is specified as mode 4	6		t_{CYK}
CI0, CI1, CTRL0, CTRL1 cycle time	t_{CYC4}	With the operation mode of the count unit is specified as mode 4	4		μs

Other Operation (Ta = -10°C to +70°C, V_{DD} = +5.0 V ±10%, V_{SS} = 0 V)

Item	Symbol	Conditions	MIN.	MAX.	Units
NMI high, low level width	t_{WNIH}, t_{WNIL}		10		μs
NTE0 high, low level width	t_{WIOH}, t_{WIOL}		3		t_{CYK}
INTE1 high, low level width	t_{WI1H}, t_{WI1L}		3		t_{CYK}
INTE2 high, low level width	t_{WI2H}, t_{WI2L}		3		t_{CYK}
$\overline{\text{RESET}}$ high, low level width	t_{WRSH}, t_{WRSL}		10		μs
V_{DD} rise time (using SBF bit)	t_{R0VD}		4		ms
V_{DD} rise, fall time	t_{RVD}, t_{FVD}		200		μs

External Clock Timing (Ta = -10°C to +70°C, V_{DD} = +5.0 V ±10%, V_{SS} = 0 V)

Item	Symbol	Conditions	MIN.	MAX.	Units
X1 input high level width	t_{WXH}		30	130	ns
X1 input low level width	t_{WXL}		30	130	ns
X1 input rise time	t_{XR}		0	30	ns
X1 input fall time	t_{XF}		0	30	ns
X1 input cycle time	t_{CYX}		83	250	ns

Definition of Bus Timing Depending on t_{CYK}

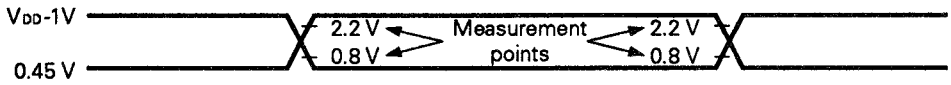
Item	Calculation formula	MIN./MAX.	Units
t_{SAL}	1.5T - 100	MIN.	ns
t_{DAR}	2T - 100	MIN.	ns
t_{DAID}	(3.5 + n)T - 170	MAX.	ns
t_{DLID}	(2 + n)T - 100	MAX.	ns
t_{DRID}	(1.5 + n)T - 70	MAX.	ns
t_{DLR}	0.5T - 20	MIN.	ns
t_{DRL}	T - 50	MIN.	ns
t_{DRA}	0.5T - 30	MIN.	ns
t_{WRL}	(1.5 + n)T - 50	MIN.	ns
t_{WLH}	T - 40	MIN.	ns
t_{DAW}	2T - 100	MIN.	ns
t_{DLOD}	0.5T + 110	MAX.	ns
t_{DLW}	0.5T - 20 (Normal operation)	MIN.	ns
	T - 50 (Refresh mode)	MIN.	ns
t_{SODWR}	(1.5 + n)T - 100	MIN.	ns
t_{SODWF}	0.5T - 50	MIN.	ns
t_{DWL}	T - 50	MIN.	ns
t_{WWL}	(1.5 + n)T - 50 (Normal operation)	MIN.	ns
	(1 + n)T - 50 (Refresh mode)	MIN.	ns

Remarks 1: n is the number of WAIT states inserted by the specification in the MM register.

2: T = t_{CYK} = 1/f_{CLK} (f_{CLK} is the internal system clock frequency)

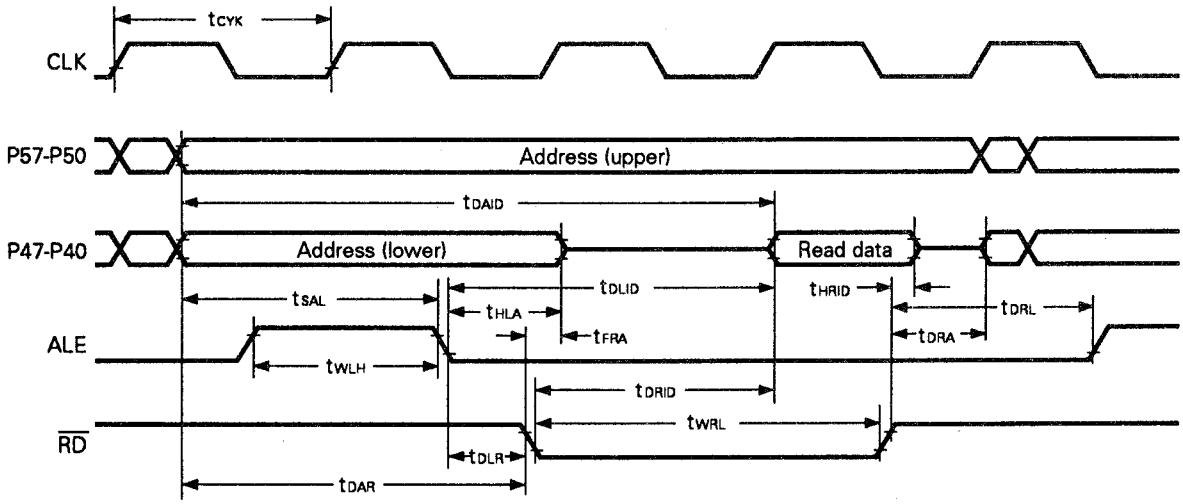
3: Items not shown in this table do not depend on the frequency of the internal system clock (f_{CLK}).

AC Timing Measurement Position

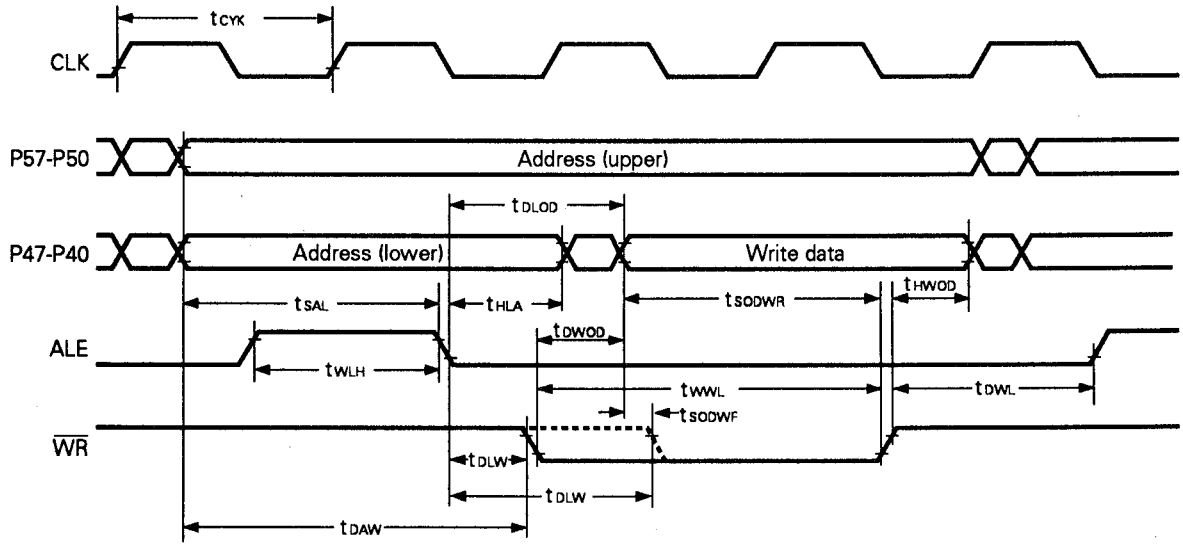


Timing Wave-Forms

Read operation:

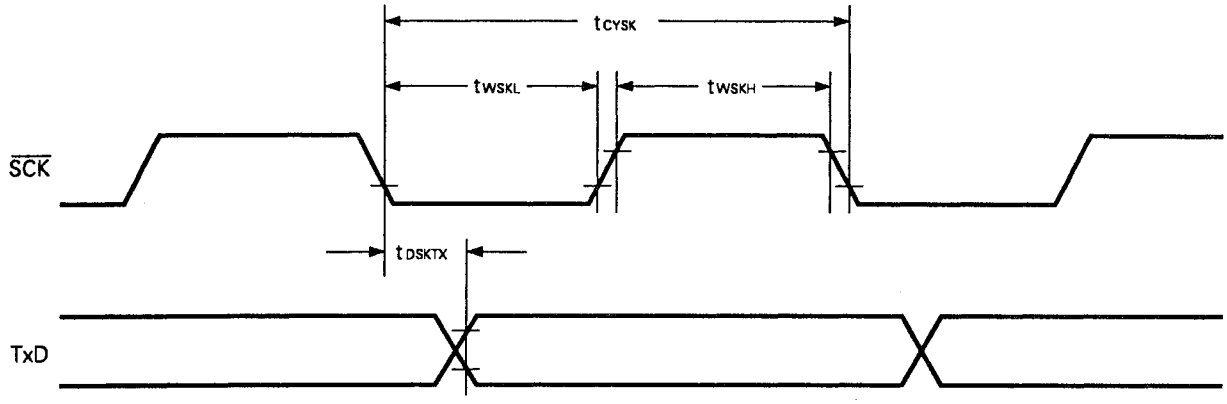


Write operation:

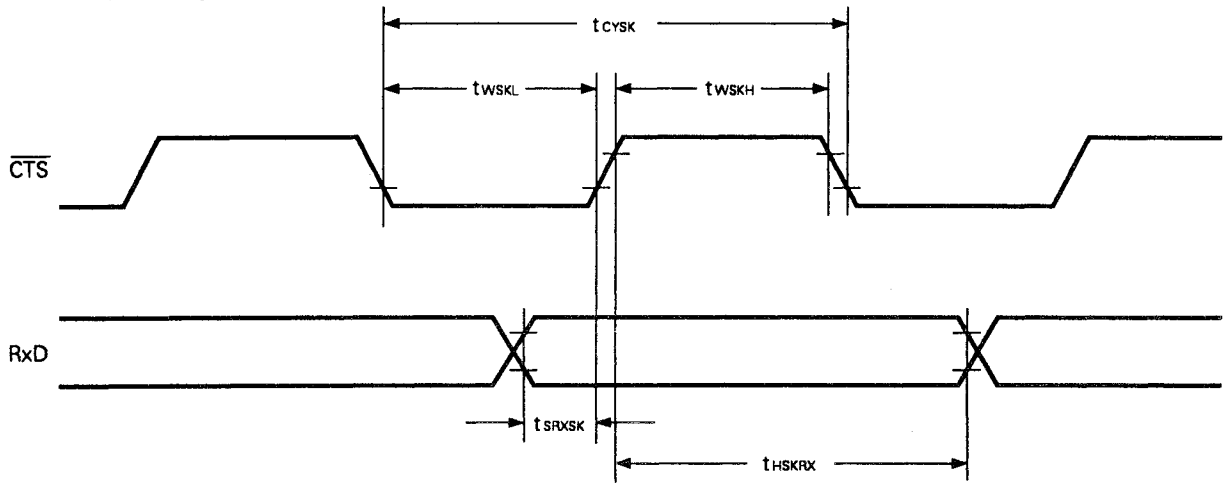


Serial Operation:

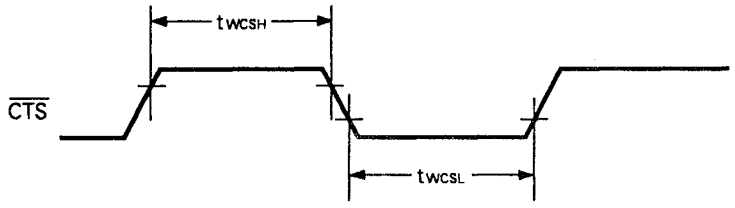
Transmission in I/O interface mode:



Receive in I/O interface mode:

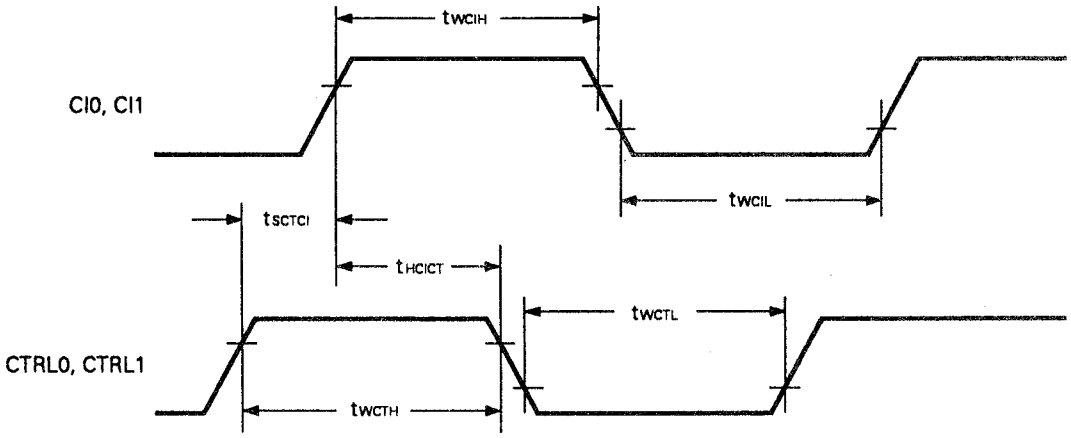


Transmit enable input timing (asynchronous mode):

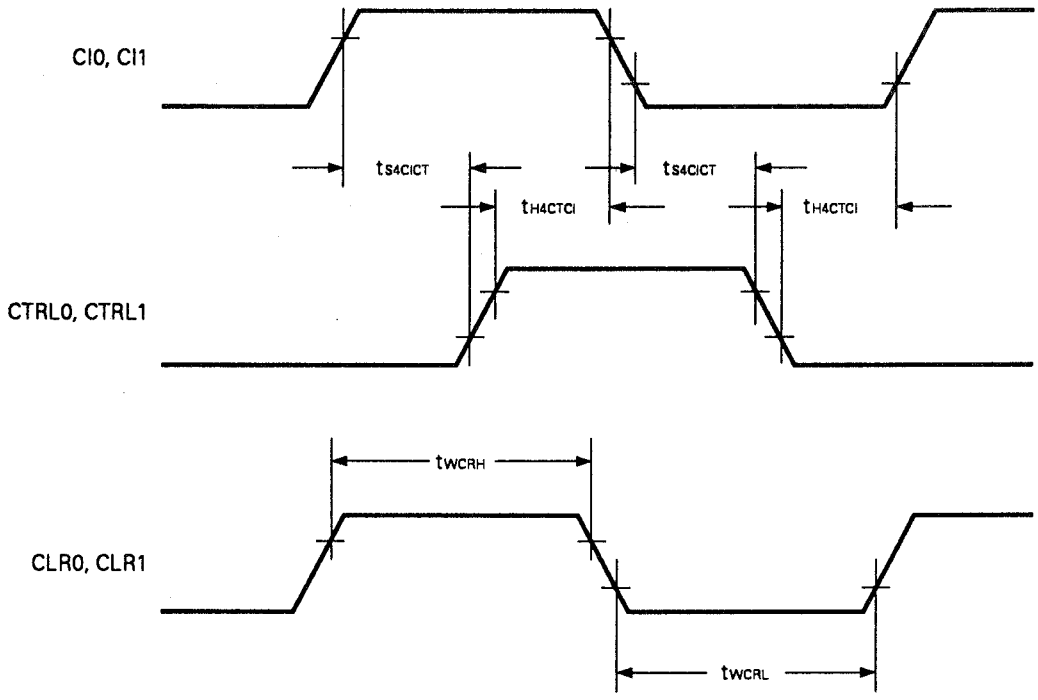


Count Unit Input Timing

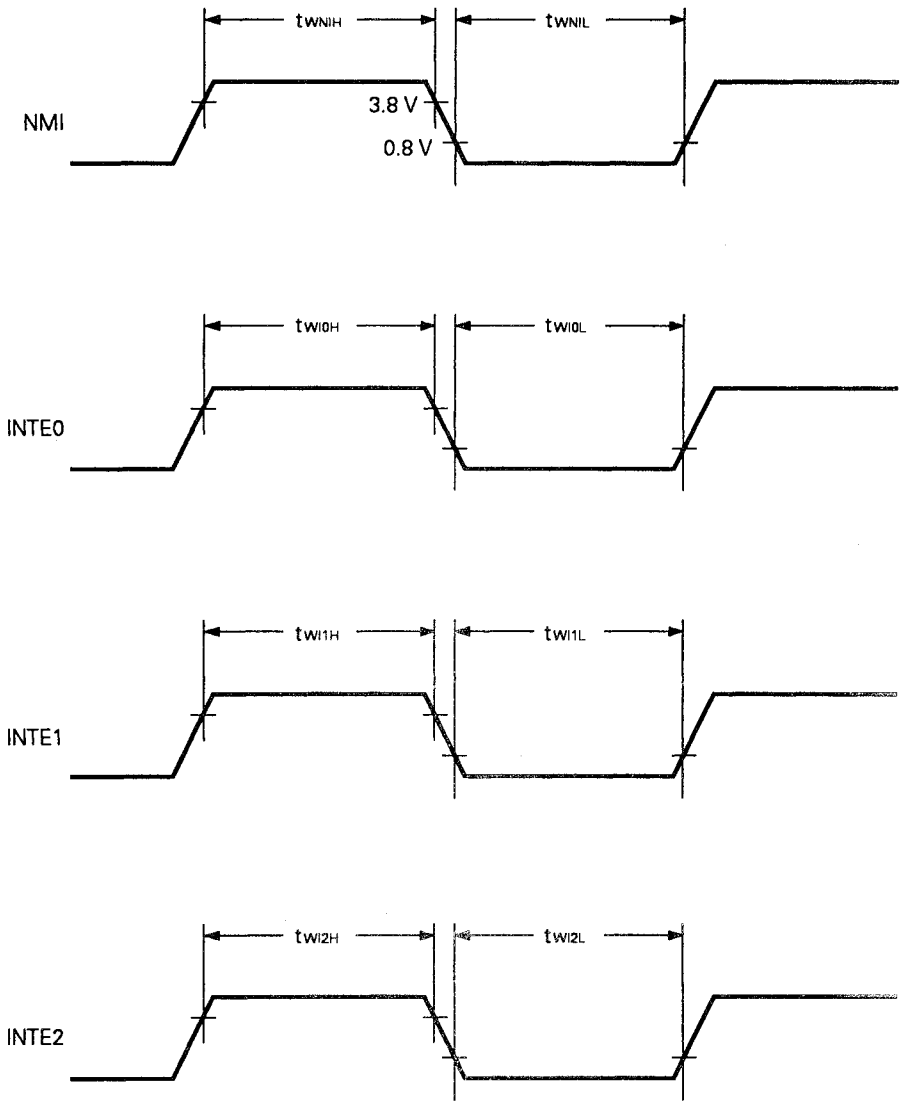
Mode 3 operation



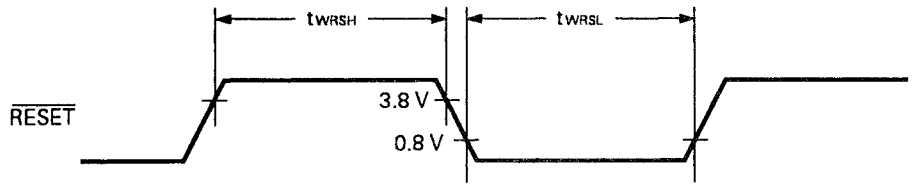
Mode 4 operation



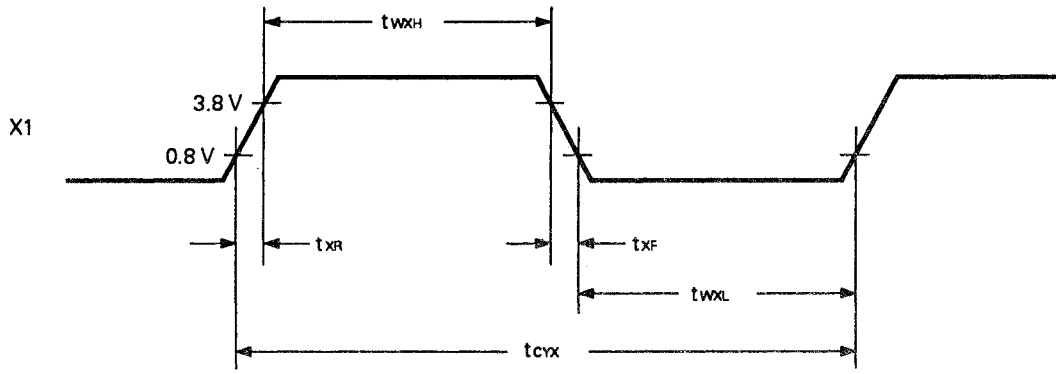
Interrupt Input Timing



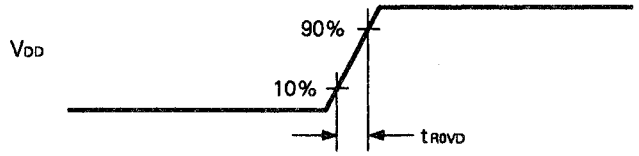
Reset Input Timing



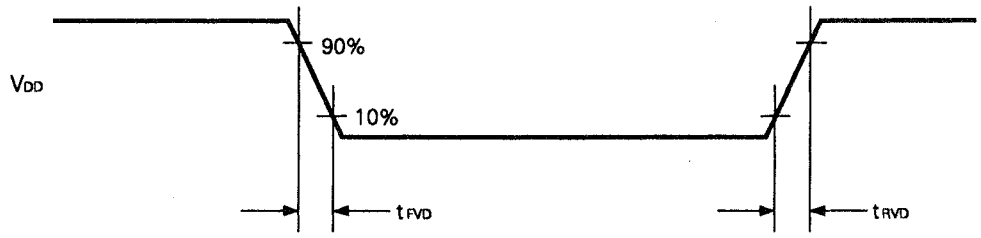
External Clock Timing



Power On Timing



Data Retention Timing



DC Programming Characteristics (T_a = 25 ±5°C, V_{IP} = 12.0 ±0.5 V, V_{SS} = 0 V)

Item	Symbol	Symbol*	Conditions	MIN.	TYP.	MAX.	Units
High level input voltage	V_{IH}	V_{IH}		2.2		V_{DDP} +0.3	V
Low level input voltage	V_{IL}	V_{IL}		-0.3		0.8	V
Input leakage current	I_{LIP}	I_{LI}	$0 \le V_I \le V_{DDP}$			10	μA
High level output voltage	V_{OH}	V_{OH}	I_{OH} = -1.0 mA	V_{DD}-1			V
Low level output voltage	V_{OL}	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output leakage current	I_{LO}	–	$0 \le V_O \le V_{DDP}$, $\overline{OE}$ = V_{IH}			10	μA
PROG pin high voltage input current	I_{IP}	–				±10	μA
V_{DDP} power supply voltage	V_{DDP}	V_{DD}	Program memory write mode	5.75	6.0	6.25	V
			Program memory read mode	4.5	5.0	5.5	V
V_{PP} power supply voltage	V_{PP}	V_{PP}	Program memory write mode	12.2	12.5	12.8	V
			Program memory read mode	V_{PP} = V_{DDP}			V
V_{DDP} power supply current	I_{DD}	I_{DD}	Program memory write mode		10	30	mA
			Program memory read mode $\overline{CE}$ = V_{IL}, V_I = V_{IH}		10	30	mA
V_{PP} power supply current	I_{PP}	I_{PP}	Program memory write mode $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		10	30	mA
			Program memory read mode		1	100	μA

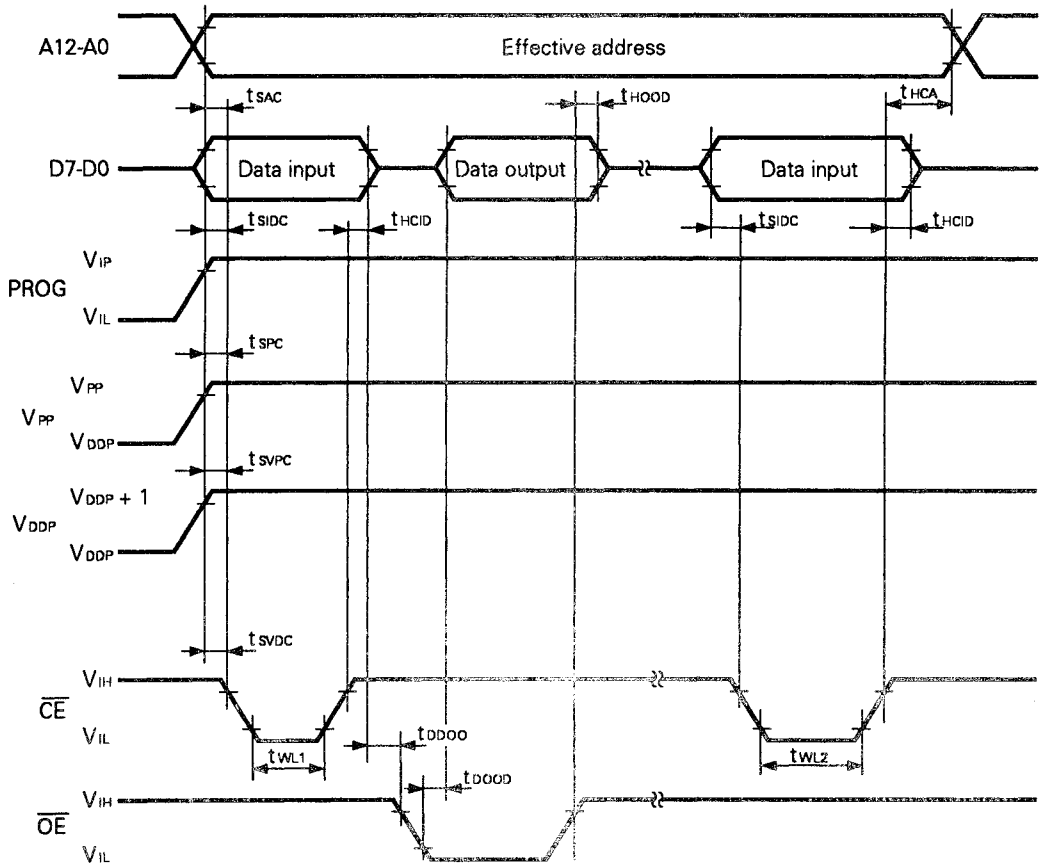
*: Corresponding symbols in the μPD27C256A.

AC Programming Characteristics (T_a = 25 ±5°C, V_{IP} = 12.0 ±0.5 V, V_{SS} = 0 V)

Item	Symbol	Symbol*	Conditions	MIN.	TYP.	MAX.	Units
Address set up time (vs. $\overline{CE}$ ↓)	t_{SAC}	t_{AS}		2			μs
Data → $\overline{OE}$ ↓ delay time	t_{DDOO}	t_{OES}		2			μs
Input data set up time (vs. $\overline{CE}$ ↓)	t_{SIDC}	t_{DS}		2			μs
Address hold time (vs. $\overline{CE}$ ↑)	t_{HCA}	t_{AH}		2			μs
Input data hold time (vs. $\overline{CE}$ ↑)	t_{HCID}	t_{DH}		2			μs
Output data hold time (vs. $\overline{OE}$ ↑)	t_{HOOD}	t_{DF}		0		130	ns
V_{PP} set up time (vs. $\overline{CE}$ ↓)	t_{SVPC}	t_{VPS}		2			μs
V_{DDP} set up time (vs. $\overline{CE}$ ↓)	t_{SVDC}	t_{VDS}		2			μs
Initial program pulse width	t_{WL1}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{WL2}	t_{OPW}		2.85		78.75	ms
PROG high voltage input set up time (vs. $\overline{CE}$ ↓)	t_{SPC}	–		2			μs
Address → Data output time	t_{DAOD}	t_{ACC}	$\overline{OE}$ = V_{IL}			2	μs
$\overline{OE}$ ↓ → Data output time	t_{DOOD}	t_{OE}				1	μs
Data hold time (vs. $\overline{OE}$ ↑)	t_{HCOD}	t_{DF}		0		130	ns
Data hold time (vs. Address)	t_{HAOD}	t_{OH}	$\overline{OE}$ = V_{IL}	0			ns

*: Corresponding symbols in the μPD27C256A.

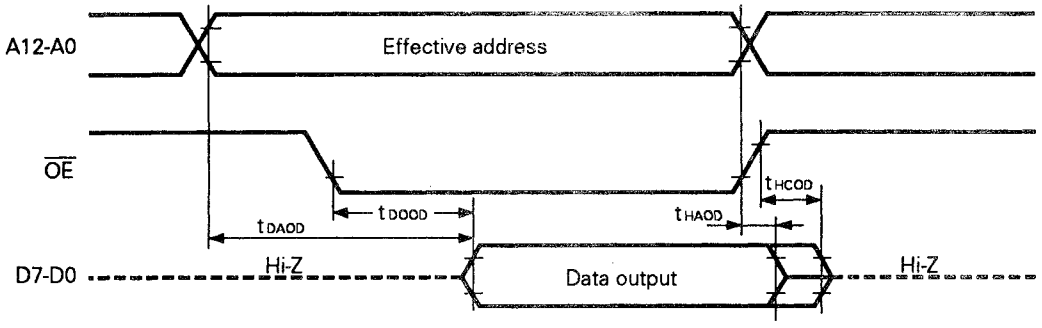
PROM Write Mode Timing



Notes 1: V_{DDP} must applied before V_{PP} is applied, must be removed after V_{PP} is removed.

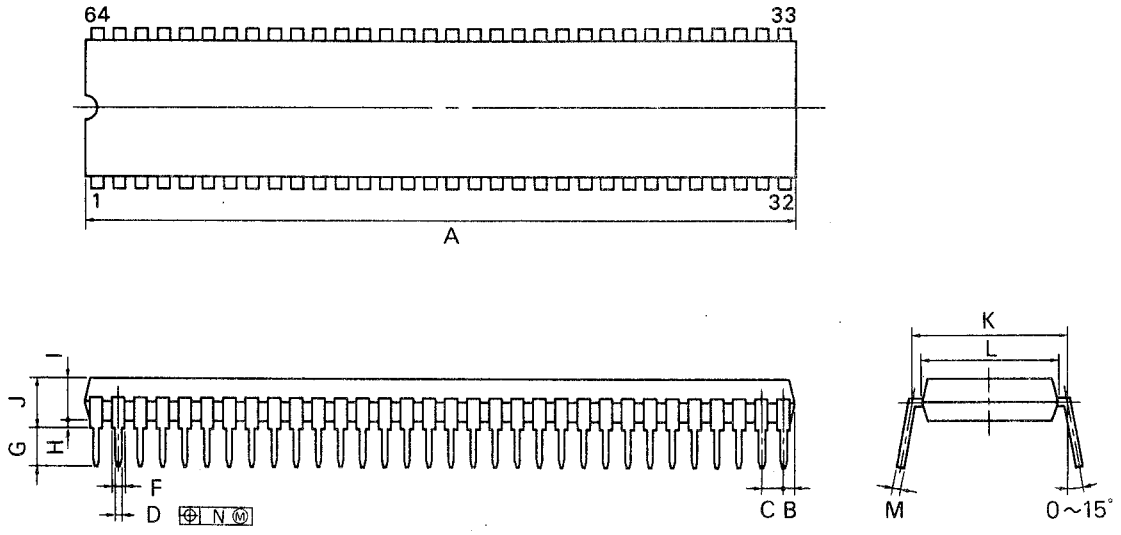
2: V_{PP} must not exceed +13 V, including overshoot voltage.

PROM Read Mode Timing



5. EXTERNAL DIMENSIONS

64PIN PLASTIC SHRINK DIP (750 mil)



P64C-70-750A,C

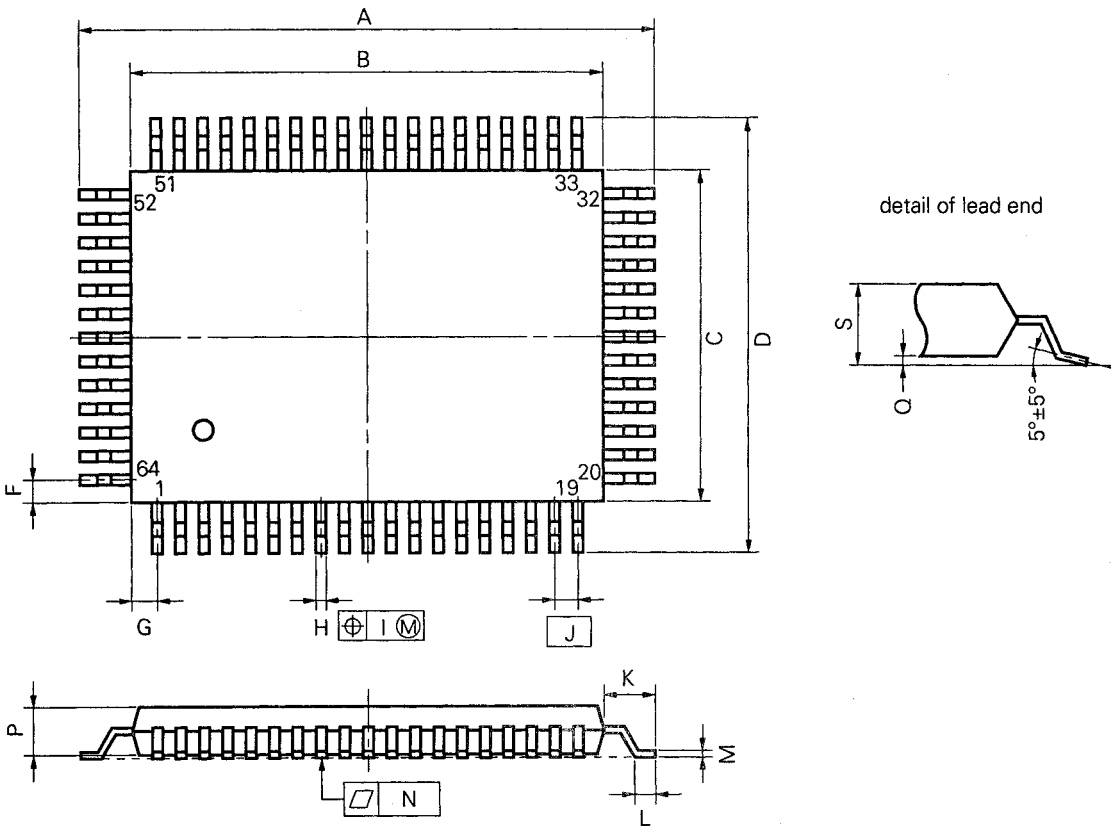
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

64 PIN PLASTIC QFP (14×20)



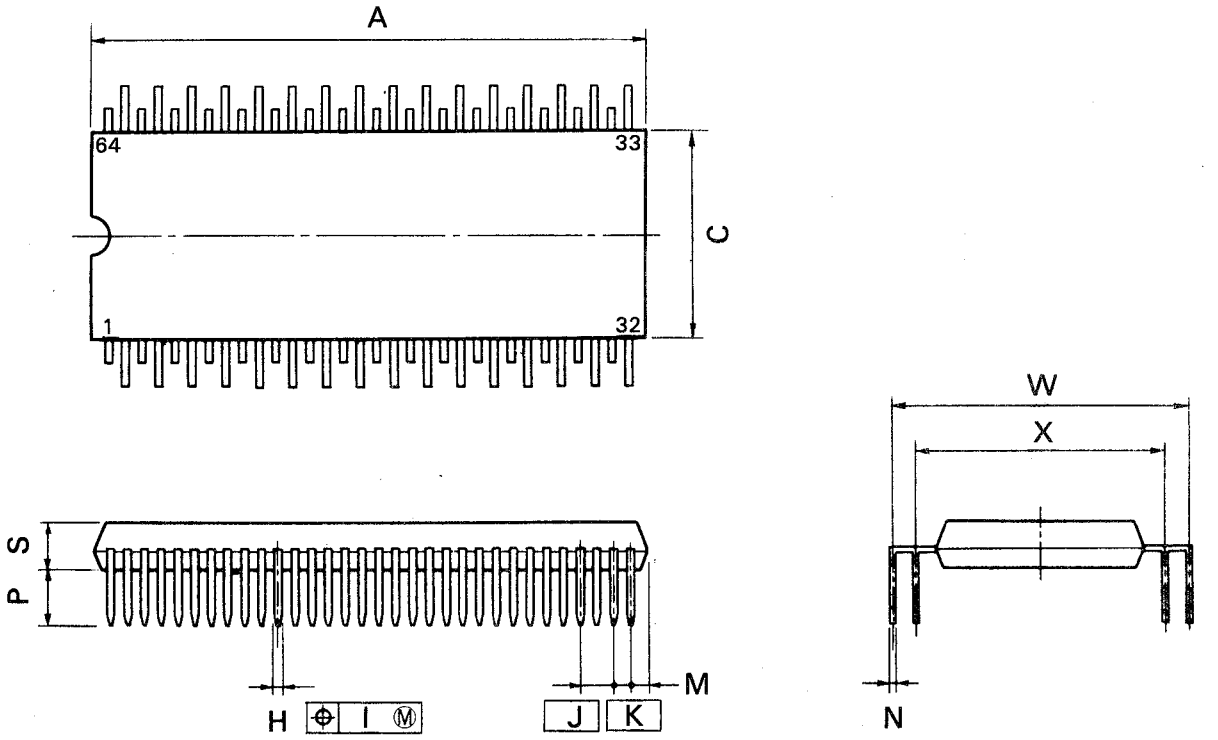
P64GF-100-3B8,3BE,3BR-1

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.12	0.005
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

64 PIN PLASTIC QUIP



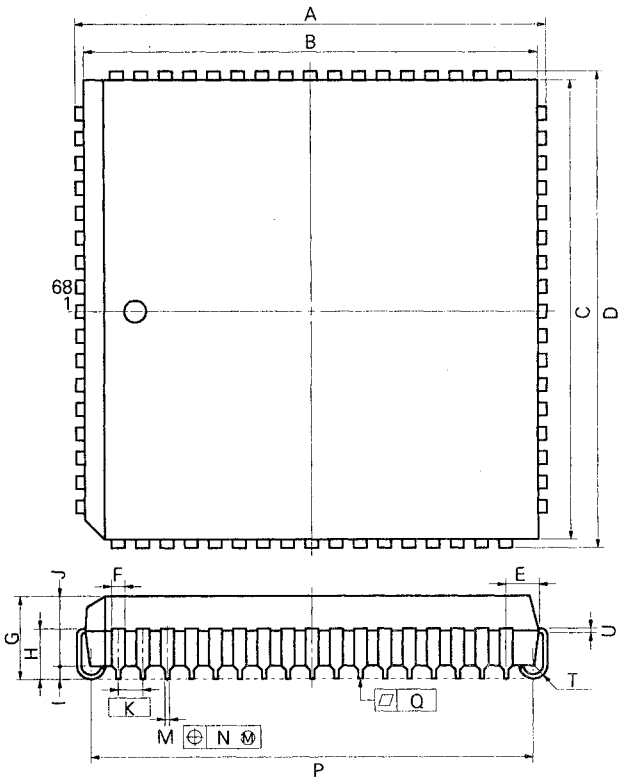
P64GQ-100-36

NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$41.5^{+0.3}_{-0.2}$	$1.634^{+0.012}_{-0.008}$
C	16.5	0.650
H	$0.50^{\pm0.10}$	$0.020^{+0.004}_{-0.005}$
I	0.25	0.010
J	2.54 (T.P.)	0.100 (T.P.)
K	1.27 (T.P.)	0.050 (T.P.)
M	$1.1^{+0.25}_{-0.15}$	$0.043^{+0.011}_{-0.006}$
N	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
P	$4.0^{\pm0.3}$	$0.157^{+0.013}_{-0.012}$
S	$3.6^{\pm0.1}$	$0.142^{+0.004}_{-0.005}$
W	$24.13^{\pm1.05}$	$0.950^{\pm0.042}$
X	$19.05^{\pm1.05}$	$0.750^{\pm0.042}$

68 PIN PLASTIC QFJ (□950 mil)



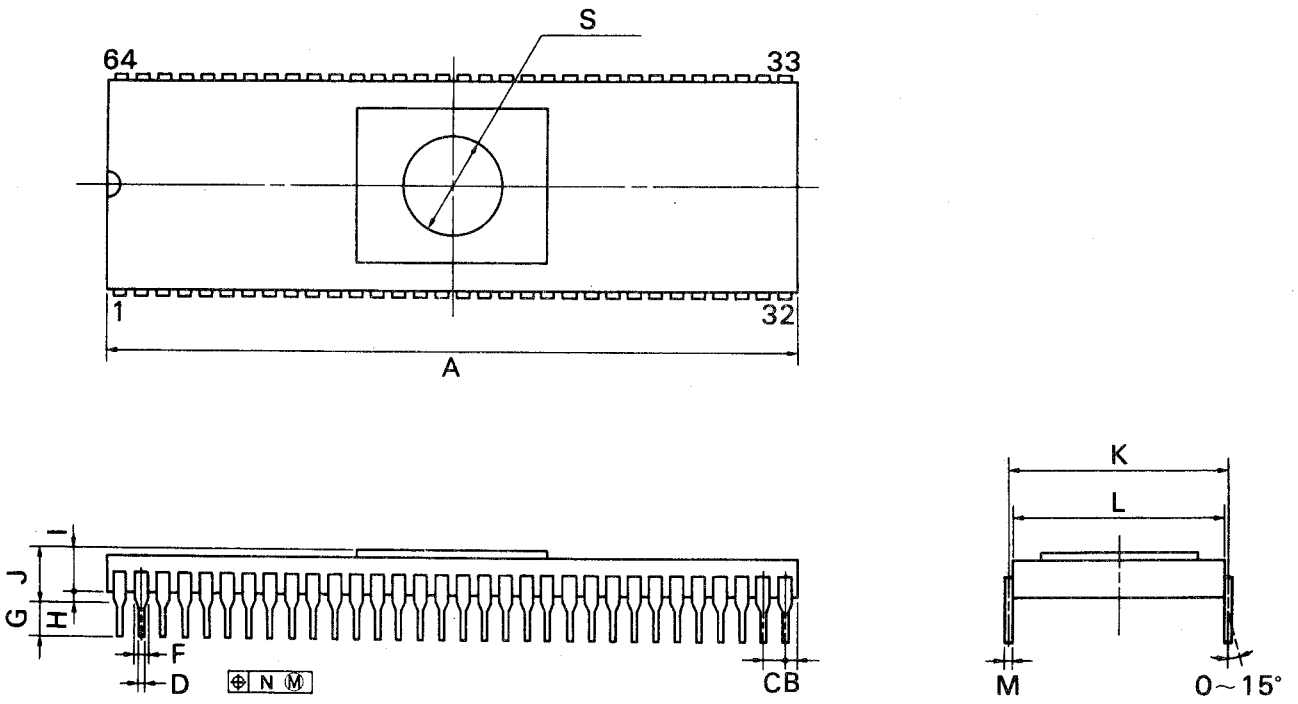
P68L-50A1-2

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	25.2±0.2	0.992±0.008
B	24.20	0.953
C	24.20	0.953
D	25.2±0.2	0.992±0.008
E	1.94±0.15	$0.076^{+0.007}_{-0.006}$
F	0.6	0.024
G	4.4±0.2	$0.173^{+0.009}_{-0.008}$
H	2.8±0.2	$0.110^{+0.009}_{-0.008}$
I	0.9 MIN.	0.035 MIN.
J	3.4	0.134
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±1.0	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	23.12±0.20	$0.910^{+0.009}_{-0.008}$
Q	0.15	0.006
T	R 0.8	R 0.031
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

64PIN CERAMIC SHRINK DIP (750 mil)



P64DW-70-750A

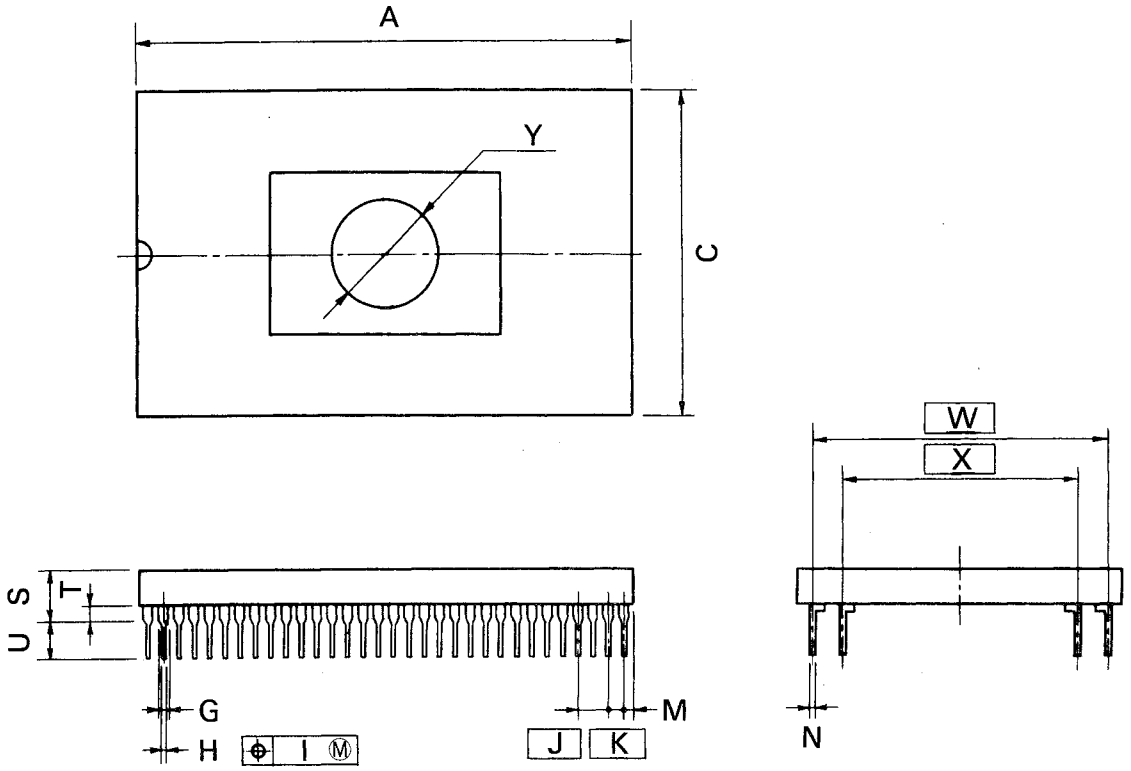
NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.310 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.46^{\pm 0.05}$	$0.018^{\pm 0.002}$
F	0.8 MIN.	0.031 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	1.0 MIN.	0.039 MIN.
I	3.0	0.118
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	18.8	0.740
M	$0.25^{\pm 0.05}$	$0.010^{+0.002}_{-0.003}$
N	0.25	0.01
S	$\phi 8.89$	$\phi 0.350$

64 PIN CERAMIC QUIP (WINDOW)



P64RQ-100-A

NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	41.91 MAX.	1.650 MAX.
C	$26.67^{\pm 0.4}$	$1.050^{\pm 0.016}$
G	0.92 MIN.	0.036 MIN.
H	$0.46^{\pm 0.05}$	$0.018^{\pm 0.002}$
I	0.25	0.010
J	2.54 (T.P.)	0.100 (T.P.)
K	1.27 (T.P.)	0.050 (T.P.)
M	1.27 MAX.	0.050 MAX.
N	$0.25^{\pm 0.05}$	$0.010^{+0.002}_{-0.003}$
S	4.72 MAX.	0.186 MAX.
T	1.0 MIN.	0.039 MIN.
U	$3.5^{\pm 0.3}$	$0.138^{+0.012}_{-0.013}$
W	24.13	0.950
X	19.05	0.750
Y	ϕ8.89	ϕ0.350

6. RECOMMENDED SOLDERING CONDITIONS

It is recommended that μPD78P312A be soldered under the following conditions.

For details on the recommended soldering conditions, refer to Information Document "Semiconductor Devices Mounting Manual" (IEI-616).

The soldering methods and conditions are not listed here, consult NEC.

Table 6-1 Soldering Conditions of Surface Mount Type

μPD78P312AGF-3BE: 64-pin plastic QFP (14 x 20 mm)

Soldering Method	Soldering Conditions	Recommended Conditions Reference Code
Infrared Reflow	Package peak temperature: 230°C, time: 30 seconds max. (210°C min.), number of times: 1, maximum number of days: 2 days* (beyond this period, 16 hours of pre-baking is required at 125°C)	IR30-162-1
VPS	Package peak temperature: 215°C, time: 40 seconds max. (200°C min.), numbr of times: 1, maximum number of days: 2 days* (beyond this period, 16 hours of pre-baking is required at 125°C)	VP15-162-1
Pin Partial Heating	Pin temperature: 300°C max., time: 3 seconds max. (per side)	—

*: Number of days after unpacking the dry pack. Storage conditions are 25°C and 65%RH max..

Caution: Do not use two or more soldering methods in combination (except the pin partial hearting method).

Table 6-2 Soldering Conditions of Surface Mount Type

μPD78P312AL: 64-pin plastic QFJ (□ 950 mil)

Soldering Method	Soldering Conditions	Recommended Conditions Reference Code
VPS	Package peak temperature: 215°C, time: 40 seconds max. (200°C), number of times: 1	VP15-00-1
Pin Partial Heating	Pin temperature: 300°C max., time: 3 seconds max. (per side)	—

Caution: Do not use two or more soldering methods in combination (except the pin partial heating method).

Table 6-3 Soldering Conditions of Through-Hole Type ★

μPD78P312ACW: 64-pin plastic shrink DIP (750 mil)
μPD78P312AGQ-36: 64-pin plastic QUIP
μPD78P312ADW: 64-pin shrink DIP with Ceramic Window (750 mil)
μPD78P312AR: 64-pin QUIPwith Ceramic Window

Soldering Method	Soldering Conditions
Wave Soldering (Only for lead part)	Solder bath temperature: 260°C max., time: 10 seconds max.
Pin Partial Heating	Pin temperature: 260°C max., time: 10 seconds max.

Caution: The wave soldering must be performed at the lead part only. Note that the solder must not be directly contacted to the package body.

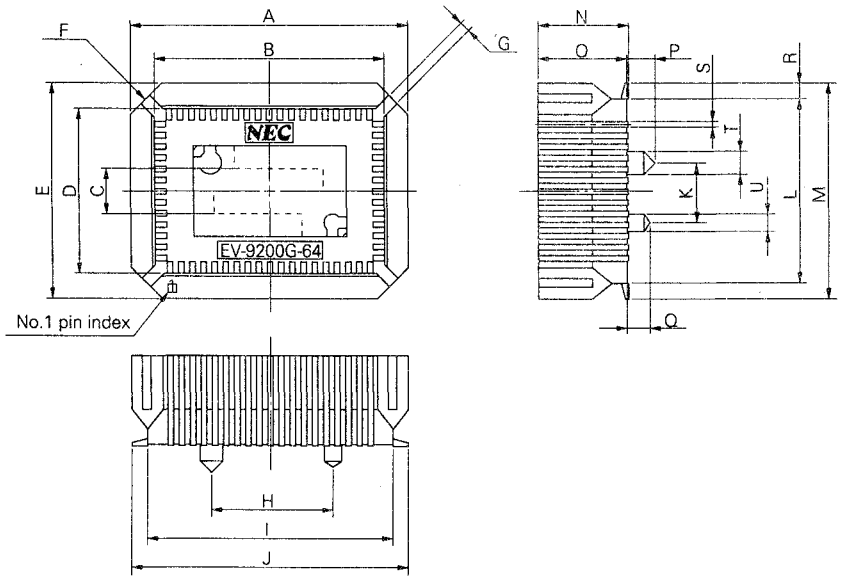
Notice ★

A model that can be soldered under the more stringent conditions (infrared reflow peak temperature: 235°C, number of times: 2, and an extended number of days) is also available.
For details, consult NEC.

APPENDIX A. DIMENTIONS OF CONVERSION SOCKET AND RECOMMENDED MOUNTING PATTERN

Connect the emulation prove for μPD78P312AGF-3BE (EP-78310GF) to the target system in conbination with a conversion socket (EV-9200G-64).

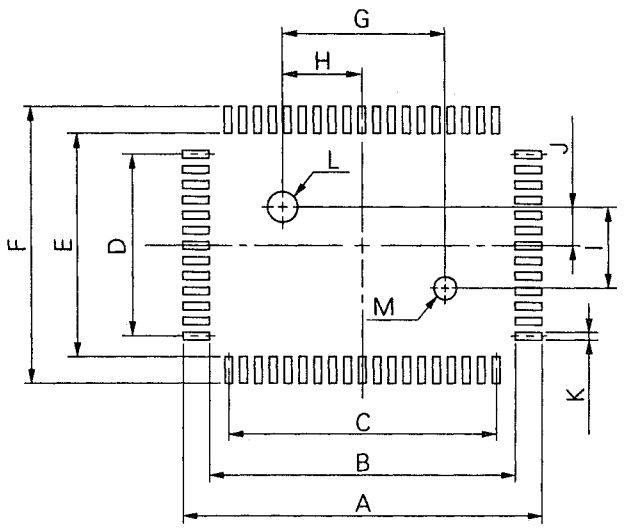
The dimensions of the conversion socket and recommended mounting pattern are shown below.



EV-9200G-64-G0

ITEM	MILLIMETERS	INCHES
A	25.0	0.984
B	20.30	0.799
C	4.0	0.157
D	14.45	0.569
E	19.0	0.748
F	4-C 2.8	4-C 0.11
G	0.8	0.031
H	11.0	0.433
I	22.0	0.866
J	24.7	0.972
K	5.0	0.197
L	16.2	0.638
M	18.9	0.744
O	8.0	0.315
N	7.8	0.307
P	2.5	0.098
Q	2.0	0.079
R	1.35	0.053
S	0.35±0.1	$0.014^{+0.004}_{-0.005}$
T	φ2.3	φ0.091
U	φ1.5	φ0.059

Fig. A-1 Conversion Socket (EV-9200G-64) (Reference) (Unit: mm)



EV-9200G-64-P0

ITEM	MILLIMETERS	INCHES
A	25.7	1.012
B	21.0	0.827
C	$1.0\pm0.02\times18=18.0\pm0.05$	$0.039^{+0.002}_{-0.001}\times0.709=0.709^{+0.002}_{-0.003}$
D	$1.0\pm0.02\times12=12.0\pm0.05$	$0.039^{+0.002}_{-0.001}\times0.472=0.472^{+0.003}_{-0.002}$
E	15.2	0.598
F	19.9	0.783
G	11.00 ± 0.08	$0.433^{+0.004}_{-0.003}$
H	5.50 ± 0.03	$0.217^{+0.001}_{-0.002}$
I	5.00 ± 0.08	$0.197^{+0.003}_{-0.004}$
J	2.50 ± 0.03	$0.098^{+0.002}_{-0.001}$
K	0.6 ± 0.02	$0.024^{+0.001}_{-0.002}$
L	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
M	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Fig. A-2 Recommended Conversion Socket (EV-9200G-64) Mounting Pattern (Reference) (Unit: mm)

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are optionally available :

Hardware

IE-78310A-R	This is an in-circuit emulator that can be used for developing and debugging an application system. It is connected to the host system when debugging is performed. Since the in-circuit emulater can transfer object files with the host machine, if enables efficient debugging to be performed.
EP-78310CW EP-78310GF EP-78310GQ EP-78310L	These emulation probes connect IE-78310A-R to the user system.
PG-1500	This is a PROM programmer that can program single-chip microcomputers with PROM in either stand-alone mode or under control of a host machine, when connected to the supplied accessory board and a programmer adapter. It can program typical PROMs from 256 K-bit to 4 M-bit models.
PA-78P312CW PA-78P312GF PA-78P312GQ PA-78P312L	These PROM programmer adapters write programs to the μPD78P312A with a general-purpose PROM programmer such as PG-1500. PA-78P312CW ----- for μPD78P312ACW, 78P312ADW PA-78P312GF ------ for μPD78P312AGF-3BE PA-78P312GQ ----- for μPD78P312AGQ-36, 78P312AR PA-78P312L ------- for μPD78P312AL

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Other PROM Programmer

The following PROM Programmer can also be used to program the μPD78P312A :

Manufacturer	Product Name
Data I/O Japan	UNISITE 2900
Ando Electric	AF-9704 AF-9705

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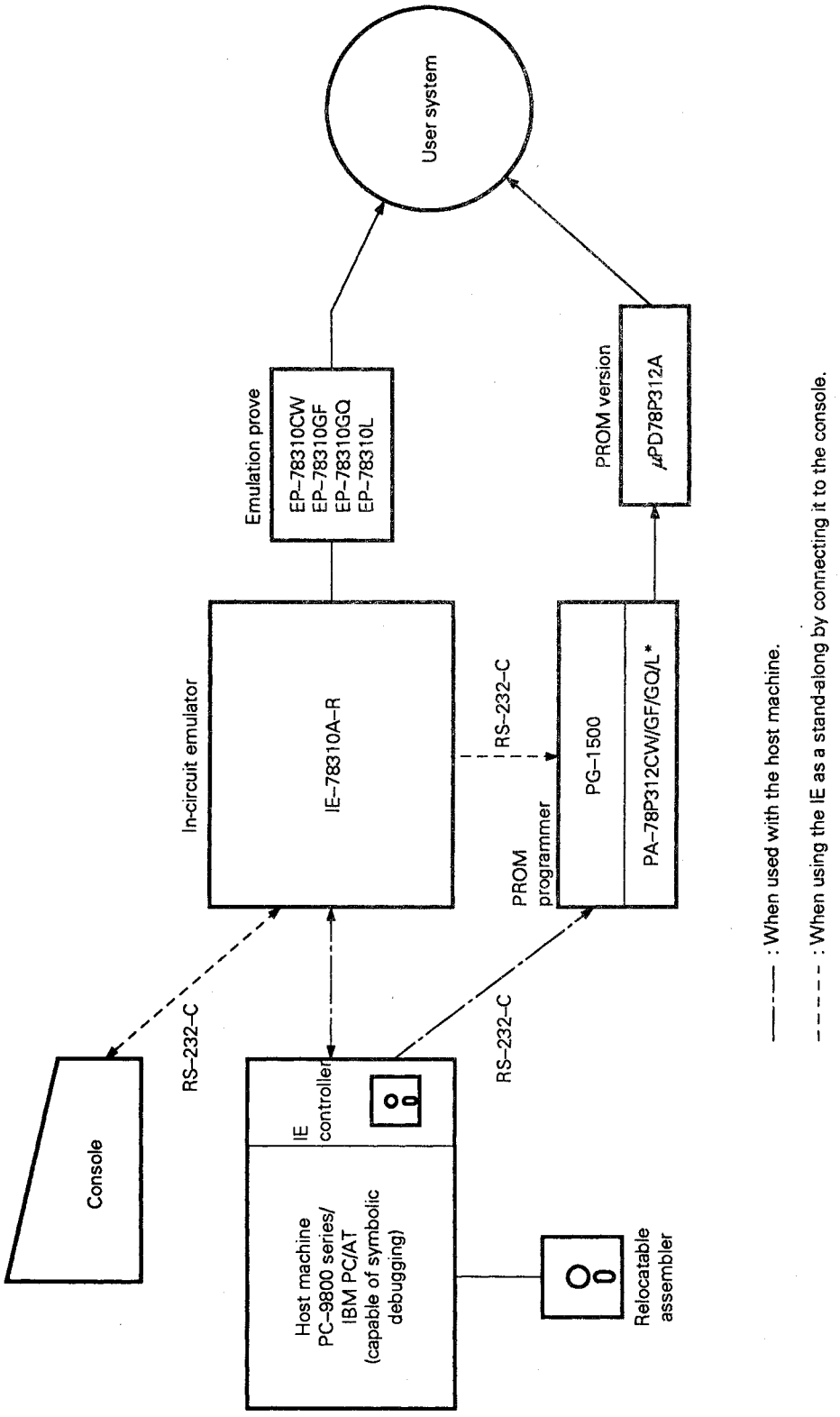
Software

IE-78310A-R Control Program (IE Controller)	Host Machine	OS	Supply Media	Ordering Code (product name)
	PC-9800 series	MS-DOS™	8" 2D *	μS5A1IE78310-P01
			3.5" 2HD	μS5A13IE78310
			5" 2HD	μS5A10IE78310-P01
	IBM PC/AT™	PC DOS™	5" 2HC	μS7B10IE78310
78K/III Series Relocatable Assembler	Host Machine	OS	Supply Media	Ordering Code (product name)
	PC-9800 series	MS-DOS	8" 2D *	μS5A1RA78K3
			3.5" 2HD	μS5A13RA78K3
			5" 2HD	μS5A10RA78K3
	IBM PC/AT	PC DOS	5" 2HC	μS7B10RA78K3
PG-1500 Controller	Host Machine	OS	Supply Media	Ordering Code (product name)
	PC-9800 series	MS-DOS	3.5" 2HD	μS5A13PG1500
			5" 2HD	μS5A10PG1500
	IBM PC/AT	PC DOS	5" 2HC	μS7B10PG1500

* : The 8" 2D model has been superseded by the 5" 2HD or 3.5" 2HD model. If you already have the 8" 2D model, the 5" 2HD model will be supplied for future upgrading.

Remarks : The operation of each software package is guaranteed only with the above host machine and OS.

DEVELOPMENT TOOL CONFIGURATION*



GENERAL NOTES ON CMOS DEVICES

① STATIC ELECTRICITY (ALL MOS DEVICES)

Exercise care so that MOS devices are not adversely influenced by static electricity while being handled.

The insulation of the gates of the MOS device may be destroyed by a strong static charge. Therefore, when transporting or storing the MOS device, use a conductive tray, magazine case, or conductive buffer materials, or the metal case NEC uses for packaging and shipment, and use grounding when assembling the MOS device system. Do not leave the MOS device on a plastic plate and do not touch the pins of the device.

Handle boards on which MOS devices are mounted similarly .

② PROCESSING OF UNUSED PINS (CMOS DEVICES ONLY)

Fix the input level of CMOS devices.

Unlike bipolar or NMOS devices, if a CMOS device is operated with nothing connected to its input pin, intermediate level input may be generated due to noise, and an inrush current may flow through the device, causing the device to malfunction. Therefore, fix the input level of the device by using a pull-down or pull-up resistor. If there is a possibility that an unused pin serves as an output pin (whose timing is not specified), each pin should be connected to V_{DD} or GND through a resistor.

Refer to "Processing of Unused Pins" in the documents of each devices.

③ STATUS BEFORE INITIALIZATION (ALL MOS DEVICES)

The initial status of MOS devices is undefined upon power application.

Since the characteristics of an MOS device are determined by the quantity of injection at the molecular level, the initial status of the device is not controlled during the production process. The output status of pins, I/O setting, and register contents upon power application are not guaranteed. However, the items defined for reset operation and mode setting are subject to guarantee after the respective operations have been executed.

When using a device with a reset function, be sure to reset the device after power application.

[MEMO]

M4 92.6