NEC

MOS INTEGRATED CIRCUIT

μPD780957(A), 780958(A)

8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD780957(A) and 780958(A) are μPD780958 Subseries products of the 78K/0 Series. These microcontrollers support ultra-low power consumption and are especially suitable for meter control.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD780958 Subseries User's Manual: U13655E
78K/0 Series User's Manual Instructions: U12326E

FEATURES

- Ultra-low power consumption supported.
- On-chip ROM and RAM

Item / Part Number	Internal ROM	Internal High-Speed RAM	Internal Expansion RAM	LCD Display RAM
μPD780957(A)	48 KB	1024 bytes	1024 bytes	30 bytes
μPD780958(A)	60 KB			

- Three channels of clock generators: Main system clock (1 MHz (RC oscillation))
  : Subsystem clock 1 (32.768 kHz)
  : Subsystem clock 2 (4.91 MHz)
- I/O ports (including segment signal output alternate function pins): 69
- LCD controller/driver
- Serial interface: 2 channels
  - UART mode (with pin switching function): 1 channel (communication is enabled with subsystem clocks 1 and 2)
  - 3-wire serial I/O mode: 1 channel
- MR sampling function: 1 channel
- Sampling output timer/detector: 1 channel
- Timer: 7 channels
  - 16-bit timer/event counter: 2 channels
  - 8-bit timer: 4 channels
  - Watchdog timer: 1 channel
- Real-time output function: 4-bit resolution × 4 channels
- Standby function: HALT mode
- Supply voltage: V_{DD} = 2.2 to 3.5 V

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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The mark ★ shows major revised points.

APPLICATIONS

Industrial meter control, etc.

ORDERING INFORMATION

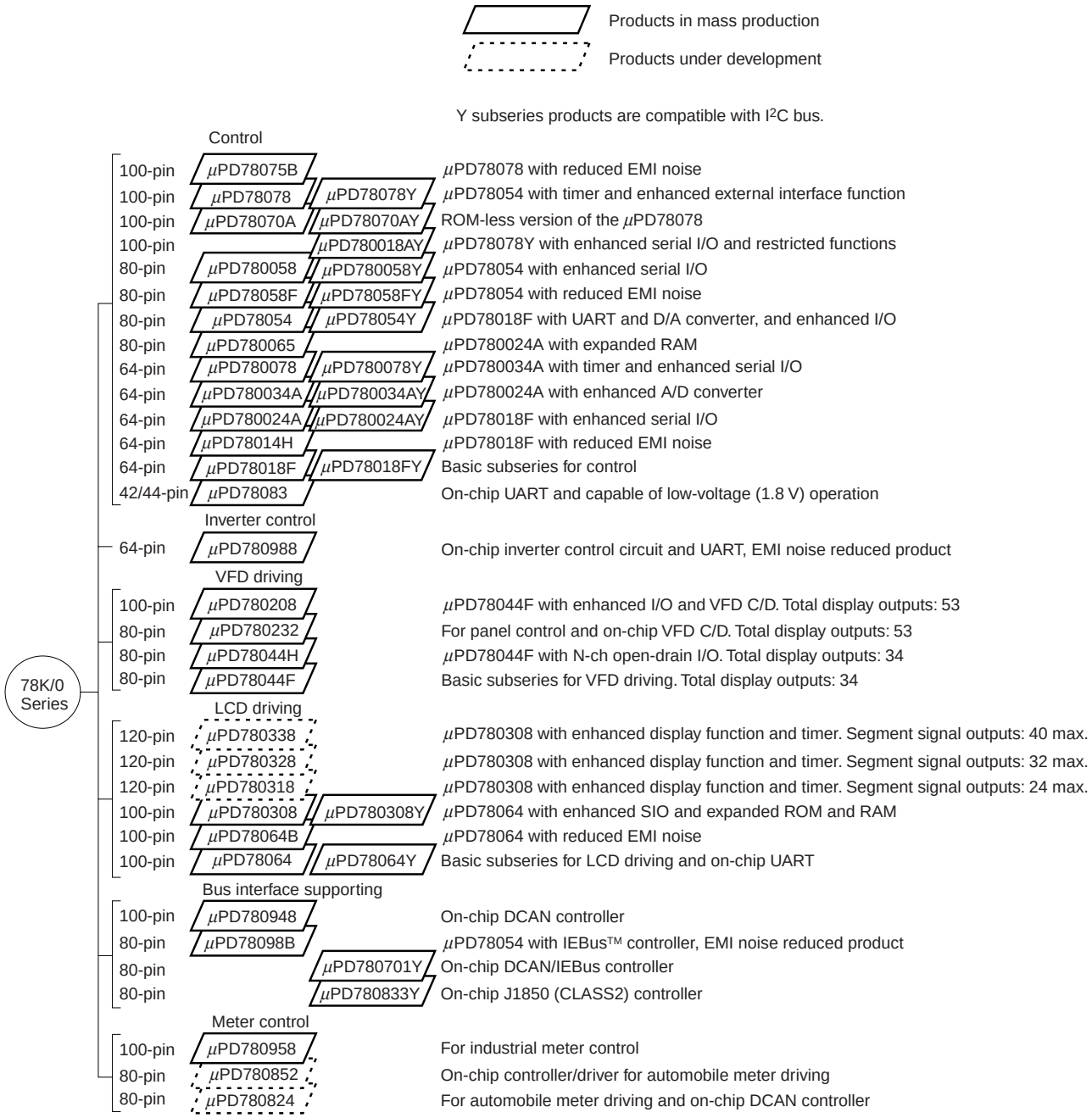
Part Number	Package	Quality Grade
μPD780957GC(A)-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special
μPD780958GC(A)-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special

Remark ××× indicates ROM code suffix.

For details of the quality grades on the devices and their applications, refer to **Quality Grades on NEC Semiconductor Devices (C11531E)** published by NEC Corporation.

★ 78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.



Remark VFD (Vacuum Fluorescent Display) is referred to as "FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences among the subseries are listed below.

Subseries Name \ Function		ROM Capacity	Timer 8-Bit	Timer 16-Bit	Timer Watch	Timer WDT	10-Bit A/D	10-Bit A/D	8-Bit A/D	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
Control	μPD78075B	32 K to 40 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1ch)	88	1.8 V	√
	μPD78078	48 K to 60 K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24 K to 60 K	2 ch							3 ch (time division UART:1 ch)	68	1.8 V	
	μPD78058F	48 K to 60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K to 60 K										2.0 V	
	μPD780065	40 K to 48 K							–	4 ch (UART: 1 ch)	60	2.7 V	
	μPD780078	48 K to 60 K		2 ch			–	8 ch		3 ch (UART: 2 ch)	52	1.8 V	
	μPD780034A	8 K to 32 K		1 ch						3 ch (UART: 1 ch)	51		
	μPD780024A						8 ch	–					
	μPD78014H									2 ch	53		
	μPD78018F	8 K to 60 K											
	μPD78083	8 K to 16 K		–	–					1 ch (UART: 1 ch)	33		–
Inverter control	μPD780988	16 K to 60 K	3 ch	**Note**	–	1 ch	–	8 ch	–	3 ch (UART: 2 ch)	47	4.0 V	√
VFD drive	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74	2.7 V	–
	μPD780232	16 K to 24 K	3 ch	–	–		4 ch			2 ch	40	4.5 V	
	μPD78044H	32 K to 48 K	2 ch	1 ch	1 ch		8ch			1 ch	68	2.7 V	
	μPD78044F	16 K to 40 K								2 ch			
LCD drive	μPD780338	48 K to 60 K	3 ch	2 ch	1 ch	1 ch	–	10 ch	1 ch	2 ch (UART: 1 ch)	54	1.8 V	–
	μPD780328										62		
	μPD780318										70		
	μPD780308	48 K to 60 K	2 ch	1 ch			8 ch	–	–	3 ch (time division UART: 1 ch)	57	2.0 V	
	μPD78064B	32 K								2 ch (UART: 1 ch)			
	μPD78064	16 K to 32 K											
Bus interface supported	μPD780948	60 K	2 ch	2 ch	1 ch	1 ch	8 ch	–	–	3 ch (UART: 1 ch)	79	4.0 V	√
	μPD78098B	40 K to 60 K		1 ch					2ch		69	2.7 V	–
Meter control	μPD780958	48 K to 60 K	4 ch	2 ch	–	1 ch	–	–	–	2 ch (UART: 1 ch)	69	2.2 V	–
Dash board control	μPD780852	32 K to 40 K	3 ch	1 ch	1 ch	1 ch	5 ch	–	–	3 ch (UART: 1 ch)	56	4.0 V	–
	μPD780824	48 K to 60 K								2 ch (UART: 2 ch)	59		

Notes 16-bit timer: 2 channels
10-bit timer: 1 channel

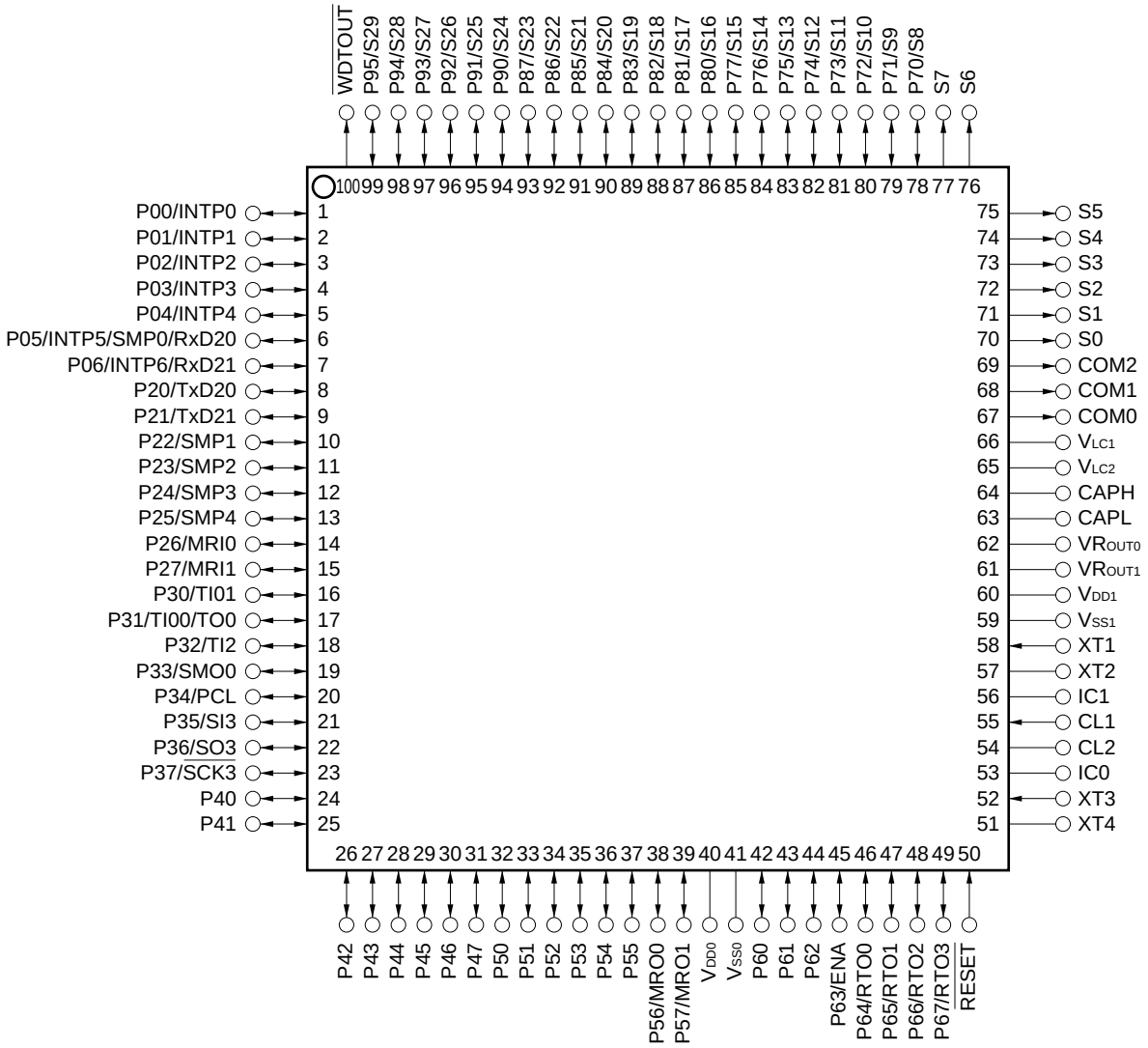
OVERVIEW OF FUNCTIONS

Item \ Part Number		μPD780957(A)	μPD780958(A)
Internal memory	ROM	48 KB	60 KB
	High-speed RAM	1024 bytes	
	Expansion RAM	1024 bytes	
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		On-chip minimum instruction execution time variable function 2 μs/4 μs/8 μs (@ 1 MHz operation (RC oscillation) with main system clock) 61 μs (@ 32.768 kHz operation with subsystem clock 1)	
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc.	
I/O ports		Total: 69 • CMOS I/O: 66 • N-ch open-drain I/O: 3 (V_{DD}-level withstand voltage)	
MR sampling function		MR sampling output/phase detection function × 1 channel (can be used as an interval timer attached to an 8-bit compare register)	
Sampling function		Sampling output timer/detector × 1 channel (can be used as two interval timers attached to 8-bit compare registers)	
Serial interface		• UART mode (with pin switching function): 1 channel • 3-wire serial I/O mode: 1 channel	
Timer		• 16-bit timer/event counter: 2 channels • 8-bit timer: 4 channels • Watchdog timer: 1 channel	
Timer outputs		1 (when sampling output and MR sampling function not used: 3)	
Clock output		256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (@ 32.768 kHz operation with subsystem clock 1)	
Real-time output		4 channels (4 bits × 4 buffers)	
LCD controller/driver		30 segments × 3 commons (static, 1/3 bias)	
Vectored interrupt sources	Maskable	Internal: 17, External: 12	
	Non-maskable	Internal: 1	
	Software	1	
Power supply voltage		V_{DD} = 2.2 to 3.5 V	
Operating ambient temperature		T_A = −40 to +80°C	
Package		100-pin plastic LQFP (fine pitch) (14 × 14)	

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- **100-pin plastic LQFP (fine pitch) (14 × 14)**
  μPD780957GC(A)-×××-8EU, 780958GC(A)-xxx-8EU

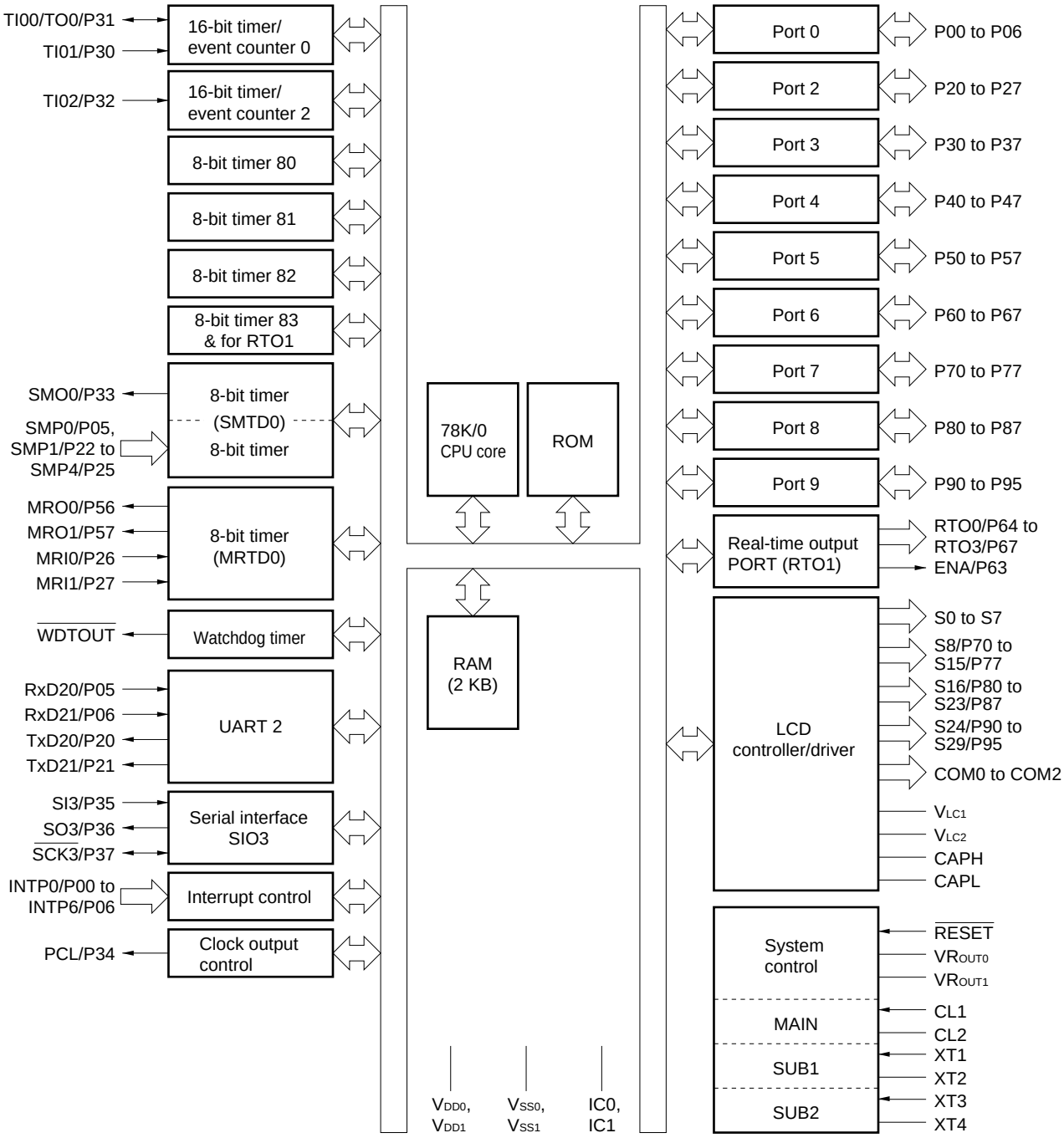


Caution Connect the IC0 and IC1 pins directly to V_{SS0}.

Remark When the μPD780957(A) and 780958(A) are used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

CAPH, CAPL:	Capacitor (for LCD)
CL1, CL2:	RC oscillator
COM0 to COM2:	Common output
ENA:	Enable
IC0, IC1:	Internally connected
INTP0 to INTP6:	External interrupt input
MRI0, MRI1:	MR sampling input
MRO0, MRO1:	MR sampling output
P00 to P06:	Port 0
P20 to P27:	Port 2
P30 to P37:	Port 3
P40 to P47:	Port 4
P50 to P57:	Port 5
P60 to P67:	Port 6
P70 to P77:	Port 7
P80 to P87:	Port 8
P90 to P95:	Port 9
PCL:	Programmable clock
$\overline{\text{RESET}}$:	Reset
RTO0 to RTO3:	Real-time output port
RxD20, RxD21:	Receive data
$\overline{\text{SCK3}}$:	Serial clock
SI3:	Serial input
SMP0 to SMP4:	Sampling input
SMO0:	Sampling output
SO3:	Serial output
S0 to S29:	Segment output
TI00, TI01, TI2:	Timer input
TO0:	Timer output
TxD20, TxD21:	Transmit data
V_{DD0}, V_{DD1}:	Power supply
V_{LC1}, V_{LC2}:	Power supply (for LCD)
VR_{OUT0}, VR_{OUT1}:	Capacitor (for regulator)
V_{SS0}, V_{SS1}:	Ground
$\overline{\text{WDTOUT}}$:	Watchdog timer output
XT1, XT2:	Crystal (subsystem clock 1)
XT3, XT4:	Crystal (subsystem clock 2)

2. BLOCK DIAGRAM



Remark The internal ROM capacity varies depending on the product.

3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P00 to P04	I/O	Port 0. 7-bit I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.		Input	INTP0 to INTP4
P05					INTP5/SMP0/RxD20
P06					INTP6/RxD21
P20	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.		Input	TxD20
P21					TxD21
P22 to P25					SMP1 to SMP4
P26					MRI0
P27					MRI1
P30	I/O	Port 3. 8-bit I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.		Input	TI01
P31					TI00/TO0
P32					TI2
P33					SMO0
P34					PCL
P35					SI3
P36					SO3
P37					$\overline{\text{SCK3}}$
P40 to P47	I/O	Port 4. 8-bit I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.		Input	–
P50 to P55	I/O	Port 5. 8-bit I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.		Input	–
P56					MRO0
P57					MRO1
P60 to P62	I/O	Port 6. 8-bit I/O port. Input/output can be specified in 1-bit units.	N-ch open-drain input/output port (3.6 V withstand voltage). An on-chip pull-up resistor can be specified by a mask option.	Input	–
P63			An on-chip pull-up resistor can be specified by software.		ENA
P64 to P67					RTO0 to RTO3

3.1 Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P70 to P77	I/O	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.	Input	S8 to S15
P80 to P87	I/O	Port 8. 8-bit I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.	Input	S16 to S23
P90 to P95	I/O	Port 9. 6-bit I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.	Input	S24 to S29

3.2 Non-port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0 to INTP4	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P00 to P04
INTP5				P05/SMP0/RxD20
INTP6				P06/RxD21
RxD20	Input	Serial data input for asynchronous serial interface (UART2)	Input	P05/INTP5/SMP0
RxD21		Serial data input for asynchronous serial interface (UART2) (switching pin)	Input	P06/INTP6
TxD20	Output	Serial data output for asynchronous serial interface (UART2)	Input	P20
TxD21		Serial data output for asynchronous serial interface (UART2) (switching pin)		P21
SMP0	Input	Sampling input	Input	P05/INTP5/RxD20
SMP1 to SMP4				P22 to P25
SMO0	Output	Sampling output	Input	P33
MRI0	Input	Phase detection input	Input	P26
MRI1				P27
MRO0	Output	MR sampling output	Input	P56
MRO1				P57
TI00	Input	External count clock input to 16-bit timer/event counter 0 Capture trigger input to capture registers (CR00/CR01) of 16-bit timer/event counter 0	Input	P31/TO0
TI01		Capture trigger input to capture register (CR00) of 16-bit timer/event counter 0	Input	P30
TI2		External count clock input to 16-bit timer/event counter 2		P32
TO0	Output	16-bit timer output	Input	P31/TI00
SI3	Input	Serial interface serial data input	Input	P35
SO3	Output	Serial interface serial data output	Input	P36
$\overline{\text{SCK3}}$	I/O	Serial interface serial clock input/output	Input	P37
PCL	Output	Clock output (for trimming subsystem clock 1)	Input	P34
S0 to S7	Output	Segment signal output of LCD controller	Output	–
S8 to S15			Input	P70 to P77
S16 to S23				P80 to P87
S24 to S29				P90 to P95
COM0 to COM2	Output	Common signal output of LCD controller	Output	–
ENA	Output	ENA output	Input	P63
RTO0 to RTO3	Output	Real-time output port from which data is output in synchronization with a trigger	Input	P64 to P67
$\overline{\text{WDTOUT}}$	Output	Overflow output of watchdog timer	Output	–
$\overline{\text{RESET}}$	Input	System reset input	–	–

3.2 Non-port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
CL1	Input	Connecting main system clock oscillation resister (R) and capacitor (C)	–	–
CL2	–		–	–
XT1	Input	Connecting crystal resonator for subsystem clock 1 oscillation	–	–
XT2	–		–	–
XT3	Input	Connecting crystal resonator for subsystem clock 2 oscillation	–	–
XT4	–		–	–
V_{DD0}	–	Positive power supply for ports	–	–
V_{DD1}	–	Positive power supply (except for ports)	–	–
V_{SS0}	–	Ground potential for ports	–	–
V_{SS1}	–	Ground potential (except for ports)	–	–
V_{LC1}, V_{LC2}	–	Positive power supply for LCD controller	–	–
VR_{OUT0}, VR_{OUT1}	–	Connecting capacitor for internal regulator	–	–
CAPH, CAPL	–	Connecting capacitor for LCD controller	–	–
IC0, IC1	–	Internally connected. Connect directly to V_{SS0}	–	–

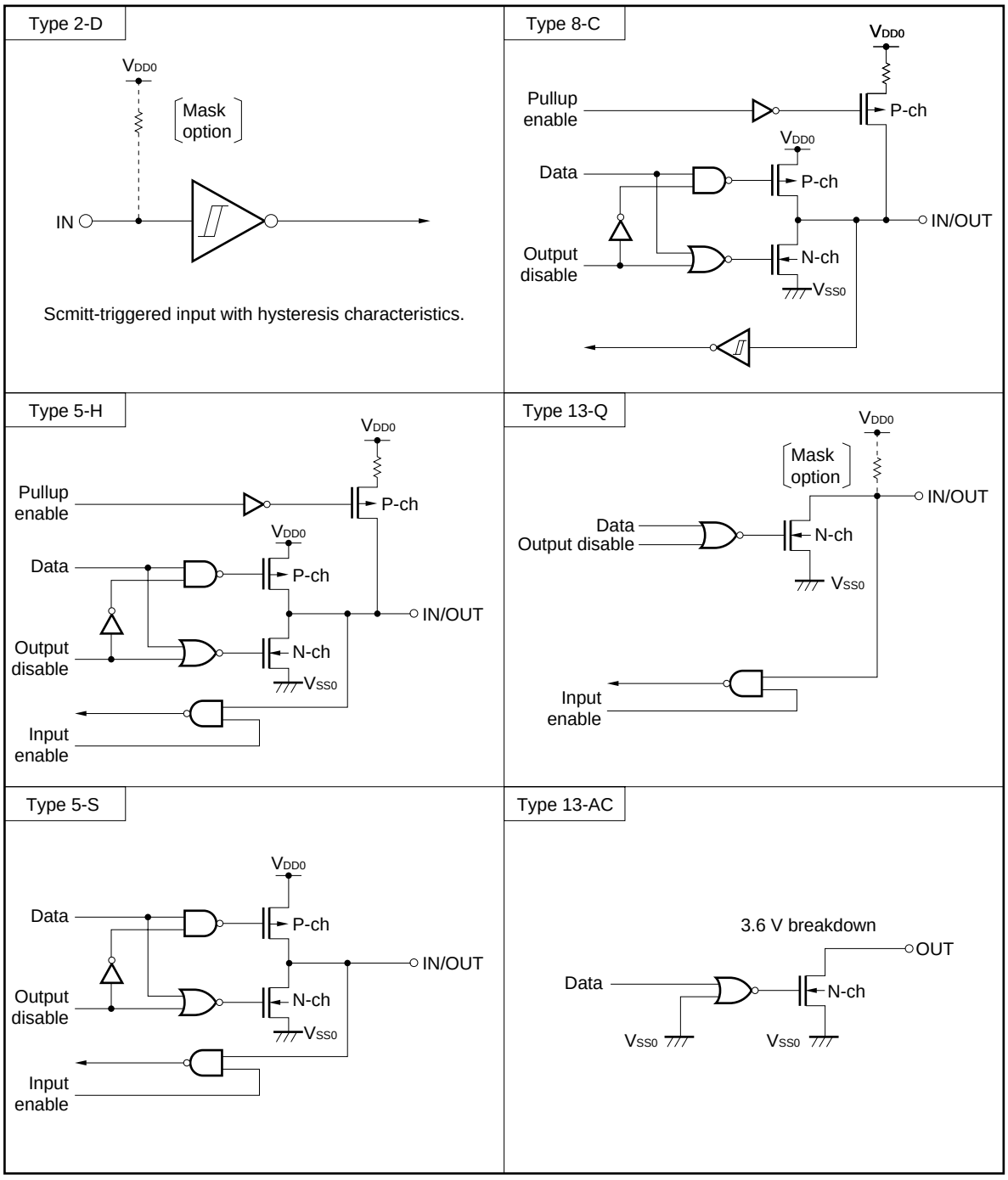
3.3 Pin Input/Output Circuits and Recommended Connection of Unused Pins

Table 3-1 shows the pin input/output circuit types and the recommended connection of unused pins.
Refer to Figure 3-1 for the configuration of the input/output circuit of each type.

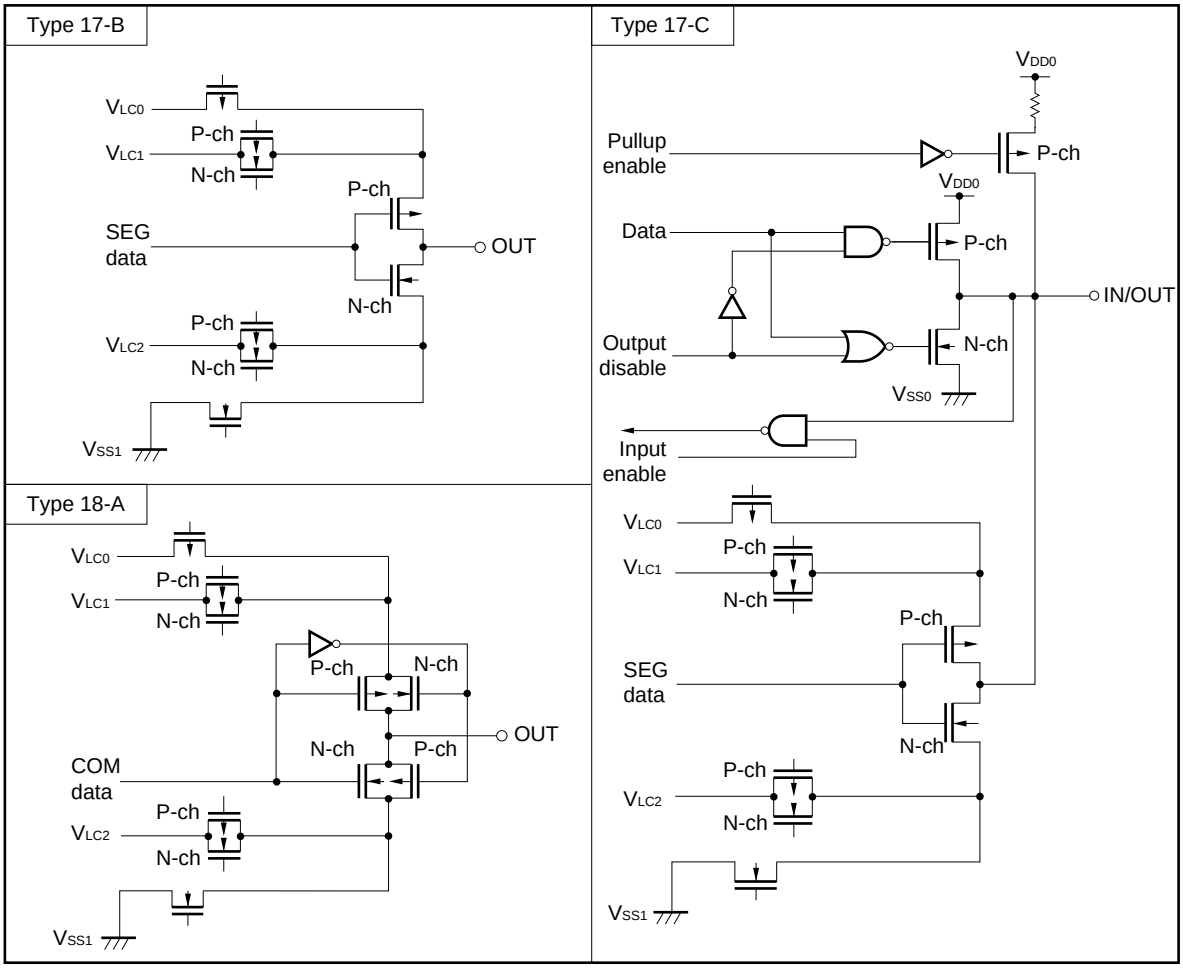
★ **Table 3-1. Pin Input/Output Circuit Types and Recommended Connection of Unused Pins**

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0 to P04/INTP4	8-C	I/O	Input: Independently connect to V_{SS0} via a resistor.
P05/INTP5/SMP0/RxD20			Output: Leave open.
P06/INTP6/RxD21			
P20/TxD20	5-H		Input: Independently connect to V_{DD0} or V_{SS0} via a resistor.
P21/TxD21			Output: Leave open.
P22/SMP1 to P25/SMP4	8-C		
P26/MRI0			
P27/MRI1			
P30/TI01			
P31/TI00/TO0			
P32/TI2			
P33/SMO0	5-H		
P34/PCL			
P35/SI3	8-C		
P36/SO3	5-H		
P37/$\overline{SCK3}$	8-C		
P40 to P47	5-H		
P50 to P55			
P56/MRO0	5-S		
P57/MRO1			
P60 to P62	13-Q		Input: Independently connect to V_{DD0} via a resistor.
			Output: Leave open.
P63/ENA	5-H		Input: Independently connect to V_{DD0} or V_{SS0} via a resistor.
P64/RTO0 to P67/RTO3			Output: Leave open.
P70/S8 to P77/S15	17-C		
P80/S16 to P87/S23			
P90/S24 to P95/S29			
S0 to S7	17-B	Output	Leave open.
COM0 to COM2	18-A		
$\overline{WDTOUT}$	13-AC		
$\overline{RESET}$	2-D	Input	–
CAPL, V_{LC1}, V_{LC2}	–	–	Independently connect to GND via a resistor.
CAPH	–	–	Independently connect to V_{DD1} via a resistor.
IC0 and IC1	–	–	Connect directly to V_{SS0}.

★ **Figure 3-1. Pin Input/Output Circuits (1/2)**



★ **Figure 3-1. Pin Input/Output Circuits (2/2)**



4. MEMORY SPACE

Figures 4-1 and 4-2 show the memory maps of the μPD780957(A) and 780958(A).

Figure 4-1. Memory Map (μPD780957(A))

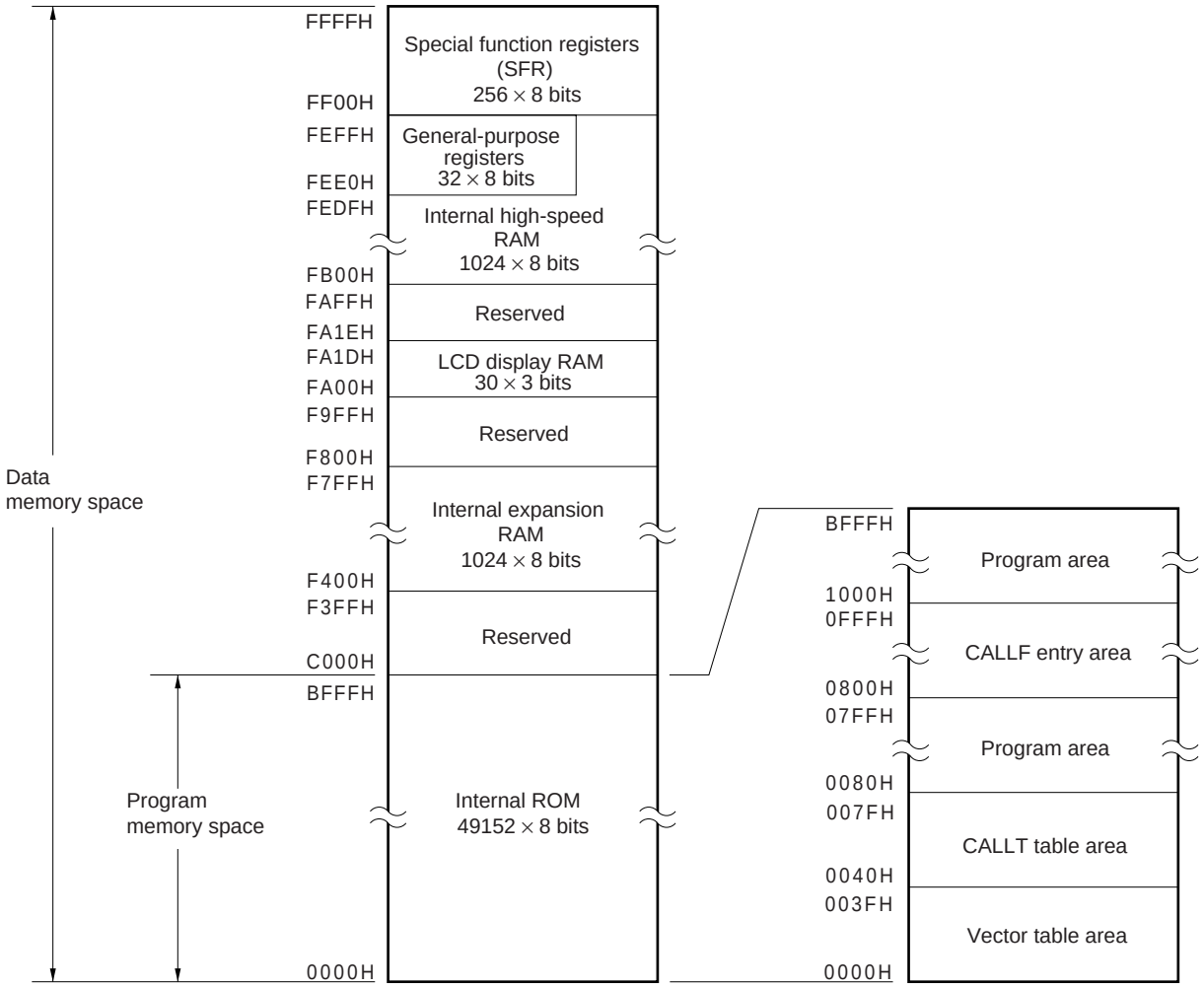
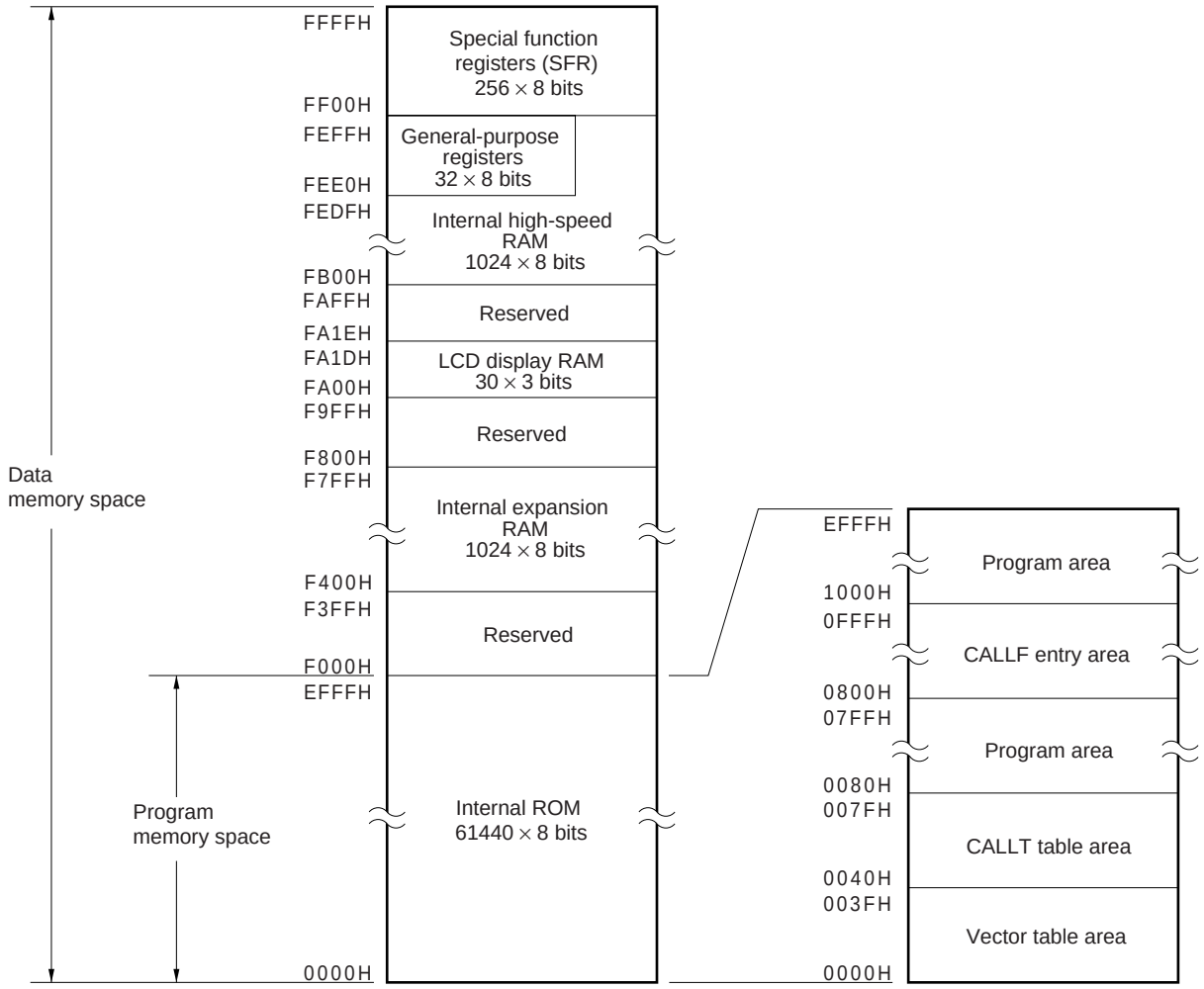


Figure 4-2. Memory Map (μPD780958(A))



5. FEATURES OF PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

The following two types of I/O ports are available.

• CMOS I/O (Ports 0, 2 to 9):	66
• N-ch open-drain I/O (P60 to P62):	3
Total:	69

Table 5-1. Port Functions

Port Name	Pin Name	Function
Port 0	P00 to P06	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.
Port 2	P20 to P27	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.
Port 3	P30 to P37	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.
Port 4	P40 to P47	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.
Port 5	P50 to P57	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.
Port 6	P60 to P62	N-ch open-drain I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by a mask option.
	P63 to P67	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.
Port 7	P70 to P77	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.
Port 8	P80 to P87	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.
Port 9	P90 to P95	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.

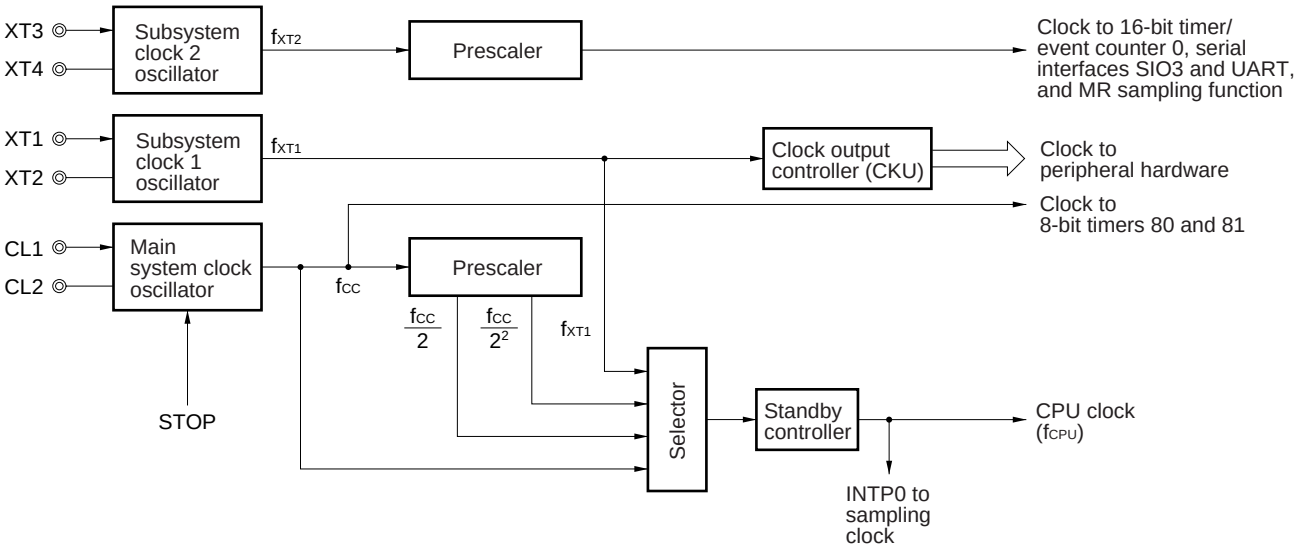
5.2 Clock Generator

Three types of generators, a main system clock generator, a subsystem clock 1 generator and a subsystem clock 2 generator, are available.

The minimum instruction execution time can be changed.

- 2 μs/4 μs/8 μs (@ 1 MHz operation (RC oscillation) with main system clock)
- 61 μs (@ 32.768 kHz operation with subsystem clock 1)

Figure 5-1. Clock Generator Block Diagram



The system clocks shown in Table 5-2 are supplied to peripheral hardware.

Table 5-2. System Clock Supplied to Each Peripheral Hardware

Peripheral Hardware	System Clock
Serial interface SIO3	Operates with subsystem clocks 1 or 2
Serial interface UART2	
16-bit timer/event counter 0	
16-bit timer/event counter 2	Operates with subsystem clock 1
8-bit timer 80	Operates with main system clock or subsystem clock 1
8-bit timer 81	
8-bit timer 82	Operates with subsystem clock 1
8-bit timer 83	
Watchdog timer	
MR sampling function	Operates with subsystem clocks 1 or 2
Sampling output timer/detector	Operates with subsystem clock 1
LCD controller/driver	
Clock output controller	

Remark Main system clock: 1 MHz (RC oscillation)
Subsystem clock 1: 32.768 kHz
Subsystem clock 2: 4.91 MHz

5.3 Timer

Seven timer channels are incorporated.

- 16-bit timer/event counter: 2 channels
- 8-bit timer: 4 channels
- Watchdog timer: 1 channel

The following 3 channels can also be used as interval timers.

- Sampling output timer/detector: 2 channels
- MR sampling function: 1 channel

Table 5-2. Timer Operation

		16-Bit Timer/Event Counter 0	16-Bit Timer/Event Counter 2	8-Bit Timers 80 to 83	Watchdog Timer	Sampling Output Timer/Detector	MR Sampling Function
★ Operation mode	Interval timer	1 channel	1 channel	4 channels	1 channel[Note 1]	2 channels[Note 2]	1 channel[Note 3]
	External event counter	1 channel	1 channel	–	–	–	–
Function	Timer output	1 output	–	–	–	1 output	1 output
	PPG output	1 output	–	–	–	–	–
	Pulse width measurement	2 inputs	–	–	–	–	–
	Square wave output	1 output	–	–	–	–	–
	Event input control function	–	1 input[Note 4]	–	–	–	–
	Interrupt sources	2	1	4	1	2	1

Notes 1. The watchdog timer has the watchdog timer and interval timer functions. However, use the watchdog timer by selecting either the watchdog timer function or the interval timer function.

2. When used as a sampling output, use as an interval timer is invalid.

3. When using the MR sampling function, use as an interval timer is invalid.

4. The event input control function should be used with 8-bit timer 82.

Figure 5-2. Block Diagram of 16-Bit Timer/Event Counter 0

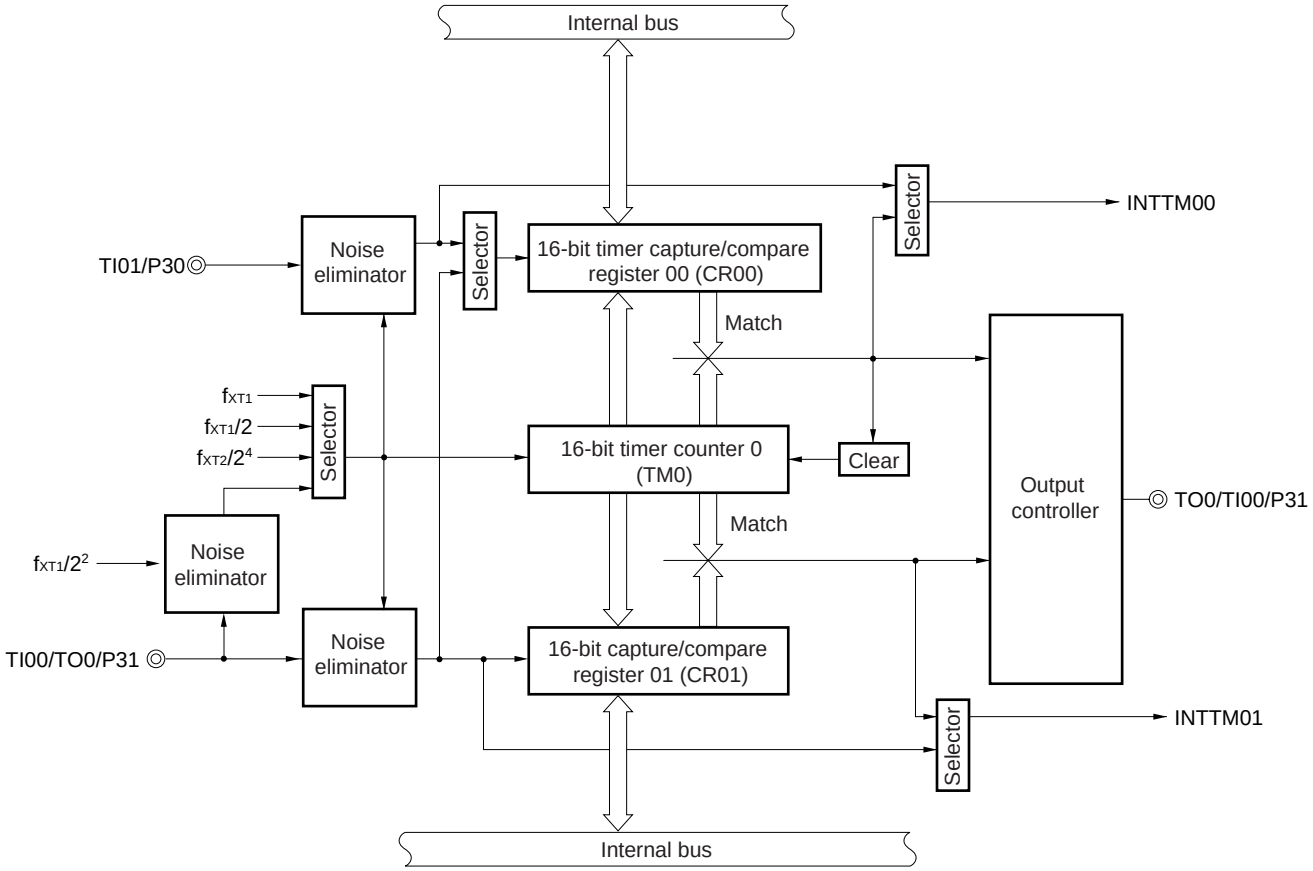
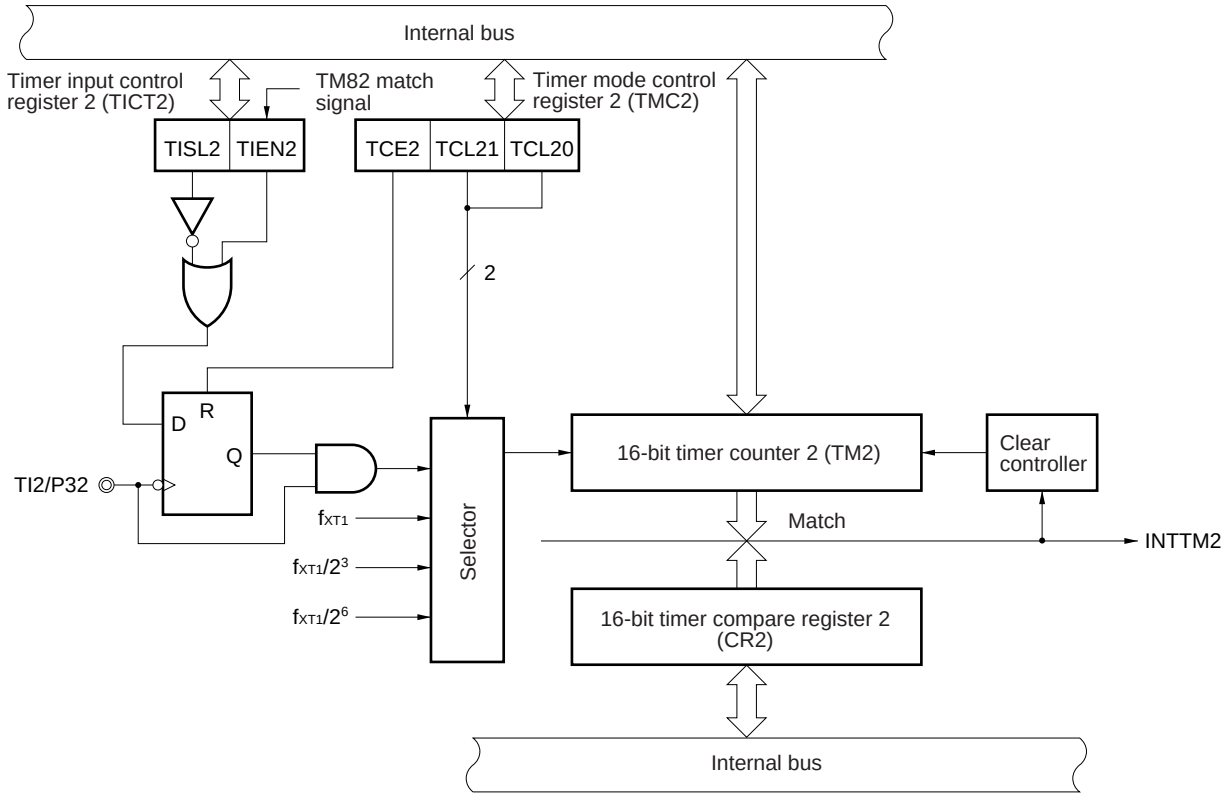
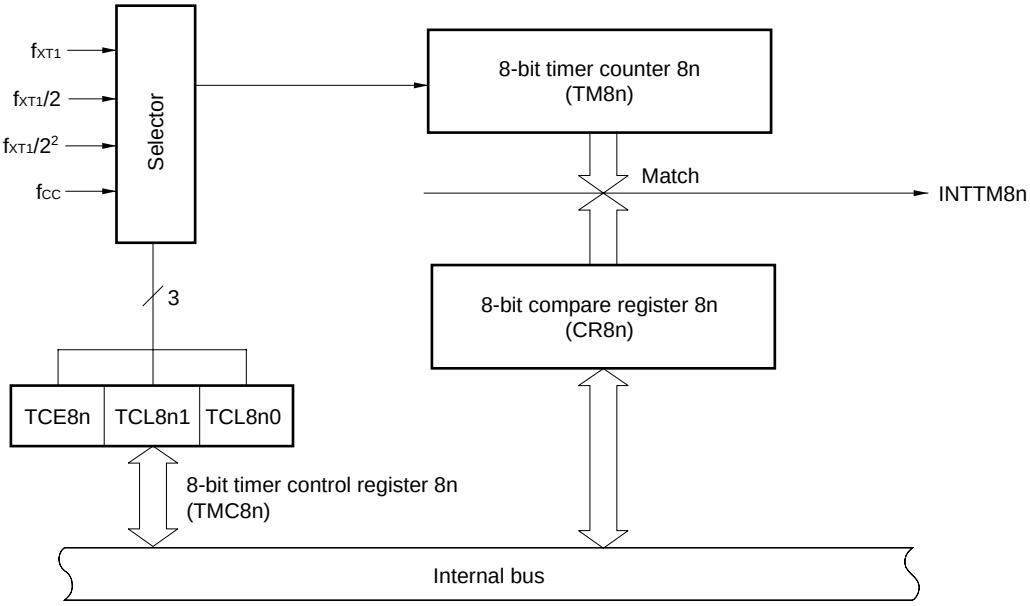


Figure 5-3. Block Diagram of 16-Bit Timer/Event Counter 2



★ **Figure 5-4. Block Diagram of 8-bit Timers 80 to 83**



Caution The count clocks in the figure above are those of 8-bit timers 80 and 81. For the count clocks of 8-bit timers 82 and 83, refer to Table 5-3.

Remark n = 0 to 3

★ **Table 5-3. Count Clock Values of 8-Bit Timers 80 to 83**

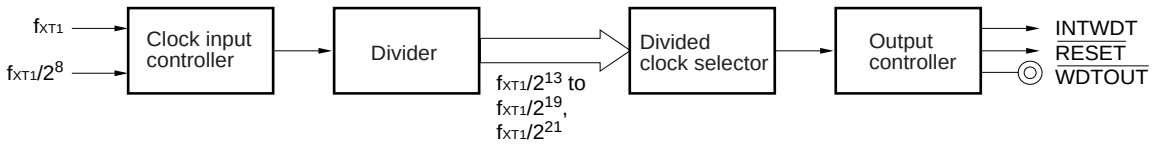
8-Bit Timer 80	8-Bit Timer 81	8-Bit Timer 82	8-Bit Timer 83
f_{XT1} (30.5 μs)		$f_{XT1}/2^7$ (3.9 ms)	f_{XT1} (30.5 μs)
$f_{XT1}/2$ (61 μs)		$f_{XT1}/2^9$ (15.6 ms)	$f_{XT1}/2^3$ (244 μs)
$f_{XT1}/2^2$ (122 μs)		$f_{XT1}/2^{11}$ (62.5 ms)	$f_{XT1}/2^6$ (1.95 ms)
f_{CC} (1 μs)		$f_{XT1}/2^{13}$ (0.25 s)	$f_{XT1}/2^9$ (15.6 ms)

Remarks 1. Figures in parentheses apply to operation with f_X = 1 MHz and f_{XT1} = 32.768 kHz.

2. f_{CC}: Main system clock oscillation frequency

f_{XT1}: Subsystem clock 1 oscillation frequency

Figure 5-5. Block Diagram of Watchdog Timer

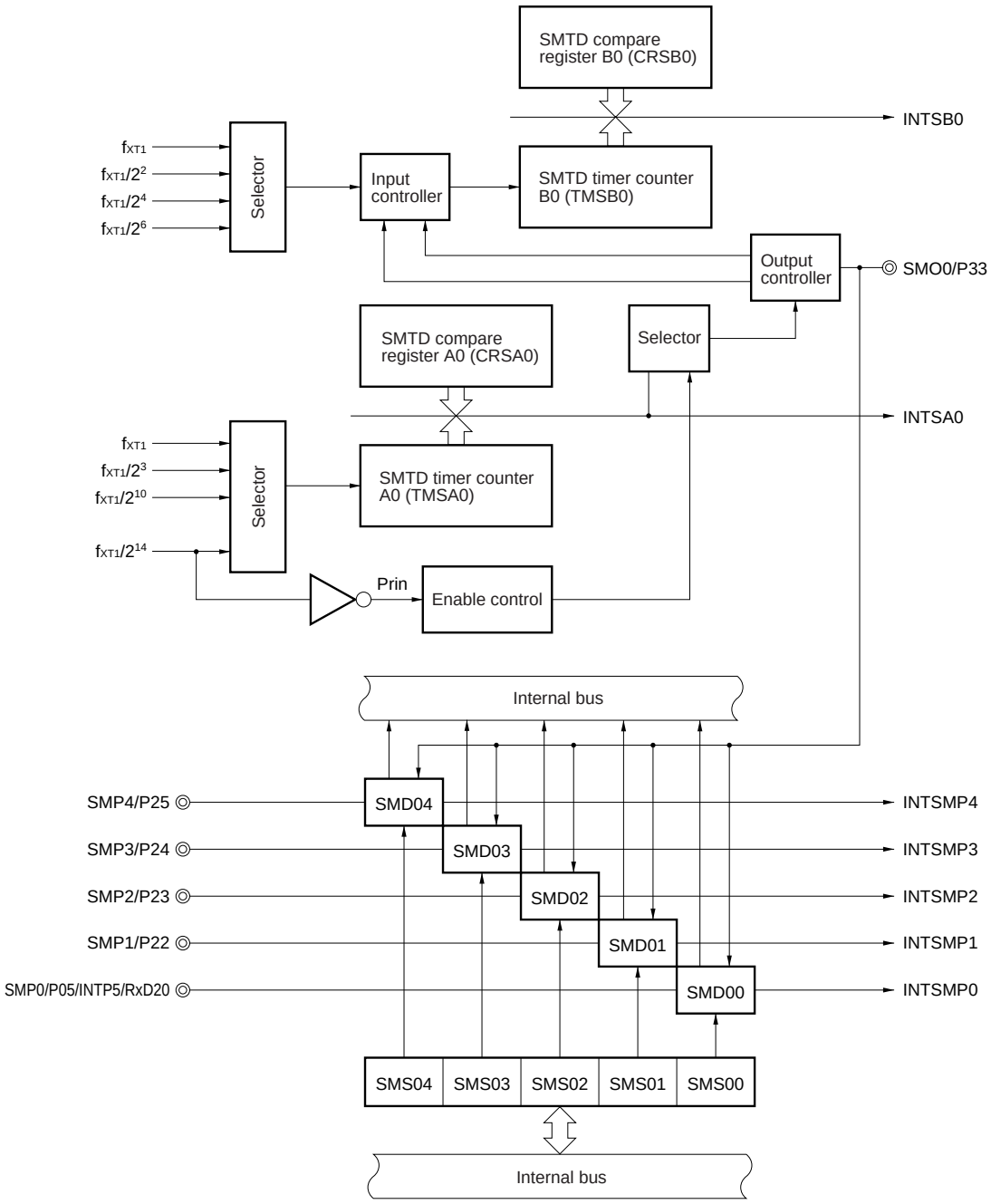


5.4 Sampling Output Timer/Detector

The sampling output timer/detector is a function that outputs or detects a sampling pulse at a regular interval.

As there is no need for the CPU to be activated by unnecessary timing, such as detection of internal conditions (switch, etc.) of meters, the current consumption can be reduced. When the sampling output is not used, use as an 8-bit timer is possible (2 channels).

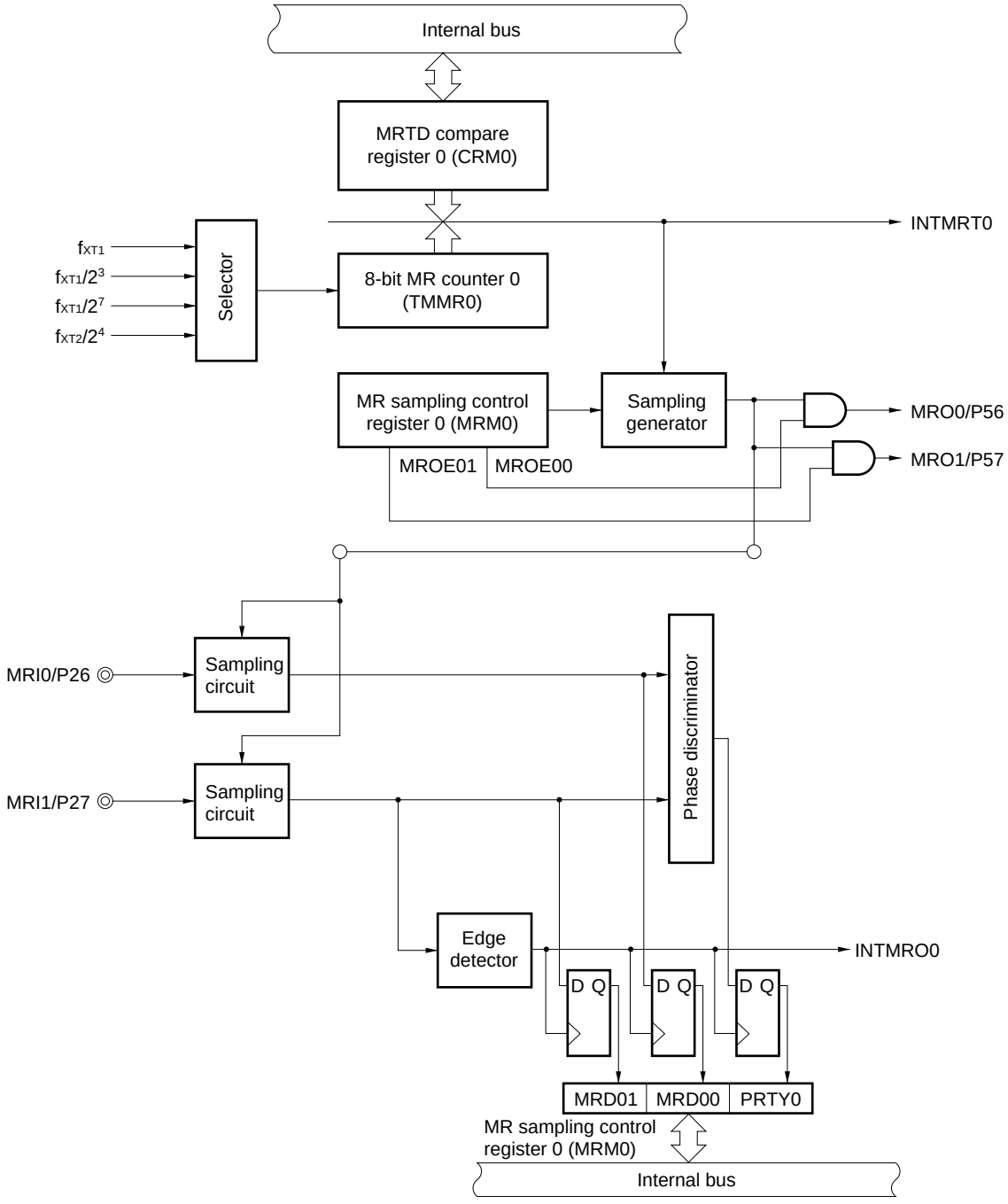
★ **Figure 5-6. Block Diagram of Sampling Output Timer/Detector**



5.5 MR Sampling Function

The MR sampling function is used to drive the MR sensor (magnetism sensor). When MR sampling output is not used, use as an 8-bit timer is possible (1 channel).

★ **Figure 5-7. Block Diagram of MR Sampling Function**



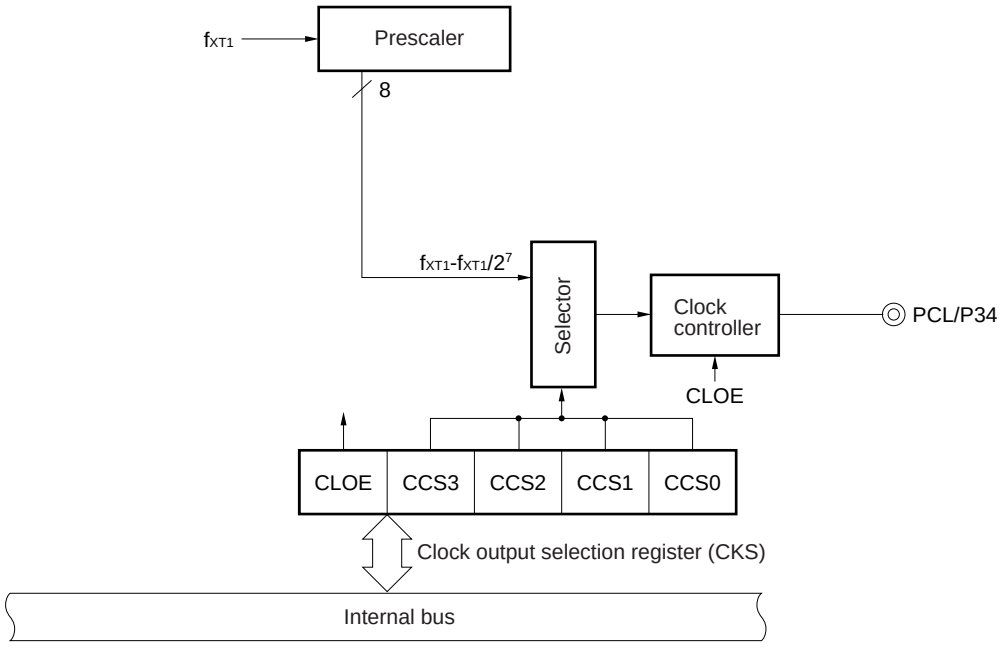
5.6 Clock Output Controller

A clock output controller (CKU) is incorporated.

Clocks with the following frequencies can be output as the clock output.

- 256 Hz/512 Hz/1.024 kHz/2.048 kHz/4.096 kHz/8.192 kHz/16.384 kHz/32.768 kHz (@ 32.768 kHz operation with subsystem clock 1)

Figure 5-8. Block Diagram of Clock Output Controller



5.7 Serial Interfaces

Two serial interface channels are incorporated.

- Serial interface UART2: 1 channel (with pin switching function)
- Serial interface SIO3: 1 channel

(1) Serial interface UART2

Serial interface UART2 operates in asynchronous serial interface (UART) mode.

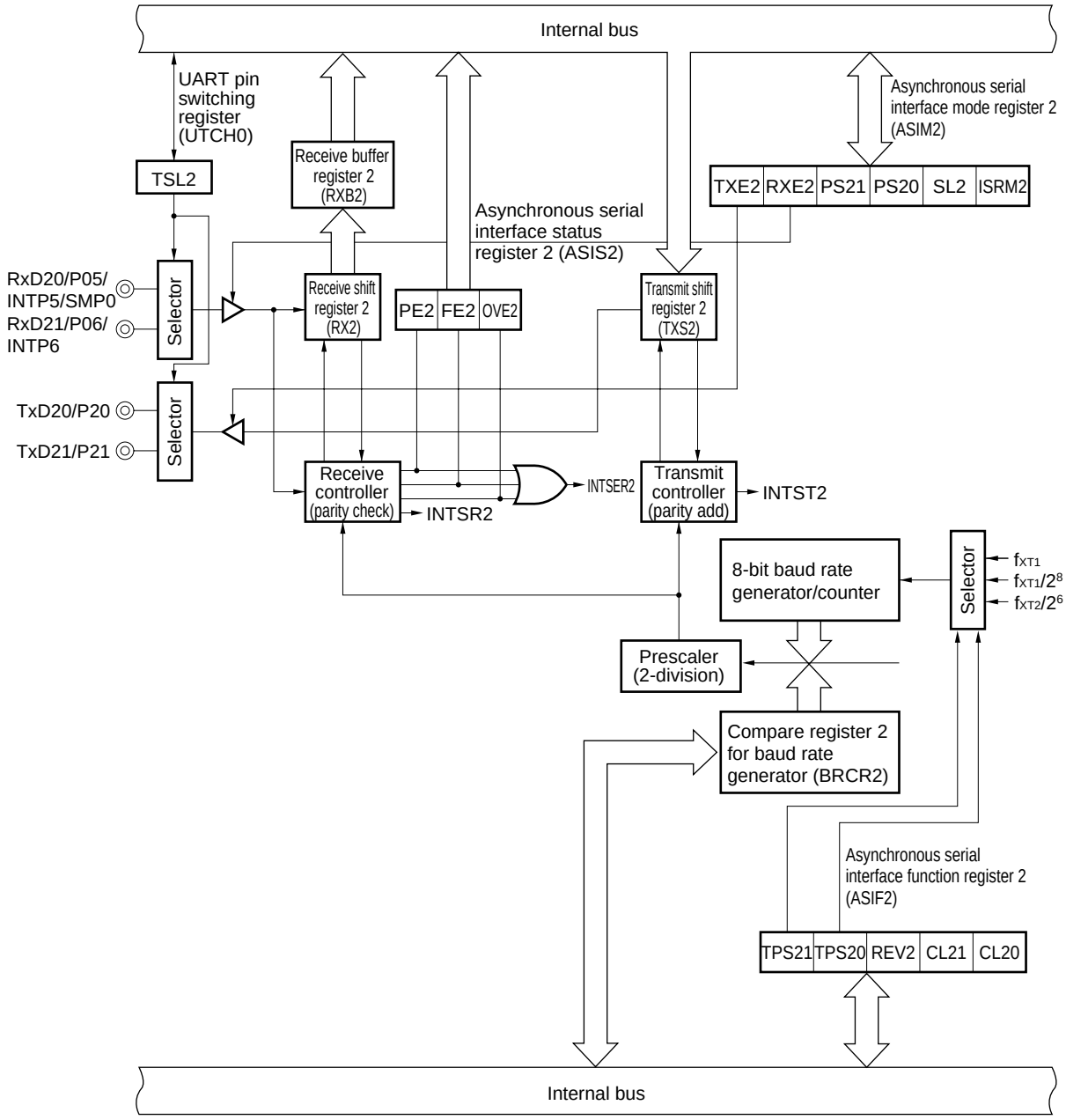
- **Asynchronous serial interface (UART) mode**

  This mode enables full-duplex operation wherein one byte of data is transmitted and received after the start bit.

  The on-chip dedicated UART baud rate generator enables communication using 200 bps or 300 bps baud rates (@ 32.768 kHz operation with subsystem clock 1).

  In addition, using subsystem clock 2 (4.91 MHz operation) enables 2400 bps baud rate communication.

★ **Figure 5-9. Block Diagram of Serial Interface UART2**



(2) Serial interface SIO3

Serial interface SIO3 operates in 3-wire serial I/O mode.

- **3-wire serial I/O mode (fixed as MSB first)**

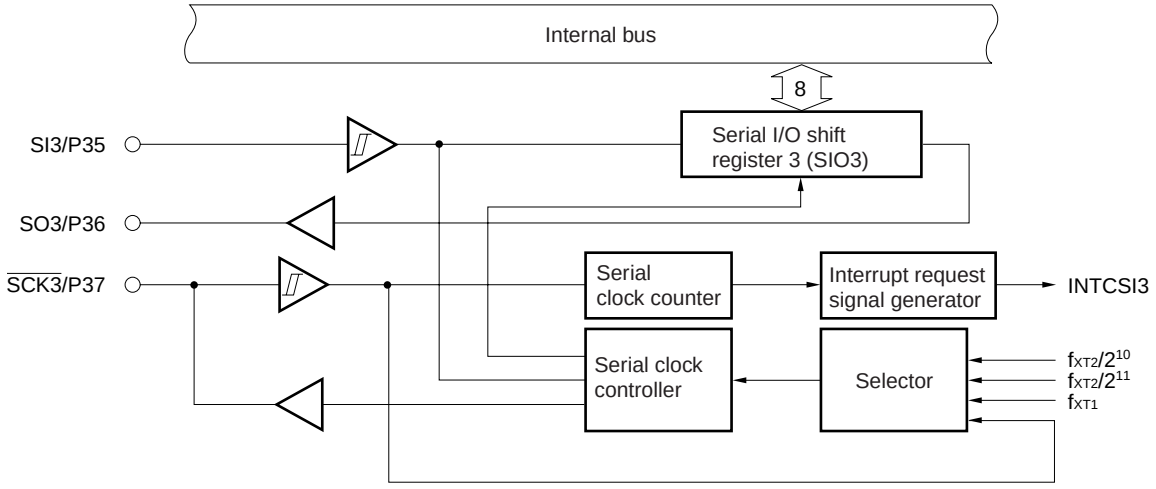
  This is an 8-bit data transfer mode using three lines: a serial clock line ($\overline{SCK3}$), serial output line (SO3), and serial input line (SI3).

  Since simultaneous transmit and receive operations are available in the 3-wire serial I/O mode, the processing time for data transfer is reduced.

  The first bit in 8-bit data in the serial transfer is fixed as MSB.

  The 3-wire serial I/O mode is useful for connection to a peripheral I/O device that includes a clocked serial interface, or a display controller, etc.

Figure 5-10. Block Diagram of Serial Interface SIO3



5.8 LCD Controller/Driver

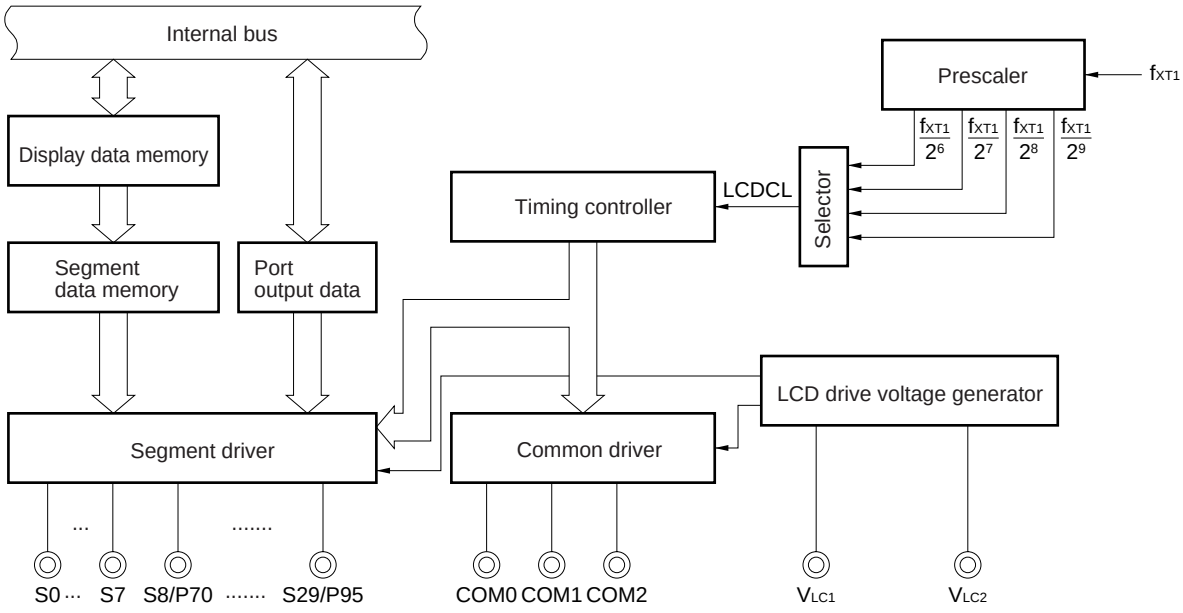
An LCD controller/driver with the following functions is incorporated.

- Display mode: 1/3 duty (1/3 bias), static mode
- 22 of the segment signal outputs can be switched with I/O port in 1-bit units (P70/S8 to P77/S15, P80/S16 to P87/S23, and P90/S24 to P95/S29).

Table 5-4. Maximum Number of Display Pixels

Bias Method	Time Division	Common Signals Used	Maximum Number of Display Pixels
1/3	3	COM0 to COM2	90 (30 segments × 3 commons)

★ **Figure 5-11. Block Diagram of LCD Controller/Driver**

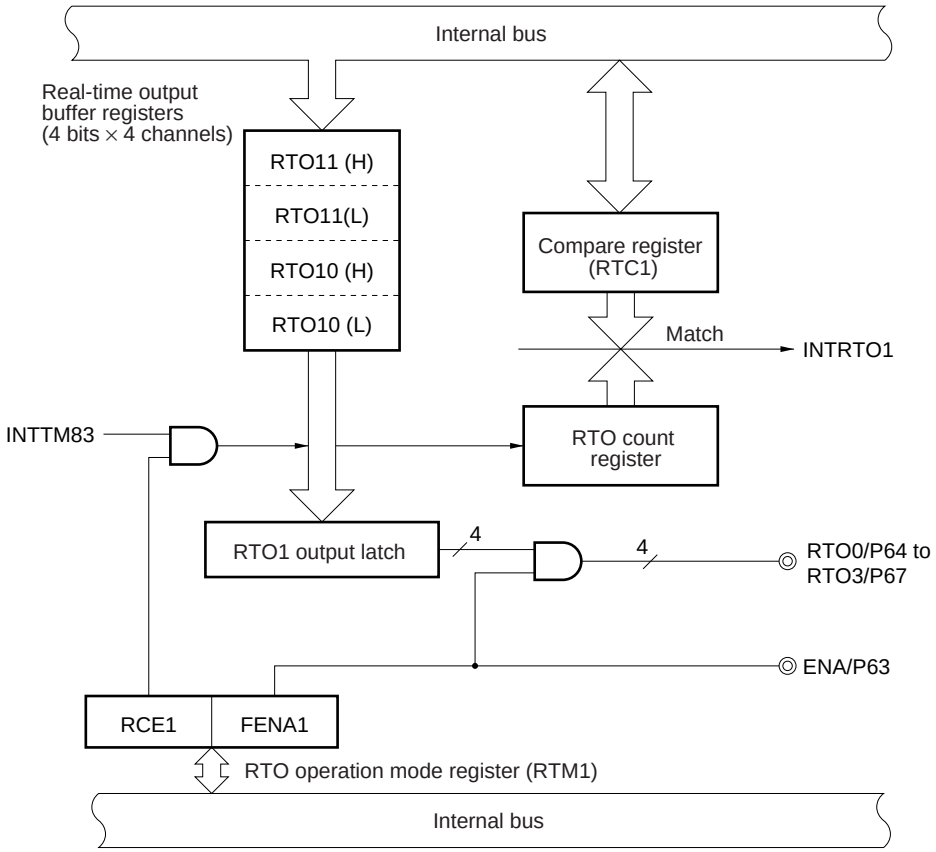


5.9 Real-Time Output Function

The real-time output function is a function that transfers and outputs externally the data preset in the real-time output buffer registers to the output latch in the hardware upon the generation of a timer interrupt (INTTM83). The pins that output this data externally are called the real-time output port.

Using the real-time output port enables generation of signals with no jitter, making it suitable for control of stepping motors, etc.

Figure 5-12. Block Diagram of Real-Time Output Function



6. INTERRUPT FUNCTIONS

A total of 31 interrupt sources divided into the following three types are provided.

- Non-maskable: 1
- Maskable: 29
- Software: 1

Table 6-1. Interrupt Source List (1/2)

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	–	INTWDT	Watchdog timer overflow (with non-maskable interrupt selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with maskable interrupt selected)			(B)
	1	INTP0	INTP0 pin input edge detection	External	0006H	(C)
	2	INTMRO0	MRTD edge detection	Internal	0008H	(B)
	3	INTP1	INTP1 pin input edge detection	External	000AH	(C)
	4	INTP2	INTP2 pin input edge detection		000CH	
	5	INTP3	INTP3 pin input edge detection		000EH	
	6	INTP4	INTP4 pin input edge detection		0010H	
	7	INTP5	INTP5 pin input edge detection		0012H	
	8	INTP6	INTP6 pin input edge detection		0014H	
	9	INTTM00	Generation of matching signal of TM0 and CR00 (when compare register selected) TI01 pin valid edge detection (when capture register selected)	Internal	0016H	(B)
	10	INTTM01	Generation of matching signal of TM0 and CR01 (when compare register selected) TI00 pin valid edge detection (when capture register selected)		0018H	
	11	INTSER2	Occurrence of serial interface UART2 reception error		001AH	
	12	INTSR2	End of serial interface UART2 reception		001CH	
	13	INTST2	End of serial interface UART2 transmission		001EH	
	14	INTCSI3	End of serial interface SIO3 transfer		0020H	
	15	INTMRT0	Generation of matching signal of MRTD timer and compare register		0022H	
	16	INTTM80	Generation of matching signal of TM80 and CR80		0024H	
	17	INTTM81	Generation of matching signal of TM81 and CR81		0026H	

Notes 1. Default priority is the priority order when several maskable interrupt requests are generated at the same time. 0 is the highest and 28 is the lowest.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 6-1.

★ **Remark** Two watchdog timer interrupt sources (INTWDT): a non-maskable interrupt and a maskable interrupt (internal), are available, either of which can be selected.

Table 6-1. Interrupt Source List (2/2)

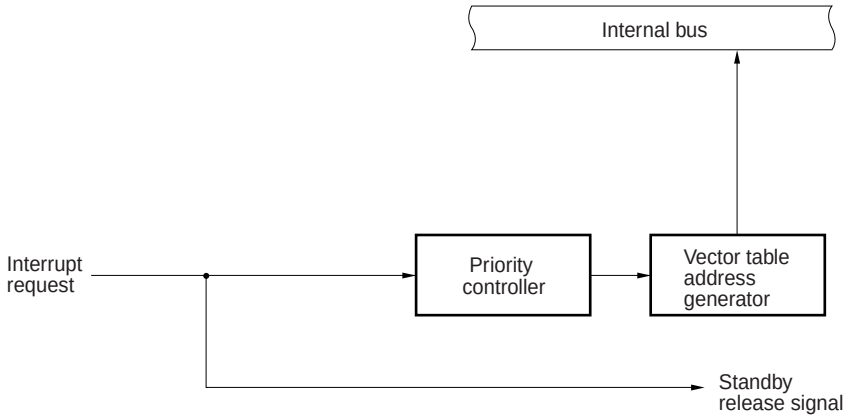
Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Maskable	18	INTTM82	Generation of matching signal of TM82 and CR82	Internal	0028H	(B)
	19	INTTM83	Generation of matching signal of TM83 and CR83		002AH	
	20	INTTM2	Generation of matching signal of TM2 and CR2		002CH	
	21	INTSA0	Generation of matching signal of Sampling timer and compare register (CRSA0)		002EH	
	22	INTSB0	Generation of matching signal of sampling timer and compare register (CRSB0)		0030H	
	23	INTRTO1	Achievement of the reload count specified for real-time output		0032H	
	24	INTSMP0	Sampling interrupt input 0	External	0034H	(C)
	25	INTSMP1	Sampling interrupt input 1		0036H	
	26	INTSMP2	Sampling interrupt input 2		0038H	
	27	INTSMP3	Sampling interrupt input 3		003AH	
	28	INSMP4	Sampling interrupt input 4		003CH	
Software	–	BRK	Execution of BRK instruction	–	003EH	(D)

Notes 1. Default priority is the priority order when several maskable interrupt requests are generated at the same time. 0 is the highest order and 28 is the lowest order.

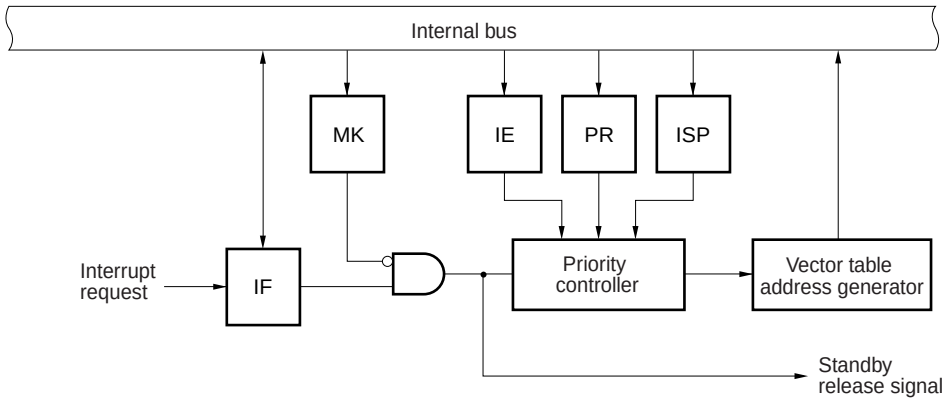
2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 6-1.

Figure 6-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0 to INTP6)

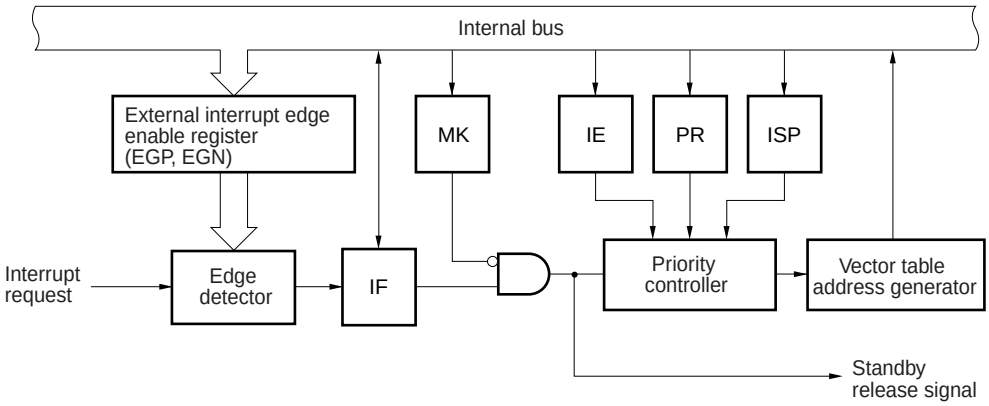
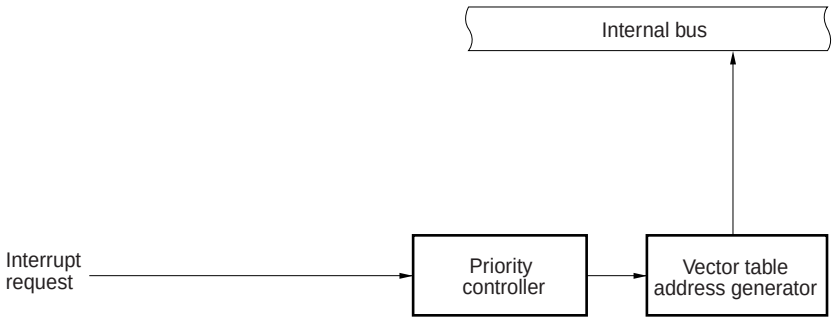


Figure 6-1. Basic Configuration of Interrupt Function (2/2)

(D) Software interrupt



IF: Interrupt request flag
IE: Interrupt enable flag
ISP: In-service priority flag
MK: Interrupt mask flag
PR: Priority specification flag

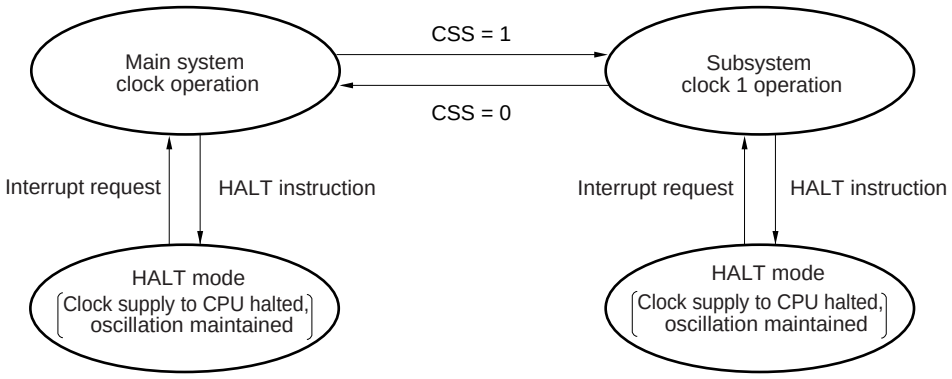
7. STANDBY FUNCTION

The following standby function is available for further reduction of system current consumption.

- HALT mode: In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.

Caution STOP mode is not supported.

Figure 7-1. Standby Function



8. RESET FUNCTION

The following two reset methods are available.

- External reset by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer runaway time detection

★ 9. MASK OPTION

The mask option can be used to specify the connection of an on-chip pull-up resistor to P60 to P62 and the $\overline{\text{RESET}}$ pin, in 1-bit units.

10. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

1st operand \ 2nd operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL+B] [HL+C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

2nd operand / 1st operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

2nd operand / 1st operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instructions/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

2nd operand / 1st operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR, DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT

★ 11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Power supply voltage	V_{DD}			−0.3 to +3.6	V
Input voltage	V_{I1}	P00 to P06, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P63 to P67, P70 to P77, P80 to P87, P90 to P95, X1, X2, XT1, XT2, $\overline{\text{RESET}}$		−0.3 to V_{DD} + 0.3 Note	V
	V_{I2}	P60 to P62	N-ch open drain	−0.3 to +3.6	V
			With pull-up resistor	−0.3 to V_{DD} + 0.3 Note	V
Output voltage	V_O			−0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin		−10	mA
		Total for all pins		−30	mA
Output current, low	I_{OL}	Per pin		30	mA
		Total for all pins		160	mA
Operating ambient temperature	T_A			−40 to +80	°C
Storage temperature	T_{stg}			−60 to +150	°C

Note 3.6 V or below

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (T_A = –40 to +80°C, V_{DD} = 2.2 to 3.5 V)

Resonator	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC resonator	Oscillation frequency (f_{CC})[Note]		1.0	1.2	1.5	MHz

Note Indicates only oscillator characteristics. The C (capacitor) and R (resistor) error is not included. For instruction execution time, refer to **AC Characteristics**.

Subsystem Clock 1 Oscillator Characteristics (T_A = –40 to +80°C, V_{DD} = 2.2 to 3.5 V)

Resonator	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator	Oscillation frequency (f_{XT1})[Note 1]		32	32.768	35	kHz
	Oscillation stabilization time[Note 2]			3	10	s

Notes 1. Indicates only oscillator characteristics. For instruction execution time, refer to **AC Characteristics**.

2. Time required to stabilize oscillation after reset. Make sure the $\overline{\text{RESET}}$ pin holds a low level during this period.

Subsystem Clock 2 Oscillator Characteristics (T_A = –40 to +80°C, V_{DD} = 2.2 to 3.5 V)

Resonator	Parameter	MIN.	TYP.	MAX.	Unit
Crystal resonator	Oscillation frequency (f_{XT2})[Note 1]	4	4.2	5	MHz
	Oscillation stabilization time[Note 2]			20	ms
External clock	XT3 input frequency (f_{XT2})	4		5	MHz
	XT3 input high-/low-level width (t_{XT2H}, t_{XT2L})	85		100	ns

Notes 1. Indicates only oscillator characteristics. For instruction execution time, refer to **AC Characteristics**.

2. Time required to stabilize oscillation after reset.

Recommended Oscillator Constant

Subsystem Clock 1: Ceramic resonator (T_A = –40 to +85°C)

Manufacturer	Part Number	Frequency (kHz)	Recommended Circuit Constant		Oscillation voltage Range		Remark
			C1	C2	MIN.(V)	MAX.(V)	
Seiko Epson Inc.	C-002RX	32.768	22	22	2.0	3.6	Rd = 330 kΩ
	MC-206						
	MC-306						

Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details, contact directly the manufacturer of the resonator used.

DC Characteristics (T_A = –40 to +80°C, V_{DD} = 2.2 to 3.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin				–1	mA
		All pins				–15	
Output current, low	I_{OL}	Per pin				15	mA
		All pins				80	
Input voltage, high	V_{IH1}	P20, P21, P33, P34, P36, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P95		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P06, P22 to P27, P30 to P32, P35, P37, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	XT3, XT4		V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P20, P21, P33, P34, P36, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P95		0		0.3V_{DD}	V
	V_{IL2}	P00 to P06, P22 to P27, P30 to P32, P35, P37, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL3}	XT3, XT4		0		0.1	V
Output voltage, high	V_{OH1}	I_{OH} = –10 mA	P56/MRO0, P57/MRO1	V_{DD} – 0.5		V_{DD}	V
		I_{OH} = –2 mA		V_{DD} – 0.1		V_{DD}	V
		I_{OH} = –5 mA	P55	V_{DD} – 0.5		V_{DD}	V
		I_{OH} = –400 μA	P00 to P06, P20 to P27, P30 to P37, P40 to P47, P50 to P54, P63 to P67, P70 to P77, P80 to P87, P90 to P95	V_{DD} – 0.5		V_{DD}	V
Output voltage, low	V_{OL1}	I_{OL} = 5 mA	P60 to P62 (N-ch open drain)	0		0.5	V
		I_{OL} = 400 μA	P00 to P06, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P63 to P67, P70 to P77, P80 to P87, P90 to P95, $\overline{\text{WDTOUT}}$	0		0.5	V
Power supply current[Note 1]	I_{DD1}	1.0 MHz RC oscillation operation mode [Note 2]	T_A = –40 to +60°C[Note 4]		230	400	μA
			T_A = +60 to +80°C[Note 5]			400	μA
	I_{DD2}	32.768 kHz crystal oscillation operation mode [Note 3]	T_A = –40 to +60°C[Note 4]		6.0	12.0	μA
			T_A = +60 to +80°C[Note 5]			18.0	μA
	I_{DD3}	32.768 kHz crystal oscillation HALT mode [Note 3]	T_A = –40 to +60°C[Note 6]		2.0	4.0	μA
			T_A = +60 to +80°C[Note 7]			8.0	μA
Subsystem clock 2 oscillation current	I_{SUB2}	CKC = 01H (When subsystem clock 2 oscillation enabled)			200	600	μA

Notes 1. Refers to the current flowing through the V_{DD0} and V_{DD1} pins. The current flowing through the LCD controller and ports is not included.

2. When PCC = 00H.

3. When the main system clock is stopped.

4. Only RAM during access (when subsystem clock 2 oscillation and all peripheral functions are stopped.)

5. During RAM access and when all peripheral functions are operating but when LCD operation and subsystem clock 2 oscillation is stopped.)

6. When only the sampling output timer/detector and 8-bit timers 80, 81 are operating but when subsystem clock 2 oscillation is stopped.)

7. When all peripheral functions are operating but when LCD operation and subsystem clock 2 oscillation is stopped.)

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +80°C, V_{DD} = 2.2 to 3.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	XT1, XT2, XT3, XT4		0.7	10	μA
	I_{LIH2}		P00 to P06, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P95, $\overline{\text{RESET}}$		0.03	3	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	XT1, XT2, XT3, XT4, P60 to P62 (Other than when reading)		–0.7	–10	μA
	I_{LIL2}		P00 to P06, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P63 to P67, P70 to P77, P80 to P87, P90 to P95, $\overline{\text{RESET}}$		–0.03	–3	μA
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$			0.03	3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V			–0.03	–3	μA
Mask option pull-up resistor	R_1	V_{IN} = 0 V	$\overline{\text{RESET}}$	10	20	40	kΩ
	R_2		P60 to P62	100	200	400	kΩ
Software pull-up resistor	R_3	V_{IN} = 0 V	P00 to P06, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P63 to P67, P70 to P77, P80 to P87, P90 to P95	100	200	400	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

LCD Controller/Driver Characteristics (T_A = –40 to +80°C, V_{DD} = 2.2 to 3.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}	$V_{DD} = V_{LCD}$		2.2		3.5	V
Power boosting time for capacitor drive[Note 1]	t_{VCLD}	C = 0.47 μF[Note 2]		500			ms
LCD output voltage deviation (common)[Note 3, 4]	V_{ODC}	I_O = ±5 μA	Static 1/3 bias method	0		±0.2	V
LCD output voltage deviation (segment)[Note 3, 4]	V_{ODS}	I_O = ±1 μA	Static 1/3 bias method	0		±0.2	V

Notes 1. Means the time required for the capacitor to boost after bit 4 (LIP0) of LCD mode register 0 (LCDM0) is set to 1 (power supply for LCD drive).

2. "C" is the capacitor connected to V_{LC1} and V_{LC2} between CAPH and CAPL.

3. The power deviation is the difference between the ideal segment and common output values (V_{LCD1}, V_{LCD2}) and the output voltage.

4. Voltage when there is no load.

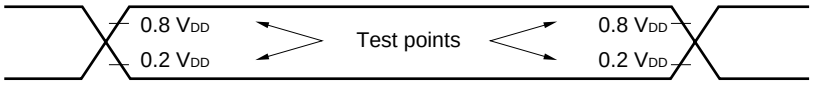
AC Characteristics

(1) Basic operation (T_A = –40 to +80°C, V_{DD} = 2.2 to 3.5 V)

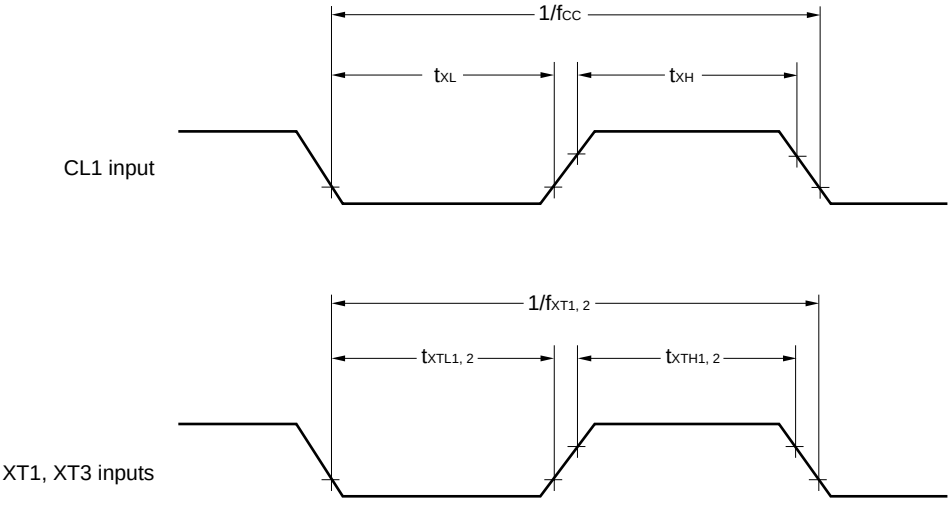
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Minimum instruction execution time)	T_{CY}	Main system clock operation		1.33		8	μs
		Subsystem clock 1 operation		57.1	61	62.5	μs
TI00, TI01, input high-/low-level width	t_{TIH0}, t_{TIL0}			$2/f_{sam}$ + 0.5 Note			μs
TI2 input frequency	f_{TI2}					500	kHz
TI2 input high-/low-level width	t_{TIH2}, t_{TIL2}			0.8			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP6	2.7 V ≤ V_{DD} ≤ 3.5 V	10			μs
			2.2 V ≤ V_{DD} < 2.7 V	20			μs
$\overline{\text{RESET}}$ input low-level width	t_{RSL}	2.7 V ≤ V_{DD} ≤ 3.5 V		10			μs
		2.2 V ≤ V_{DD} < 2.7 V		20			μs
$\overline{\text{WDTOUT}}$ output low-level width	t_{WDTL}			20			μs

Note At each capture trigger, sampling is performed with the count clock selected by bits 0 and 1 (PRM00, PRM01) of prescaler mode register 0 (PRM0) (f_{sam} = f_{XT1}, $f_{XT1}/2$, $f_{XT2}/2^4$). However, if the TI00 valid edge is selected as the count clock, the value becomes f_{sam} = $f_{XT1}/4$.

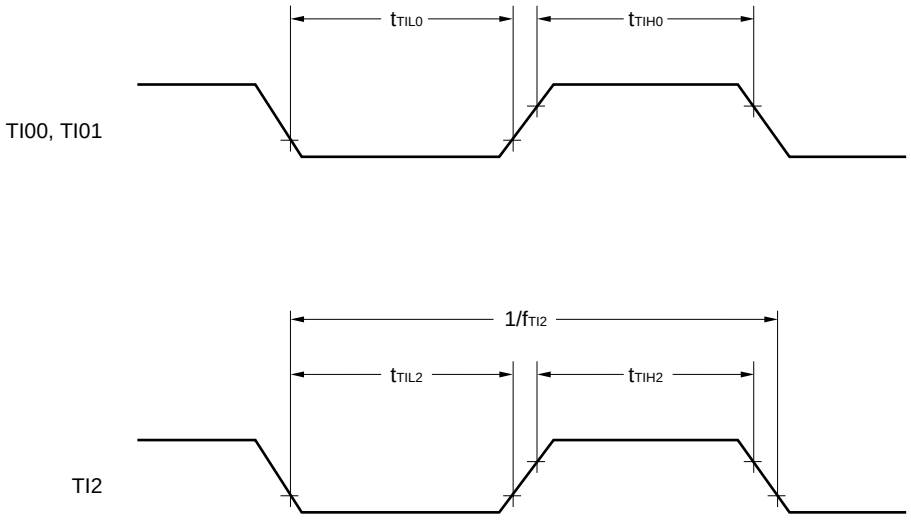
AC Timing Test Points (excluding X1, XT1 inputs)



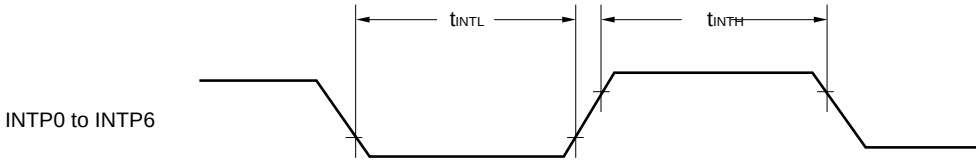
Clock Timing



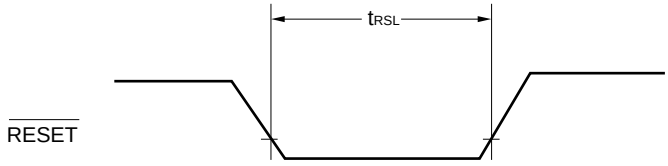
TI Timing



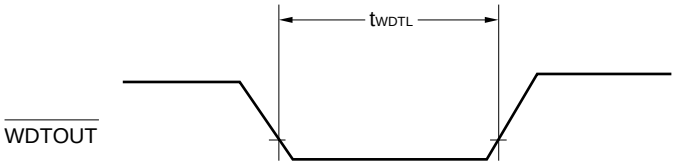
Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing



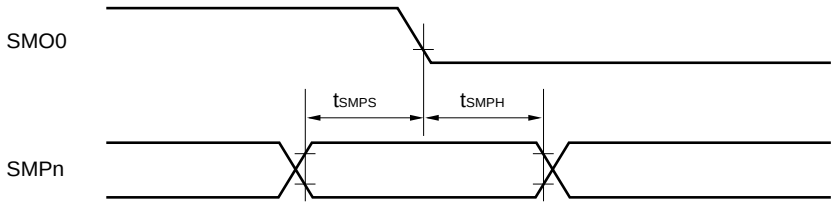
$\overline{\text{WDTOUT}}$ Output Timing



(2) Sampling output timer/detector

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Sampling input setup time	t_{SMPS}		500			ns
Sampling input hold time	t_{SMPH}		500			ns

Sampling output timer/detector input timing

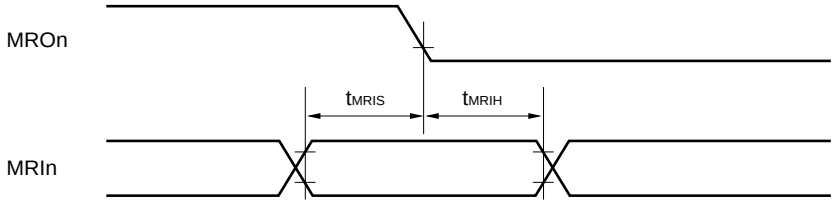


n = 1 to 4

(3) MR sampling function

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Phase detection input setup time	t_{MRIS}		500			ns
Phase detection input hold time	t_{MRIH}		500			ns

MR sampling function input timing



n = 0, 1

(4) Serial interface

(a) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		Select subsystem clock 1 for the input clock of the baud rate generator (ASIF2 TPS21 = 0, TPS20 = 0)			1200	bps
		Select subsystem clock 2 for the input clock of the baud rate generator (ASIF2 TPS21 = 1, TPS20 = 0)			4800	

Remark ASIF2: Asynchronous serial interface function register 2

(b) 3-wire serial I/O mode (internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY1}		30.5			μs
$\overline{SCK3}$ high-/low-level width	t_{KH1}, t_{KL1}		$t_{KCY1}/2 - 50$			ns
SI3 setup time (to $\overline{SCK3}$↑)	t_{SIK1}		300			ns
SI3 hold time (from $\overline{SCK3}$↑)	t_{KSI1}		400			ns
Delay time from $\overline{SCK3}$↓ to SO3 output	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK3}$ and SO3 output lines.

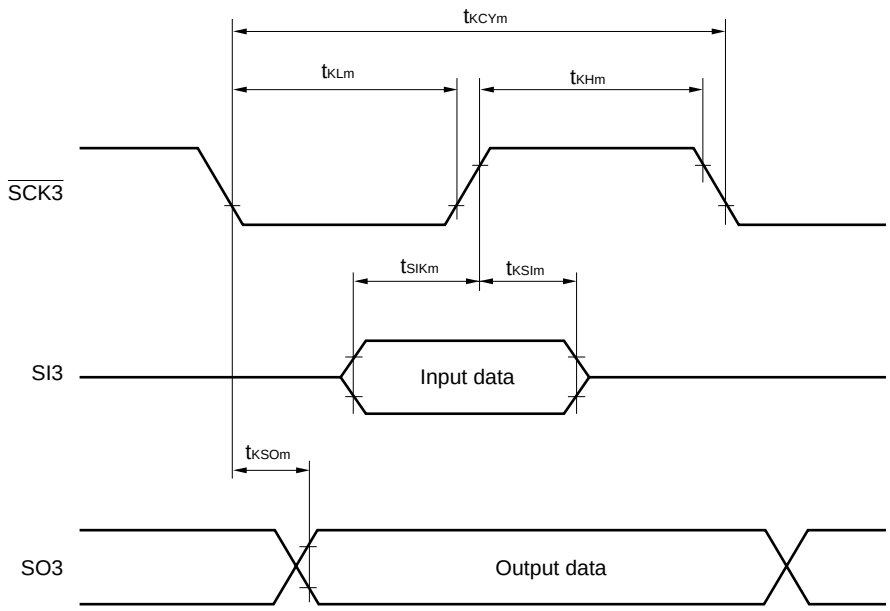
(c) 3-wire serial I/O mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY2}		3.2			μs
$\overline{SCK3}$ high-/low-level width	t_{KH2}, t_{KL2}		1600			ns
SI3 setup time (to $\overline{SCK3}$↑)	t_{SIK2}		100			ns
SI3 hold time (from $\overline{SCK3}$↑)	t_{KSI2}		400			ns
Delay time from $\overline{SCK3}$↓ to SO3 output	t_{KSO2}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the SO3 output line.

Serial Transfer Timing

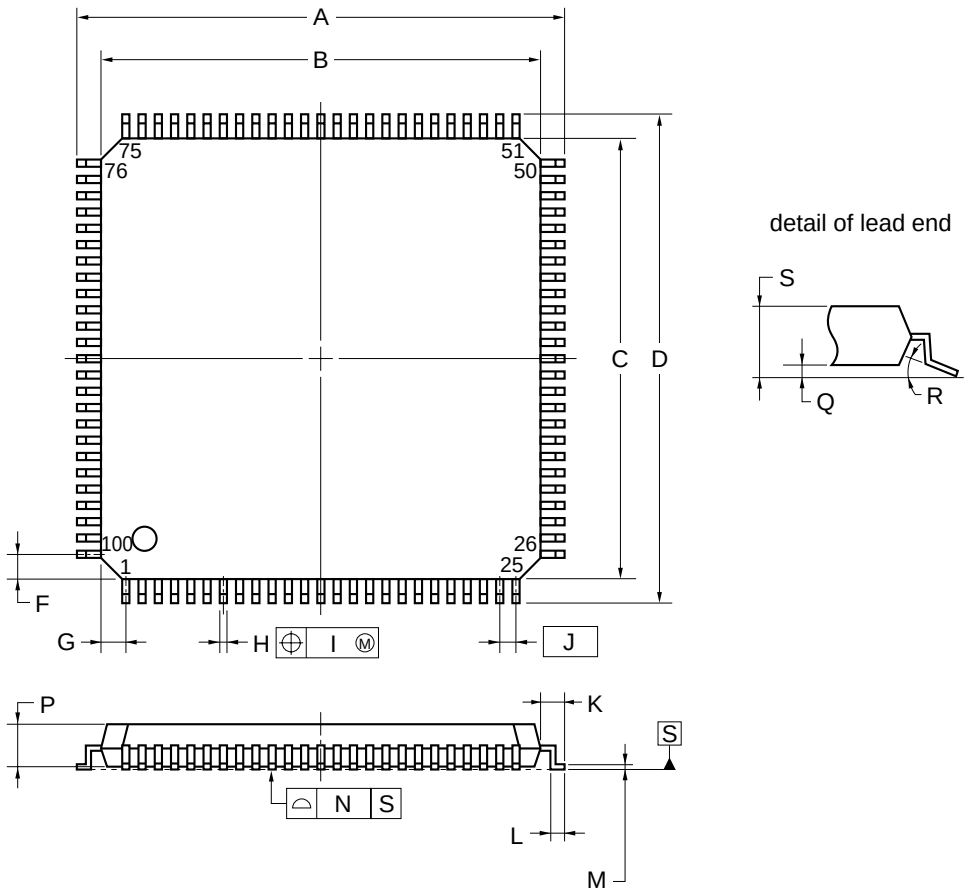
3-wire serial i/o mode:



Remark m = 1, 2

12. PACKAGE DRAWING

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



detail of lead end

NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	$0.22^{+0.05}_{-0.04}$
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.

S100GC-50-8EU, 8EA-2

★ 13. RECOMMENDED SOLDERING CONDITIONS

The μPD780957(A) and 780958(A) should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 13-1. Surface Mounting Type Soldering Conditions

μPD780957GC(A)-×××-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
μPD780958GC(A)-×××-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. max. (at 210°C or higher), Count: two times or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 sec. max. (at 200°C or higher), Count: two times or less	VP15-00-2
Partial heating	Pin temperature: 300°C max., Time: 3 sec. max. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

⋆ APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD780958 Subseries. Also refer to **(4) Cautions on Using Development Tools**.

(1) Language Processing Software

RA78K0	Assembler package common to 78K/0 Series
CC78K0	C compiler package common to 78K/0 Series
DF780958	Device file for μPD780958 Subseries
CC78K0-L	C compiler library source file common to 78K/0 Series

(2) Debugging Tools

- **When IE-78K0-NS in-circuit emulator is used**

IE-78K0-NS		In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B		Power supply unit for IE-78K0-NS
IE-78K0-NS-PA		Performance board to enhance and expand the functions of IE-78K0-NS
IE-70000-98-IF-C		Adapter necessary when using PC-9800 series PC (except notebook type) as host machine (C bus supported)
IE-70000-CD-IF-A		PC card and interface cable necessary when using notebook PC as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C		Adapter necessary when using IBM PC/AT™ compatible as host machine (ISA bus supported)
IE-70000-PCI-IF-A		Adapter necessary when using PC in which PCI bus is incorporated as host machine
IE-780958-NS-EM4		Emulation board to emulate μPD780958 Subseries
IE-78K0-NS-P02		I/O board to emulate μPD780958 Subseries
NP-100GC		Emulation probe for 100-pin plastic LQFP (fine pitch) (GC-8EU type)
	TGC-100SDW	Conversion adapter to connect the NP-100GC and a target system board on which a 100-pin plastic LQFP (fine pitch) (GC-8EU type) can be mounted
ID78K0-NS		Integrated debugger for IE-78K0-NS
SM78K0		System simulator common to 78K/0 Series
DF780958		Device file for μPD780958 Subseries

- **When IE-78001-R-A in-circuit emulator is used**

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-C	Adapter necessary when using PC-9800 series PC (except notebook type) as host machine (C bus supported)
IE-70000-PC-IF-C	Adapter necessary when using IBM PC/AT compatibles as host machine (ISA bus supported)
IE-70000-PCI-IF-A	Adapter necessary when using PC in which PCI bus is incorporated as host machine
IE-78000-R-SV3	Interface adapter and cable necessary when using EWS as host machine
IE-780958-NS-EM4	Probe board to emulate μPD780958 Subseries
IE-78K0-NS-P02	I/O board necessary to emulate μPD780958 Subseries
IE-78K0-R-EX1	Emulation probe conversion board necessary when using IE-780958-NS-EM4+IE-78K0-NS-P02 on IE-78001-R-A
EP-78064GC-R	Emulation probe for 100-pin plastic LQFP (fine pitch) (GC-8EU type)
TGC-100SDW	Adapter to be mounted on a target system board made for 100-pin plastic LQFP (fine pitch) (GC-8EU type)
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF780958	Device file for μPD780958 Subseries

(3) Real-time OS

RX78K0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

(4) Cautions on Using Development Tools

- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780958.
- The CC78K0 and RX78K0 are used in combination with the RA78K0 and DF780958.
- The NP-100GC is a product made by Naito Densei Machidas Mfg. Co., Ltd. (TEL +81-44-822-3813).
- The TGC-100SDW is a product made by TOKYO ELETECH CORPORATION.
  For further information, contact: Daimaru Kogyo, Ltd.
  Tokyo Electronics Department (TEL +81-3-3820-7112)
  Osaka Electronics Department (TEL +81-6-6244-6672)
- TGC-100SDW is sold in single units.
- For third party development tools, see the **Single-Chip Microcontroller Development Tools Selection Guide (U11069E)**.
- The host machine and OS suitable for each software are as follows:

Host Machine [OS] / Software	PC	EWS
	PC-9800 series [Japanese Windows™] IBM PC/AT and compatibles [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K0	√Note	√
CC78K0	√Note	√
ID78K0-NS	√	–
ID78K0	√	√
SM78K0	√	–
RX78K0	√Note	√
MX78K0	√Note	√

Note DOS-based software

APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

★ **● Documents Related to Devices**

Document Name	Document No.
μPD780958 Subseries User's Manual	U13655E
μPD780957(A), 780958(A) Data Sheet	This document
78K/0 Series User's Manual Instructions	U12326E

★ **● Documents Related to Development Tools (User's Manuals)**

Document Name		Document No.
RA78K0 Assembler Package	Operation	U11802E
	Language	U11801E
	Structured Assembly Language	U11789E
CC78K0 C Compiler	Operation	U11517E
	Language	U11518E
IE-78K0-NS In-Circuit Emulator		U13731E
IE-78001-R-A In-Circuit Emulator		To be prepared
IE-780958-NS-EM4 Emulation Board		To be prepared
EP-78064 Emulation Probe		EEU-1469
SM78K0S, SM78K0 System Simulator Ver. 2.10 or Later Windows Based	Operation	U14611E
SM78K Series System Simulator Ver. 2.10 or Later	External Part User Open Interface Specifications	U15006E
ID78K0-NS Integrated Debugger Ver. 2.00 or Later Windows Based	Operation	U14379E
ID78K0-NS, ID78K0S-NS Integrated Debugger Ver. 2.20 or Later Windows Based	Operation	U14910E
ID78K0 Integrated Debugger Windows Based	Reference	U11539E
	Guide	U11649E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

- **Documents Related to Embedded Software (User's Manuals)**

Document Name		Document No.
78K/0 Series Real-Time OS	Fundamental	U11537E
	Installation	U11536E
78K/0 Series OS MX78K0	Fundamental	U12257E

- **Other Related Documents**

Document Name	Document No.
★ SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

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[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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Fax: 408-588-6130
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  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.
  The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.
  (Note)
  (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.
  (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).

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