NEC

MOS INTEGRATED CIRCUIT

μPD78094, 78095, 78096, 78098A

8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD78094, 78095, 78096, 78098A are members of the μPD78098 subseries of the 78K/0 series of microcontrollers. Besides a high-speed and high-performance CPU, each microcontroller has on-chip ROM, RAM, I/O ports, an IEBus™ controller, an 8-bit resolution A/D converter, an 8-bit resolution D/A converter, a timer, serial interface, real-time output port, interrupt control, and various other peripheral hardware.

PROM versions (μPD78P098A) will be added to this subseries. These μPD78P098A devices will consist of a one-time PROM version and an EPROM version, both of which operating in the same power supply voltage range as the mask ROM version. Various development tools are currently being developed.

The details of the functions are described in the following user's manuals. Be sure to read them before starting design.

μPD78098 Subseries User's Manual: IEU-1381

78K/0 Series User's Manual – Instructions: IEU-1372

FEATURES

- Internal high capacity ROM and RAM

Item / Part number	Program memory (ROM)	Data memory			Package
		Internal high-speed RAM	Buffer RAM	Internal expansion RAM	
μPD78094	32 Kbytes	1024 bytes	32 bytes	None	80-pin plastic QFP (14 x 14 mm)
μPD78095	40 Kbytes				
μPD78096	48 Kbytes				
μPD78098A	60 Kbytes			2048 bytes	

- External memory expansion space: 64 Kbytes
- Instruction execution time can be varied from high-speed (0.5 μs) to ultra-low-speed (122 μs)
- I/O ports: 69 (N-ch open-drain: 4)
- IEBus controller
  - Effective transmission rate: 3.9 kbps/17 kbps/26 kbps
- 8-bit resolution A/D converter: 8 channels
- 8-bit resolution D/A converter: 2 channels
- Serial interface: 3 channels
  - 3-wire/SBI/2-wire mode: 1 channel
  - 3-wire mode: 1 channel
  - 3-wire/UART mode: 1 channel
- Timer: 5 channels
- Supply voltage: V_{DD} = 2.7 to 5.5 V

APPLICATIONS

Car audio, CD (compact disk) changer, etc.

Document No. U10146EJ1V0DS00 (1st edition)
Date Published October 1995 P
Printed in Japan

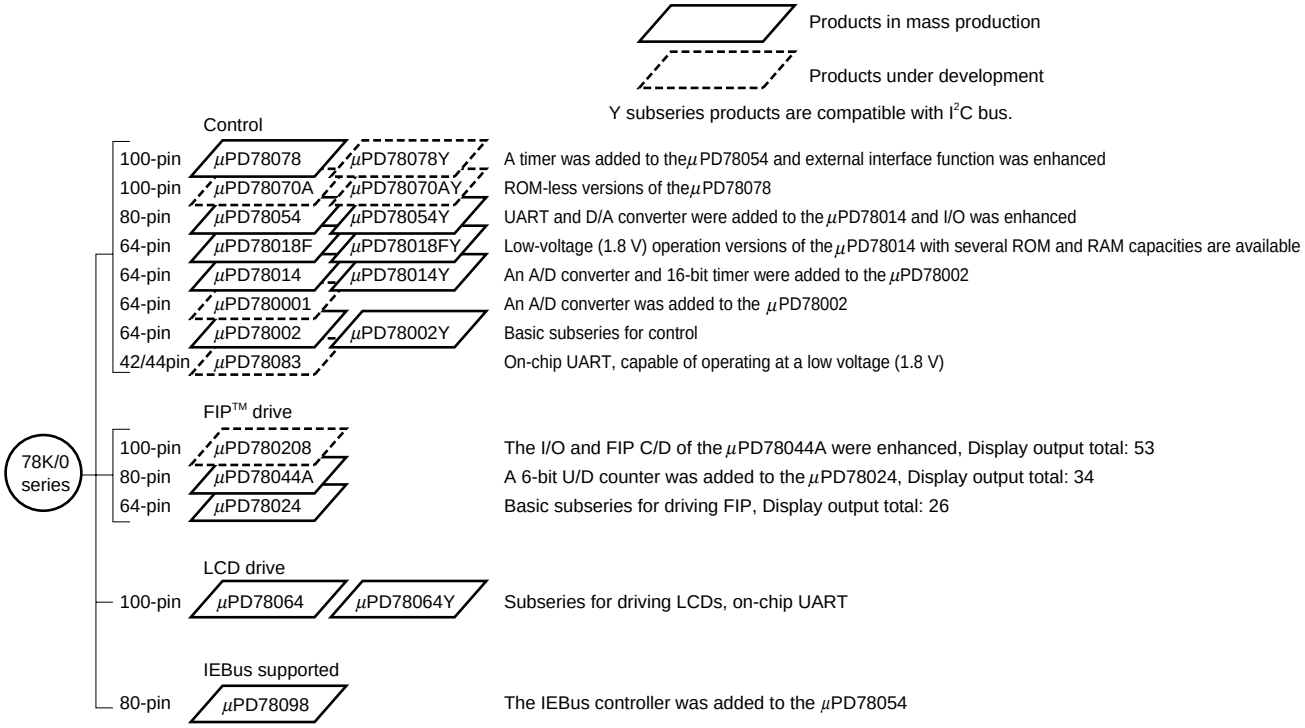
ORDERING INFORMATION

Part Number	Package
μPD78094GC-×××-3B9	80-pin plastic QFP (14 × 14 mm)
μPD78095GC-×××-3B9	80-pin plastic QFP (14 × 14 mm)
μPD78096GC-×××-3B9	80-pin plastic QFP (14 × 14 mm)
μPD78098AGC-×××-3B9	80-pin plastic QFP (14 × 14 mm)

Remark ××× indicates a ROM code suffix.

78K/0 SERIES DEVELOPMENT

The following shows the 78K/0 series products development. Subseries names are shown inside frames.



The following table shows the differences among subseries functions.

Part number \ Function		ROM capacity	Timer				8-bit A/D	8-bit D/A	Serial interface	I/O	V_{DD} MIN. Value	External expansion
			8-bit	16-bit	Watch	WDT						
Control	μPD78078	32K-60K	4ch	1ch	1ch	1ch	8ch	2ch	3ch (UART: 1ch)	88	1.8 V	Available
	μPD78070A	–								61	2.7 V	
	μPD78054	16K-60K	2ch							69	2.0 V	
	μPD78018F	8K-48K						–	2ch	53	1.8 V	
	μPD78014	8K-32K									2.7 V	
	μPD780001	8K		–	–				1ch	39		–
	μPD78002	8K-16K			1ch		–			53		Available
	μPD78083				–		8ch		1ch (UART: 1ch)	33	1.8 V	–
FIP drive	μPD780208	32K-40K	2ch	1ch	1ch	1ch	8ch	–	2ch	74	2.7 V	–
	μPD78044A	16K-40K								68		
	μPD78024	24K-32K								54		
LCD drive	μPD78064	16K-32K	2ch	1ch	1ch	1ch	8ch	–	2ch (UART: 1ch)	57	2.0 V	–
IEBus Supported	μPD78098	32K-60K	2ch	1ch	1ch	1ch	8ch	2ch	3ch (UART: 1ch)	69	2.7 V	Available

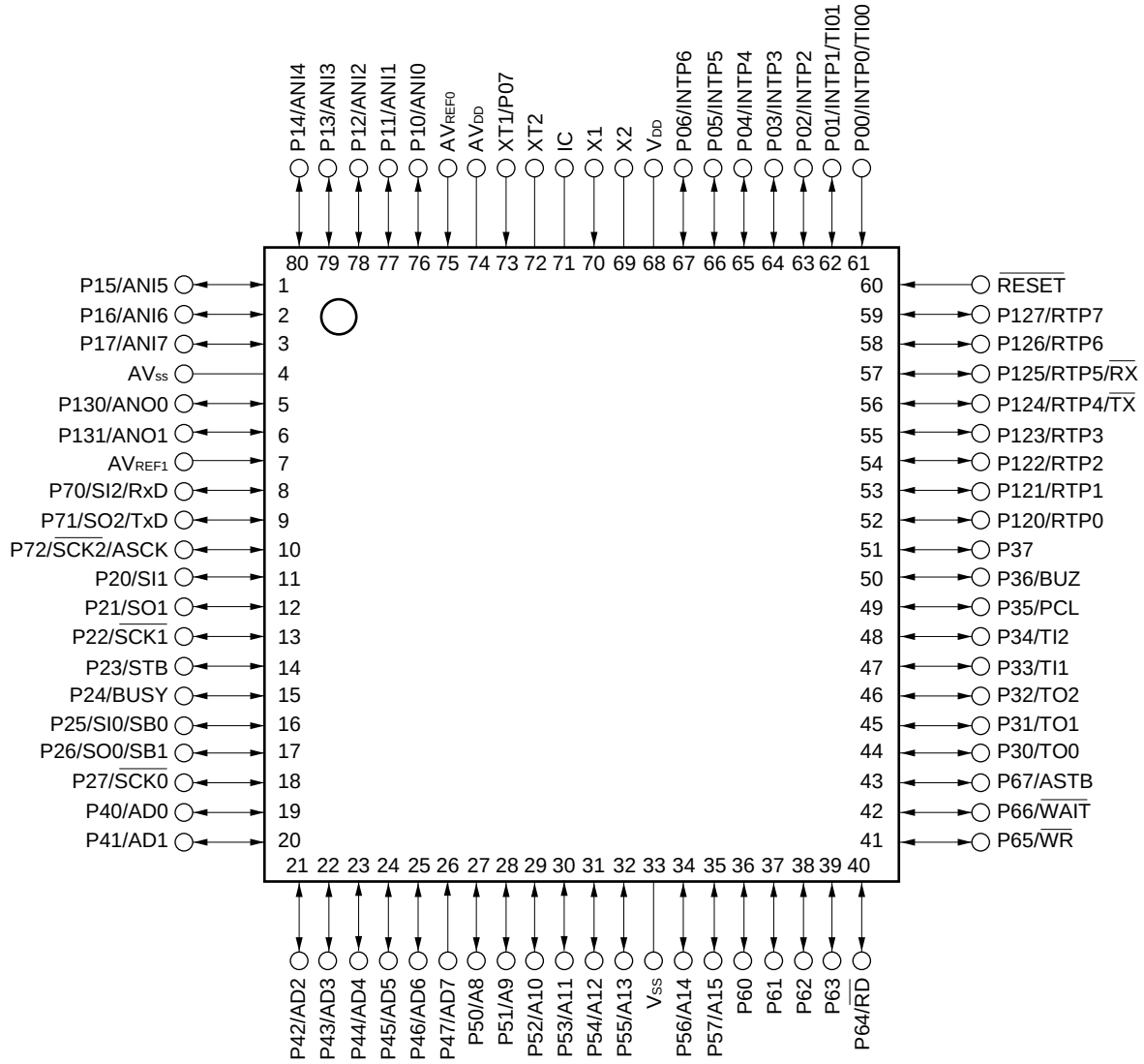
Overview of Function

Item \ Part number		μPD78094	μPD78095	μPD78096	μPD78098A
Internal memory	ROM	32 Kbytes	40 Kbytes	48 Kbytes	60 Kbytes
	Internal high-speed RAM	1024 bytes			
	Buffer RAM	32 bytes			
	Internal expansion RAM	None			2048 bytes
Memory space		64 Kbytes			
General registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Instruction cycle		On-chip instruction execution time cycle variable function			
	When main system clock selected	0.5 μs/1.0 μs/2.0 μs/4.0 μs/8.0 μs/16.0 μs (at main system clock of 6.0 MHz)			
	When subsystem clock selected	122 μs (at subsystem clock of 32.768 kHz)			
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, boolean operation) • BCD adjust, etc.			
I/O ports		Total : 69 • CMOS input : 2 • CMOS I/O : 63 • N-ch open-drain I/O : 4			
IEBus controller		Effective transmission rate : 3.9 kbps/17 kbps/26 kbps			
A/D converter		• 8-bit resolution × 8 channels			
D/A converter		• 8-bit resolution × 2 channels			
Serial interface		• 3-wire/SBI/2-wire mode selectable : 1 channel • 3-wire mode (on-chip max. 32 bytes automatic data transmit/receive function): 1 channel • 3-wire/UART mode selectable : 1 channel			
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel			
Timer output		3 (14-bit PWM output × 1)			
Clock output		15.6 kHz, 31.3 kHz, 62.5 kHz, 125 kHz, 250 kHz, 500 kHz, 1.0 MHz, 2.0 MHz, 4.0 MHz (at main system clock of 6.0 MHz) 32.768 kHz (at subsystem clock of 32.768 kHz)			
Buzzer output		977 Hz, 1.95 kHz, 3.9 kHz, 7.8 kHz (at main system clock of 6.0 MHz)			
Vectored interrupts	Maskable interrupts	Internal: 14, external: 7			
	Non-maskable interrupt	Internal: 1			
	Software interrupt	Internal: 1			
Test input		Internal: 2, external: 1			
Supply voltage		V_{DD} = 2.7 to 5.5 V			
Package		80-pin plastic QFP (14 x 14 mm)			

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- 80-pin plastic QFP (14 × 14 mm)
  μPD78094GC-×××-3B9
  μPD78095GC-×××-3B9
  μPD78096GC-×××-3B9
  μPD78098AGC-×××-3B9



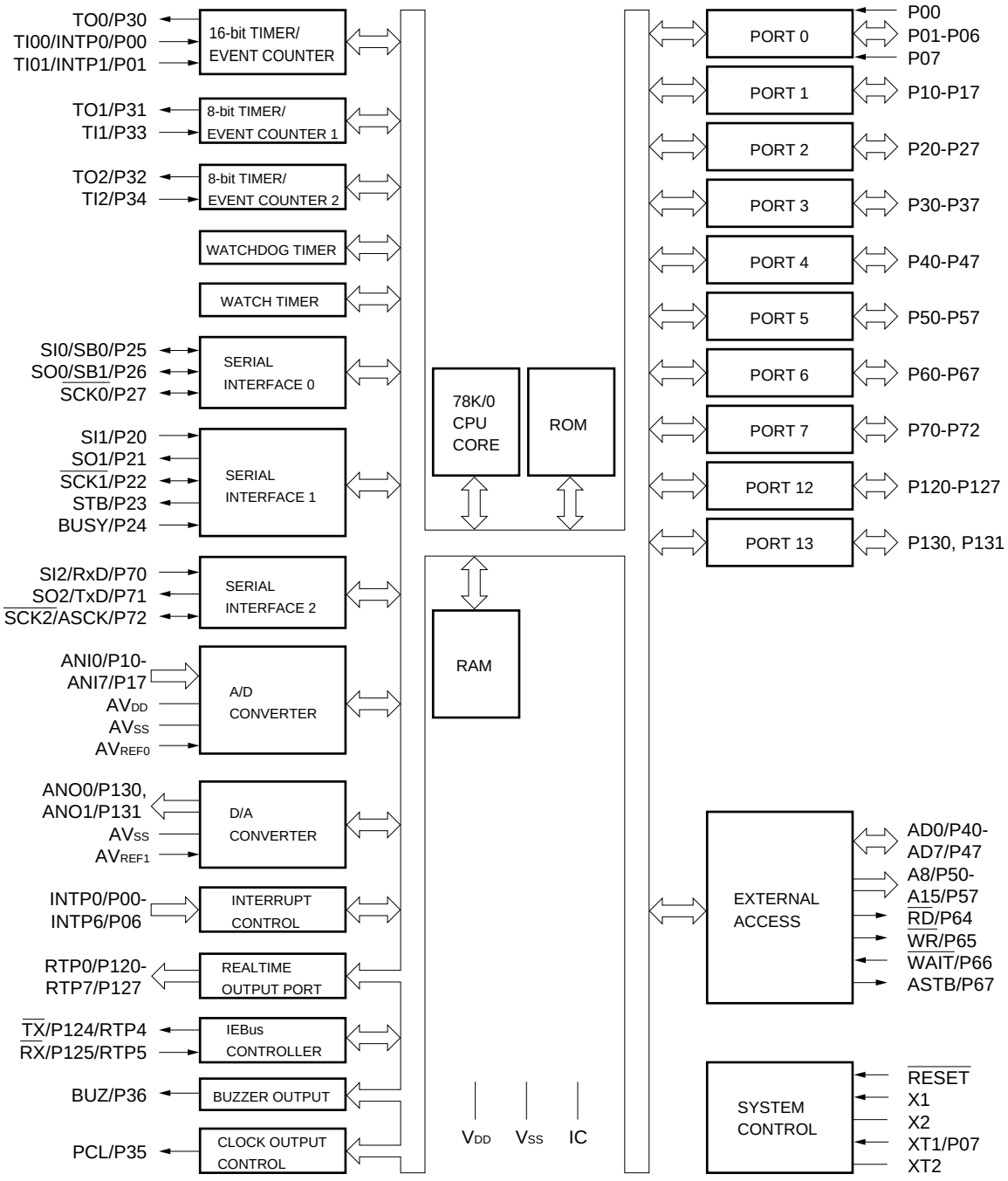
Cautions 1. Connect IC (Internally Connected) pin directly to V_{SS}.

2. AV_{DD} pin should be connected to V_{DD}.

3. AV_{SS} pin should be connected to V_{SS}.

P00–P07	: Port0
P10–P17	: Port1
P20–P27	: Port2
P30–P37	: Port3
P40–P47	: Port4
P50–P57	: Port5
P60–P67	: Port6
P70–P72	: Port7
P120–P127	: Port12
P130, P131	: Port13
RTP0–RTP7	: Realtime Output Port
INTP0–INTP6	: Interrupt from Peripherals
TI00, TI01	: Timer Input
TI1, TI2	: Timer Input
TO0–TO2	: Timer Output
SB0, SB1	: Serial Bus
SI0–SI2	: Serial Input
SO0–SO2	: Serial Output
$\overline{\text{SCK0}}$–$\overline{\text{SCK2}}$	: Serial Clock
RxD	: Receive Data (UART)
TxD	: Transmit Data (UART)
ASCK	: Asynchronous Serial Clock
$\overline{\text{RX}}$	: Receive Data (IEBus Controller)
$\overline{\text{TX}}$	: Transmit Data (IEBus Controller)
PCL	: Programmable Clock
BUZ	: Buzzer Clock
STB	: Strobe
BUSY	: Busy
AD0–AD7	: Address/Data Bus
A8–A15	: Address Bus
$\overline{\text{RD}}$	: Read Strobe
$\overline{\text{WR}}$	: Write Strobe
$\overline{\text{WAIT}}$	: Wait
ASTB	: Address Strobe
X1, X2	: Crystal (Main System Clock)
XT1, XT2	: Crystal (Subsystem Clock)
$\overline{\text{RESET}}$	: Reset
ANI0–ANI7	: Analog Input
ANO0, ANO1	: Analog Output
AV_{DD}	: Analog Power Supply
AV_{SS}	: Analog Ground
$AV_{REF0, 1}$	: Analog Reference Voltage
V_{DD}	: Power Supply
V_{SS}	: Ground
IC	: Internally Connected

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function Pin
P00	Input	Port 0	Input only	Input	INTP0/TI00
P01	Input/ Output	8-bit I/O port	Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P06					INTP6
P07[Note 1]	Input		Input only	Input	XT1
P10-P17	Input/ Output	Port 1 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.[Note 2]		Input	ANI0-ANI7
P20	Input/ Output	Port 2 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	SI1
P21					SO1
P22					$\overline{SCK1}$
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					$\overline{SCK0}$
P30	Input/ Output	Port 3 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—
P40-P47	Input/ Output	Port 4 8-bit input/output port. Input/output can be specified in 8-bit units. When used as an input port, pull-up resistor can be connected by software.		Input	AD0-AD7

Notes 1. When using the P07/XT1 pins as an input port, set 1 to bit 6 of the processor clock control register (FRC). Do not use the on-chip feedback resistor of the subsystem clock oscillator.

2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input, the pull-up resistor is automatically disconnected.

3.1 Port Pins (2/2)

Pin Name	I/O	Function		After Reset	Alternate Function Pin
P50-P57	Input/ Output	Port 5 8-bit input/output port. LEDs can be driven directly. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	A8-A15
P60	Input/ Output	Port 6 8-bit input/output port. Input/output can be specified bit-wise.	N-ch open-drain input/output port. On-chip pull-up resistor can be specified by mask option. LED can be driven directly.	Input	—
P61					
P62					
P63					
P64			When used as an input port, pull-up resistor can be connected by software.	Input	$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB
P70	Input/ Output	Port 7 3-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	SI2/RxD
P71					SO2/TxD
P72					$\overline{SCK2}$/ASCK
P120-P123	Input/ Output	Port 12 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	RTP0-RTP3
P124					RTP4/$\overline{TX}$
P125					RTP5/$\overline{RX}$
P126, P127					RTP6, RTP7
P130, P131	Input/ Output	Port 13 2-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	ANO0, ANO1

3.2 Non-port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function Pin
INTP0	Input	External interrupt input by which the active edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
INTP6				P06
SI0	Input	Serial interface serial data input.	Input	P25/SB0
SI1				P20
SI2				P70/RxD
SO0	Output	Serial interface serial data output.	Input	P26/SB1
SO1				P21
SO2				P71/TxD
SB0	Input/ Output	Serial interface serial data input/output.	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	Input/ Output	Serial interface serial clock input/output.	Input	P27
$\overline{SCK1}$				P22
$\overline{SCK2}$				P72/ASCK
STB	Output	Serial interface automatic transmit/receive strobe output.	Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input.	Input	P24
RxD	Input	Asynchronous serial interface serial data input.	Input	P70/SI2
TxD	Output	Asynchronous serial interface serial data output.	Input	P71/SO2
ASCK	Input	Asynchronous serial interface serial clock input.	Input	P72/$\overline{SCK2}$
TI00	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00).		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1).		P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TO0	Output	16-bit timer output (also used for 14-bit PWM output).	Input	P30
TO1		8-bit timer output.		P31
TO2				P32
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
RTP0-RTP3	Output	Real-time output port by which data is output in synchronization with a trigger.	Input	P120-P123
RTP4				P124/$\overline{TX}$
RTP5				P125/$\overline{RX}$
RTP6, RTP7				P126, P127
$\overline{TX}$	Output	IEBus controller data output	Input	P124/RTP4
$\overline{RX}$	Input	IEBus controller data input	Input	P125/RTP5

3.2 Non-port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function Pin
AD0-AD7	Input/ Output	Low-order address/data bus at external memory expansion.	Input	P40-P47
A8-A15	Output	High-order address bus at external memory expansion.	Input	P50-P57
$\overline{RD}$	Output	External memory read operation strobe signal output.	Input	P64
$\overline{WR}$		External memory write operation strobe signal output.		P65
$\overline{WAIT}$	Input	Wait insertion at external memory access.	Input	P66
ASTB	Output	Strobe output which latches the address data output for ports 4 or 5 to access external memory.	Input	P67
AN10-AN17	Input	A/D converter analog input.	Input	P10-P17
ANO0, ANO1	Output	D/A converter analog output.	Input	P130, P131
AV_{REF0}	Input	A/D converter reference voltage input.	—	—
AV_{REF1}	Input	D/A converter reference voltage input.	—	—
AV_{DD}	—	A/D converter analog power supply. Connect to V_{DD}.	—	—
AV_{SS}	—	A/D converter ground potential. Connect to V_{SS}.	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P07
XT2	—		—	—
V_{DD}	—	Positive power supply.	—	—
V_{SS}	—	Ground potential.	—	—
IC	—	Internal connection. Connected directly to V_{SS}.	—	—

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, see Figure 3-1.

Table 3-1. Types of Pin Input/Output Circuits (1/2)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection for Unused Pins
P00/INTP0/TI00	2	Input	Connect to V_{SS}.
P01/INTP1/TI01	8-A	Input/output	Independently connect to V_{SS} via a resistor.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P06/INTP6			
P07/XT1	16	Input	Connect to V_{DD} or V_{SS}.
P10/ANI0-P17/ANI7	11	Input/output	Independently connect to V_{DD} or V_{SS} via a resistor.
P20/SI1	8-A		
P21/SO1	5-A		
P22/$\overline{\text{SCK1}}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/$\overline{\text{SCK0}}$			
P30/TO0	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0-P47/AD7	5-E		Independently connect to V_{DD} via a resistor.
P50/A8-P57/A15	5-A		Independently connect to V_{DD} or V_{SS} via a resistor.
P60-P63	13-B		Independently connect to V_{DD} via a resistor.
P64/$\overline{\text{RD}}$	5-A		Independently connect to V_{DD} or V_{SS} via a resistor.
P65/$\overline{\text{WR}}$			
P66/$\overline{\text{WAIT}}$			
P67/ASTB			

Table 3-1. Types of Pin Input/Output Circuits (2/2)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection for Unused Pins
P70/SI2/RxD	8-A	Input/output	Independently connect to V_{DD} or V_{SS} via a resistor.
P71/SO2/TxD	5-A		
P72/$\overline{SCK2}$/ASCK	8-A		
P120/RTP0-P123/RTP3	5-A		
P124/RTP4/$\overline{TX}$			
P125/RTP5/$\overline{RX}$			
P126/RTP6, P127/RTP7			
P130/ANO0, P131/ANO1	12-A		Independently connect to V_{SS} via a resistor.
$\overline{RESET}$	2	Input	—
XT2	16	—	Leave open.
AV_{REF0}	—		Connect to V_{SS}.
AV_{REF1}			Connect to V_{DD}.
AV_{DD}			
AV_{SS}			Connect to V_{SS}.
IC			Connect directly to V_{SS}.

Figure 3-1. Pin Input/Output Circuits (1/2)

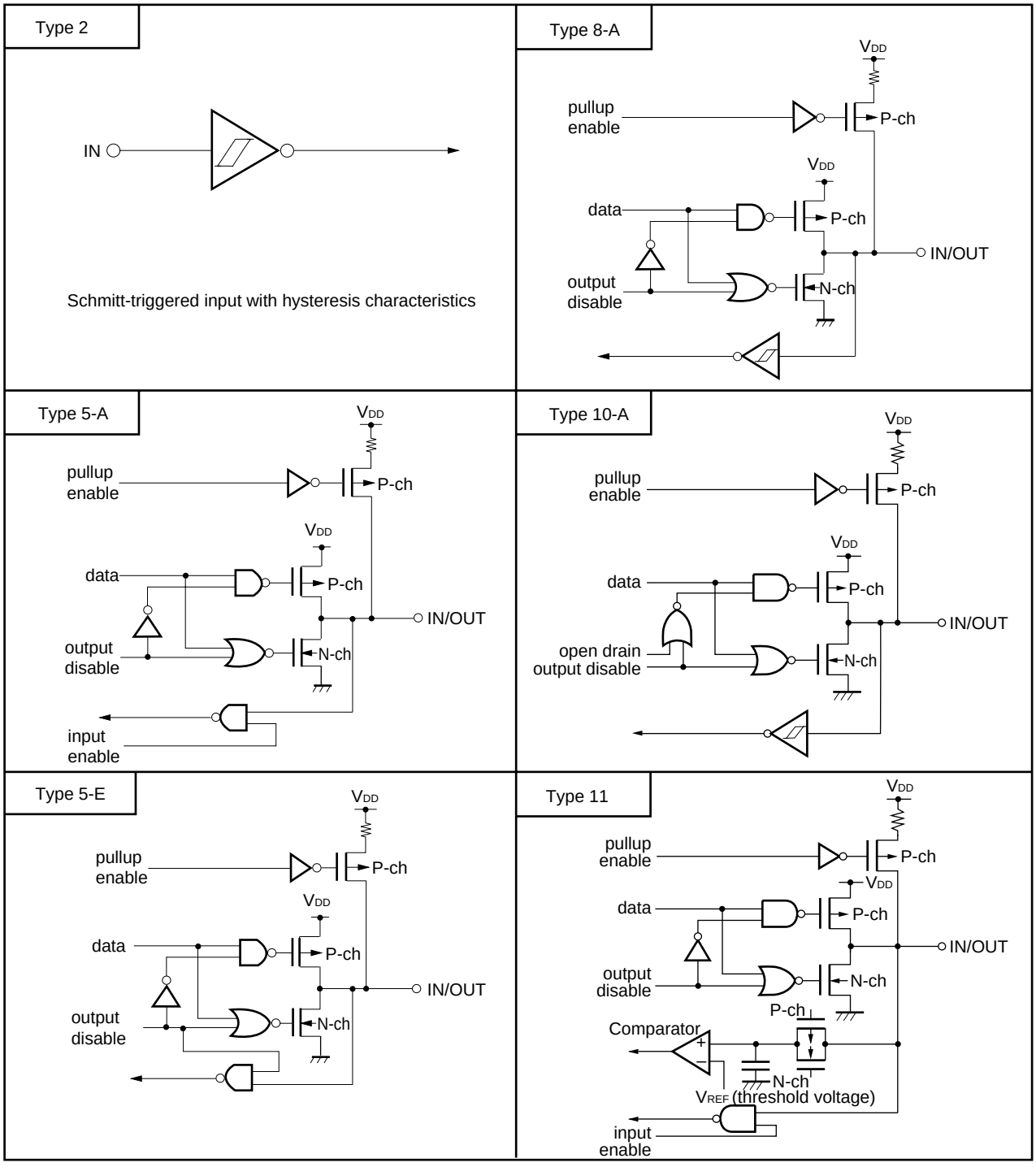
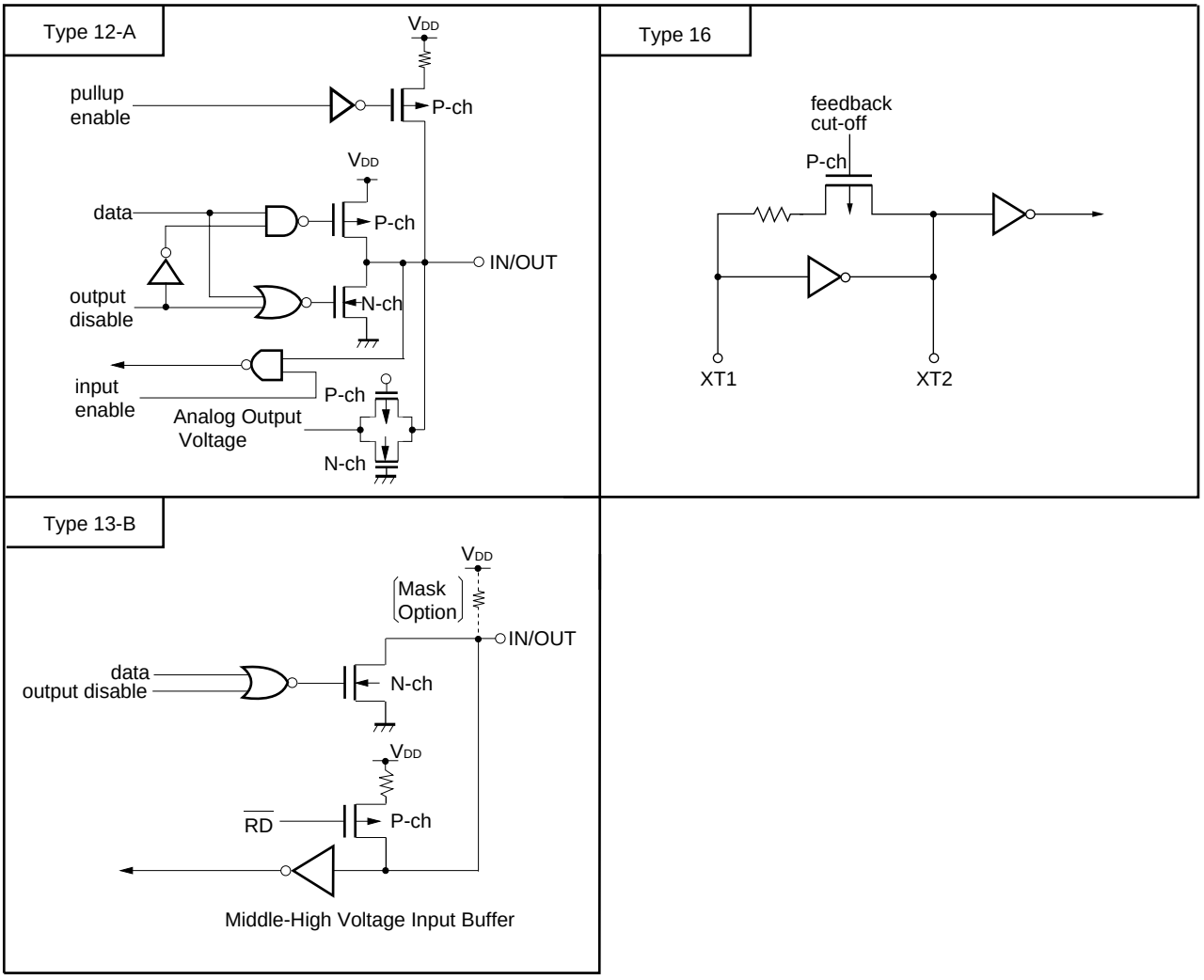


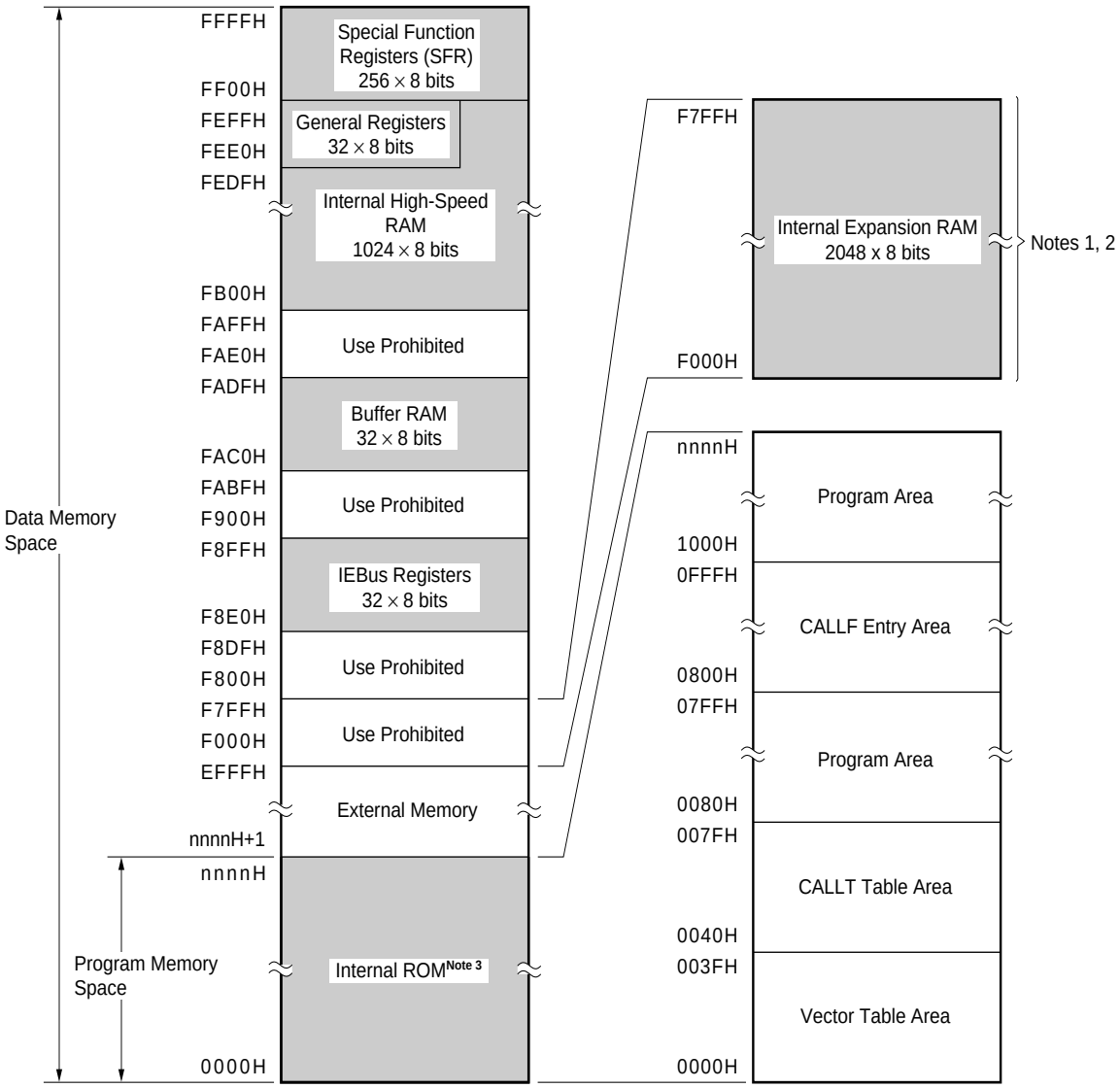
Figure 3-2. Pin Input/Output Circuits (2/2)



4. MEMORY SPACE

The memory map of the μPD78094, 78095, 78096, and 78098A is shown in Figure 4-1.

Figure 4-1. Memory Map



Notes 1. Only μPD78098A.

2. When using the external device expansion function with the μPD78098A, set the internal ROM capacity to below 56 Kbytes by using a memory size switching register.

3. Internal ROM capacity is different among products.

Target Part number	Internal ROM last address nnnnH	Target part number	Internal ROM last address nnnnH
μPD78094	7FFFFH	μPD78096	BFFFH
μPD78095	9FFFFH	μPD78098A	EFFFH

Remark Shaded areas indicate internal memory.

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

Input/output ports are classified into three types.

- CMOS input (P00, P07) : 2
- CMOS input/output (P01-P06, Ports 1-5, P64-P67, Port 7, Port 12, Port 13) : 63
- N-ch open-drain input/output (P60-P63) : 4

Total : 69

Table 5-1. Functions of Ports

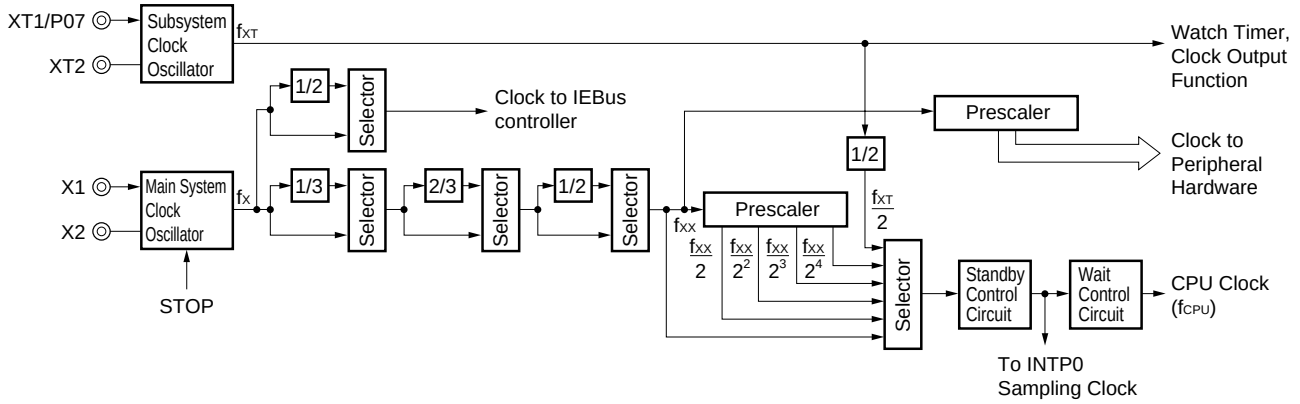
Port Name	Pin Name	Function
Port 0	P00, P07	Input only.
	P01-P06	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 1	P10-P17	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 2	P20-P27	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 3	P30-P37	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 4	P40-P47	Input/output port. Input/output can be specified in 8-bit units. When used as an input port, on-chip pull-up resistor can be connected by software. The test input flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50-P57	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software. LEDs can be driven directly.
Port 6	P60-P63	N-ch open-drain input/output port. Input/output can be specified bit-wise. On-chip pull-up resistor can be connected by mask option. LEDs can be driven directly.
	P64-P67	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 7	P70-P72	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 12	P120-P127	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 13	P130, P131	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.

5.2 Clock Generator

There are two kinds of clock generators: main system and subsystem clock generators. It is possible to change the instruction execution time.

- 0.5 μs/1.0 μs/2.0 μs/4.0 μs/8.0 μs/16.0 μs (at main system clock frequency of f_{XX} = 6.0 MHz)
- 122 μs (at subsystem clock frequency of f_{XT} = 32.768 kHz)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer/Event Counter

There are the following five timer/event counter channels:

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Types and Functions of Timer/Event Counters

		16-bit Timer/Event Counter	8-bit Timer/Event Counter	Watch Timer	Watchdog Timer
Type	Interval timer	1 channel	2 channels	1 channel	1 channel
	External event counter	1 channel	2 channels	—	—
Function	Timer output	1 output	2 outputs	—	—
	PWM output	1 output	—	—	—
	Pulse width measurement	2 inputs	—	—	—
	Square wave output	1 output	2 outputs	—	—
	One-shot pulse output	1 output	—	—	—
	Interrupt request	2	2	1	1
	Test input	—	—	1	—

Figure 5-2. 16-Bit Timer/Event Counter Block Diagram

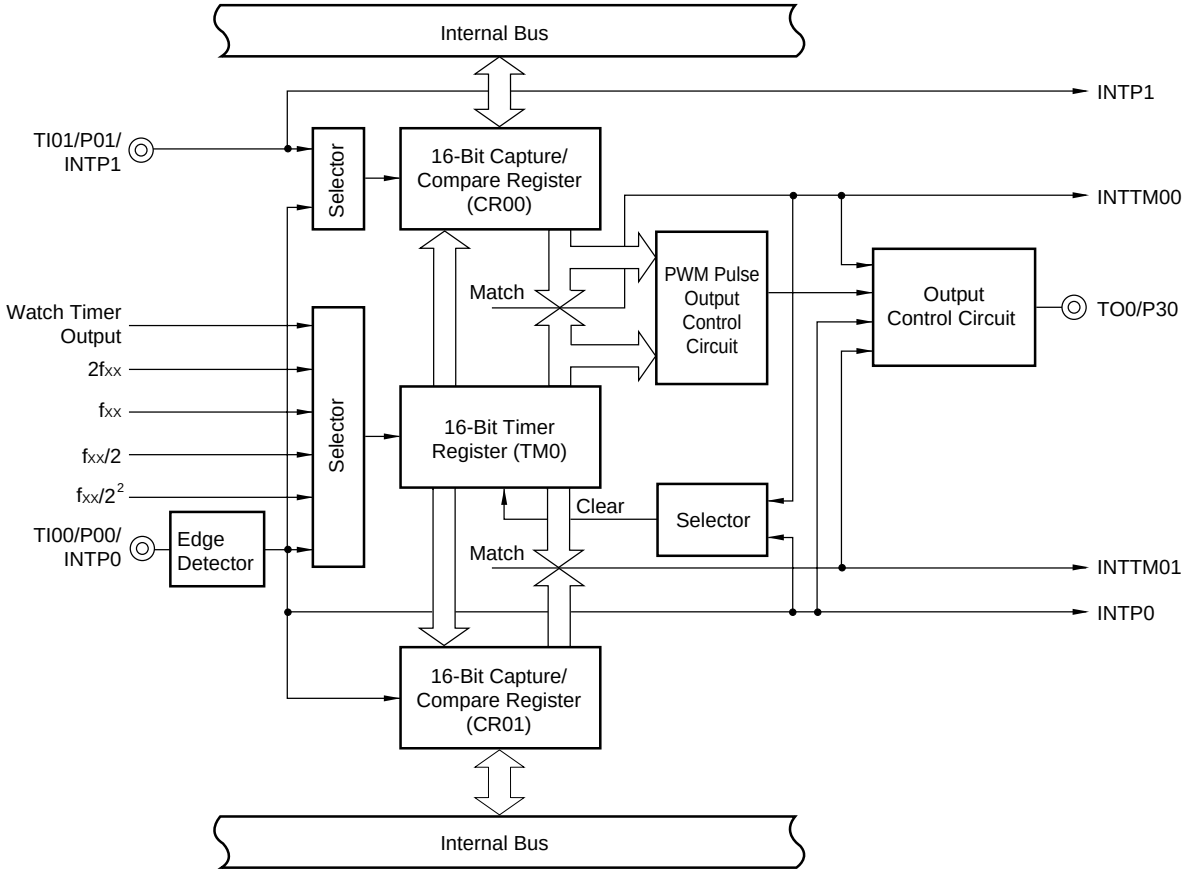


Figure 5-3. 8-Bit Timer/Event Counter Block Diagram

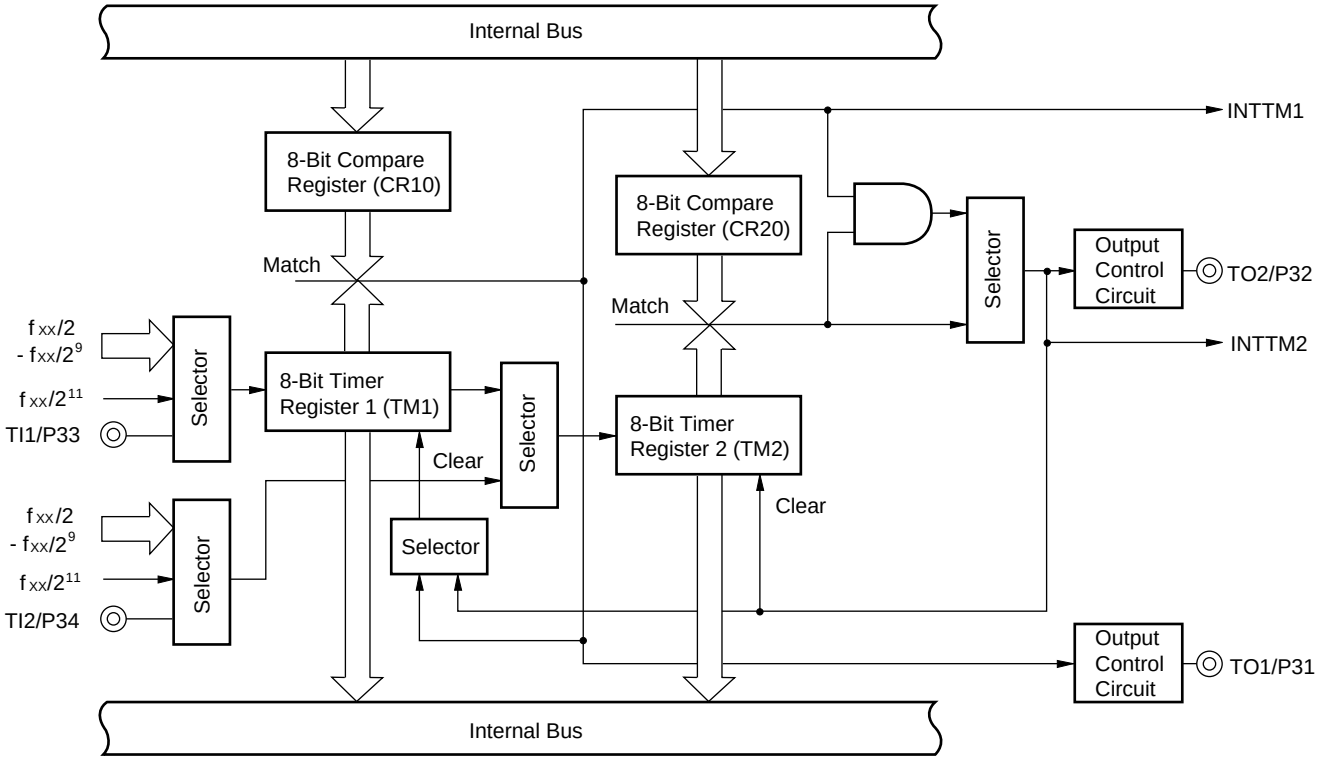


Figure 5-4. Watch Timer Block Diagram

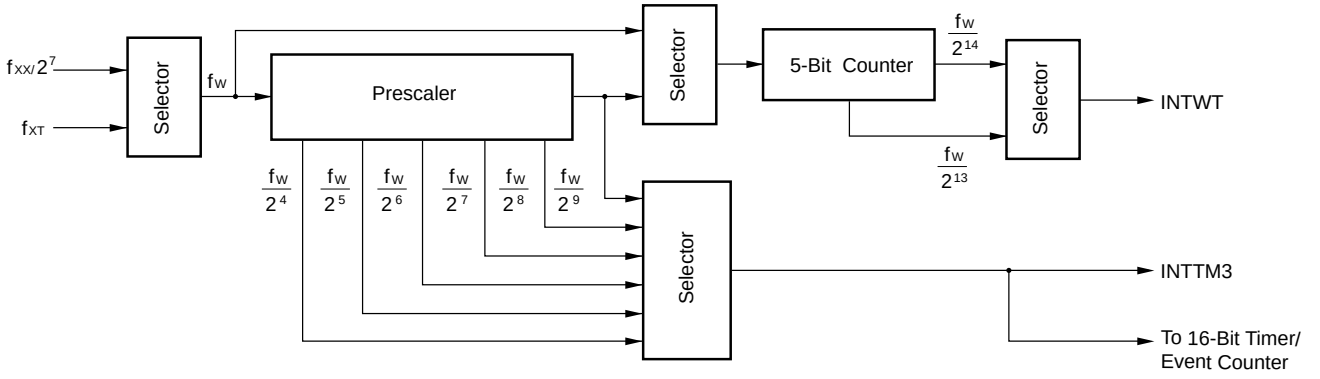
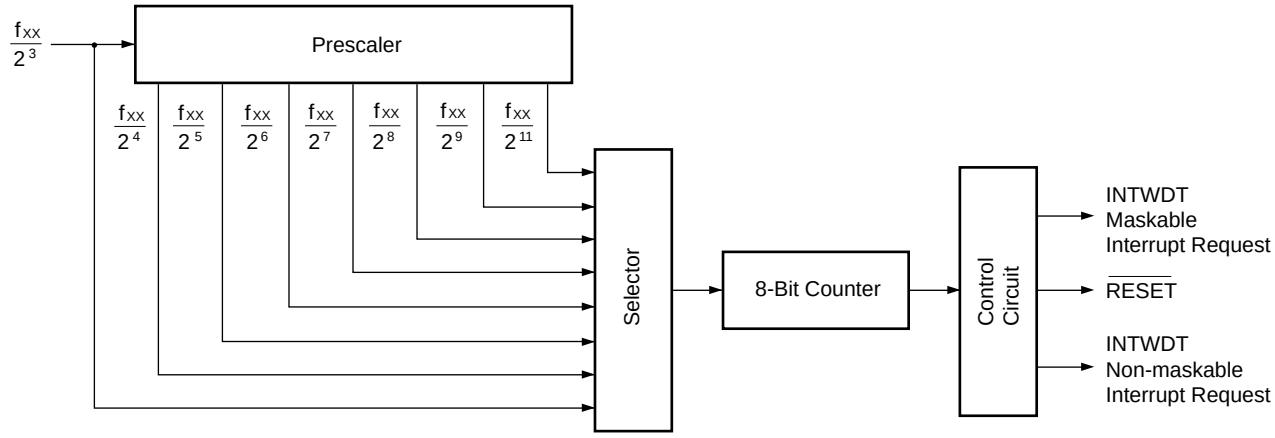


Figure 5-5. Watchdog Timer Block Diagram

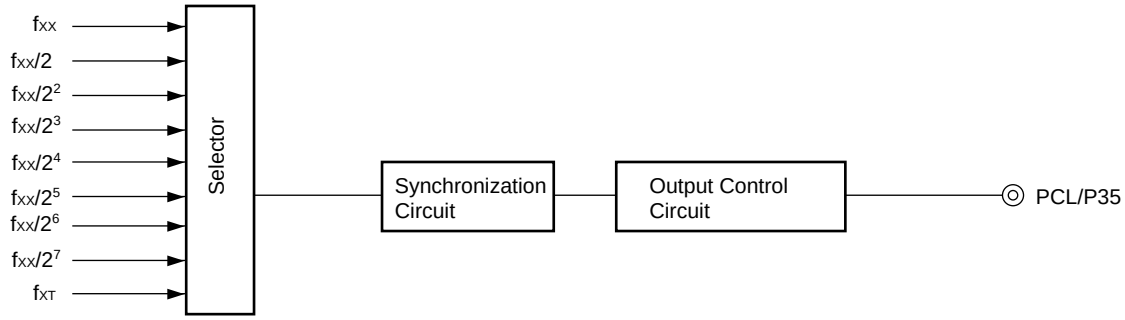


5.4 Clock Output Control Circuit

This circuit can output clocks of the following frequencies:

- 15.6 kHz/31.3 kHz/62.5 kHz/125 kHz/250 kHz/500 kHz/1.0 MHz/2.0 MHz/4.0 MHz (at main system clock frequency of f_{XX} = 6.0 MHz)
- 32.768 kHz (at subsystem clock frequency of f_{XT} = 32.768 kHz)

Figure 5-6. Clock Output Control Circuit Block Diagram

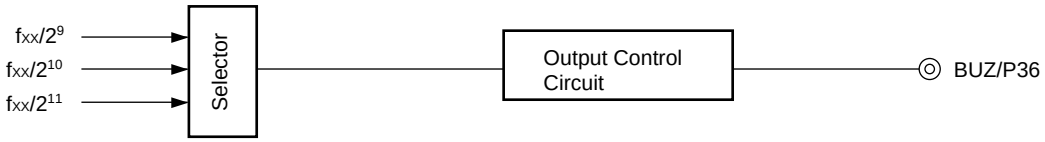


5.5 Buzzer Output Control Circuit

This circuit can output clocks of the following frequencies that can be used for driving buzzers:

- 977 Hz/1.95 kHz/3.9 kHz/7.8 kHz (at main system clock frequency of f_{XX} = 6.0 MHz)

Figure 5-7. Buzzer Output Control Circuit Block Diagram



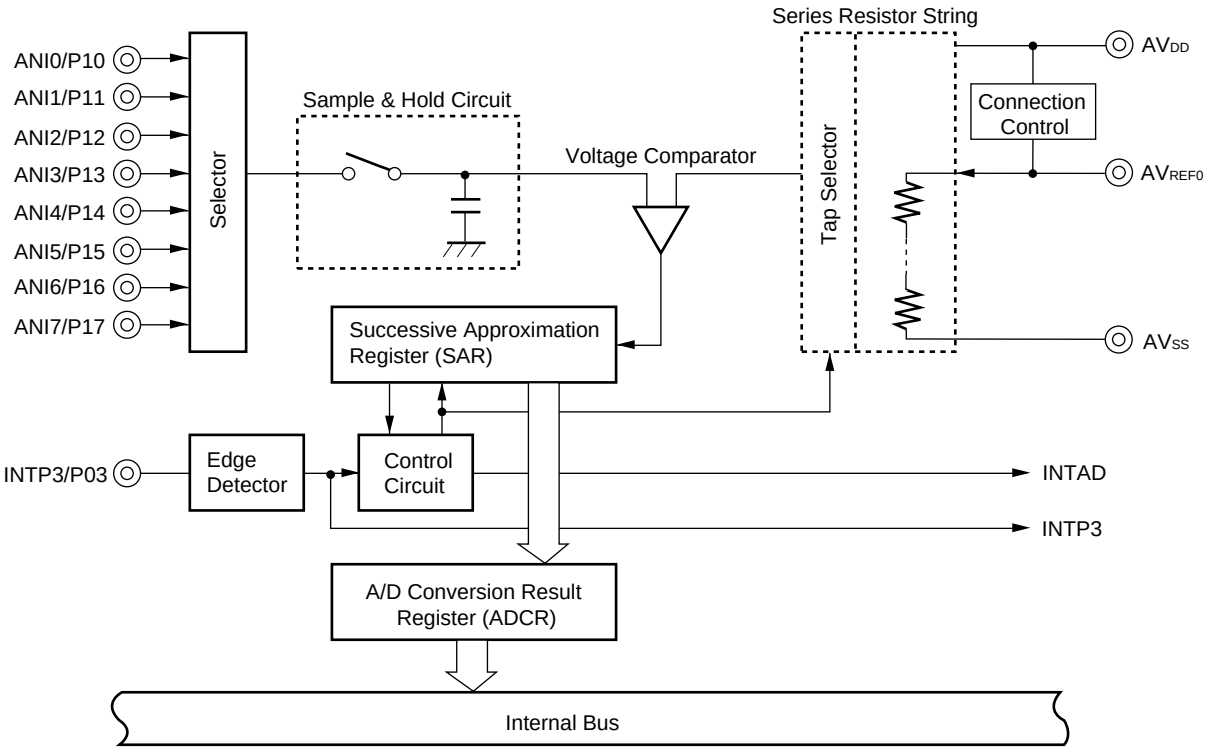
5.6 A/D Converter

The A/D converter consists of eight 8-bit resolution channels.

A/D conversion can be started by the following two methods:

- Hardware starting
- Software starting

Figure 5-8. A/D Converter Block Diagram

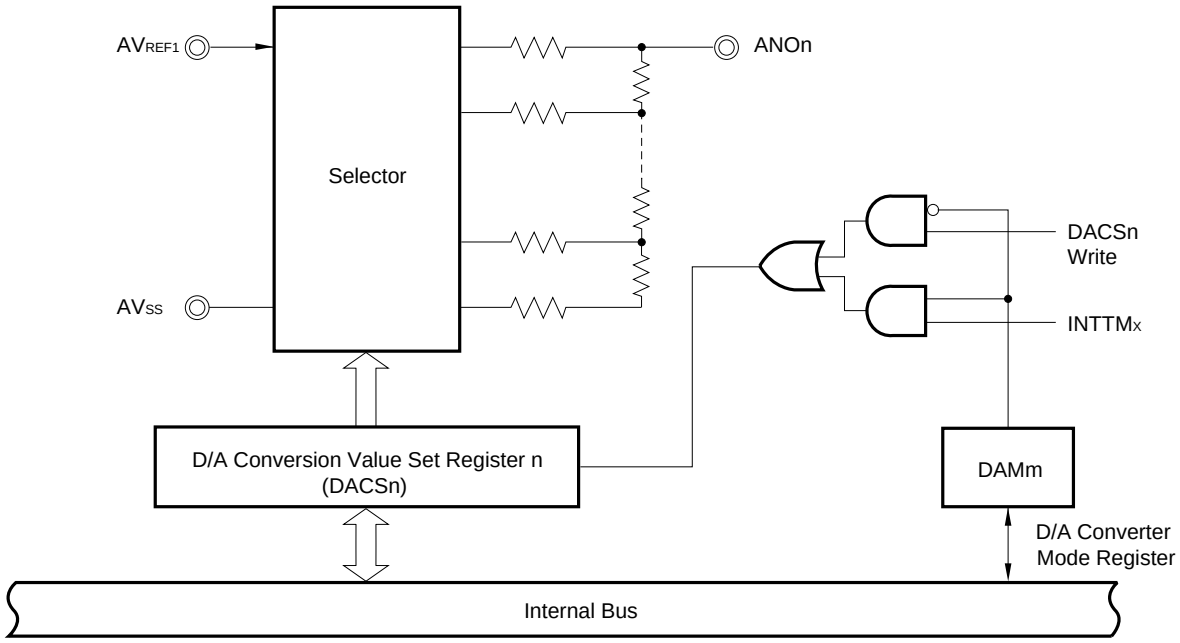


5.7 D/A Converter

The D/A converter consists of two 8-bit resolution channels.

The conversion method is the R-2R resistor ladder method.

Figure 5-9. D/A Converter Block Diagram



n = 0, 1

m = 4, 5

x = 1, 2

5.8 Serial Interfaces

There are the following three on-chip serial interface channels synchronous with the clock:

- Serial interface channel 0
- Serial interface channel 1
- Serial interface channel 2

Table 5-3. Types and Functions of Serial Interfaces

Function	Serial Interface Channel 0	Serial Interface Channel 1	Serial Interface Channel 2
3-wire serial I/O mode	○ (MSB/LSB first switching possible)	○ (MSB/LSB first switching possible)	○ (MSB/LSB first switching possible)
3-wire serial I/O mode with automatic data transmit/receive function	—	○ (MSB/LSB first switching possible)	—
2-wire serial I/O mode	○ (MSB first)	—	—
SBI (Serial bus interface) mode	○ (MSB first)	—	—
Asynchronous serial interface (UART) mode	—	—	○ (On-chip dedicated baud rate generator)

Figure 5-10. Serial Interface Channel 0 Block Diagram

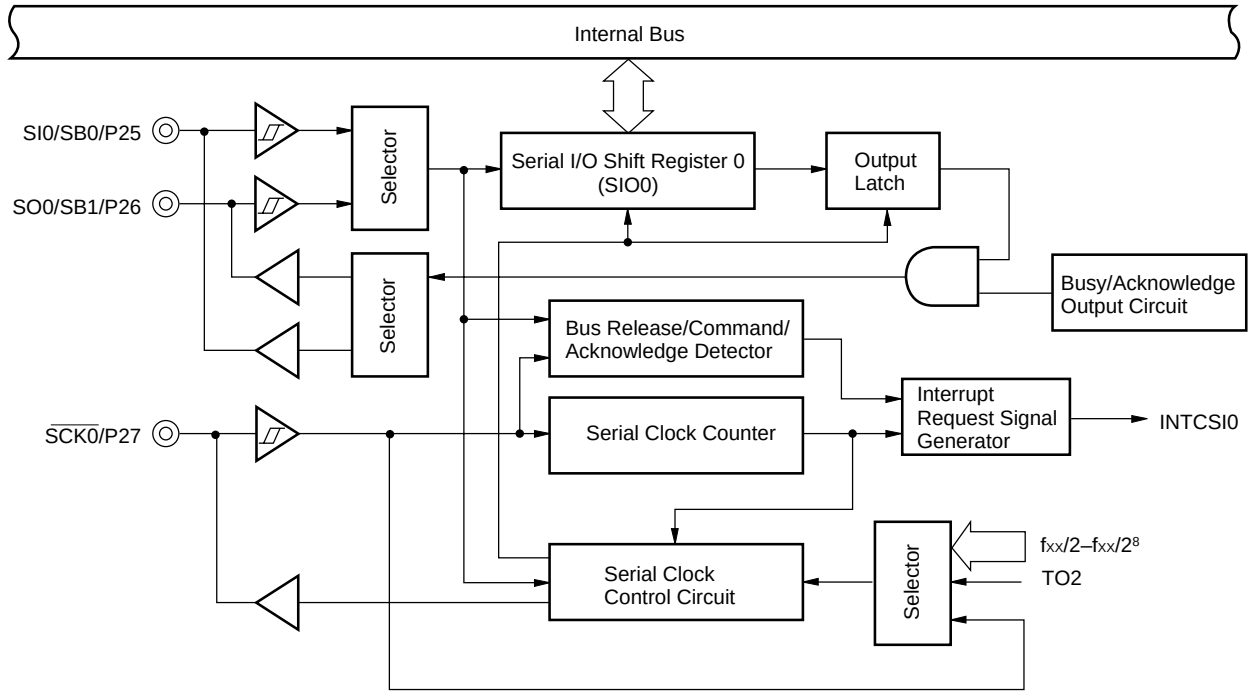


Figure 5-11. Serial Interface Channel 1 Block Diagram

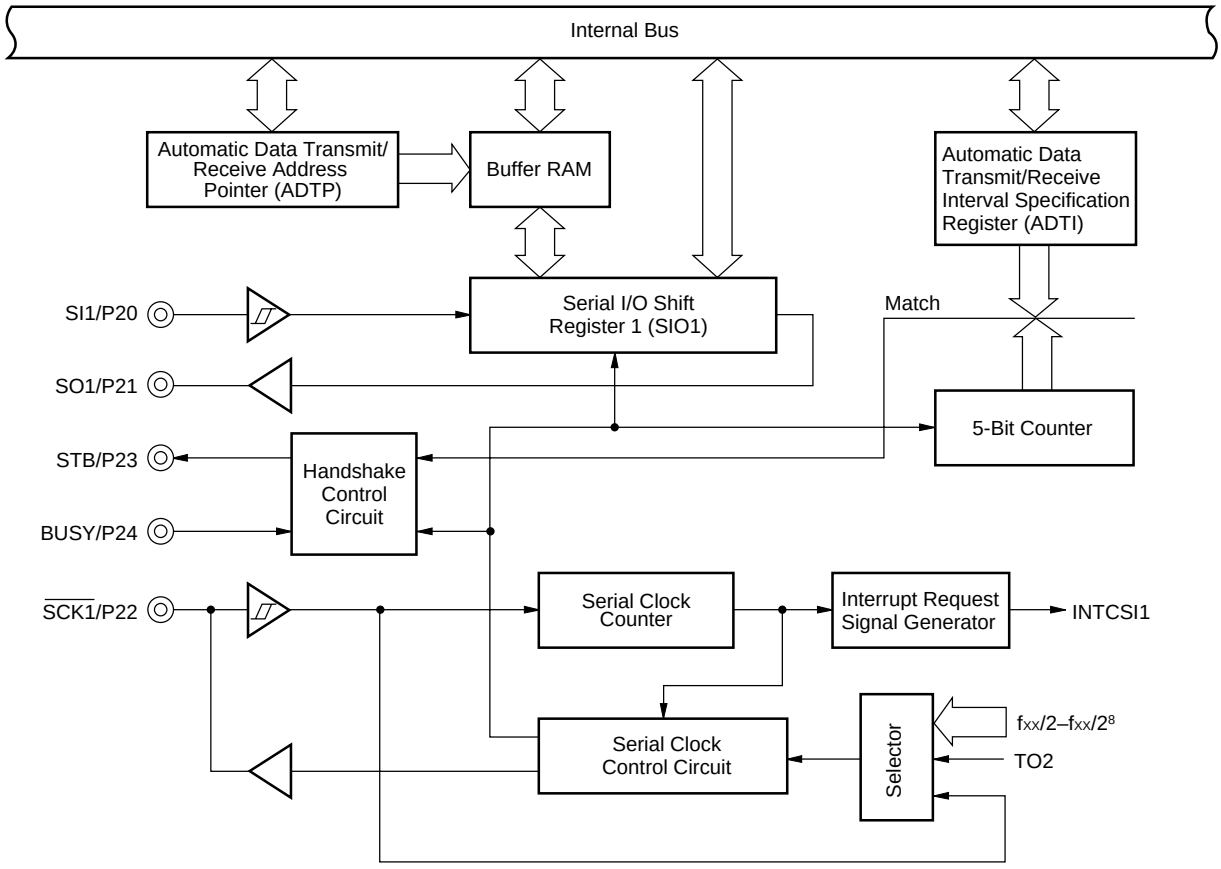
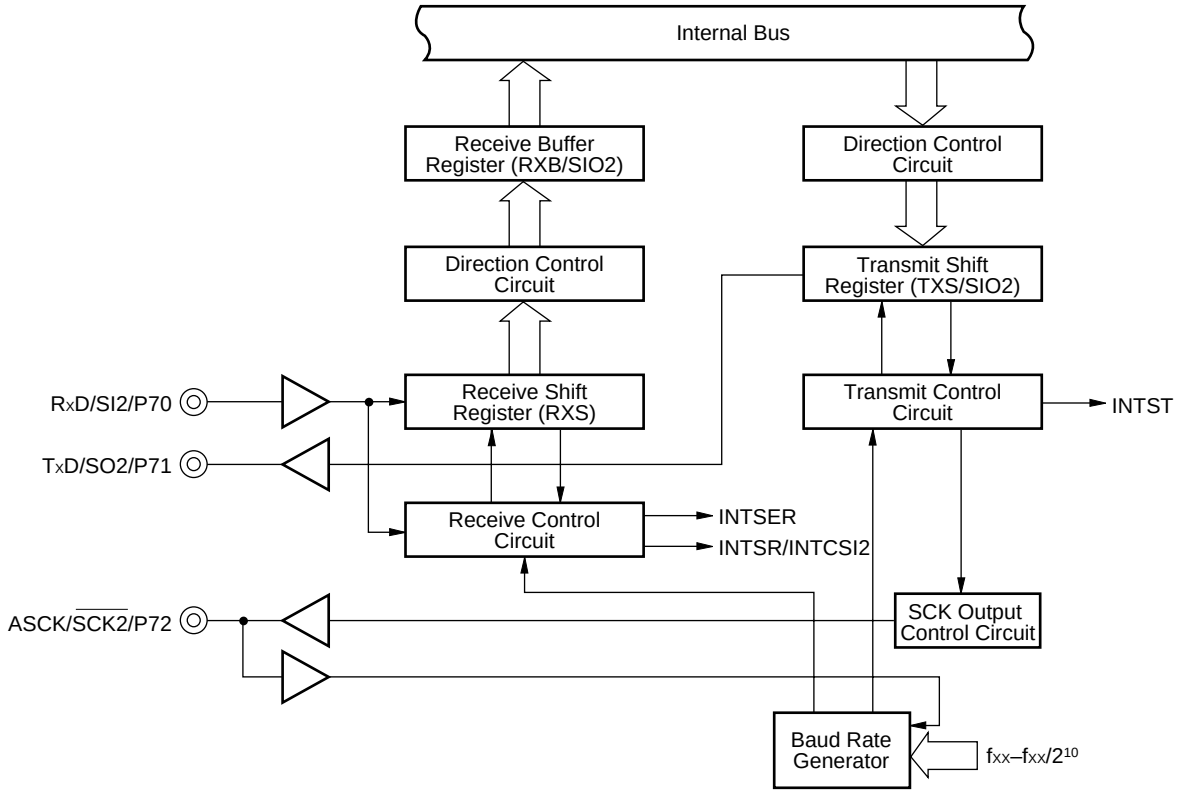


Figure 5-12. Serial Interface Channel 2 Block Diagram

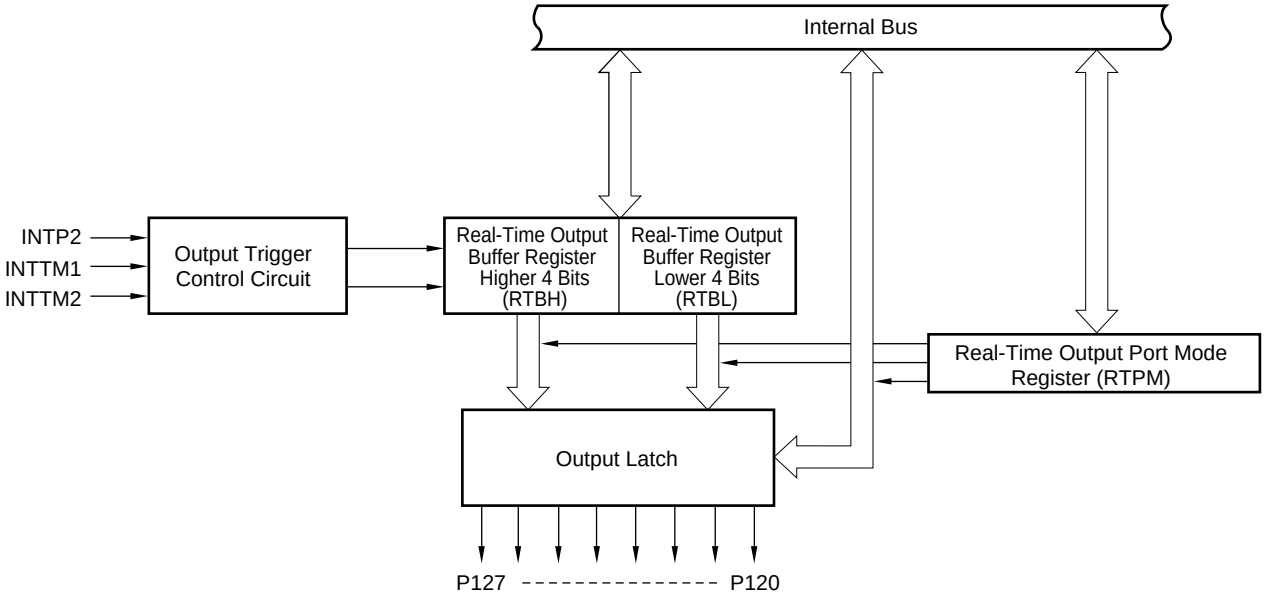


5.9 Real-Time Output Port

Data set previously in the real-time output buffer is transferred to the output latch by hardware concurrently with timer interrupt or external interrupt generation in order to output to off-chip. This is a real-time output function. Pins used to output to off-chip are called real-time output ports.

By using a real-time output port, a signal which has no jitter can be output. This is most applicable to control of stepping motors, etc.

Figure 5-13. Real-Time Output Port Block Diagram



5.10 IEBus Controller

IEBus (Inter Equipment Bus™) is a small-scale digital data transmission system for transmitting data between units. When configuring the IEBus with the μPD78098 subseries, the IEBus driver/receiver need to be connected externally as they are not incorporated.

Using the IEBus controller incorporated in the μPD78098 subseries, positive logic/negative logic can be selected by software for the externally connected IEBus driver/receiver.

6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

6.1 Interrupt Functions

A total of 23 interrupt functions are provided, divided into the following three types.

- Non-maskable interrupt : 1
- Maskable interrupts : 21
- Software interrupt : 1

Table 6-1. List of Interrupt Factors

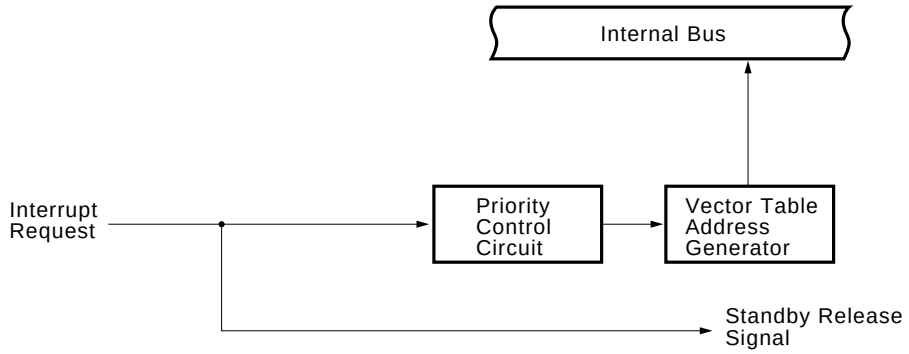
Interrupt Type	Default[Note1] Priority	Interrupt Factor		Internal/ External	Vector Table Address	Basic[Note2] Structure Type
		Name	Trigger			
Non-maskable	—	INTWDT	Overflow of watchdog timer (When the watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Overflow of watchdog timer (When the interval timer mode is selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	(D)
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTP4			000EH	
	6	INTP5			0010H	
	7	INTP6			0012H	
	8	INTCSI0	Completion of serial interface channel 0 transfer	Internal	0014H	(B)
	9	INTCSI1	Completion of serial interface channel 1 transfer		0016H	
	10	INTSER	Occurrence of serial interface channel 2 UART reception error		0018H	
	11	INTSR	Completion of serial interface channel 2 UART reception		001AH	
		INTCSI2	Completion of serial interface channel 2 3-wire transfer			
	12	INTST	Completion of serial interface channel 2 UART transmission		001CH	
	13	INTTM3	Reference interval signal from watch timer		001EH	
	14	INTTM00	Generation of matching signal of 16-bit timer register and capture/compare register (CR00)		0020H	
	15	INTTM01	Generation of matching signal of 16-bit timer register and capture/compare register (CR01)		0022H	
	16	INTTM1	Generation of matching signal of 8-bit timer/event counter 1		0024H	
	17	INTTM2	Generation of matching signal of 8-bit timer/event counter 2		0026H	
	18	INTAD	Completion of A/D conversion		0028H	
	19	INTIE	Writing data from the IEBus controller to the return code register (RCR) (including the same value) or detecting an IEBus interface runaway.		002AH	
Software	—	BRK	Execution of BRK instruction	Internal	003EH	(E)

Notes 1. Default priority is the priority order when several maskable interrupts are generated at the same time. 0 is the highest order and 19 is the lowest order.

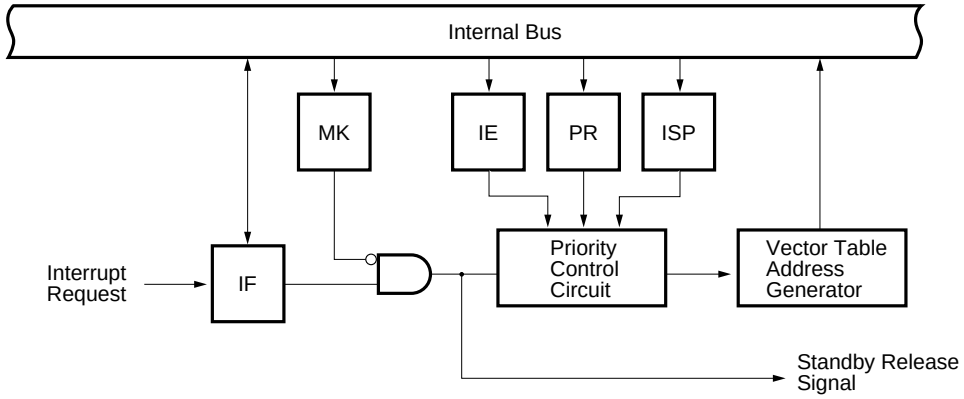
2. Basic structure types (A) to (E) correspond to (A) to (E) in Figure 6-1.

Figure 6-1. Interrupt Function Basic Configuration (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0)

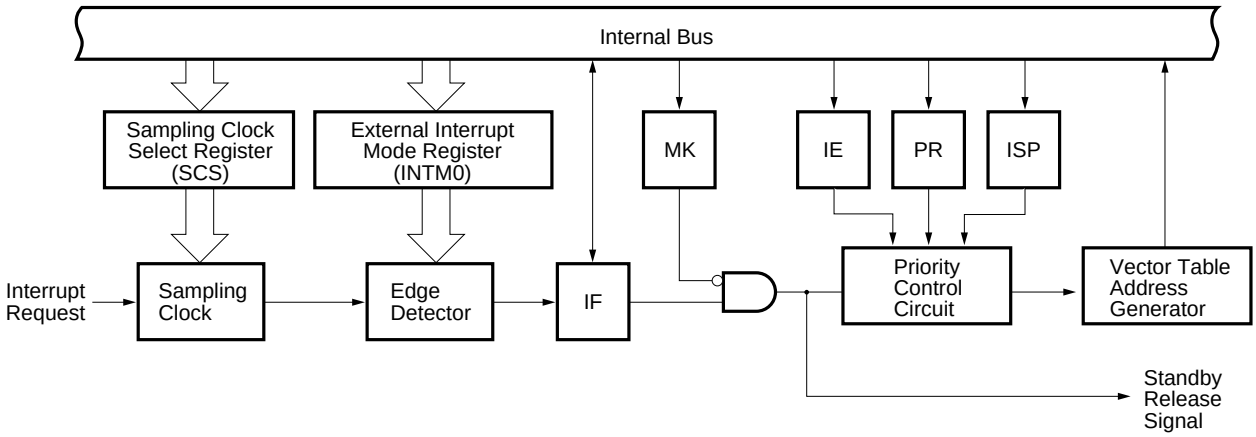
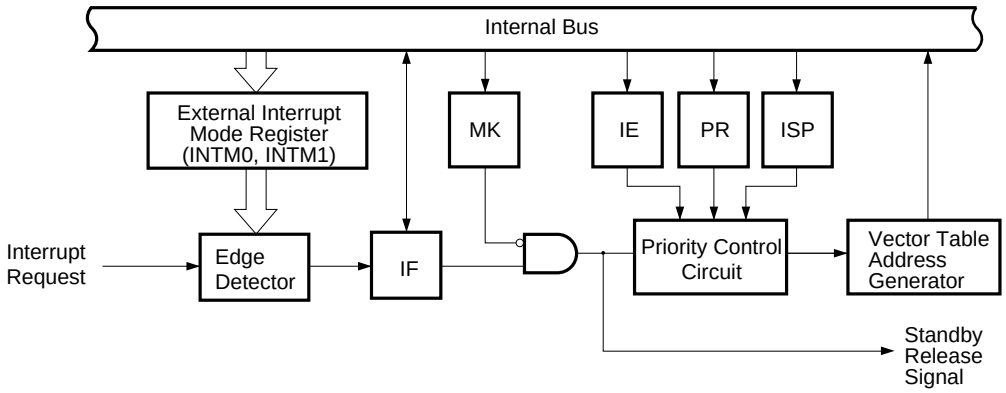
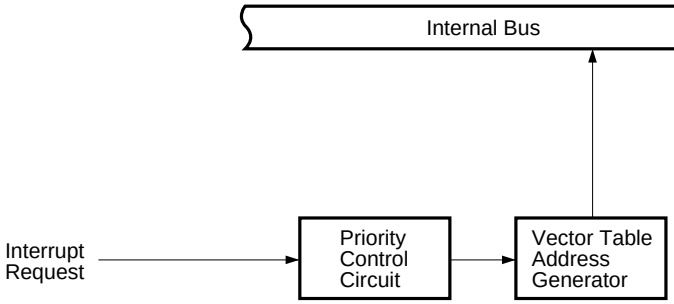


Figure 6-1. Interrupt Function Basic Configuration (2/2)

(D) External maskable interrupt (except INTP0)



(E) Software interrupt



IF : Interrupt request flag
IE : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority specification flag

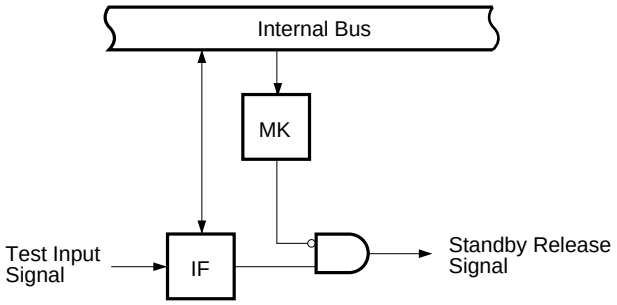
6.2 Test Functions

Table 6-2 shows the two test functions available.

Table 6-2. Test Input Factors

Test Input Factor		Internal/
Name	Trigger	External
INTWT	Overflow of watch timer	Internal
INTPT4	Detection of falling edge of port 4	External

Figure 6-2. Basic Configuration of Test Function



IF : Test input flag
MK : Test mask flag

7. EXTERNAL DEVICE EXPANSION FUNCTIONS

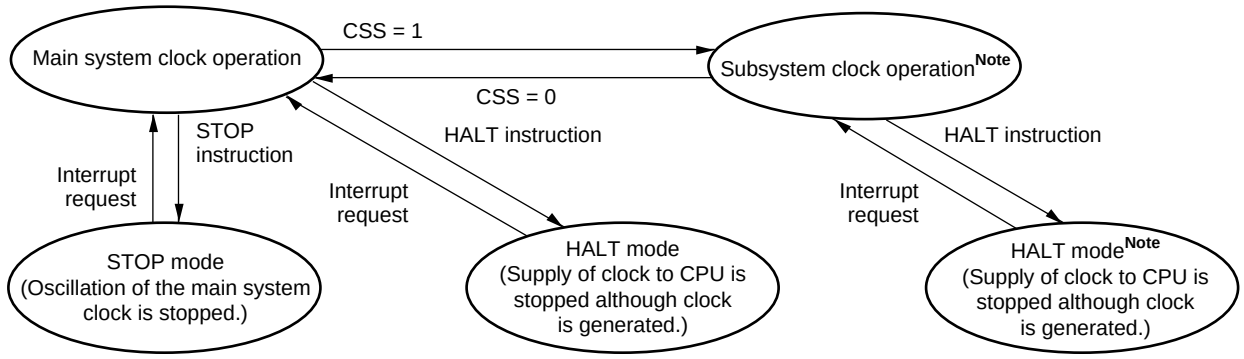
The external device expansion functions connect external devices to areas other than the internal ROM, RAM, and SFR. External devices connection uses ports 4 to 6.

8. STANDBY FUNCTION

The standby function is designed to reduce current consumption.
It has the following two modes:

- HALT mode : In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- STOP mode : In this mode, oscillation of the main system clock is stopped. All the operations performed on the main system clock are suspended, and only the subsystem clock is used for extremely small power consumption.

Figure 8-1. Standby Function



Note Current consumption is reduced by shutting off the main system clock. If the CPU is operating on the subsystem clock, shut off the main system clock by setting MCC. You cannot use a STOP instruction.

Caution When switching on the main system clock again after the subsystem clock has been used with the main system clock stopped, be sure to provide enough time for the generation to be stable with the program first.

9. RESET FUNCTION

There are the following two reset methods.

- External reset input by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer runaway time detection

10. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

2nd Operand / 1st Operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
r1											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

1st Operand \ 2nd Operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

1st Operand \ 2nd Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instruction/Branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

2nd Operand / 1st Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC, BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

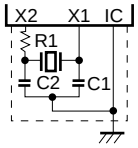
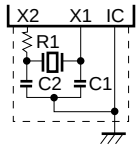
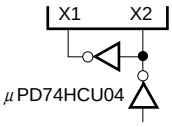
Parameter	Symbol	Test Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{REF0}			–0.3 to V_{DD} + 0.3	V
	AV_{REF1}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67, P70-P72, P120-P127, P130, P131, X1, X2, XT2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P60-P63	N-ch open-drain	–0.3 to +16	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10-P17	Analog input pins	AV_{SS} – 0.3 to AV_{REF0} + 0.3	V
Output current, high	I_{OH}	Per pin		–10	mA
		Total for P01-P06, P30-P37, P56, P57, P60-P67, P120-P127		–15	mA
		Total for P10-P17, P20-P27, P40-P47, P50-P55, P70-P72, P130, P131		–15	mA
Output current, low	I_{OL} Note	Per pin	Peak value	30	mA
			r.m.s. value	15	mA
		Total for P50-P55	Peak value	100	mA
			r.m.s. value	70	mA
		Total for P56, P57, P60-P63	Peak value	100	mA
			r.m.s. value	70	mA
		Total for P10-P17, P20-P27, P40-P47, P70-P72, P130, P131	Peak value	50	mA
			r.m.s. value	20	mA
		Total for P01-P06, P30-P37, P64-P67, P120-P127	Peak value	50	mA
			r.m.s. value	20	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C
Power dissipation	P_d			650	mW

Note The r.m.s. value should be calculated as follows: [r.m.s. value] = [Peak value] x $\sqrt{\text{Duty}}$

Caution Exposure to Absolute Maximum Ratings for extended periods may affect device reliablity; exceeding the ratings could cause permanent damege. The parameters apply independently.

Remark Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

Main System Clock Oscillator Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X) Note 1	V_{DD} = Oscillation voltage range	1.0	6.0	6.29	MHz
		Oscillation stabilization time Note 2	After V_{DD} came to MIN. of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X) Note 1		1.0	6.0	6.29	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X) Note 1		1.0	6.0	6.29	MHz
		X1 input high- and low-level widths (t_{XH}, t_{XL})	Using at $f_{XX} = f_X$	85		500	ns
			Other than above	72		500	

Notes 1. Only the oscillator characteristics are shown. For instruction execution time, refer to AC Characteristics.

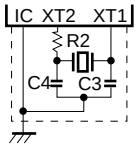
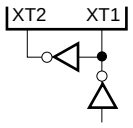
2. Time required for oscillation to stabilize after a reset or the STOP mode has been released.

Cautions 1. When using the main system clock oscillator, wire the portion enclosed in dotted line in the figures as follows to avoid adverse influences on the wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring over other signal lines.**
- **Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.**
- **Always keep the ground point of the capacitor of the oscillator circuit at the same potential as V_{DD}.**
- **Do not connect the power source pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

2. When switching on the main system clock again after the subsystem clock has been used with the main system clock stopped, be sure to provide enough time for the generation to be stable with the program first.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_X) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT}) Note 1		32		100	kHz
		XT1 input high-, low-level widths (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Only the oscillator characteristics are shown. For instruction execution time, refer to AC Characteristics.

2. Time required for oscillation to stabilize after power (V_{DD}) is turned on.

Cautions 1. When using the subsystem clock oscillator, wire the portion enclosed in dotted line in the figures as follows to avoid adverse influences on the wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring over other signal lines.**
- **Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.**
- **Always keep the ground point of the capacitor of the oscillator circuit at the same potential as V_{DD}.**
- **Do not connect the power source pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

2. The amplification factor of the subsystem clock oscillator circuit is designed to be low to reduce the current consumption and therefore, the subsystem clock circuit is influenced by noise more easily than the main system clock oscillator. When using the subsystem clock, therefore, exercise utmost care in wiring the circuit.

Capacitance (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V.	P01-P06, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67, P70-P72, P120-P127, P130, P131			15	pF
			P60-P63			20	pF

Remark Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10-P17, P21, P23, P30-P32, P35-P37, P40-P47, P50-P57, P64-P67, P71, P120-P127, P130, P131		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00-P06, P20, P22, P24-P27, P130, P131 $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	P60-P63	N-ch open-drain	0.7V_{DD}		15	V
	V_{IH4}	X1, X2		V_{DD} – 0.5		V_{DD}	V
	V_{IH5}	XT1/P07, XT2	4.5 ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			2.7 ≤ V_{DD} ≤ 4.5 V	0.9V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10-P17, P21, P23,P30-P32, P35-P37, P40-P47 P50-P57, P64-P67, P71, P120-P127, P130, P131		0		0.3V_{DD}	V
	V_{IL2}	P00-P06, P20, P22, P24-P27, P33, P34, P70, P72 $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL3}	P60-P63 (N-ch open drain)	4.5 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			2.7 V ≤ V_{DD} ≤ 4.5 V	0		0.2V_{DD}	V
	V_{IL4}	X1, X2		0		0.4	V
	V_{IL5}	XT1/P07, XT2	V_{DD} = 4.5 to 5.5 V	0		0.2V_{DD}	V
				0		0.1V_{DD}	V
Output voltage, high	V_{OH1}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P50-P57, P60-P63	V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA		0.4	2.0	V
		P01-P06, P10-P17, P20-P27, P30-P37, P40-P47, P64-P67, P70-P72, P120-P127, P130, P131	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 5.5 V, open-drain pulled high (R = 1 kΩ)			0.2V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V

Remark Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00-P06, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P72, P120-P127, P130, P131, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1/P07, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P60-P63			80	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00-P06, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67, P70-P72, P120-P127, P130, P131, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2, XT1/P07, XT2			–20	μA
	I_{LIL3}		P60-P63			–3[Note]	μA
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Mask option pull-up resistor	R_1	V_{IN} = 0 V, P60-P63		20	40	90	kΩ
Software pull-up resistor	R_2	V_{IN} = 0 V, P01-P06, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67, P70-P72, P120-P127, P130, P131	4.5 V ≤ V_{DD} ≤ 5.5 V	15	40	90	kΩ
			2.7 V ≤ V_{DD} ≤ 4.5 V	20		500	kΩ

Note When no pull-up resistor is incorporated to P60-63 (to be specified by mask option), the value is –200 μA in either of the following cases.

(1) When external device expansion function is used and low-level is input to P60 to P63 pins.

(2) During the 1.5 clocks when read out instruction is executed to port 6 (P6) and port mode register 6 (PM6).

Remark Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	5.0-MHz crystal oscillation operating mode (f_{XX} = 2.5 MHz) Note 2	V_{DD} = 5.0 V ± 10% Note 6		4	15	mA
			V_{DD} = 3.0 V ± 10% Note 7		0.6	2.4	mA
		5.0-MHz crystal oscillation operating mode (f_{XX} = 5.0 MHz) Note 3	V_{DD} = 5.0 V ± 10% Note 6		6.5	22.5	mA
			V_{DD} = 3.0 V ± 10% Note 7		0.8	3.1	mA
		6.29-MHz crystal oscillation operating mode (f_{XX} = 2.1 MHz) Note 4	V_{DD} = 5.0 V ± 10% Note 6		3.8	14.5	mA
		6.29-MHz crystal oscillation operating mode (f_{XX} = 4.19 MHz) Note 5	V_{DD} = 5.0 V ± 10% Note 6		6	21	mA

Notes 1. Not including AV_{REF0}, AV_{REF1}, AV_{DD} currents and port currents (including current flowing into on-chip pull-up resistors).

2. When bit 0 of the clock switch selection register 1 is set to 0, bit 0 of the clock switch selection register 2 is set to 0, and oscillation mode selection register is set to 00H.

3. When bit 0 of the clock switch selection register 1 is set to 0, bit 0 of the clock switch selection register 2 is set to 0, and oscillation mode selection register is set to 01H.

4. When bit 0 of the clock switch selection register 1 is set to 1, bit 0 of the clock switch selection register 2 is set to 0, and oscillation mode selection register is set to 00H.
Only the characteristics of the supply current are shown. For the IEBus standards, refer to IEBus controller characteristics.

5. When bit 0 of the clock switch selection register 1 is set to 1, bit 0 of the clock switch selection register 2 is set to 0, and oscillation mode selection register is set to 01H.
Only the characteristics of the supply current are shown. For the IEBus standards, refer to IEBus controller characteristics.

6. High-speed mode operation (when processor clock control register is set to 00H).

7. Low-speed mode operation (when processor clock control register is set to 04H).

Remark f_{XX}: Main system clock frequency.

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2}	5.0-MHz crystal oscillation HALT mode (f_{XX} = 2.5 MHz) Note 2	V_{DD} = 5.0 V ± 10% Note 7		1.5	4.5	mA
			V_{DD} = 3.0 V ± 10% Note 8		0.5	1.5	mA
		5.0-MHz crystal oscillation HALT mode (f_{XX} = 5.0 MHz) Note 3	V_{DD} = 5.0 V ± 10% Note 7		1.8	5.4	mA
			V_{DD} = 3.0 V ± 10% Note 8		0.7	2.1	mA
		6.29-MHz crystal oscillation HALT mode (f_{XX} = 2.1 MHz) Note 4	V_{DD} = 5.0 V ± 10% Note 7		1.5	4.5	mA
		6.29-MHz crystal oscillation HALT mode (f_{XX} = 4.19 MHz) Note 5	V_{DD} = 5.0 V ± 10% Note 7		1.8	5.4	mA
	I_{DD3}	32.768-kHz crystal oscillation operating mode Note 6	V_{DD} = 5.0 V ± 10%		60	120	μA
			V_{DD} = 3.0 V ± 10%		32	64	μA
	I_{DD4}	32.768-kHz crystal oscillation HALT mode Note 6	V_{DD} = 5.0 V ± 10%		25	55	μA
			V_{DD} = 3.0 V ± 10%		5	15	μA
	I_{DD5}	XT1 = 0 V STOP mode, feedback resistor used	V_{DD} = 5.0 V ± 10%		1	30	μA
			V_{DD} = 3.0 V ± 10%		0.5	10	μA
	I_{DD6}	XT1 = 0 V STOP mode, feedback resistor not used	V_{DD} = 5.0 V ± 10%		0.1	30	μA
			V_{DD} = 3.0 V ± 10%		0.05	10	μA

Notes 1. Not including AV_{REF0}, AV_{REF1}, AV_{DD} currents and port currents (including current flowing into internal pull-up resistors).

2. When bit 0 of the clock switch selection register 1 is set to 0, bit 0 of the clock switch selection register 2 is set to 0, and oscillation mode selection register is set to 00H.

3. When bit 0 of the clock switch selection register 1 is set to 0, bit 0 of the clock switch selection register 2 is set to 0, and oscillation mode selection register is set to 01H.

4. When bit 0 of the clock switch selection register 1 is set to 1, bit 0 of the clock switch selection register 2 is set to 0, and oscillation mode selection register is set to 00H.
Only the characteristics of the supply current are shown. For the IEBus standards, refer to IEBus controller characteristics.

5. When bit 0 of the clock switch selection register 1 is set to 1, bit 0 of the clock switch selection register 2 is set to 0, and oscillation mode selection register is set to 01H.
Only the characteristics of the supply current are shown. For the IEBus standards, refer to IEBus controller characteristics.

6. When the main system clcok is stopped.

7. High-speed mode operation (when processor clock control register is set to 00H).

8. Low-speed mode operation (when processor clock control register is set to 04H).

Remark f_{XX}: Main system clock frequency.

AC Characteristics

(1) Basic Operation (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions			MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operating on main system clock (MCS = 0) Note1	$f_{XX} = f_X/3$	$4.0 \le V_{DD} \le 5.5$ V	0.95		64	μs
			$f_{XX} = f_X/6$	$2.7 \le V_{DD} \le 5.5$ V	1.91		64	μs
			$f_{XX} = f_X/9$	$4.0 \le V_{DD} \le 5.5$ V	2.86		64	μs
			$f_{XX} = f_X/2$	$2.7 \le V_{DD} \le 5.5$ V	0.8		64	μs
		Operating on main system clock (MCS = 1) Note2	$f_{XX} = 2f_X/3$	$4.5 \le V_{DD} \le 5.5$ V	0.48		32	μs
				$4.0 \le V_{DD} \le 4.5$ V	0.95		32	μs
			$f_{XX} = f_X/3$	$2.7 \le V_{DD} \le 5.5$ V	0.95		32	μs
			$f_{XX} = 2f_X/9$	$4.0 \le V_{DD} \le 5.5$ V	1.43		32	μs
			$f_{XX} = f_X$	$4.5 \le V_{DD} \le 5.5$ V	0.4		32	μs
				$2.7 \le V_{DD} \le 4.5$ V	0.8		32	μs
		Operating on subsystem clock			114	122	125	μs
TI input frequency	f_{TI}	TI1, TI2	V_{DD} = 4.5 to 5.5 V		0		4	MHz
					0		275	kHz
		TI01			0		50	kHz
		TI00			0		$f_{sam}/16$ Note3	MHz
TI input high-, low-level widths	t_{TIH}, t_{TIL}	TI1, TI2	V_{DD} = 4.5 to 5.5 V		100			ns
					1.8			μs
		TI01			10			μs
		TI00			$8/f_{sam}$	Note3		μs
Interrupt input high-, low-level widths	t_{INTH}, t_{INTL}	INTP0			$8/f_{sam}$	Note3		μs
		INTP1-INTP6			10			μs
		KR0-KR7			10			μs
$\overline{\text{RESET}}$ low-level width	t_{RST}				10			μs

Notes 1. When oscillation mode selection register is set to 00H.

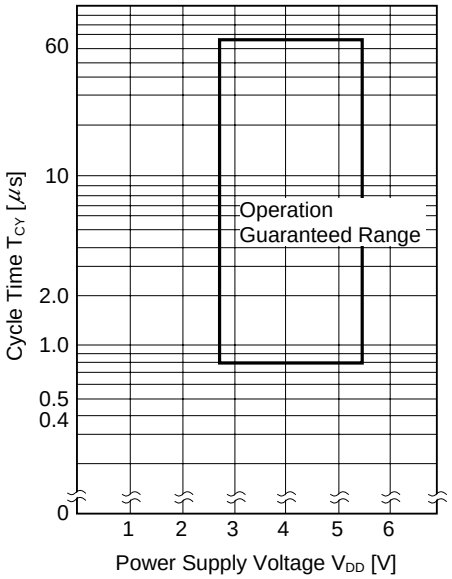
2. When oscillation mode selection register is set to 01H.

3. f_{sam} can be selected as $f_{XX}/2^N$, $f_{XX}/32$, $f_{XX}/64$, or $f_{XX}/128$ (N = 0 to 4) by bits 0 and 1 (SCS0, SCS1) of the sampling clock selection register.

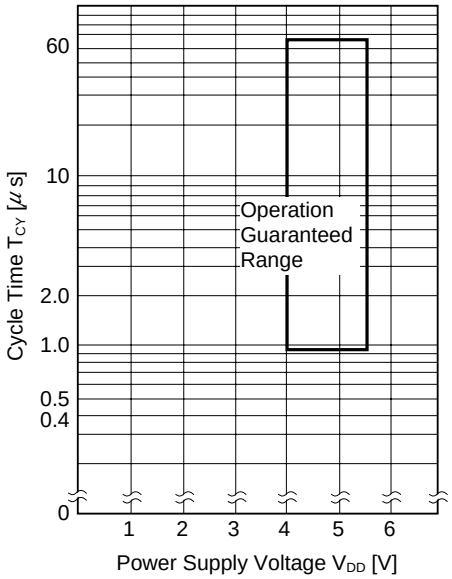
Remarks 1. f_{XX} : Main system clock frequency (fx or fx/2).

2. f_X : Main system clock oscillation frequency.

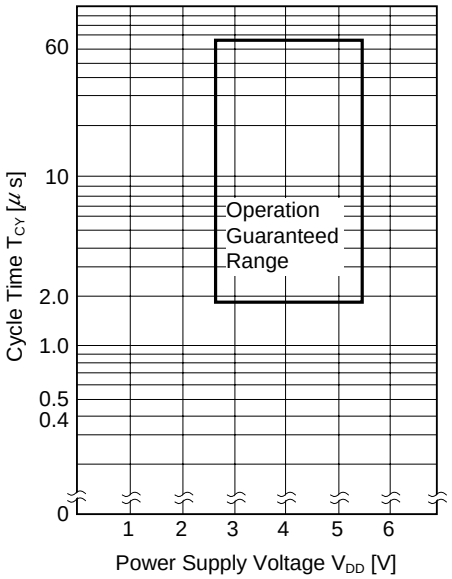
T_{CY} vs V_{DD} Main System Clock
(IECL10 = 0, IECL20 = 0, MCS = 0) operation



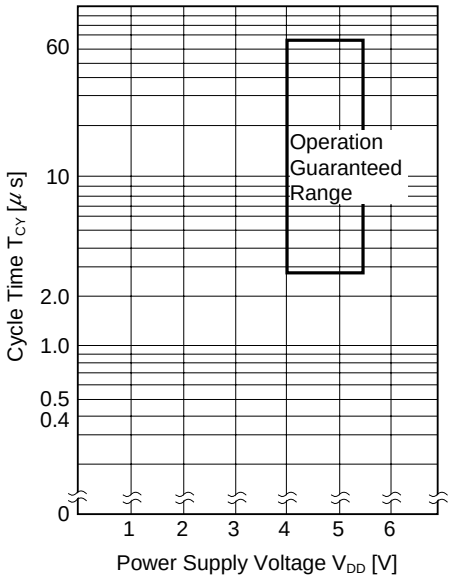
T_{CY} vs V_{DD} Main System Clock
(IECL10 = 1, IECL20 = 0, MCS = 0) operation



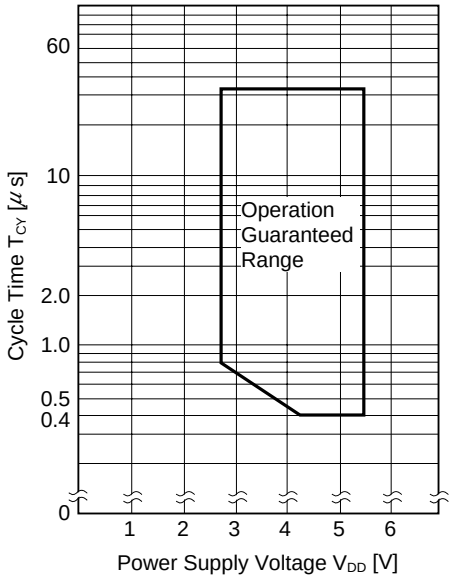
T_{CY} vs V_{DD} Main System Clock
(IECL10 = 0, IECL20 = 1, MCS = 0) operation



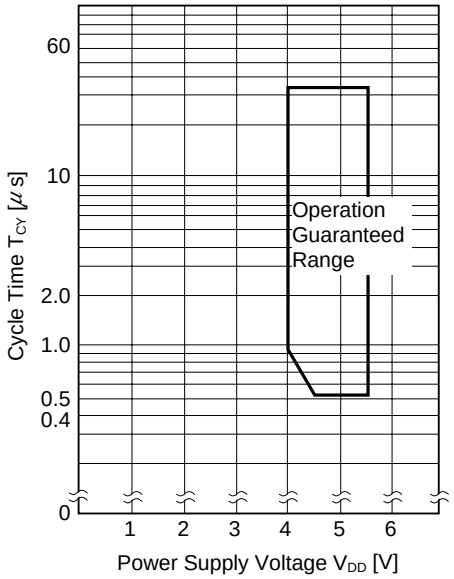
T_{CY} vs V_{DD} Main System Clock
(IECL10 = 1, IECL20 = 1, MCS = 0) operation



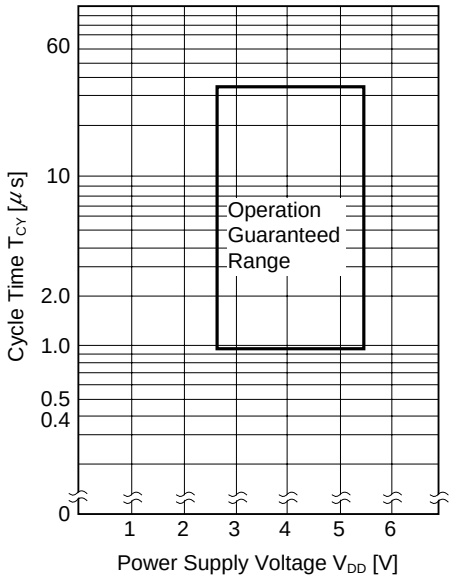
T_{CY} vs V_{DD} Main System Clock
(IECL10 = 0, IECL20 = 0, MCS = 1) operation



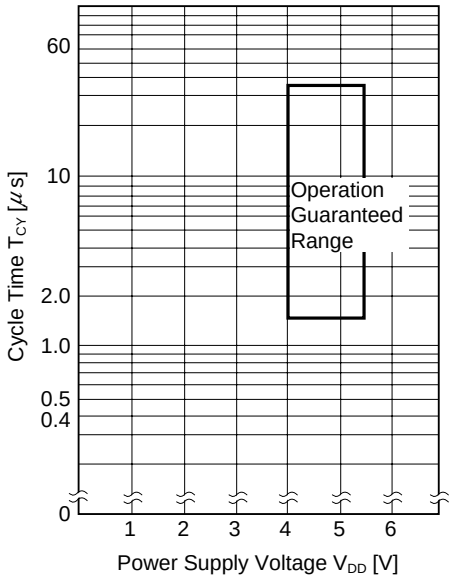
T_{CY} vs V_{DD} Main System Clock
(IECL10 = 1, IECL20 = 0, MCS = 1) operation



T_{CY} vs V_{DD} Main System Clock
(IECL10 = 0, IECL20 = 1, MCS = 1) operation



T_{CY} vs V_{DD} Main System Clock
(IECL10 = 1, IECL20 = 1, MCS = 1) operation



(2) Read/Write Operation

(a) **When MCS = 1, PCC2-PCC0 = 000B** (T_A = –40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.85t_{CY}$ – 50		ns
Address setup time	t_{ADS}		$0.85t_{CY}$ – 50		ns
Address hold time	t_{ADH}		50		ns
Address → data input time	t_{ADD1}			(2.85 + 2n) t_{CY} – 80	ns
	t_{ADD2}			(4 + 2n) t_{CY} – 100	ns
$\overline{RD}$ ↓ → data input time	t_{RDD1}			(2 + 2n) t_{CY} – 100	ns
	t_{RDD2}			(2.85 + 2n) t_{CY} – 100	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(2 + 2n) t_{CY} – 60		ns
	t_{RDL2}		(2.85 + 2n) t_{CY} – 60		ns
$\overline{RD}$ ↓ → $\overline{WAIT}$ ↓ input time	t_{RDWT1}			$0.85t_{CY}$ – 50	ns
	t_{RDWT2}			$2t_{CY}$ – 60	ns
$\overline{WR}$ ↓→ $\overline{WAIT}$ ↓ input time	t_{WRWT}			$2t_{CY}$ – 60	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1.15 + 2n) t_{CY}	(2 + 2n) t_{CY}	ns
Write data setup time	t_{WDS}		(2.85 + 2n) t_{CY} – 100		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL}		(2.85 + 2n) t_{CY} – 60		ns
ASTB ↓ → $\overline{RD}$ ↓ delay time	t_{ASTRD}		25		ns
ASTB ↓ → $\overline{WR}$ ↓ delay time	t_{ASTWR}		$0.85t_{CY}$ + 20		ns
In external fetch $\overline{RD}$ ↑ → ASTB ↑ delay time	t_{RDAST}		$0.85t_{CY}$ – 10	$1.15t_{CY}$ + 20	ns
In external fetch $\overline{RD}$ ↑ → address hold time	t_{RDADH}		$0.85t_{CY}$ – 50	$1.15t_{CY}$ + 50	ns
$\overline{RD}$ ↑ → write data output time	t_{RDWD}		40		ns
$\overline{WR}$ ↓ → write data output time	t_{WRWD}		0	50	ns
$\overline{WR}$ ↑ → address hold time	t_{WRADH}		$0.85t_{CY}$ + 40	$1.15t_{CY}$ + 40	ns
$\overline{WAIT}$ ↑ → RD ↑ delay time	t_{WTRD}		$1.15t_{CY}$ + 40	$3.15t_{CY}$ + 40	ns
$\overline{WAIT}$ ↑ → WR ↑ delay time	t_{WTWR}		$1.15t_{CY}$ + 30	$3.15t_{CY}$ + 30	ns

Remarks **1.** MCS: Bit 0 of the oscillation mode selection register.

2. PCC2-PCC0: Bit 2-bit 0 of the processor clock control register.

3. $t_{CY} = T_{CY}/4$.

4. n indicates the number of waits.

(b) **Except when MCS = 1, PCC2-PCC0 = 000B** (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		t_{CY} – 80		ns
Address setup time	t_{ADS}		t_{CY} – 80		ns
Address hold time	t_{ADH}		0.4t_{CY} – 10		ns
Address → data input time	t_{ADD1}			(3 + 2n) t_{CY} – 160	ns
	t_{ADD2}			(4 + 2n) t_{CY} – 200	ns
$\overline{RD}$ ↓ → data input time	t_{RDD1}			(1.4 + 2n) t_{CY} – 70	ns
	t_{RDD2}			(2.4 + 2n) t_{CY} – 70	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(1.4 + 2n) t_{CY} – 20		ns
	t_{RDL2}		(2.4 + 2n) t_{CY} – 20		ns
$\overline{RD}$ ↓ → $\overline{WAIT}$ ↓ input time	t_{RDWT1}			t_{CY} – 100	ns
	t_{RDWT2}			2t_{CY} – 100	ns
$\overline{WR}$ ↓→ $\overline{WAIT}$ ↓ input time	t_{WRWT}			2t_{CY} – 100	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1 + 2n) t_{CY}	(2 + 2n) t_{CY}	ns
Write data setup time	t_{WDS}		(2.4 + 2n) t_{CY} – 60		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL}		(2.4 + 2n) t_{CY} – 20		ns
ASTB ↓ → $\overline{RD}$ ↓ delay time	t_{ASTRD}		0.4t_{CY} – 30		ns
ASTB ↓ → $\overline{WR}$ ↓ delay time	t_{ASTWR}		1.4t_{CY} –30		ns
In external fetch $\overline{RD}$ ↑ → ASTB ↑delay time	t_{RDAST}		t_{CY} – 10	t_{CY} + 20	ns
In external fetch $\overline{RD}$ ↑ → address hold time	t_{RDADH}		t_{CY} – 50	t_{CY} + 50	ns
$\overline{RD}$ ↑ → write data output time	t_{RDWD}		0.4t_{CY} – 20		ns
$\overline{WR}$ ↓ → write data output time	t_{WRWD}		0	60	ns
$\overline{WR}$ ↑ → address hold time	t_{WRADH}		t_{CY}	t_{CY} + 60	ns
$\overline{WAIT}$ ↑ → $\overline{RD}$ ↑ delay time	t_{WTRD}		0.6t_{CY} + 180	2.6t_{CY} + 180	ns
$\overline{WAIT}$ ↑ → $\overline{WR}$ ↑ delay time	t_{WTWR}		0.6t_{CY} + 120	2.6t_{CY} + 120	ns

Remarks **1.** MCS: Bit 0 of the oscillation mode selection register.

2. PCC2-PCC0: Bit 2-bit 0 of the processor clock control register.

3. $t_{CY} = T_{CY}/4$.

4. n indicates the number of waits.

(3) Serial Interface (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

(a) **Serial Interface Channel 0**

(i) 3-wire serial I/O mode ($\overline{SCK0}$ ··· internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK0}$ high-/low-level widths	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 5.5 V	t_{KCY1}/2–50			ns
			t_{KCY1}/2–100			ns
SI0 setup time (to $\overline{SCK0}$ ↑)	t_{SIK1}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI0 hold time (from $\overline{SCK0}$ ↑)	t_{KSI1}		400			ns
$\overline{SCK0}$ ↓ → SO0 output delay time	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the SO0 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$ ··· external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK0}$ high-/low-level widths	t_{KH2}, t_{KL2}	V_{DD} = 4.5 to 5.5 V	400			ns
			800			ns
SI0 setup time (to $\overline{SCK0}$ ↑)	t_{SIK2}		100			ns
SI0 hold time (from $\overline{SCK0}$ ↑)	t_{KSI2}		400			ns
$\overline{SCK0}$ ↓ → SO0 output delay time	t_{KSO2}	C = 100 pF[Note]			300	ns
$\overline{SCK0}$ rise, fall time	t_{R2}, t_{F2}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO0 output line load capacitance.

(iii) SBI mode ($\overline{SCK0}$ ··· internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high-/low-level widths	t_{KH3}, t_{KL3}	V_{DD} = 4.5 to 5.5 V		t_{KCY3}/2–50			ns
				t_{KCY3}/2–150			ns
SB0, SB1 setup time (to $\overline{SCK0}$ ↑)	t_{SIK3}	V_{DD} = 4.5 to 5.5 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK0}$ ↑)	t_{KSI3}			t_{KCY3}/2			ns
$\overline{SCK0}$ ↓ → SB0, SB1 output delay time	t_{KSO3}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		250	ns
				0		1000	ns
$\overline{SCK0}$ ↑ → SB0, SB1 ↓	t_{KSB}			t_{KCY3}			ns
SB0, SB1 ↓ → $\overline{SCK0}$ ↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R and C are the SB0 and SB1 output line load resistance and load capacitance.

(iv) SBI mode ($\overline{SCK0}$ ··· external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high-/low-level widths	t_{KH4}, t_{KL4}	V_{DD} = 4.5 to 5.5 V		400			ns
				1600			ns
SB0, SB1 setup time (to $\overline{SCK0}$ ↑)	t_{SIK4}	V_{DD} = 4.5 to 5.5 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK0}$ ↑)	t_{KSI4}			t_{KCY4}/2			ns
$\overline{SCK0}$ ↓ → SB0, SB1 output delay time	t_{KSO4}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		300	ns
				0		1000	ns
$\overline{SCK0}$ ↑ → SB0, SB1 ↓	t_{KSB}			t_{KCY4}			ns
SB0, SB1 ↓ → $\overline{SCK0}$ ↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ rise, fall time	t_{R4}, t_{F4}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note R and C are the SB0 and SB1 output line load resistance and load capacitance.

(v) 2-wire serial I/O mode ($\overline{SCK0}$ ··· internal clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	1600			ns
				3200			ns
$\overline{SCK0}$ high-level widths	t_{KH5}			t_{KCY5}/2–160			ns
$\overline{SCK0}$ low-level width	t_{KL5}		V_{DD} = 4.5 to 5.5 V	t_{KCY5}/2–50			ns
SB0, SB1 setup time (to $\overline{SCK0}$ ↑)	t_{SIK5}		V_{DD} = 4.5 to 5.5 V	100			ns
				150			ns
SB0, SB1 hold time (from $\overline{SCK0}$ ↑)	t_{KSI5}			600			ns
$\overline{SCK0}$ ↓ → SB0, SB1 output delay time	t_{KSO5}			0		300	ns

Note R and C are the $\overline{SCK0}$, SB0, and SB1 output line load resistance and load capacitance.

(vi) 2-wire serial I/O mode ($\overline{SCK0}$ ··· external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}	V_{DD} = 4.5 to 5.5 V	1600			ns
			3200			ns
$\overline{SCK0}$ high-level widths	t_{KH6}		650			ns
$\overline{SCK0}$ low-level width	t_{KL6}		800			ns
SB0, SB1 setup time (to $\overline{SCK0}$ ↑)	t_{SIK6}		100			ns
SB0, SB1 hold time (from $\overline{SCK0}$ ↑)	t_{KSI6}		t_{KCY6}/2			ns
$\overline{SCK0}$ ↓ → SB0, SB1 output delay time	t_{KSO6}	R = 1 kΩ, C = 100 pF[Note]	0		300	ns
$\overline{SCK0}$ rise, fall time	t_{R6}, t_{F6}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note R and C are the $\overline{SCK0}$, SB0, and SB1 output line load resistance and load capacitance.

(b) **Serial Interface Channel 1**

(i) 3-wire serial I/O mode ($\overline{SCK1}$ ··· internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high-/low-level widths	t_{KH7}, t_{KL7}	V_{DD} = 4.5 to 5.5 V	t_{KCY7}/2–50			ns
			t_{KCY7}/2–100			ns
SI1 setup time (to $\overline{SCK1}$ ↑)	t_{SIK7}	V_{DD} = 4.5 to 5.5 V	300			ns
			350			ns
SI1 hold time (from $\overline{SCK1}$ ↑)	t_{KSI7}		400			ns
$\overline{SCK1}$ ↓ → SO1 output delay time	t_{KSO7}	C = 100 pF[Note]			300	ns

Note C is the SO1 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$ ··· external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high-/low-level widths	t_{KH8}, t_{KL8}	V_{DD} = 4.5 to 5.5 V	400			ns
			800			ns
SI1 setup time (to $\overline{SCK1}$ ↑)	t_{SIK8}		100			ns
SI1 hold time (from $\overline{SCK1}$ ↑)	t_{KSI8}		400			ns
$\overline{SCK1}$ ↓ → SO1 output delay time	t_{KSO8}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ rise, fall time	t_{R8}, t_{F8}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO1 output line load capacitance.

(iii) Automatic transmission/reception function 3-wire serial I/O mode ($\overline{SCK1}$ ··· internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	V_{DD} = 4.5 to 5.5 V		800			ns
				1600			ns
$\overline{SCK1}$ high-/low-level widths	t_{KH9}, t_{KL9}	V_{DD} = 4.5 to 5.5 V		t_{KCY9}/2–50			ns
				t_{KCY9}/2–100			ns
SI1 setup time (to $\overline{SCK1}$ ↑)	t_{SIK9}	V_{DD} = 4.5 to 5.5 V		100			ns
				150			ns
SI1 hold time (from $\overline{SCK1}$ ↑)	t_{KSI9}			400			ns
$\overline{SCK1}$ ↓ → SO1 output delay time	t_{KSO9}	C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V			300	ns
$\overline{SCK1}$ ↑ → STB ↑	t_{SBD}			t_{KCY9}/2–100		t_{KCY9}/2+100	ns
Strobe signal high-level width	t_{SBW}			t_{KCY3}–30		t_{KCY3}+30	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}			100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	V_{DD} = 4.5 to 5.5 V		100			ns
				150			ns
Busy inactivation → $\overline{SCK1}$ ↓	t_{SPS}					2t_{KCY9}	ns

Note C is the SO1 output line load capacitance.

(iv) Automatic transmission/reception function 3-wire serial I/O mode ($\overline{SCK1}$ ··· external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	V_{DD} = 4.5 V to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high-/low-level widths	t_{KH10}, t_{KL10}	V_{DD} = 4.5 V to 5.5 V	400			ns
			800			ns
SI1 setup time (to $\overline{SCK1}$ ↑)	t_{SIK10}		100			ns
SI1 hold time (from $\overline{SCK1}$ ↑)	t_{KSI10}		400			ns
$\overline{SCK1}$ ↓ → SO1 output delay time	t_{KSO10}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ rise, fall time	t_{R10}, t_{F10}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO1 output line load capacitance.

(c) **Serial Interface Channel 2**

(i) 3-wire serial I/O mode ($\overline{SCK2}$ ··· internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY11}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK2}$ high-/low-level widths	t_{KH11}, t_{KL11}	V_{DD} = 4.5 to 5.5 V	t_{KCY11}/2–50			ns
			t_{KCY11}/2–100			ns
SI2 setup time (to $\overline{SCK2}$ ↑)	t_{SIK11}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI2 hold time (from $\overline{SCK2}$ ↑)	t_{KSI11}		400			ns
$\overline{SCK2}$ ↓ → SO2 output delay time	t_{KSO11}	C = 100 pF[Note]			300	ns

Note C is the SO2 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{SCK2}$ ··· external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY12}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK2}$ high-/low-level widths	t_{KH12}, t_{KL12}	V_{DD} = 4.5 to 5.5 V	400			ns
			800			ns
SI2 setup time (to $\overline{SCK2}$ ↑)	t_{SIK12}		100			ns
SI2 hold time (from $\overline{SCK2}$ ↑)	t_{KSI12}		400			ns
$\overline{SCK2}$ ↓ → SO2 output delay time	t_{KSO12}	C = 100 pF[Note]			300	ns
$\overline{SCK2}$ rise, fall time	t_{R12}, t_{F12}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO2 output line load capacitance.

(iii) UART mode (dedicated baud rate generator output)

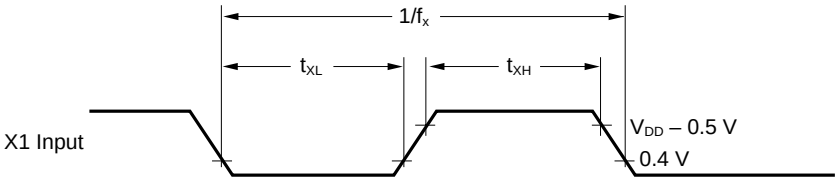
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 4.5 to 5.5 V			78125	bps
					39063	bps

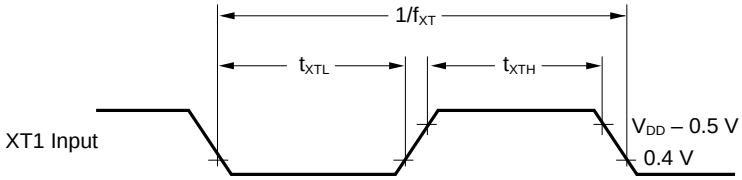
(iv) UART mode (external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY13}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
ASCK high-/low-level widths	t_{KH13}, t_{KL13}	V_{DD} = 4.5 to 5.5 V	400			ns
			800			ns
Transfer rate		V_{DD} = 4.5 to 5.5 V			39063	bps
					19531	bps
ASCK rise, fall time	t_{R13}, t_{F13}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

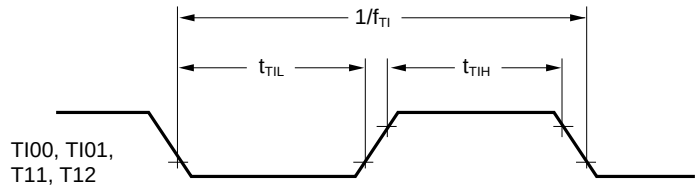
AC Timing Test Point (Excluding X1, XT1 Input)

Clock Timing



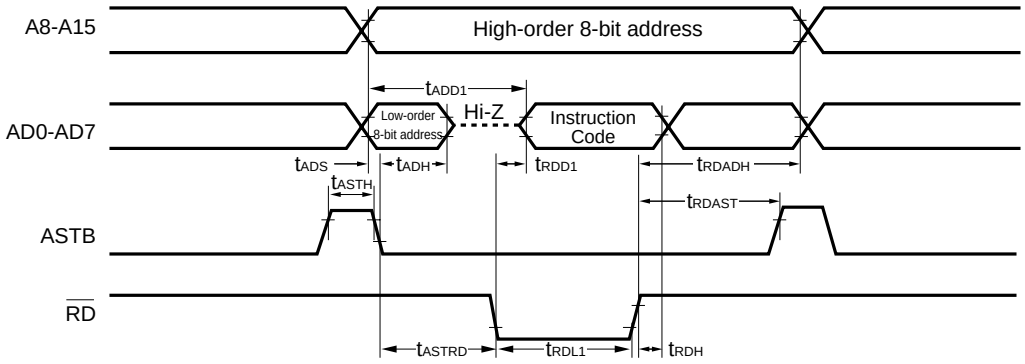


TI Timing

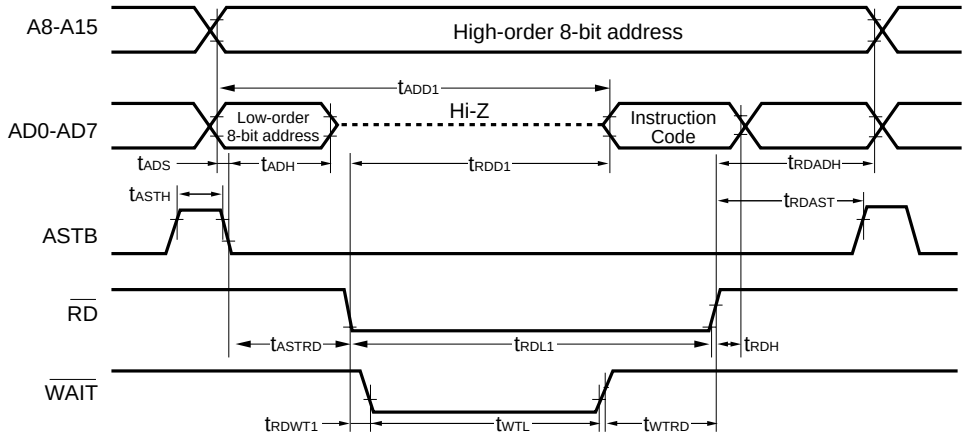


Read/Write Operations

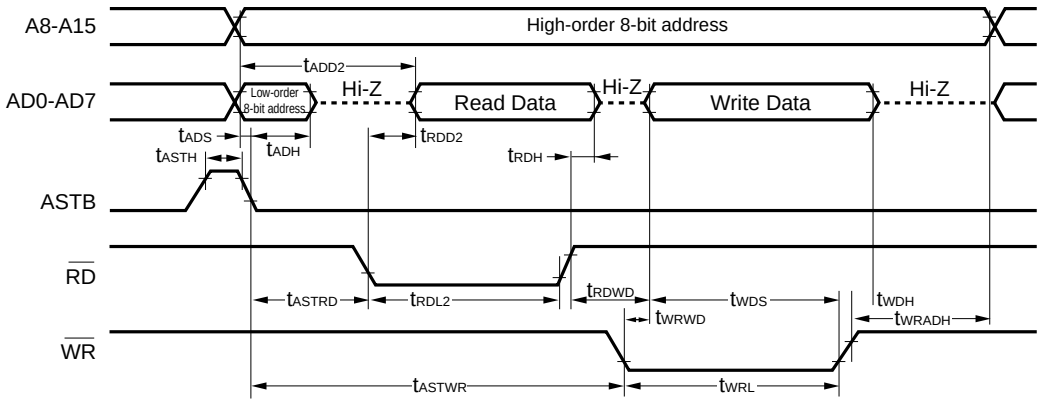
External fetch (no wait):



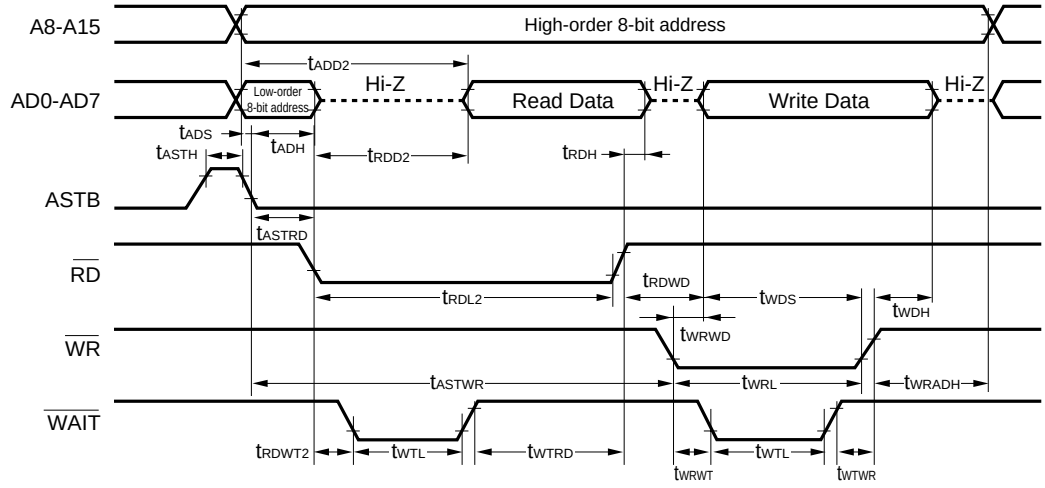
External fetch (wait insertion):



External data access (no wait):

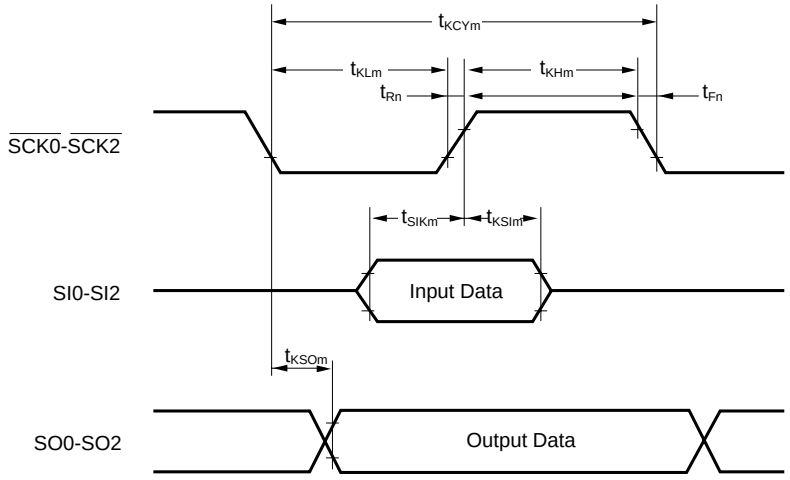


External data access (wait insertion):



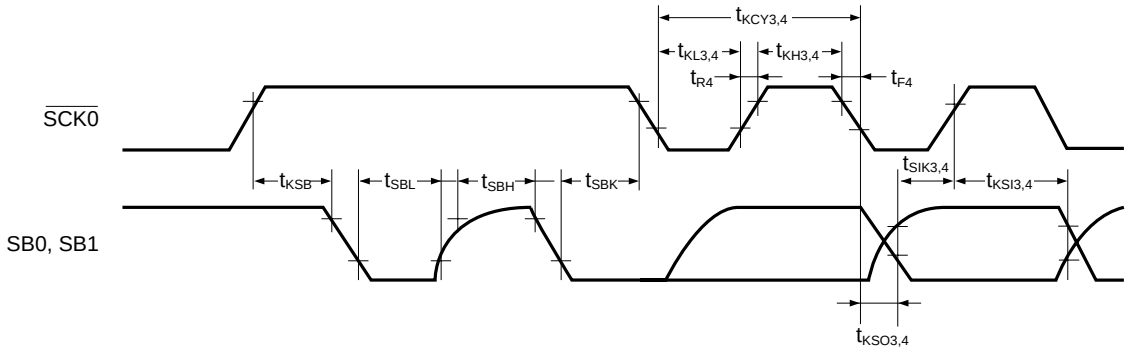
Serial Transfer Timing

3-wire serial I/O mode:

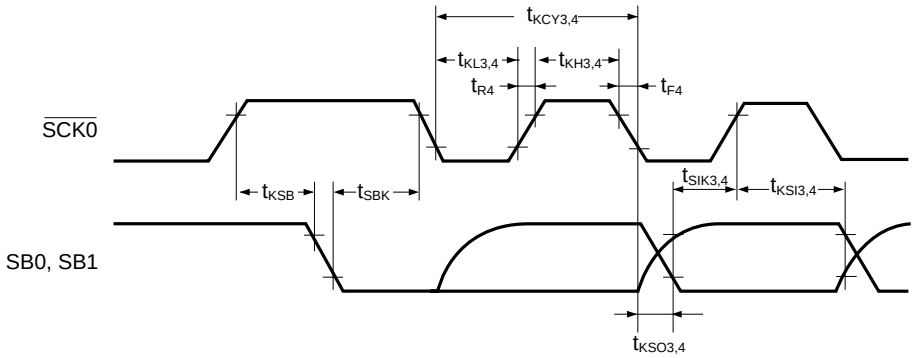


Remark m = 1, 2, 7, 8, 11 or 12
n = 2, 8 or 12

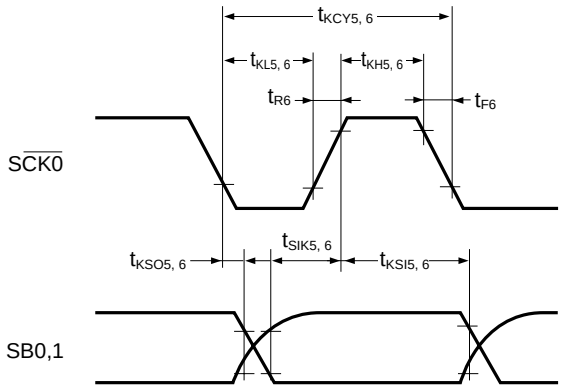
SBI mode (bus release signal transfer):



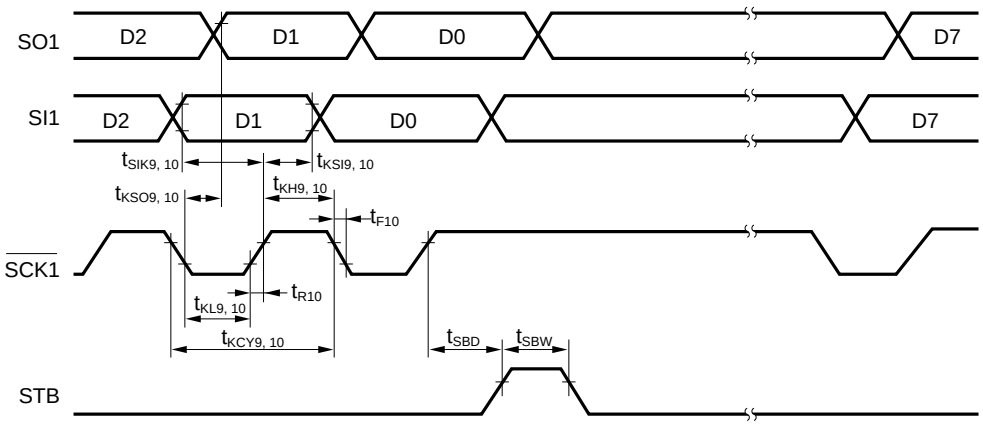
SBI mode (command signal transfer):



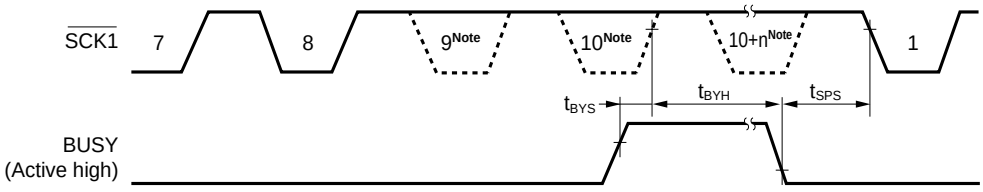
2-wire serial I/O mode:



Automatic transmission/reception function 3-wire serial I/O mode:

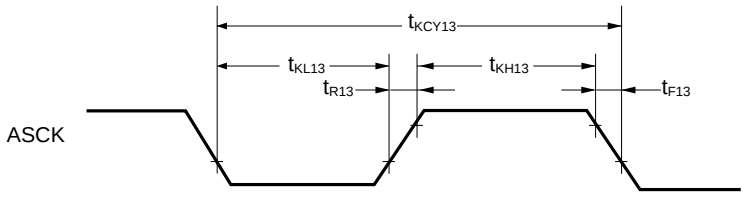


Automatic transmission/reception function 3-wire serial I/O mode (busy processing):



Note The signals are not actually low here, but are represented in this way to show the timing convention.

UART Mode (External Clock Input)



A/D Converter Characteristics (T_A = –40 to +85 °C, AV_{DD} = V_{DD} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Resolution				8	8	8	bit
Total error Note		IEAD = 00H				0.6	%
		IEAD = 01H	V_{DD} = 4.5 to 5.5 V		1	2.2	%
					1.4	2.6	%
Conversion time	t_{CONV}			19.1		200	μs
Sampling time	t_{SAMP}			24/f_{XX}			μs
Analog input voltage	V_{IAN}			AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}			2.7		AV_{DD}	V
AV_{REF0}-AV_{SS} resistance	R_{AIREF0}			4	14		kΩ

Note Excluding quantization error (±1/2 LSB). Shown as a percentage of the full scale value.

Remarks **1.** f_{XX}: Main system clock frequency (f_X or f_X/2).
2. f_X: Main system clock oscillation frequency.

D/A Converter Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Resolution						8	bit
Total error		R = 2 MΩ Note1				1.2	%
		R = 4 MΩ Note1				0.8	%
		R = 10 MΩ Note1				0.6	%
Settling time		C = 30 pF Note1	V_{DD} = 4.5 to 5.5 V			10	μs
						15	μs
Output resistor	R_O	DACS0, DACS1 = 55H Note2			10		kΩ
Analog reference voltage	AV_{REF1}			2.7		V_{DD}	V
AV_{REF1} current	I_{REF1}	**Note2**				1.5	mA

Notes **1.** R and C are the D/A converter output pin load resistance and load capacitance.
2. Value for one D/A converter channel.

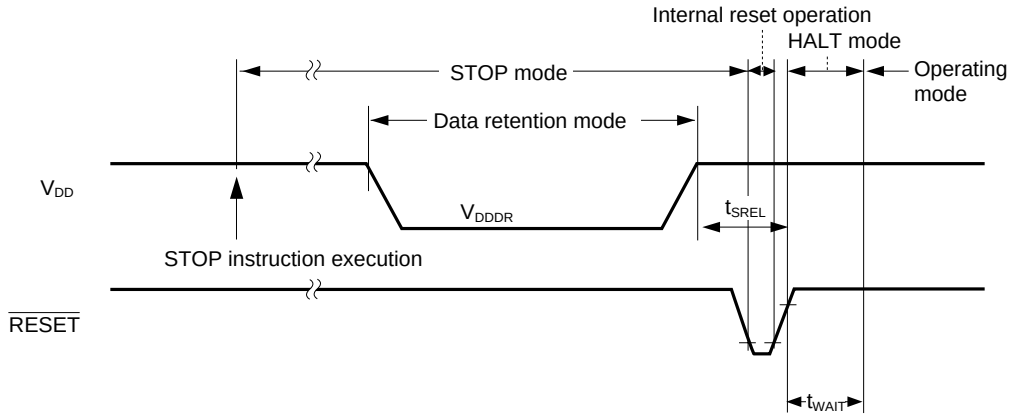
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to 85 °C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.0 V Subsystem clock stopped, feedback resistor disconnected		0.1	10	μA
Release signal setup time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_x$		ms
		Release by interrupt		**Note**		ms

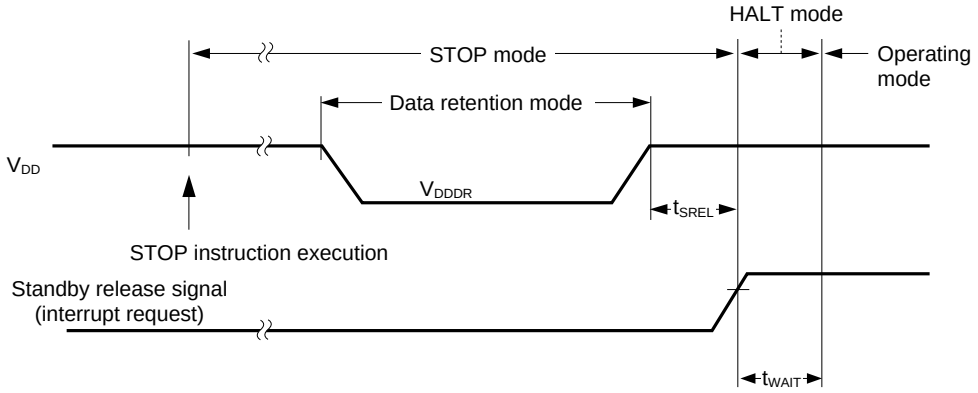
Note $2^{12}/f_{xx}$, or $2^{14}/f_{xx}$ through $2^{17}/f_{xx}$ can be selected by bits 0 to 2 (OSTS0-OSTS2) of the oscillation stabilization time selection register.

Remarks f_{xx}: Main system clock frequency
f_x : Main system clock oscillation frequency

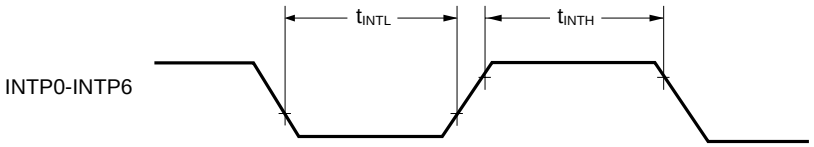
Data Retention Timing (STOP mode released by $\overline{RESET}$)



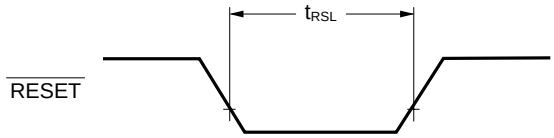
Data Retention Timing (Standby released signal: STOP mode released by interrupt signal)



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



IEBus Controller Characteristics (T_A = –40 to 85 °C, V_{DD} = 5 V ± 10 %)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
IEBus controller system clock frequency	f_S	When using mode 0 or mode 1[Note1]		5.91	6.00	6.09	MHz
				6.20	6.29	6.39	MHz
		When using mode 2[Note1]		5.97	6.00	6.03	MHz
				6.26	6.29	6.32	MHz
Driver delay time ($\overline{\text{TX}}$ output → Bus line)		C = 50 pF[Note2]	f_S = 6.00 MHz			1.6	μs
			f_S = 6.29 MHz			1.5	μs
Receiver delay time (Bus line → $\overline{\text{RX}}$ input)		f_S = 6.00 MHz				0.75	μs
		f_S = 6.29 MHz				0.7	μs
Propagation delay time on the bus		f_S = 6.00 MHz				0.90	μs
		f_S = 6.29 MHz				0.85	μs

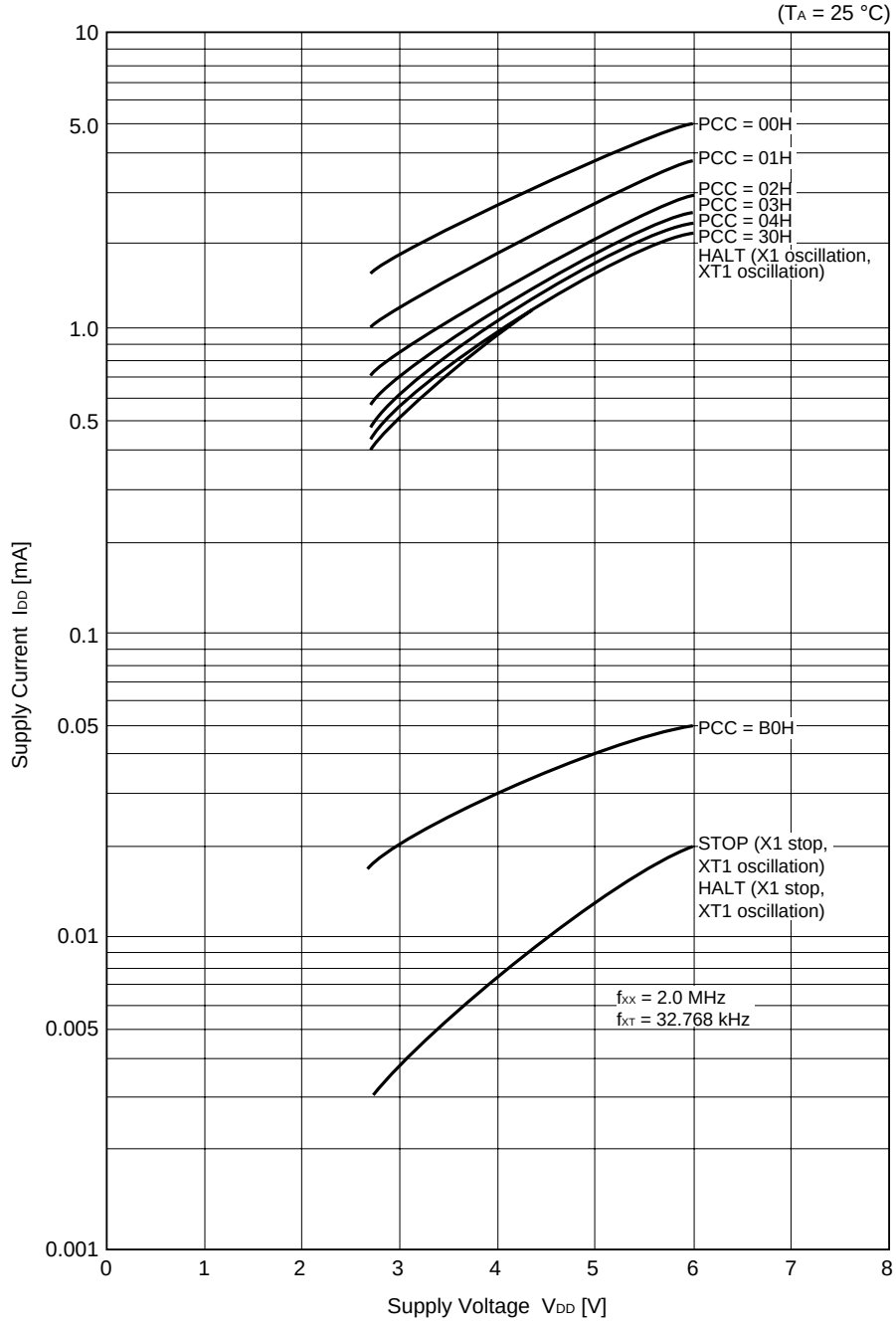
Notes 1. Values in lower line do not satisfy the standard as IEBus.

2. C is the $\overline{\text{TX}}$ output line load capacitance.

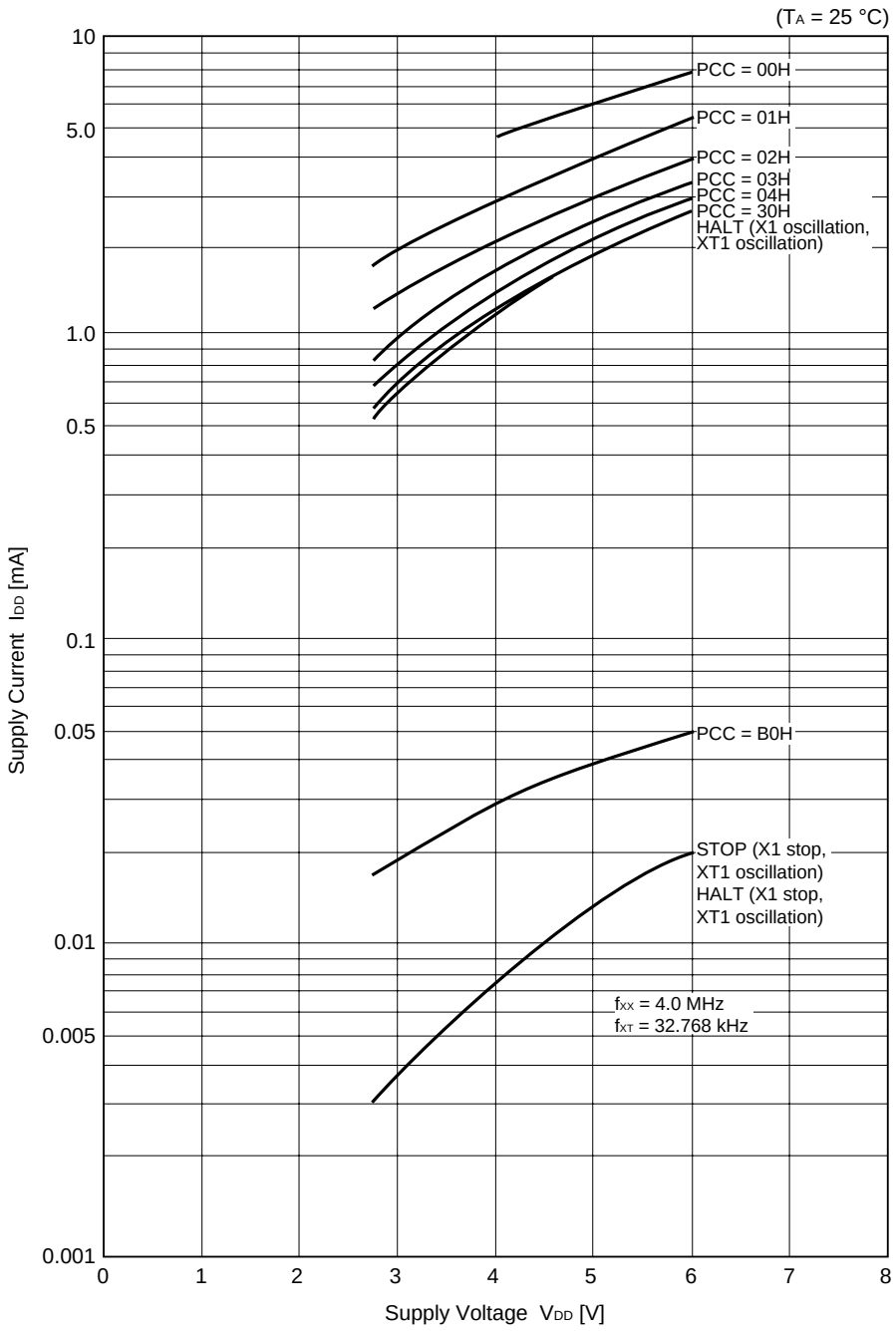
12. CHARACTERISTIC CURVES (REFERENCE VALUES)

I_{DD} vs V_{DD} (f_X = 6.0 MHz, f_{XX} = 2.0 MHz)

(T_A = 25 °C)

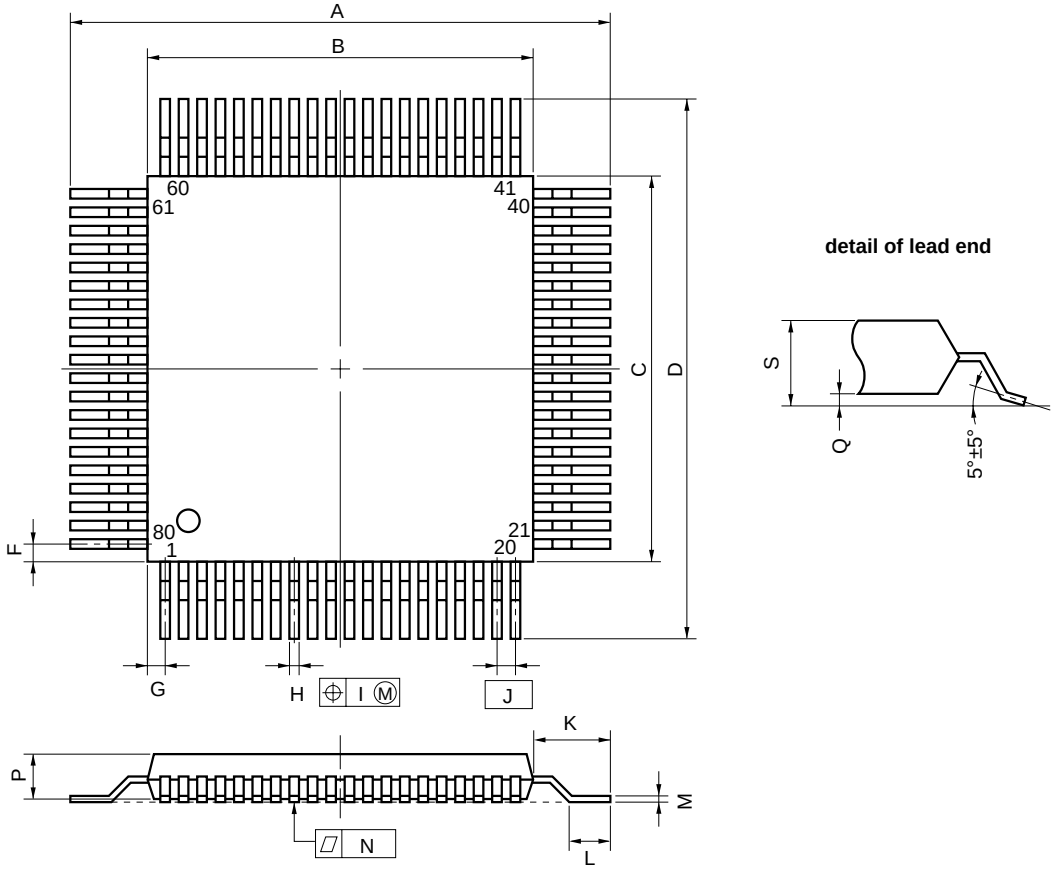


I_{DD} vs V_{DD} (f_X = 6.0 MHz, f_{XX} = 4.0 MHz)



13. PACKAGE DRAWING

80 PIN PLASTIC QFP (□14)



S80GC-65-3B9-3

NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.8	0.031
G	0.8	0.031
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

14. RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the conditions recommended below.

For details on the recommended soldering conditions, refer to information document **"Semiconductor Device Mounting Technology Manual" (IEI-1207)**.

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

Table 14-1. Soldering Conditions for Surface Mount Devices

μPD78094GC-×××-3B9: 80-pin plastic QFP (14 x 14 mm)
μPD78095GC-×××-3B9: 80-pin plastic QFP (14 x 14 mm)
μPD78096GC-×××-3B9: 80-pin plastic QFP (14 x 14 mm)
μPD78098AGC-×××-3B9: 80-pin plastic QFP (14 x 14 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Package peak temperature: 235 °C, Reflow time: 30 seconds or less (at 210 °C or higher), Number of reflow processes: 2 or less < Cautions > (1) Wait for the device temperature to return to normal after the first reflow before starting the second reflow. (2) Do not perform flux cleaning with water after the first reflow.	IR35-00-2
VPS	Package peak temperature: 215 °C, Reflow time: 40 seconds or less (at 200 °C or higher), Number of reflow processes: 2 or less < Cautions > (1) Wait for the device temperature to return to normal after the first reflow before starting the second reflow. (2) Do not perform flux cleaning with water after the first reflow.	VP15-00-2
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or less, Number of flow processes: 1, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 °C or below, Flow time: 3 seconds or less (per device side)	—

APPENDIX A. DEVELOPMENT TOOLS

The following tools are available for system development using the μPD78098 subseries.

Language Processing Software

RA78K/0[Note 1, 2, 3]	Assembler package used in common for the 78K/0 series
CC78K/0[Note 1, 2, 3]	C compiler package used in common for the 78K/0 series
DF78098[Note 1, 2, 3]	Device file used for the μPD78098 subseries
CC78K/0-L[Note 1, 2, 3]	C compiler library source file used in common for the 78K/0 series

PROM Writing Tools

PG-1500	PROM programmer
PA-78P054GC PA-78P054KK-T	Programmer adapter connected to the PG-1500
PG-1500 Controller[Note 1, 2]	Control program for the PG-1500

Debugging Tools

IE-78000-R	In-circuit emulator used in common for the 78K/0 series
IE-78000-R-BK	Break board used in common for the 78K/0 series
IE-78098-R-EM	Emulation board for evaluation of the μPD78098 subseries
EP-78230GC-R	Emulation probe used in common for the μPD78234 subseries
EV-9200GC-80	Socket mounted on the user system board prepared for 80-pin plastic QFP
EV-9900	Tool used for removing the μPD78P098AKK-T from the EV-9200GF-80.
SM78K0[Note 4, 5]	System simulator used in common for the 78K/0 series
SD78K/0[Note 1, 2]	Screen debugger for the IE-78000-R
DF78098[Note 1, 2, 4, 5]	Device file used for the μPD78098 subseries

Real-Time OS

RX78K/0[Note 1, 2, 3]	Real-time OS used for the 78K/0 series
MX78K0[Note 1, 2, 3]	OS used for the 78K/0 series

Fuzzy Inference Development Support System

FE9000[Note 1]/FE9200[Note 5]	Fuzzy knowledge data creation tool
FT9080[Note 1]/FT9085[Note 2]	Translator
FI78K0[Note 1, 2]	Fuzzy inference module
FD78K0[Note 1, 2]	Fuzzy inference debugger

Notes 1. Based on PC-9800 series (MS-DOS™)

2. Based on IBM PC/AT™ (PC DOS™)

3. Based on HP9000 series 300™, HP9000 series 700™ (HP-UX™), SPARCstation™ (SunOS™), and EWS-4800 series (EWS-UX/V)

4. Based on PC-9800 series (MS-DOS + Windows™)

5. Based on IBM PC/AT (PC DOS + Windows)

Remark Use the RA78K/0, CC78K/0, SM78K0, and SD78K/0 in combination with the DF78098.

APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document	Document No.	
	Japanese	English
μPD78P098A Preliminary Product Information	IP-9135	In preparation
μPD78098 Subseries User's Manual	IEU-854	IEU-1381
78K/0 Series User's Manual—Instructions	IEU-849	IEU-1372
78K/0 Series Instruction Table	IEM-5522	—
78K/0 Series Instruction Set	IEM-5521	—
μPD78098 Subseries Special Function Register Table	IEM-5591	—
78K/0 Series Application Note—Basic III	IEA-767	In preparation

Documents Related to Development Tools (User's Manual)

Document		Document No.	
		Japanese	English
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K Series Library Source File		EEU-777	—
CC78K/0 C Compiler Application Note	Programming Know-How	EEA-618	In preparation
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller PC-9800 Series (MS-DOS based)		EEU-704	Planned
PG-1500 Controller IBM PC Series (PC DOS based)		EEU-5008	EEU-1291
IE-78000-R		EEU-810	EEU-1398
IE-78000-R-BK		EEU-867	EEU-1427
IE-78098-R-EM		EEU-933	EEU-1473
EP-78230		EEU-985	EEU-1515
SM78K0 System Simulator	Reference	EEU-5002	In preparation
SD78K/0 Screen Debugger	Introduction	EEU-852	—
PC-9800 Series (MS-DOS based)	Reference	EEU-816	—
SD78K/0 Screen Debugger	Introduction	EEU-5024	EEU-1414
IBM PC/AT (PC DOS based)	Reference	EEU-993	EEU-1413

Caution The contents of the documents listed above are subject to change without prior notice. Make sure to use the latest edition when starting design.

Documents Related to Embedded Software (User's Manual)

Document		Document No.	
		Japanese	English
78K/0 Series Real-time OS	Basic	EEU-912	—
	Installation	EEU-911	—
	Technical	EEU-913	—
78K/0 Series OS MX78K0	Basic	EEU-5010	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, and 87AD Series Fuzzy Inference Development Support System Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-921	EEU-1458

Other Documents

Document	Document No.	
	Japanese	English
Package Manual	IEI-635	IEI-1213
Semiconductor Device Mounting Technology Manual	IEI-616	IEI-1207
NEC Semiconductor Device Quality Grades	IEI-620	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	IEM-5068	—
Electrostatic Discharge (ESD) Test	MEM-539	—
Semiconductor Device Quality Assurance Guide	MEI-603	MEI-1202
Microcomputer-Related Product Guide – Third Party Products –	MEI-604	—

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

The related documents indicated in this publication may include preliminary versions.
However, preliminary versions are not marked as such.

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