405-760
405 772

705-772

NEC

μPD7225
LCD 7/14 Segment Controller/Driver

DESCRIPTION

The μPD7225 is a programmable peripheral device containing all the circuitry necessary for interfacing a microprocessor to a wide variety of alpha-numeric Liquid Crystal Displays (LCDs). The display controller hardware automatically synchronizes the drive signals for any static or multiplexed LCD containing up to 4 backplanes, and up to 32 segments . The μPD7225 is fully compatible with most microprocessors, and communicates with them through a 2-line, 8-bit Serial port. It can be easily configured into multiple chip designs for larger LCD applications. In addition, the μPD7225 includes on board 8-segment Numeric and 15-segment Alpha-Numeric decoders, and programmable blinking capabilities. The μPD7225 is manufactured with a low-power single 5V CMOS process, and is available in a 52-pin plastic flat package.

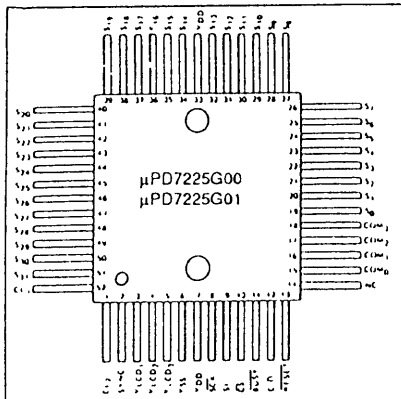
FEATURES

- Single Chip LCD Controller
- Direct LCD Drive
- Selectable Backplace Drive Configuration
  - Static; 2-, 3-, or 4-Backplane Multiplexed
- Programmable Display Configurations
  - 8-Segment Numeric – up to 16 Characters
  - 15-Segment Alpha-Numeric – up to 8 Characters
- 32-Segment Drive Lines
- Selectable Display Bias Configuration
  - Static; 1/2 or 1/3
- Automatic Synchronization of Segment and Backplane Drive Lines
- Dual 32 x 4 Bit RAMs for Display Data Storage
- Programmable Display Data Addressing
  - Individual Segment
  - 16-Character, 8-Segment Numeric Decoder
  - 64-Character, 15-Segment Alpha-Numeric Decoder
- Programmable Blinking Capability
  - Individual Segment, Individual Character, or Entire Display
- 8-Bit Serial Interface
- Compatible with most 4-Bit, 8-Bit, and 16-Bit Microprocessors
- Fully Cascadable for Larger LCD Applications
- Single +5V Power Supply
- CMOS Technology

ORDER INFORMATION

Order code	Package
μPD7225G01	52-pin plastic QFP (straight)
μPD7225G00	52-pin plastic QFP (bend)
μPD7225GB-3B7	56-pin plastic QFP (bend)

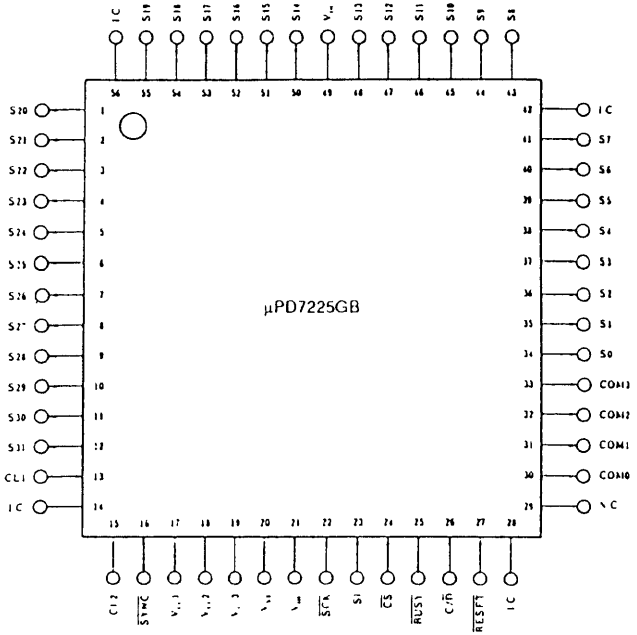
PIN CONFIGURATION



PIN DESCRIPTION

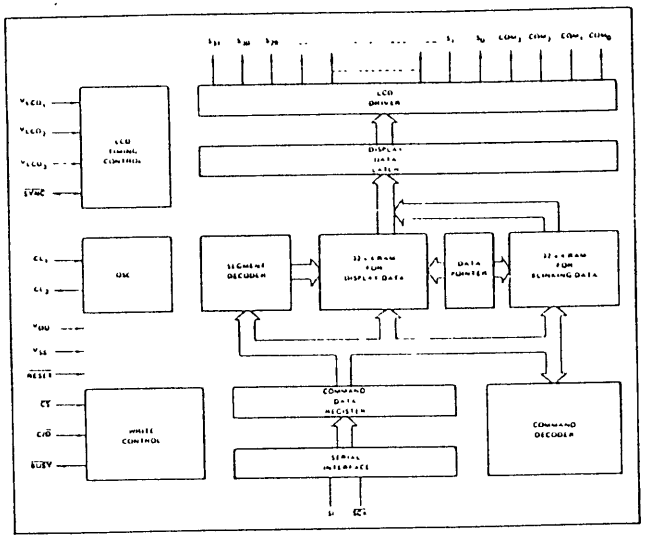
SYMBOL	DESCRIPTION
S_0-S_{31}	LCD Segment Drive Outputs
COM_0-COM_3	LCD Backplane Drive Outputs
V_{SS}	Ground
V_{DD}	Power Supply Positive
V_{LCD_1}, V_{LCD_3}	LCD Power Supply
$\overline{SCK}$	Serial Clock Input
SI	Serial Input
$\overline{CS}$	Chip Select
C/$\overline{D}$	Command/Data Select
CL_1, CL_2	System Clock Input, Output
$\overline{SYNC}$	Synchronization Signal I/O Port for multiple chip
$\overline{BUSY}$	Busy Output
$\overline{RESET}$	Reset Input
NC	No Connection

Pin Configuration: 56-pin QFP (Top View)



Note: I.C. pin must be connected to V_{DD} or left unconnected.

BLOCK DIAGRAM



COMMAND DESCRIPTION

1 MODE SET

0	1	0	D_4	D_3	D_2	D_1	D_0	40 5F

The MODE SET command sets up the Backplane Drive Configuration, the Display Bias Voltage Configuration, and the A/C Drive Frequency for the μPD7225

The Backplane Drive Configuration is defined as follows

D_3	D_2	Backplane Drive Configuration
0	1	Static (1 Backplane)
1	1	2 Backplane Multiplexed
1	0	3 Backplane Multiplexed
0	0	4 Backplane Multiplexed

The Display Bias Voltage Configuration is defined as follows

D_4	Display Bias Voltage Configuration
0	1/3 (three voltage)
1	1/2 (two voltage)
X	Static (single voltage, default when D_3D_2 = 00)

The A/C Drive Frequency is defined as follows

D_1	D_0	A/C Drive Frequency
0	0	$f_c/2^7$ Hz
0	1	$f_c/2^8$ Hz
1	0	$f_c/2^9$ Hz
1	1	$f_c/2^{11}$ Hz

Note LCD Frame Frequency = $\frac{\text{A/C Drive Frequency}}{\text{\# of active Backplane Drive lines}}$

2 UNSYNCHRONOUS DATA TRANSFER

0 0 1 1 0 0 0 0	30

The Normal Transfer of data from the Display Data RAM to the segment output latches latches occurs with the rising edge of CS. The UNSYNCHRONOUS DATA TRANSFER command implements this mode of data transfer, and also disables the SYNCHRONOUS DATA TRANSFER operation

3 SYNCHRONOUS DATA TRANSFER

0 0 1 1 0 0 0 1	31

Data can also be transferred from the Display Data RAM to the segment output latches with the rising edge of f_c. The SYNCHRONOUS DATA TRANSFER command implements this mode of data transfer, and also disables the UNSYNCHRONOUS DATA TRANSFER operation

4 INTERRUPT DATA TRANSFER

0 0 1 1 1 0 0 0	38

Occasionally, the Host microprocessor system may experience events, such as prioritized Hardware interrupts, that may disrupt communications with the μPD7225. Display Data transfers to the μPD7225 may be interrupted, without disrupting the μPD7225 internal display data protocol, by issuing an INTERRUPT DATA TRANSFER command at the beginning of the interrupt service routine. Display data updating may be resumed in an orderly fashion after the interrupt service routine is completed

5 CLEAR Display Data

0 0 1 0 0 0 0 0	20

All locations in the Display Data RAM are set to zero by executing the CLEAR DISPLAY DATA command. The Data Pointer is also cleared, and set to its initial location

6 CLEAR BLINKING DATA

0 0 0 0 0 0 0 0	00

All locations in to Blinking Data RAM are set to zero by executing the CLEAR BLINKING DATA command. The Data Pointer is also cleared, and set to its initial location

7 LOAD DATA POINTER

0 0 0 D_4 D_3 D_2 D_1 D_0	E0-FF

To access a particular location in either the Display Data RAM or the BLINKING DATA RAM the Data Pointer must be given the corresponding address of that location. The LOAD DATA POINTER command transfers 5 bits of immediate data to the Data Pointer

8 WRITE DISPLAY DATA

1 1 0 1 D_3 D_2 D_1 D_0	D0 DF

The WRITE DISPLAY DATA command transfers 4 bits of immediate data to the Display Data RAM location addressed by the Data Pointer. After the transfer is complete, the Data Pointer is automatically incremented

9 WRITE BLINKING DATA

1 1 0 0 D_3 D_2 D_1 D_0	C0 CF

The WRITE BLINKING DATA command transfers 4 bits of immediate data to the Blinking Data RAM location addressed by the Data Pointer. After the transfer is complete, the Data Pointer is automatically incremented

10 ENABLE DISPLAY

0 0 0 1 0 0 0 1	11

The ENABLE DISPLAY command turns on the LCD, and starts the automatic display controller hardware of the μPD7225

11 DISABLE DISPLAY

0 0 0 1 0 0 0 0	10

The DISABLE DISPLAY command turns off the LCD, and stops the automatic display controller hardware of the μPD7225

12 ENABLE BLINKING

0 0 0 1 1 0 1 D_0	1A 1B

If a particular LCD application requires blinking several segments, the appropriate information must have been transferred to the Blinking Data RAM previously. The ENABLE BLINKING command selects the Blinking frequency according to the value of D_0, and turns the Blinking feature on

D_0	Blinking Frequency
0	$f_c/2^{16}$ Hz
1	$f_c/2^{17}$ Hz

13 DISABLE BLINKING

0 0 0 1 1 0 0 0	18

The DISABLE BLINKING command turns the Blinking feature OFF

14 ENABLE SEGMENT DECODER

0 0 0 1 0 1 0 1	15

The μPD7225 has an internal 8 segment Numeric data decoder and an internal 15 segment Alpha Numeric data decoder. These decoders can be used for automatic display data addressing, by the Host microprocessor to absorb some of the system overhead required to decode display data for the μPD7225

The ENABLE SEGMENT DECODER command implements this mode of display data addressing. Upon execution, display data received by the μPD7225 is diverted to one of the segment decoders. The segment decoder then writes display data to the Display Data RAM. The distinction between 8 segment decoding and 15 segment decoding is made by the MSB of the display data

MSB	Decoding Selected
0	8 segment Numeric
1	15 segment Alpha Numeric

15 DISABLE SEGMENT DECODER | 0 0 0 1 0 1 0 0 | 14

The DISABLE SEGMENT DECODER command stops the segment decode addressing, and enables the transfers of Display Data from the Host microprocessor directly to the Display Data RAM

16 OR DISPLAY DATA | 1 0 1 1 D_3 D_2 D_1 D_0 | B0-BF

The OR DISPLAY DATA command performs a LOGICAL OR between the Display Data addressed by the Data Pointer, and 4 bits of immediate data The result is written to the same Display Data location and the Data Pointer is automatically incremented

17 AND DISPLAY DATA | 1 0 0 1 D_3 D_2 D_1 D_0 | 90-9F

The AND DISPLAY DATA command performs a LOGICAL AND between the Display Data addressed by the Data Pointer, and 4 bits of immediate data The result is written to the same Display Data location, and the Data Pointer is automatically incremented

18 OR BLINKING DATA | 1 0 1 0 D_3 D_2 D_1 D_0 | A0-AF

The OR BLINKING DATA command performs a LOGICAL OR between the Blinking Data addressed by the Data Pointer, and 4 bits of immediate data The result is written to the same Blinking Data location, and the Data Pointer is automatically incremented

19 AND BLINKING DATA | 1 0 0 0 D_3 D_2 D_1 D_0 | 80-8F

The AND BLINKING DATA command performs a LOGICAL AND between the Blinking Data addressed by the Data Pointer, and 4 bits of immediate data The result is written to the same Blinking Data location, and the Data Pointer is automatically incremented

Command Summery

COMMAND	DESCRIPTION	INSTRUCTION CODE BINARY D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX
1 Mode Set	Set up Driving Mode of LCD including 1) Backplane drive 2) Display Blink 3) LCD Frame Frequency	0	1	0	D_4	D_3	D_2	D_1	D_0	40-5F
2 Unsynchronous Data Transfer	Synchronize writing of display data with CS	0	0	1	1	0	0	0	0	30
3 Synchronous Data Transfer	Synchronize writing of display data with LCD Frame Frequency	0	0	1	1	0	0	0	1	31
4 Interrupt Data Transfer	Interrupt writing of display data	0	0	1	1	1	0	0	0	38
5 Clear Display Data	Clear the Display Data RAM and the Data Pointer	0	0	1	0	0	0	0	0	20
6 Clear Blinking Data	Clear the Blinking Data RAM and the Data Pointer	0	0	0	0	0	0	0	0	00
7 Load Data Pointer	Load Data Pointer with 5 Bits of Immediate Data	1	1	1	D_4	D_3	D_2	D_1	D_0	E0-FF
8 Write Display Data	Write 4 Bits of Immediate Data to the Display Data Location addressed by the Data Pointer Increment Data Pointer	1	1	0	1	D_3	D_2	D_1	D_0	D0-DF
9 Write Blinking Data	Write 4 Bits of Immediate Data to the Blinking Data Location addressed by the Data Pointer Increment Data Pointer	1	1	0	0	D_3	D_2	D_1	D_0	C0-CF
10 Enable Display	Start Automatic LCD Controller Hardware	0	0	0	1	0	0	0	1	11
11 Disable Display	Stop Automatic LCD Controller Hardware	0	0	0	1	0	0	0	0	10
12 Enable Blinking	Start the Blinking Operation at the Frequency Specified by 1 Bit of Immediate Data	0	0	0	1	1	0	1	D_0	1A-1B
13 Disable Blinking	Stop Blinking Operation	0	0	0	1	1	0	0	0	18
14 Enable Segment Decoder	Select 8 Segment Numeric or 15 Segment Alphanumeric Decoder Addressing	0	0	0	1	0	1	0	1	15
15 Disable Segment Decoder	Stop Segment Decoder Addressing Return to individual segment addressing	0	0	0	1	0	1	0	0	14
16 OR Display Data	Perform a Logical OR between the Display Data addressed by the Data Pointer and 4 Bits of Immediate Data Write Result to same Display Data Location Increment Data Pointer	1	0	1	1	D_3	D_2	D_1	D_0	B0-BF
17 AND Display Data	Perform a Logical AND between the Display Data addressed by the Data Pointer and 4 Bits of Immediate Data Write Result to same Display Data Location Increment Data Pointer	1	0	0	1	D_3	D_2	D_1	D_0	90-9F
18 OR Blinking Data	Perform a Logical OR between Blinking Data addressed by the Data Pointer and 4 Bits of Immediate Data Write Result to same Blinking Data Location Increment Data Pointer	1	0	1	0	D_3	D_2	D_1	D_0	A0-AF
19 AND Blinking Data	Perform a Logical AND between Blinking Data addressed by the Data Pointer and 4 Bits of Immediate Data Write Result to same Location Increment Data Pointer	1	0	0	0	D_3	D_2	D_1	D_0	80-8F

Absolute Maximum Ratings*

Supply Voltage	−0.3~+7.0V
Input Voltage	−0.3~V_{DD} + 0.3V
Output Voltage	−0.3~V_{DD} + 0.3V
Operating Temperature	−40~+85°C
Storage Temperature	−40~+125°C

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC Electrical Characteristics

D.C. Characteristics (T_a = −10~+70°C, V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input High Voltage	V_{IH}		0.7V_{DD}		V_{DD}	V
Input Low Voltage	V_{IL}		0		0.3V_{DD}	V
Output High Voltage	V_{OH}	$\overline{SYNC}$, $\overline{BUSY}$, I_{OH} = −10μA	V_{DD}−0.5			V
Output Low Voltage	V_{OL1}	$\overline{BUSY}$, I_{OL} = 100μA			0.5	V
	V_{OL2}	$\overline{SYNC}$, I_{OL} = 900μA			1.0	V
Output Short Circuit Current	I_{OS}	$\overline{SYNC}$, V_O = 1V			−300	μA
Input Leakage High	I_{LIH}	V_I = 5.5V			2	μA
Input Leakage Low	I_{LIL}	V_I = 0V			−2	μA
Output Leakage High	I_{LOH}	V_O = V_{DD}			2	μA
Output Leakage Low	I_{LOL}	V_O = 0V			−2	μA
Common Output Impedance	R_{COM}	COM0-COM3 : $V_{DD} \geq V_{LCD}$		5	7	KΩ
Segment Output Impedance	R_{SEG}	S0-S31 : $V_{DD} \geq V_{LCD}$		7	14	KΩ
Supply Current	I_{DD}	CL1: External Clock, f_C = 200KHz		100	250	μA

AC Characteristics

A.C. Characteristics (T_a = −10~+70°C, V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Frequency	f_C		50		200	KHz
Oscillation Frequency	f_{OSC}	R = 180KΩ ± 5%	85	130	175	KHz
Clock Pulse Width High	t_{WHC}	CL1: External Clock	2		16	μs
Clock Pulse Width Low	t_{WLC}	CL1: External Clock	2		16	μs
$\overline{SCK}$ Cycle	t_{CYK}		1			μs
$\overline{SCK}$ Pulse Width High	t_{WHK}		400			ns
$\overline{SCK}$ Pulse Width Low	t_{WLK}		400			ns
$\overline{BUSY}$ ↑ ~ $\overline{SCK}$ ↓ Hold Time	t_{HBK}		0			ns
SI Setup Time to $\overline{SCK}$ ↑	t_{SIK}		250			ns
SI Hold Time after $\overline{SCK}$ ↑	t_{HKI}		200			ns
8th SCK ↑ ~ $\overline{BUSY}$ ↓ Delay Time	t_{DKB}	C_L = 50pF			3	μs
$\overline{CS}$ ↓ ~ $\overline{BUSY}$ ↓ Delay Time	t_{DCB}	C_L = 50pF			1.5	μs
C/$\overline{D}$ Setup Time to 8th $\overline{SCK}$ ↑	t_{SDK}		9			μs
C/$\overline{D}$ Hold Time after 8th $\overline{SCK}$ ↑	t_{HKD}		1			μs
$\overline{CS}$ Hold Time after 8th $\overline{SCK}$ ↑	t_{HKC}		1			μs
$\overline{CS}$ Pulse Width High	t_{WCH}		(2)			μs
$\overline{CS}$ Pulse Width Low	t_{WLC}		(2)			μs
$\overline{SYNC}$ Load Capacitance	C_{LSY}	t_{CYC} = 5μs			50	pF

Notes (1) Applies to static and 1/2 and 1/3 multiplexed drive
(2) 8/f_C

AC Characteristics

A.C. Characteristics (T_a = 0~+70°C, V_{DD} = 2.7V~5.5V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Frequency	f_C		50		140	KHz
Oscillation Frequency	f_{OSC}	R = 180KΩ ± 5%, V_{DD} = 3V ± 10%	50	40	140	KHz
Clock Pulse Width High	t_{WHC}	CL1: External Clock	3		18	μs
Clock Pulse Width Low	t_{WLC}	CL1: External Clock	3		18	μs
$\overline{SCK}$ Cycle	t_{CYK}		4			μs
$\overline{SCK}$ Pulse Width High	t_{WHK}		1.8			μs
$\overline{SCK}$ Pulse Width Low	t_{WLK}		1.8			μs
$\overline{BUSY}$ ↑ ~ $\overline{SCK}$ ↓ Hold Time	t_{HBK}		0			ns
SI Setup Time to $\overline{SCK}$ ↑	t_{SIK}		1			μs
SI Hold Time after $\overline{SCK}$ ↑	t_{HKI}		1			μs
8th SCK ↑ ~ $\overline{BUSY}$ ↓ Delay Time	t_{DKB}	C_L = 50pF			5	μs
$\overline{CS}$ ↓ ~ $\overline{BUSY}$ ↓ Delay Time	t_{DCB}	C_L = 50pF			5	μs
C/$\overline{D}$ Setup Time to 8th $\overline{SCK}$ ↑	t_{SDK}		18			μs
C/$\overline{D}$ Hold Time after 8th $\overline{SCK}$ ↑	t_{HKD}		1			μs
$\overline{CS}$ Hold Time after 8th $\overline{SCK}$ ↑	t_{HKC}		1			μs
$\overline{CS}$ Pulse Width High	t_{WCH}		(2)			μs
$\overline{CS}$ Pulse Width Low	t_{WLC}		(2)			μs
$\overline{SYNC}$ Load Capacitance	C_{LSY}	t_{CYC} = 5μs			50	pF

Notes (1) Applies to static and 1/3 multiplexed drive
(2) 8/f_C

DC Electrical Characteristics for LCD

2.7 ≤ V_{LCD} ≤ V_{DD}

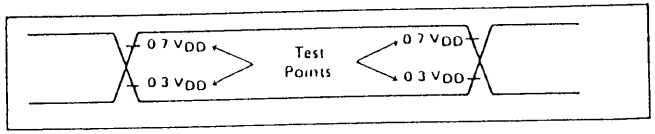
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
Backplane Drive Output Impedance	R_{COM}		2		kΩ	COM_0 - COM_3, Display Bias = 1/3 or Static
					kΩ	COM_0 - COM_3 Display Bias = 1/2
Segment Drive Output Impedance	R_{SEG}		11		kΩ	S_0 - S_{31}

Capacitance

Capacitance (T_a = 25°C, V_{DD} = 0V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Capacitance	C_{IN}		f_C = 1MHz, Unmeasured pins returned to 0V			10	pF
Output Capacitance	C_{OUT1}	Except $\overline{BUSY}$				20	pF
Output Capacitance	C_{OUT2}	$\overline{BUSY}$				15	pF
I/O Capacitance	C_{IO}	$\overline{SYNC}$				15	pF
Clock Capacitance	C_C	CL1				30	pF

A.C. Timing Measurement Voltage



EXTENDED TEMPERATURE RANGE (−40 to +85 °C)

DC Electrical Characteristics

D C Characteristics (T_a = −40 to +85 °C V_{DD} = 5V ± 10%

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input High Voltage	V_{IH1}	Except $\overline{SCK}$	0.7V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{SCK}$	0.75V_{DD}		V_{DD}	V
Input Low Voltage	V_{IL1}	Except $\overline{SCK}$	0		0.3V_{DD}	V
	V_{IL2}	$\overline{SCK}$	0		0.25V_{DD}	V
Output High Voltage	V_{OH}	$\overline{SYNC}$ $\overline{BUSY}$ I_{OH} = −2μA	V_{DD} −0.5*			V
Output Low Voltage	V_{OL1}	BUSY I_{OL} = 100μA			0.5	V
	V_{OL2}	$\overline{SYNC}$ I_{OL} = 100μA			0.5	V
Output Short Circuit Current	I_{OS}	$\overline{SYNC}$ V_O = 0.5V (1)			−350	μA
Input Leakage High	I_{LIH}	V_I = 5.5V			2	μA
Input Leakage Low	I_{LIL}	V_I = 0V			−2	μA
Output Leakage High	I_{LOH}	V_O = V_{DD}			2	μA
Output Leakage Low	I_{LOL}	V_O = 0V			−2	μA
Common Output	R_{COM}	COM 0 COM 3 $\pm$0.1V_{DD} ≥ V_{LCD}		5	8	KΩ
Segment Output Impedance	R_{SEG}	SO-S31 $\pm$0.1V_{DD} ≥ V_{LCD}		7	20	KΩ
Supply Current	I_{DD}	CL1: External Clock V_{DD} = 3V ± 10% f_C = 140KHz		90	250	μA

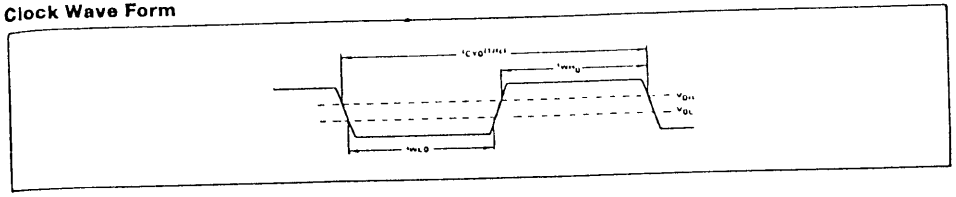
AC Characteristics

A C Characteristics (T_a = −40 to +85 °C V_{DD} = 5V ± 10%

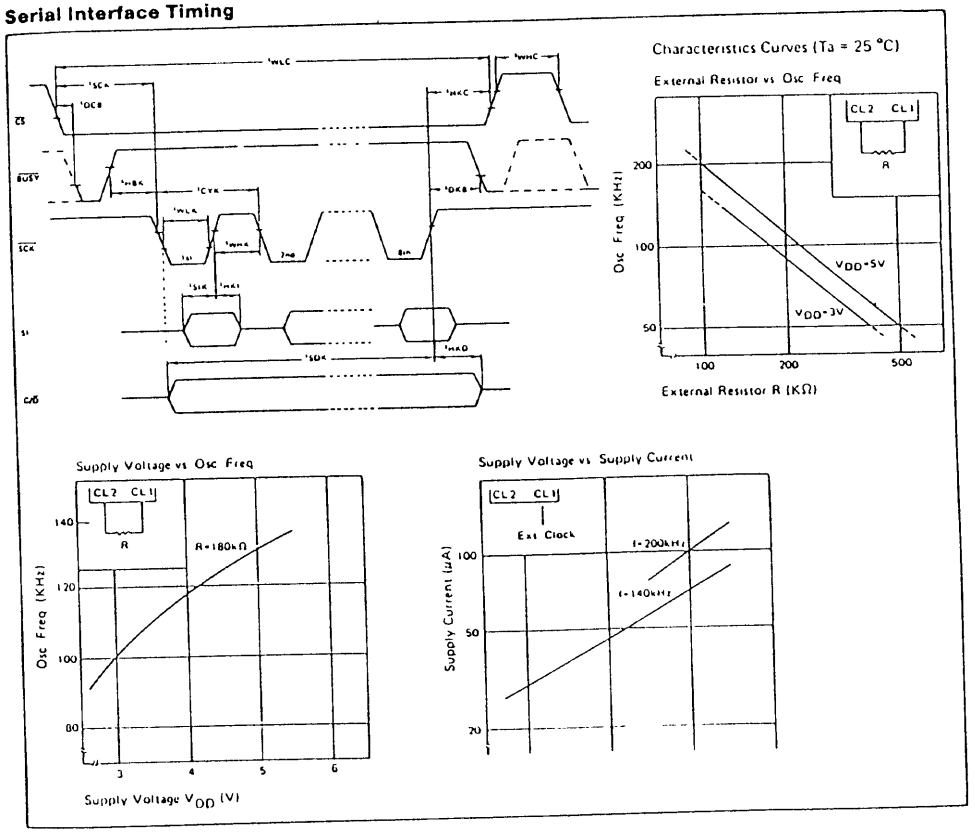
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Frequency	f_C		75		180	KHz
Oscillation Frequency	f_{OSC}	R = 180KΩ ± 5%	80*	130	180	KHz
Clock Pulse Width High	t_{WHC}	CL1: External Clock	2		10	μs
Clock Pulse Width Low	t_{WLC}	CL1: External Clock	2		10	μs
$\overline{SCK}$ Cycle	t_{CYK}		12			μs
$\overline{SCK}$ Pulse Width High	t_{WHK}		500			ns
$\overline{SCK}$ Pulse Width Low	t_{WLK}		500			ns
$\overline{BUSY}$ ↑ − $\overline{SCK}$ ↓ Hold Time	t_{HBK}		0			ns
SI Setup Time to $\overline{SCK}$ ↑	t_{SIK}		100			ns
SI Hold Time after $\overline{SCK}$ ↑	t_{HKI}		200			ns
8th SCK ↑ − $\overline{BUSY}$ ↓ Delay Time	t_{DKB}	C_L = 50pF			3	μs
CS ↓ − $\overline{BUSY}$ ↓ Delay Time	t_{DCB}	C_L = 50 pf			1.5	μs
C/D Setup Time to 8th $\overline{SCK}$ ↑	t_{SDK}		9			μs
C/D Hold Time after 8th $\overline{SCK}$ ↑	t_{HKD}		1			μs
$\overline{CS}$ Hold Time after 8th SCK ↑	t_{HKC}		1			μs
$\overline{CS}$ Pulse Width High	t_{WCH}		(3)			μs
$\overline{CS}$ Pulse Width Low	t_{WLC}		(3)			μs
$\overline{SYNC}$ Load Capacitance	C_{LSY}	t_{CYC} < 5μs			50	pF

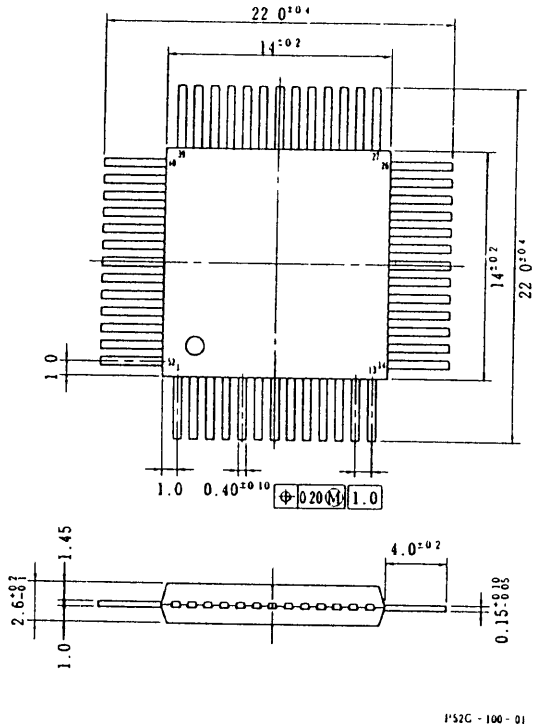
Notes (1) Output short circuit caused by conflict among $\overline{SYNC}$ outputs in multi chip configuration
(2) Applies to static 1/2 and 1/3 multiplexed drive
(3) 8/f_C

Clock Wave Form



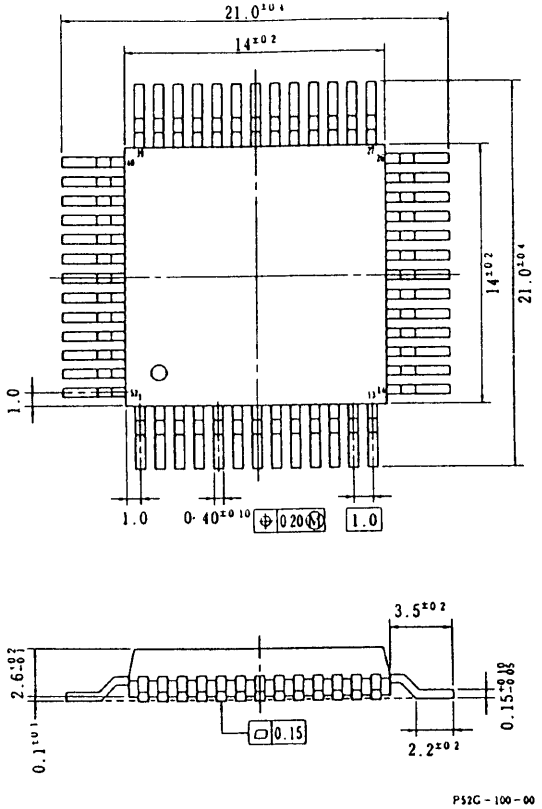
Serial Interface Timing





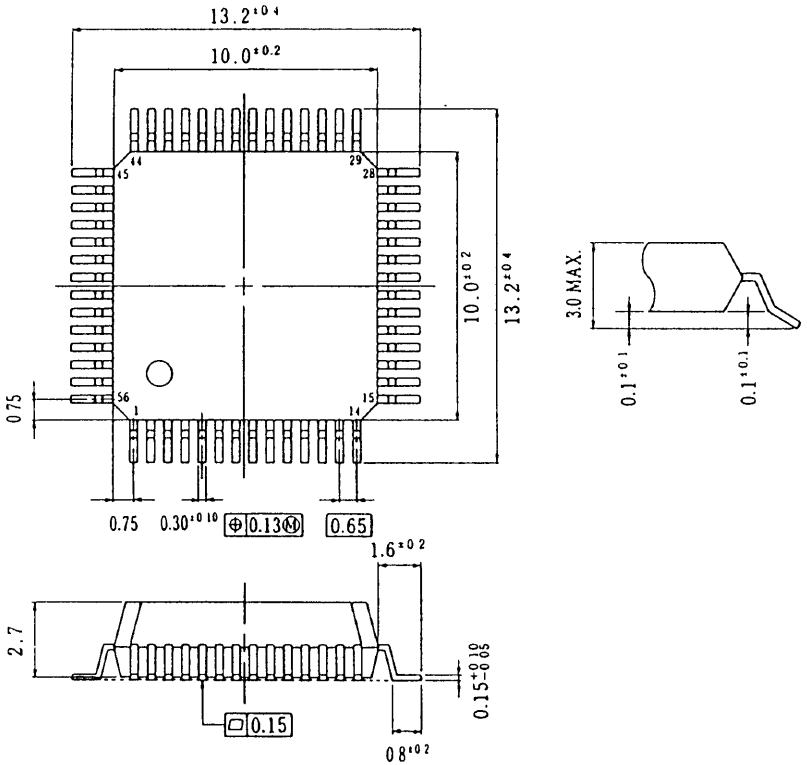
P52G-100-01

μPD7225G01



P52G-100-00

μPD7225G00



S56GB-65-3B7

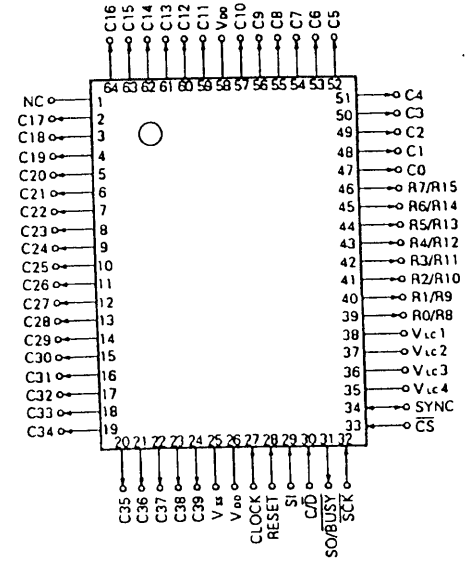
DESCRIPTION

μPD7227 is an LCD (Liquid Crystal Display) controller/driver that can be programmed by software. It can be interfaced with the CPU in a microcomputer application system, capable of directly driving LCD in 8 or 16 time-sharing dot matrix configuration. In addition, it incorporates a character generator capable of generating a specific pattern.

FEATURES

- LCD Direct Drive
  320 dots (8 time-sharings)
  640 dots × n (16 time-sharings): n chip configuration
- Displayed digits can be extended through the multi-chip configuration.
- Character generator (5 × 7)
  Alphanumeric characters: 36
  Signs: 28
- 8-bit Serial Input/Output
  (μPD7500 series, μCOM-43NA series, μCOM-87 serial interface compatible)
- 12 kinds of control commands
- CMOS
- Single power source

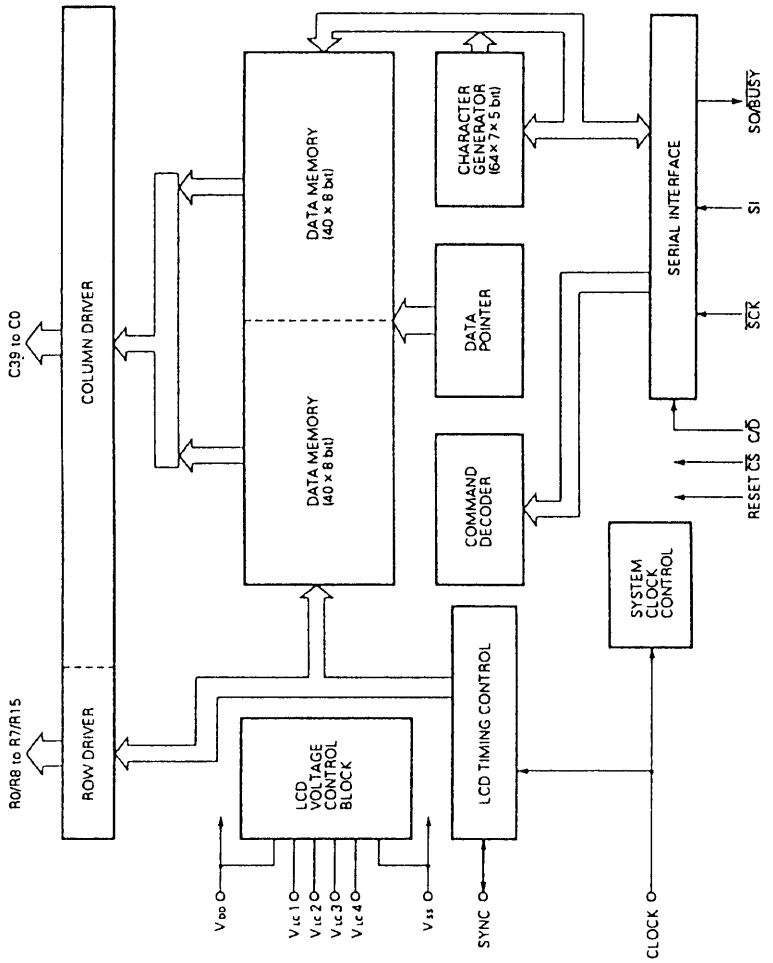
PIN CONFIGURATION (Top View)



ORDERING INFORMATION*

Part Number	Package	Quality Grade
μPD7227G-11	64-pin plastic QFP (Straight)	Standard
μPD7227G-12	64-pin plastic QFP (Bent leads)	Standard

BLOCK DIAGRAM



1. PIN FUNCTION

(1) SI (Serial Input) ..... Input

This pin inputs serial data (command/data) to μPD7227.

(2) SO/$\overline{\text{BUSY}}$ ..... Output

This pin can be used as the output pin of serial data (SO function) and also as the output pin of a $\overline{\text{BUSY}}$ signal to specify to enable/disable serial transfer ($\overline{\text{BUSY}}$ function). The switching of the SO function and the $\overline{\text{BUSY}}$ function is carried out based on the state of the C/$\overline{\text{D}}$ pin, only in the READ mode (set by an SRM command). Modes other than READ always result in the $\overline{\text{BUSY}}$ function.

High impedance is obtained while $\overline{\text{CS}}$ is at the high level.

The SO function is selected when the C/$\overline{\text{D}}$ pin is at a low level in READ mode, and it is used when the contents of data memory are output.

The $\overline{\text{BUSY}}$ function is used when the CPU side checks if the input/output of the serial data can be made by μPD7227

(3) $\overline{\text{SCK}}$ ..... Input

This pin inputs a serial clock that shifts the contents of a serial register and latches a signal from an SI pin. It carries out the input/output operation of serial data, synchronizing with the input serial clock.

While $\overline{\text{CS}}$ is at a high level, the serial clock is not accepted. It is ignored even if it is input.

(4) C/$\overline{\text{D}}$ ..... Input

This pin specifies the command/data of serial data input from the SI pin. In the READ mode, the SO/$\overline{\text{BUSY}}$ pin can provide the $\overline{\text{BUSY}}$ function by setting the C/$\overline{\text{D}}$ pin at a high level and the SO/$\overline{\text{BUSY}}$ pin can provide the SO function by setting the C/$\overline{\text{D}}$ pin at a low level.

Operation Mode	C/$\overline{\text{D}}$	SO/$\overline{\text{BUSY}}$	SI
WRITE mode AND mode OR mode Character mode	0	$\overline{\text{BUSY}}$	Data input
	1	$\overline{\text{BUSY}}$	Command input
READ mode	0	SO	Invalid
	1	$\overline{\text{BUSY}}$	Command input

(5) SYNC (Synchronous) . . . Input/Output

The SYNC pin is the input/output pin, which is wired-or-connected when the number of displayed digits is increased in multi-chip configuration. In the multi-chip configuration (where the common row drive signal is used), this pin uses the SYNC pin of the master chip as the output mode and the SYNC pin of the slave chip as the input mode, with either chip as the master. Input and output are specified by the SMM command.

The master chip outputs the SYNC signal to each frame. Other slave chips fetch this SYNC signal to the LCD timing control, matching the AC drive signal and the frame cycle to the master chip.

If the SYNC pin is set to output, μPD7227 outputs the SYNC signal in the timing shown in Fig. 1 and Fig. 2.

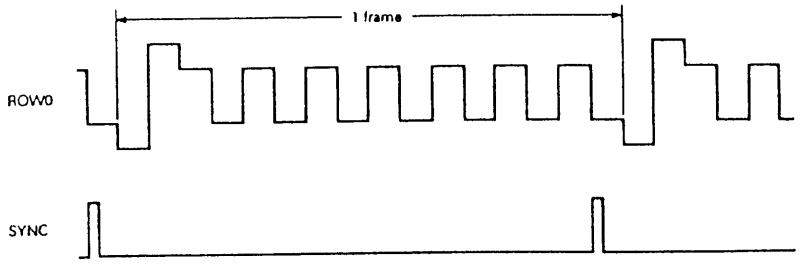


Fig. 1 SYNC Signal at 8 Time-Sharings

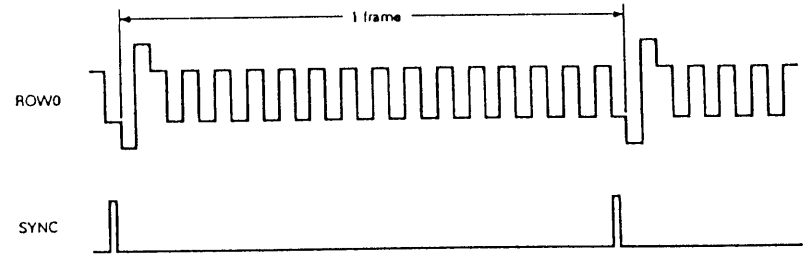


Fig. 2 SYNC Signal at 16 Time-Sharings

(6) $\overline{CS}$ (Chip select) ..... Input
This is the ACTIVE LOW chip select input pin. Setting this pin at a low level makes it possible to transmit/receive data through a serial transfer with a microcomputer.

(7) C0 to C39 (Column) ..... Output
This is the output pin of a column drive signal.

(8) R0/R8 to R7/R15 (Row) ..... Output
This is the output pin of row drive signals ROW0 to ROW7 and ROW8 to ROW15. The SMM command selects ROW0 to ROW7 and ROW8 to ROW15.

(9) V_{LC1} to V_{LC4} (LCD Drive Voltage) ..... Input
This is a LCD drive reference voltage input pin for generating LCD drive signals (row/column drive signals).

(10) RESET (Reset) ..... Input
This is an ACTIVE HIGH reset input pin.

(11) CLOCK (Clock) ..... Input
This pin is used to input a clock directly from the outside. For the multi-chip configuration, supply the CLOCK pin of each μPD7227 with a clock of the same phase at the same frequency.

(12) V_{DD}
This is a positive power supply pin for system.

(13) Vss
This is a GND for system.

2 COMMAND

Input a command after setting the C/$\overline{D}$ pin at a high level (command input specified) and confirming that the $\overline{BUSY}$ signal reaches the high level. Then, fetch only from the SI pin, synchronizing one with the serial clock to be input to the $\overline{SCK}$ pin. If all the data is stored in a serial register, decode the contents (command) with a command decoder and start the processing according to the command.

2.1 LCD DISPLAY MODE COMMAND

i) SFF (Set Frame Frequency)

0	0	0	1	0	F_2	F_1	F_0

The frame frequency is set. The frame frequency assumes the value obtained by dividing the clock input from the CLOCK pin with the division ratio specified by F_2 to F_0 of the command.

F_2	F_1	F_0	Frame Frequency
0	0	0	$f_{CL}/2^{14}$
0	0	1	$f_{CL}/2^{13}$
0	1	0	$f_{CL}/2^{12}$
0	1	1	$f_{CL}/2^{11}$
1	0	0	$f_{CL}/2^{10}$

Remarks: f_{CL} = clock frequency

ii) SMM (Set Multiplexing Mode)

0	0	0	1	1	M_2	M_1	M_0

This command carries out selection of the number of time-sharings, the low driver function, the bank of data memory (only if 8 time-sharings are specified).

M_2	M_1	M_0	Number of Time Sharings	ROW0-ROW7/ROW8 ROW15 Function Selection	SYNC Pin	Specification of the Data Memory Bank
0	0	0	8	ROW0 to ROW7	Input	Bank 0
0	0	1		ROW0 to ROW7	Input	Bank 1
0	1	0		ROW0 to ROW7	Output	Bank 0
0	1	1		ROW0 to ROW7	Output	Bank 1
1	0	0	16	ROW8 to ROW15	Input	Bank 0, 1
1	0	1		ROW8 to ROW15	Input	Bank 0, 1
1	1	0		ROW0 to ROW7	Output	Bank 0, 1
1	1	1		ROW0 to ROW7	Output	Bank 0, 1

iii) DISP OFF (Display Off)

0	0	0	0	1	0	0	0

Irrespective of display data, this command sets the relation between the row signal and the column signal at the non-selective level, putting out the display.

iv) DISP ON (Display On)

0	0	0	0	1	0	0	1

This command operates the display, according to the display data.

2.2 DATA PROCESSING MODE SETTING COMMAND

There are five commands, SRM, SWM, SANDM, SORM and SCM, which set each mode (such as READ/WRITE/AND/OR/CHARACTER), to control the data input/output operation. These commands specify MODIFY operation of the data pointer by I_1 and I_0 of each command. This MODIFY operation is carried out only at the time of data input/output, and it is not carried out at the time of command input.

I_1	I_0	Data Pointer Operation
0	0	"1" is incremented every time data is input/output
0	1	"1" is decremented every time data is input/output.
1	0	Inhibition
1	1	Hold the same address after data is input/output

For example, when I_1, I_0 = 00 is specified in the SWM command, the data pointer is incremented by (+1) every time data is written. This means that continuous data writing after execution of the SWM command causes the sequential data to be written from data memory shown by the contents of the data pointer.

Meanwhile, the mode set by the input/output command is held until other input/output command are executed.

i) SRM (Set Read Mode)

0	1	1	0	0	0	I_1	I_2

This command sets the READ mode and at the same time specifies the MODIFY operation of the data pointer every time data is read out by I_1, I_0 of the command. It also loads the contents of memory addressed by the present data pointer into the serial register.

ii) SWM (Set Write Mode)

0	1	1	0	0	1	I_1	I_0

This command sets the WRITE mode and at the same time specifies the MODIFY operation of the data pointer every time data is written by I_1, I_0 of the command.

In case of the WRITE mode, serial data stored in the serial register from the external is written directly into data memory.

iii) SANDM (Set AND Mode)

0	1	1	0	1	1	I_1	I_0

This command sets the AND mode and at the same time specifies the MODIFY operation of the data pointer every time data is written by I_1, I_0 of the command.

In the AND mode, serial data stored in the serial register from the outside is ANDed with the contents of data memory addressed by the data pointer, and the result is written into data memory.

iv) SORM (Set OR Mode)

0	1	1	0	1	0	I_1	I_0

This command sets the OR mode and at the same time specifies the MODIFY operation of the data pointer every time data is written by I_1, I_0 of the command.

In the OR mode, serial data stored in the serial register from the outside is ORed with the contents of data memory addressed by the data pointer, and the result is written into data memory.

v) SCM (Set Character Mode)

0	1	1	1	0	0	1	0

The character mode is set

In the character mode, serial data stored in the serial register from the outside is written into data memory through the character generator. In the character mode, every time data (5 × 7 bits) for one character is written into data memory, the data pointer is incremented by (+5)

2.3 MEMORY BIT OPERATION COMMAND

i) BSET (Bit Set)

0	1	0	B_2	B_1	B_0	J_1	J_0

This command sets (1) bit set by B_2 to B_0 of data memory addressed by the data pointer. After setting, the data pointer is modified by the specification of J_1 and J_0. In this case, the data pointer is modified by the specification of J_1 and J_0 only when the BSET command and BRESET command are executed. After the data pointer is modified by J_1 and J_0 when the BSET command is executed, the processing returns to the modify specification (I_1, I_0) by means of input/output commands (SRM, SWM, SANDM, SORM).

For example, suppose that the reading up to the 15th address was made after specifying I_1, I_0 = 00 (Auto Increment) by the SRM command. (As the data pointer is incremented after the data of the 15th address was read, the 16th address is shown.) If the BSET command is executed as J_1, J_0 = 01 (Auto Decrement), the specified bit of the 16th address is set and the data pointer is decremented by (-1), showing the 15th address. Then, if the data is read later, the data of the 15th address is read, and the data pointer is incremented by (+1), showing the 16th address.

J_1	J_0	Data Pointer Operation
0	0	Increment of (+1)
0	1	Decrement of (-1)
1	0	Inhibition
1	1	The same address is held

ii) BRESET (Bit Reset)

0	0	1	B_2	B_1	B_0	J_1	J_0

This command resets (0) bit specified by B_2 to B_0 of data memory addressed by the data pointer. After being reset, the data pointer is modified by the specification of J_1 and J_0. Meanwhile, J_1 and J_0 codes are the same as those of the BSET command.

2.4 DATA POINTER SPECIFICATION COMMAND

LDPI (Load Data Pointer with Immediate data)

1	D_6	D_5	D_4	D_3	D_2	D_1	D_0

This command sets immediate data D_6 to D_0 to the data pointer.

3. INPUT/OUTPUT OF DATA

3.1 INPUT OF DATA

i) WRITE mode

The WRITE mode is set by the SWM command. Input serial data (data) after confirming that the $\overline{BUSY}$ signal output from the SO/$\overline{BUSY}$ pin has reached the high level. Then, supply the $\overline{SCK}$ pin with a serial clock and at the same time supply the SI pin with serial data at the MSB first by synchronizing it with a serial clock. μPD7227 synchronizes serial data input from the SI pin with the serial clock, fetching it into the serial register. When all serial data of the 8 bits are fetched into the serial register, μPD7227 writes the contents of the serial register directly into data memory addressed by the data pointer at the 8th rise of the serial clock. Then, the data pointer is modified by specification of I_1 and I_0. In this case, after μPD7227 fetches the serial data of 8 bits into the serial register, it reaches the $\overline{BUSY}$ state, outputting the $\overline{BUSY}$ signal (SO/$\overline{BUSY}$ = Low level) from the SO/$\overline{BUSY}$ pin. This $\overline{BUSY}$ signal is output while the stored serial data (data) is internally processed, and the input of serial data is inhibited during this period. Therefore, input the next serial data after this $\overline{BUSY}$ signal is canceled (SO/$\overline{BUSY}$ = High level)

ii) AND mode

The serial data stored in the serial register is ANDed with data memory addressed at the data pointer, and the result is written into data memory. All other operations are the same as those of the WRITE mode.

iii) OR mode

The serial data stored in the serial register is ORed with data memory addressed at the data pointer, and the result is written into data memory. All other operations are the same as those of the WRITE mode.

iv) Character mode

The serial data (data) stored in the serial register is decoded through the character generator, and decode data (5 × 7 bits) is written into data memory. In the character mode, the data pointer is incremented by (+5) every time decode data for one character is written into data memory. The input operation of serial data is the same as that of the WRITE mode.

3.2 OUTPUT OF DATA

i) READ mode

To read out the contents of the serial register, first set the C/$\overline{D}$ pin at the high level. Then, provide the SO/$\overline{BUSY}$ pin with the $\overline{BUSY}$ function, and confirm that the $\overline{BUSY}$ signal has reached the high level. If the $\overline{BUSY}$ signal has reached the high level, set the C/$\overline{D}$ pin at the low level. Then, provide the SO/$\overline{BUSY}$ pin with the SO function, and the output of the serial data is ready. Then, synchronize serial data with the serial clock, and output serial data at the MBS first from the SO/$\overline{BUSY}$ (SO function) pin. After outputting the 8-bit data from the SO/$\overline{BUSY}$ pin, according to the serial clock of 8 clocks, load into the serial register the contents of the data memory shown by the data pointer at the rise of the 8th serial clock. μPD7227 reaches the $\overline{BUSY}$ status during this period. Therefore, to next read out the contents of the serial register, bring the C/$\overline{D}$ pin to the high level again, providing the SO/$\overline{BUSY}$ pin with the $\overline{BUSY}$ function, and confirm that the $\overline{BUSY}$ signal reaches the high level (the cancellation of the $\overline{BUSY}$ status).

ii) Command input in the READ mode

The input of SWM, SANDM, SORM and SCM commands causes these commands to be modified to each mode. When other commands are input, after these commands are processed, the contents of the data memory specified by the data pointer are stored in the serial register, and the data pointer is modified according to I_1 and I_0 of the SRM command. When BSET and BRESET commands are input, however, after these commands are executed, the contents of the data memory addressed by the contents of the data pointer modified by the specification of J_1 and J_0 are stored in the serial register. As μPD7227 always modifies the data pointer according to I_1 and I_0 (J_1, J_0) after the processing (writing or reading of data) is executed, caution must be taken to the operation of the data pointer. For example, if the contents of the n-address are stored in the serial register after SRM (I_1, I_0 = 0, 0) was set, the data pointer shows the (n+1) address. Therefore, if the DISP OFF command is input at this stage, the processing returns to the READ mode, and the contents of the (n+1) address are stored in the serial register. In this case, caution must be taken, for the contents of the n address are not output from the SO/$\overline{BUSY}$ pin. (As the DISP OFF command is input at the high level C/$\overline{D}$, the SO/$\overline{BUSY}$ pin has to be the $\overline{BUSY}$ function.)

4. INTERNAL BLOCK FUNCTION

4.1 SERIAL INTERFACE

The serial interface consists of the 8-bit serial register and the 3-bit SCK counter, inputting the operation command and inputting/outputting the data in 8-bit units.

i) Input of the serial data

The serial data is input to the serial interface by synchronizing it with the serial clock to the $\overline{SCK}$ pin.

The serial data is fetched from the SI pin in one-bit units, one by one, from MSB of the data at the rise of the serial clock, stored in LSB (bit 0) of the serial register of μPD7227.

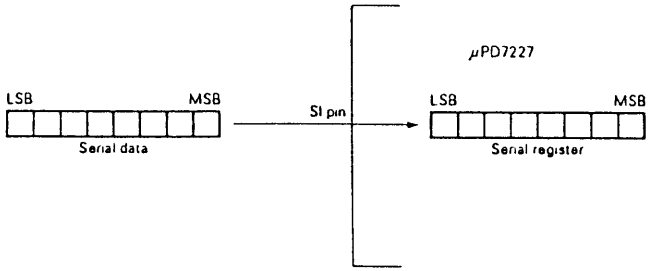


Fig. 3 Serial Data Configuration

The stored serial data is shifted by the fall of the following serial clock. The SCK counter, which is counted up by the rise of the serial clock, generates the overflow that shows that the input of 1 byte of serial data has ended at the rise of the 8th serial clock. In this case, the serial interface fetches the contents of the C/$\overline{D}$ pin by synchronizing with the 8th serial clock. Then, it checks whether the contents of the serial data fetched to the serial register is the command or the data. If the content is the command (C/$\overline{D}$ = high level), the contents of the serial register are fed to the command decoder. If the content is the data (C/$\overline{D}$ = low level), the data is processed according to each mode of WRITE/AND/OR/CHARACTER.

Transfer of the 8-bit serial data (i.e. supply of the 8th serial clock) results in the output of the $\overline{BUSY}$ signal (SO/$\overline{BUSY}$ = low level). This $\overline{BUSY}$ signal is output while serial data input previously by μPD7227 internally are processed, and during this period, input of serial data is inhibited. Therefore, input of the next serial data must be made after this $\overline{BUSY}$ signal is canceled (SO/$\overline{BUSY}$ = high level).

ii) Output of the serial data

Output of data from the serial register is made by supplying the $\overline{SCK}$ pin with the serial clock in the same manner as in the input. The contents of the serial register are shifted at the fall of the serial clock, output from the SO/$\overline{BUSY}$ pin one by one starting with MSB. The SCK counter is counted up at the rise of the serial clock. As soon as the output of 1 byte ends at the rise of the 8th serial clock (8-bit data), the contents of data memory addressed by the data pointer are loaded in the serial register. When the serial clock is supplied, the contents of the serial register are output from the (C/$\overline{D}$ = low level) SO/$\overline{BUSY}$ pin. In this case, after output of 8-bit serial data ends, SCK input is inhibited until the next data is stored in the serial register, and the $\overline{BUSY}$ signal (SO/$\overline{BUSY}$ = low level) is output (C/$\overline{D}$ = high level). Therefore, to output data from the serial register, set the C/$\overline{D}$ pin at the high level beforehand, and check the SO/$\overline{BUSY}$ pin to confirm that the $\overline{BUSY}$ signal (SO/$\overline{BUSY}$ = high level) has been canceled.

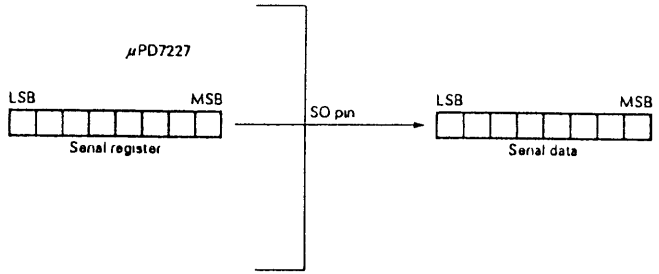


Fig. 4 Serial Data Configuration

4.2 COMMAND DECODER

After fetching and decoding the contents (or commands) of the serial register, μPD7227 is controlled in accordance with each command.

4.3 CHARACTER GENERATOR

After executing the SCM command (in case of the character mode), the character generator becomes usable, generating 36 kinds of alphanumeric characters and 28 sign patterns due to 7 × 5 dot matrix, corresponding to the input data.

In the character mode, data input to a serial register as C/$\overline{D}$ = low level is written into data memory after being converted to decode data fetched to the character generator. In this case, as the decode data is written into data memory in 7 bits × 5 configuration, bit 7 of data memory each address holds the previous data without being affected by decode data writing.

The data pointer is counted up by (+5) each time one character is written in the data memory.

Shown bellow are the LCD configuration (in the character mode) to be used when a character generator is used and the correspondence between the serial data and the display pattern.

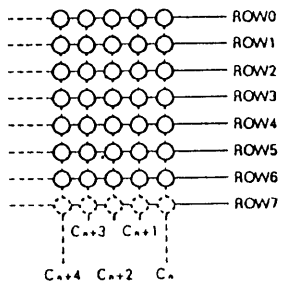


Fig. 5 LCD Configuration in 8 Time-Sharings

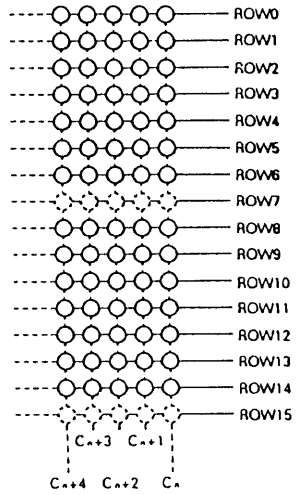
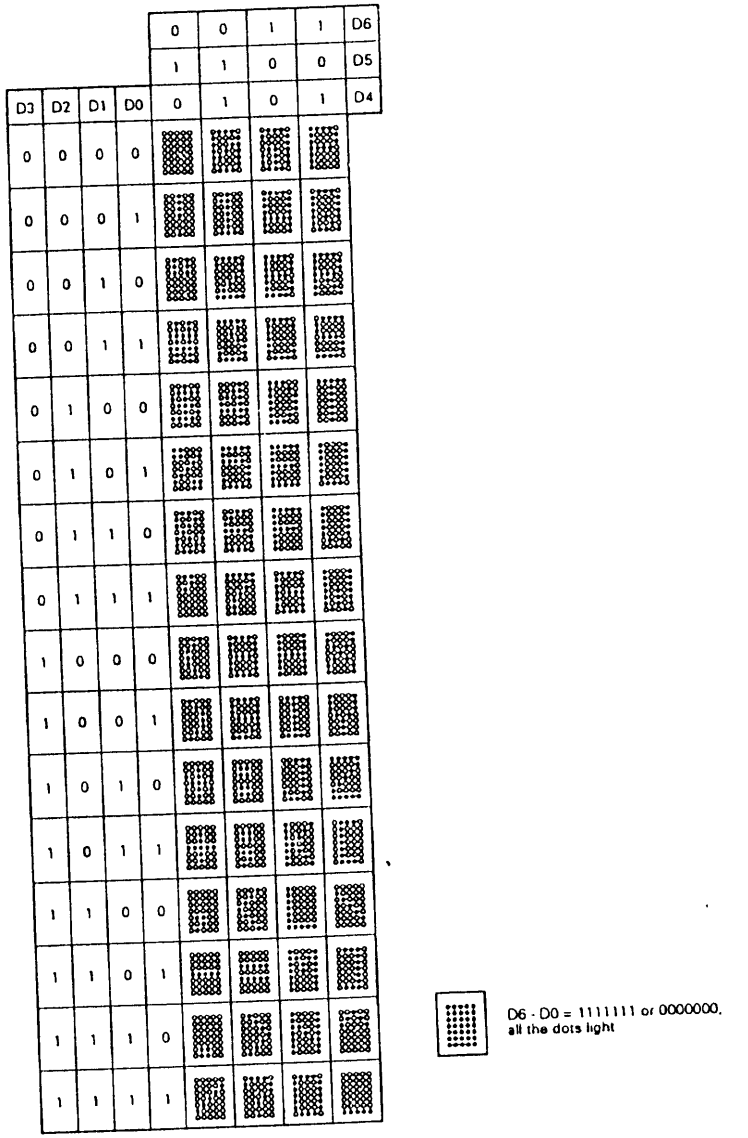


Fig. 6 LCD Configuration in 16 Time-Sharings

Remarks: Sections marked ◌ indicate the contents of bit 7 of data memory irrespective of the display of characters, so they can be used as a cursor or an indicator.



				0	0	1	1	D6
				1	1	0	0	D5
D3	D2	D1	D0	0	1	0	1	D4
0	0	0	0					
0	0	0	1					
0	0	1	0					
0	0	1	1					
0	1	0	0					
0	1	0	1					
0	1	1	0					
0	1	1	1					
1	0	0	0					
1	0	0	1					
1	0	1	0					
1	0	1	1					
1	1	0	0					
1	1	0	1					
1	1	1	0					
1	1	1	1					

Fig. 7 Correspondence between Serial Data and Display in Character Mode

4.4 DATA POINTER

A data pointer, which consists of a 6-bit binary counter and a 1-bit bank flag, specifies the bank and address of the data memory.

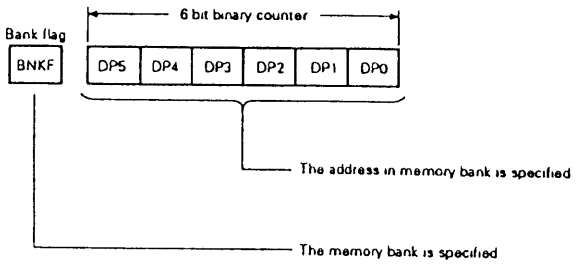


Fig. 8 Data Pointer Configuration

A bank flag specifies bank 0 (40 × 8 bits) and bank 1 (40 × 8 bits). It is set or reset by D_6 of the LDPI command. $D_6 = 0$ specifies the bank 0 and $D_6 = 1$ specifies the bank 1.

A 6-bit binary counter specifies the address in each bank, and it is set by D_5 to D_0 of the LDPI commands. The address specifying areas of each bank are 0 to 39 addresses. Although the binary counter can assume the values of 40 to 63 (for example, 63, when decremented from 0) by setting the immediate data or by auto increment/decrement. There is not data memory corresponding to these values, and no action is taken. When the serial data is input/output, the contents of the 6-bit binary counter are modified as follows.

i) At the time of data input/output

In each mode, READ/WRITE/AND/OR, the data pointer is modified by the specification of I_1 and I_0 of the commands (SRM, SWM, SANDM, SORM) that set the mode. This modification is made each time data is input or output.

In the character mode, the data pointer is counted up by (+5) each time 8-bit data is input.

ii) At the time of command input (execution)

The data pointer is modified according to J_1 and J_0 of BSET and BRESET commands, only when these commands are executed, and then it returns to I_1 and I_0 of the commands in the state before they were executed. Execution of the SRM command causes the READ mode to be set, the contents of the data memory to be loaded to the serial register according to the data pointer, and the data pointer to be modified according to I_1 and I_0 of the SRM command. When commands other than BSET, BRESET, SRM and LDPI are executed, the data pointer is not modified.

4.5 DATA MEMORY

Data memory (40 × 8 bits × 2) is used to store data, divided into bank 0 and bank 1. Written in data memory are character generator output (character mode) and display data from a serial register (WRITE mode). It can also carry out AND operation (AND mode) with the serial register OR (OR mode) operation and specific bits setting (when the BSET command is executed)/ resetting (when the BRESET command is executed). In the READ mode, the contents of data memory are loaded into the serial register. The READ/WRITE operation of data memory is addressed by the data pointer. The data pointer also specifies bank 0 and bank 1.

The contents of data memory are separately read automatically in units of bits from the input/output operation of the serial register. After they are sent to a column driver and converted to a column drive signal, they are output from a column drive signal output pin. Since this operation is carried out automatically inside μPD7227, it does not affect the writing of data by means of serial transfer.

Regarding the relation between the column drive signal and the row drive signal, if the content of the bit read from data memory is 1, the corresponding LCD element reaches the selection level and lights. If the content is 0, the corresponding LCD element reaches the nonselection level and does not light.

i) Writing into data memory

As shown below, there are four modes and the bit set/reset operation for writing into data memory.

- WRITE mode

This mode is set by the SWM command. Data fetched in the serial register is written directly into the memory bank addressed by the data pointer.

- Character mode

This mode is selected by the SCM command. The data fetched in the serial register is written into the memory bank addressed by the data pointer through a character generator.

In the character mode, data is decoded in 7 bits × 5 bits (1 character) and written into data memory. Therefore, decode data of one character (character generator output) is written into data memory in 5 byte units. Meanwhile, the most significant bit (bit 7) of each address is not used in this mode and previous data is held even after decode data is written.

- AND mode

This mode is set by the SANDM command. The data fetched in the serial register is ANDed with the contents of the data memory addressed by the data pointer, and the result is written into data memory.

- OR mode

This mode is set by the SORM command. Data fetched in the serial register is ORed with the contents of data memory addressed by the data pointer, and the result is written into data memory.

- Bit set operation

This operation is carried out by the BSET command. Among the contents (8 bits) of data memory addressed by the data pointer, the bit specified by B_2 to B_0 of the command is set. This operation is canceled the moment the execution of the command ends, returning to the each mode (WRITE, CHARACTER, AND, OR, READ) before the command is executed.

- Bit reset operation

This operation is carried out by the BRESET command. Among the contents (8 bits) of data memory addressed by the data pointer, the bit specified by B_2 to B_0 of the command is reset. This operation is canceled the moment the command is executed, returning to the each mode (WRITE, CHARACTER, AND, OR, READ) before the command is executed.

ii) Read to a serial register

This mode is set by the SRM command. The contents of data memory addressed by the data pointer are loaded into the serial register.

iii) Read to a column driver

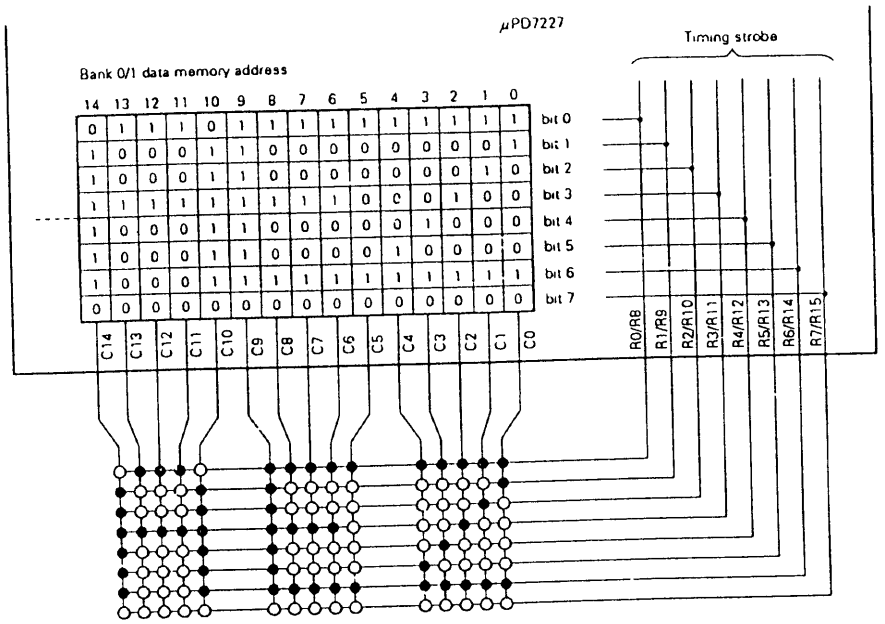
Display data for driving LCD is read from data memory. The display data is read in bit units. After the read display data is converted to the column drive signal by the column driver, the display data is output from the column drive signal output pin. In this case, the read of the display data is different depending on the number of time-sharings of the display.

- 8 time-sharings

In 8 time-sharing drive, the data memory contents of either bank 0 or bank 1 are displayed. (Specified by the SMM command.)

Display data is read one by one from the bit 0 of the data memory of the specified bank, synchronized with row drive signals. Then, the output display data is modified to column drive signals by the column driver, output from the column drive signal output pin.

Shown next are examples of the μPD7227 and LCD connection in 8 time-sharings and the correspondence between the contents of data memory and the display pattern.



Note: Display data is read for bank 0 or bank 1.

Fig. 9 8 Time-Sharings

- 16 time-sharings

In 16 time-sharings drive, bank 0 and bank 1 function as the data memory of 16 bits x 40. Display data is read one by one from bit 0 of each bank 0 address, synchronized with row drive signals.

Meanwhile, two or more μPD7227s are necessary to display LCD in 16 time-sharings. In fig. 10, R0/R8 to R7/R15 pins above the figure are used as ROW0 to ROW7 outputs, and ROW8 to ROW15 are supplied from a slave chip.

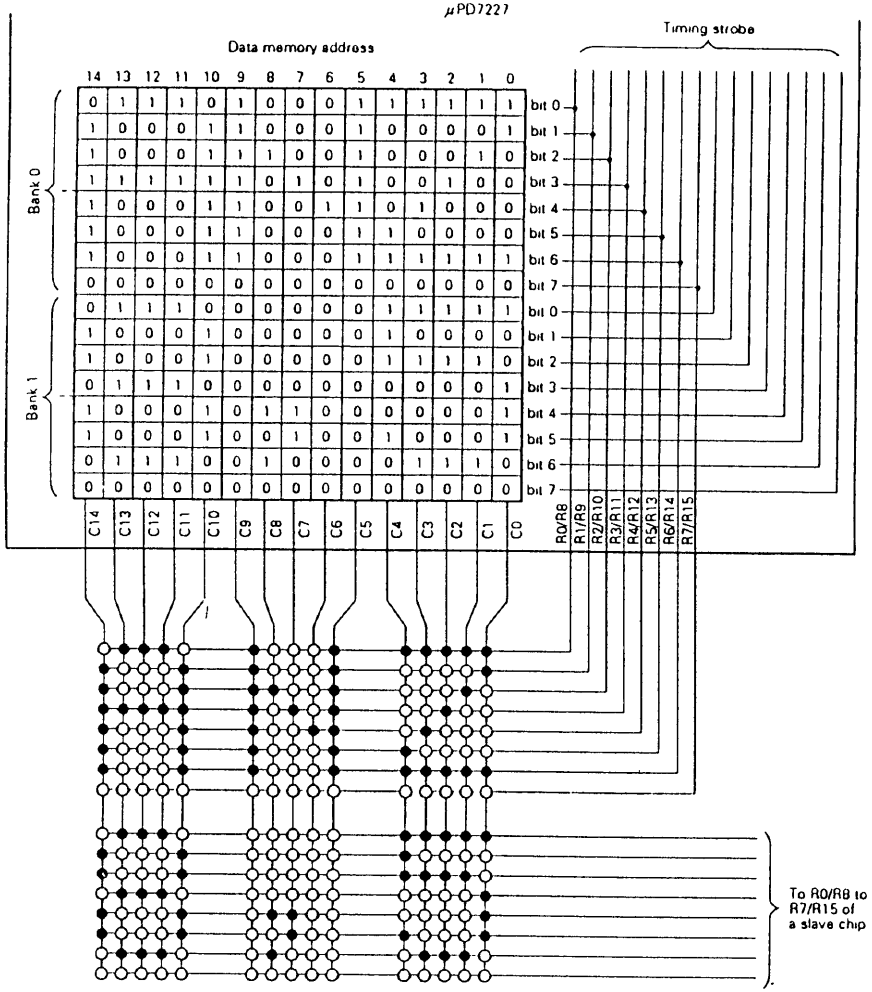


Fig 10 16 Time-Sharings

4.6 COLUMN DRIVER (C0 TO C39)

Display data read out from 0 to 39 addresses of data memory is fetched, and after the data is converted to a column drive signal, it is output from a column drive signal output pin. The column drive signal is determined by the LCD timing controller and the display data, based on the LCD drive reference voltage input from the LCD voltage control block. One AC column drive signal of the column drive signal contains 1-bit information.

4.7 ROW DRIVERS (R0/R8 TO R7/R15)

This driver has occurrence functions of row drive signals ROW0 to ROW7 and ROW8 to ROW15.

When M2 to M0 = 0 to 3 is executed by the SMM command, the row driver has the output function of ROW0 to ROW7 signals at 8 time-sharings, generating row drive signals ROW0 to ROW7 at 8 time-sharings drive timing input from the LCD timing controller, and outputs them from the row drive signal output pin.

Where M2 to M0 = 6, 7 is executed by the SMM command, the row driver has ROW0 to ROW7 signal output function at 16 time-sharings, generating the row drive signals ROW0 to ROW7 at 16 time-sharings, driving timing input from the LCD timing controller. These signals are output from the row drive signal output pin.

Where M2 to M0 = 4, 5 is executed by the SMM command, the row driver has ROW8 to ROW15 signal output function at 16 time-sharings, generating the row drive signals ROW8 to ROW15 at 16 time-sharings, driving timing input from the LCD timing controller. These signals are output from the row drive signal output pin.

In 16 time-sharings, the row driver can generate only row drive signal of ROW0 to ROW7 or ROW8 to ROW15 Therefore, to display LCD in 16 time-sharings, it is necessary to constitute one set of row drive signals ROW0 to ROW15 by using two or more μPD7227s, outputting ROW0 to ROW7 from the master chip and outputting ROW8 to ROW15 from the slave chip.

4.8 LCD TIMING CONTROLLER

The LCD Timing controller generates LCD drive timing according to the number of time-sharings and the division ratio, supplying it to the column driver and the row driver. At the same time, in case of the multi-chip configuration, it outputs from the SYNC pin the SYNC signal that synchronizes with the display timing of each μPD7227.

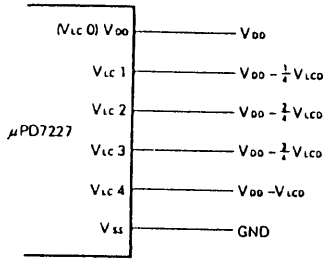
In the multi-chip configuration, the wired-or connection of the SYNC pin of each μPD7227 allows shared use of the ROW signal and extension of the display digit

4.9 LCD VOLTAGE CONTROL BLOCK

The LCD voltage control block inputs the LCD drive reference voltage from V_{LC1} to V_{LC4}, supplying it to the column driver and the row driver.

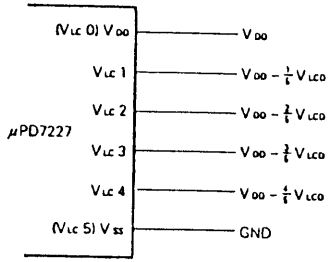
Based on the LCD drive reference voltage input from the LCD drive voltage control block, the column driver and the row driver generate various drive voltages of the column drive signal and of the row drive signal

The LCD drive reference voltage is supplied to μPD7227 according to the number of time-sharings, as shown in Fig 11 (a) and Fig. 11 (b).



Note LCD drive voltage: $V_{LCD} < V_{DD}$

Fig. 11 (a) 8 Time-Sharings



Note: LCD drive voltage: $V_{LCD} = V_{DD}$

Fig. 11 (b) 16 Time-Sharings

Circuits examples used when the LCD drive reference voltage is supplied through resistor split are shown in Fig 12 (a) and Fig. 12 (b).

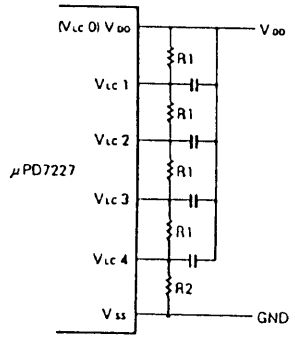


Fig. 12 (a) 8 Time-Sharings

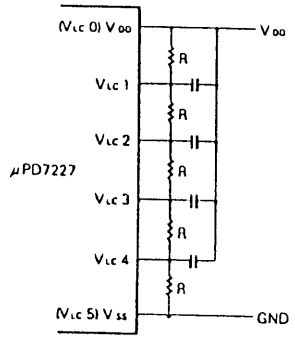


Fig. 12 (b) 16 Time-Sharings

The resistor values of R1 and R2 at 8 time-sharings in Fig 12 (a) are determined by the following formula.

$$V_{LCD} = \frac{V_{DD}}{1 + R2/4R1}$$

5. CONTROL FUNCTION

5.1 CHIP SELECT FUNCTION

Low level input to a $\overline{CS}$ pin makes μPD7227 active and serial data can be input or output

i) The state of $\overline{CS}$ = 1
- Regardless of the input level, SI, $\overline{SCK}$, C/$\overline{D}$ pin reaches a high level state inside μPD7227.
- SO/$\overline{BUSY}$ pin reaches a high impedance state

ii) Operation by means of the rise of $\overline{CS}$

The SCK counter is cleared. Therefore, when $\overline{CS}$ is actuated (or raised) while serial data is input/output, reception or transfer of data becomes invalid, and next when the $\overline{CS}$ pin is brought to the low level, it becomes possible to make a new 8-bit data transmission/reception.

5.2 RESET FUNCTION

The input of three clock cycles or more to the RESET pin causes μPD7227 to be reset and brought to the states of i) or ii).

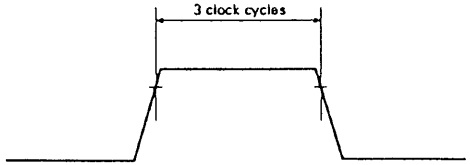


Fig. 13 RESET Waveform

i) The state during RESET
- The SO/$\overline{BUSY}$ pin reaches the low level if the $\overline{CS}$ pin is at the low level, reaching the high impedance if the $\overline{CS}$ pin is at the high level.
- The signal of the V_{LC3} level is out from the column drive signal output pin and the row drive signal output pin.

ii) The state after RESET cancellation
- The SCK counter is cleared.
- The state where the following commands are executed is reached.

SWM (I_1, I_0 = 00)	:	In the WRITE mode, the data pointer is incremented by (+1) every time data is input
LDPI (D_6 to D_0 = 0000000)	:	The data pointer is cleared to "0".
DISP OFF	:	The relation between the row drive and the column drive is non-selective level
SMM (M_2 to M_0 = 000)	:	LCD becomes 8 time-sharing driving, R0/R8 to R7/R15 pins output ROW0 to ROW7, the SYNC pin inputs them, and displaying data memory specifies "0".
SFF (F_2 to F_0 = 000)	:	Set the frame frequency to $f_{CU}/2^{14}$.

6. DISPLAY OUTPUT

This section shows the waveforms of a row drive signal and a column drive signal, when A is indicated at 8 time-sharings and both A and B are indicated at 16 time-sharings.

For the connections of μPD7227, LCD and the contents of data memory, refer to the read of display data.

ROW0 to ROW7 in the Fig. 14 shows the timing waveform of the row drive signal output from the row drive signal output pin. C0 to C4 shows the timing waveform of the column drive signal based on the display data of address 0 to address 4 of data memory. ROW0 to C1 shows the impressed voltage of the LCD element positioned at the intersecting point of the R0/R8 line and the C1 line. In this case, ROW0 to C1 is at the selection level (V_{LCD}), and this element lights.

ROW0 to ROW15 in Fig. 15 shows the timing waveform of the row drive signal output from the row drive signal output pin. C0 to C4 shows the column drive signal waveform output from the column drive signal output pin via the column driver, namely the contents of address 0 to address 4 of data memory. ROW1 to C0 shows the impressed voltage of the LCD element positioned at the intersecting point of the R1/R0 line and the C0 line. In this case, ROW1 to C0 is at the selection level and this element lights.

When A is indicated

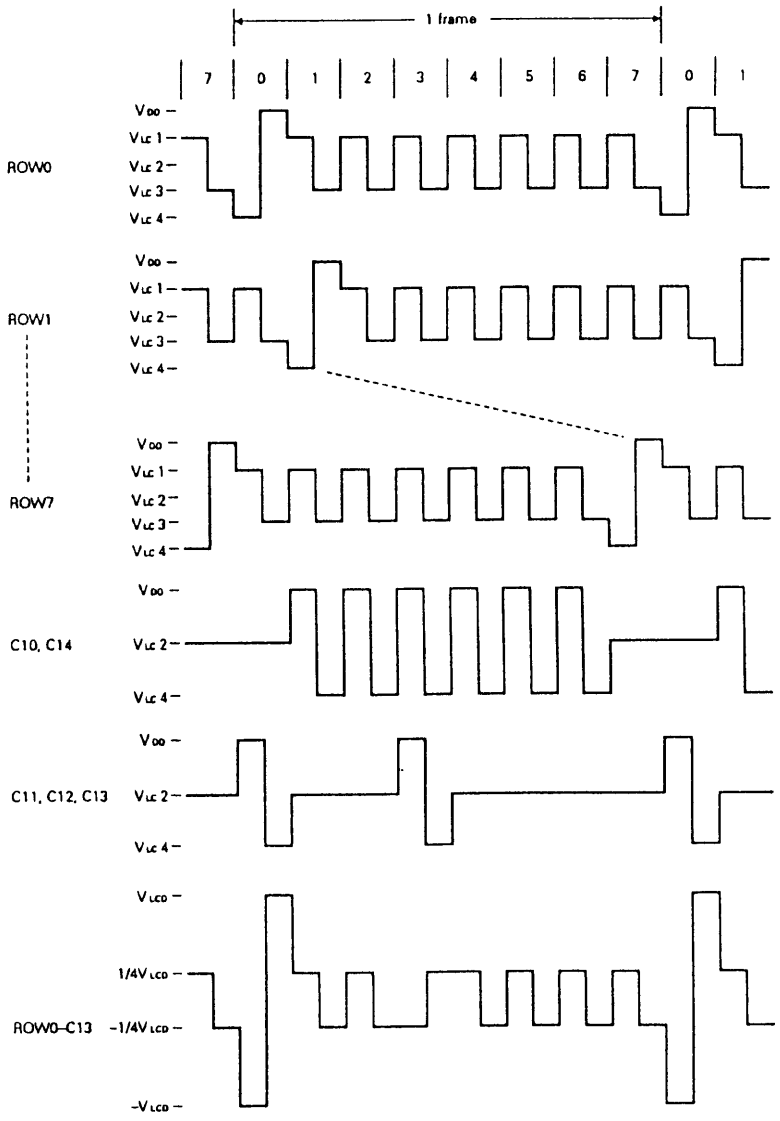


Fig. 14 8 Time-Sharings

When A and 8 are indicated

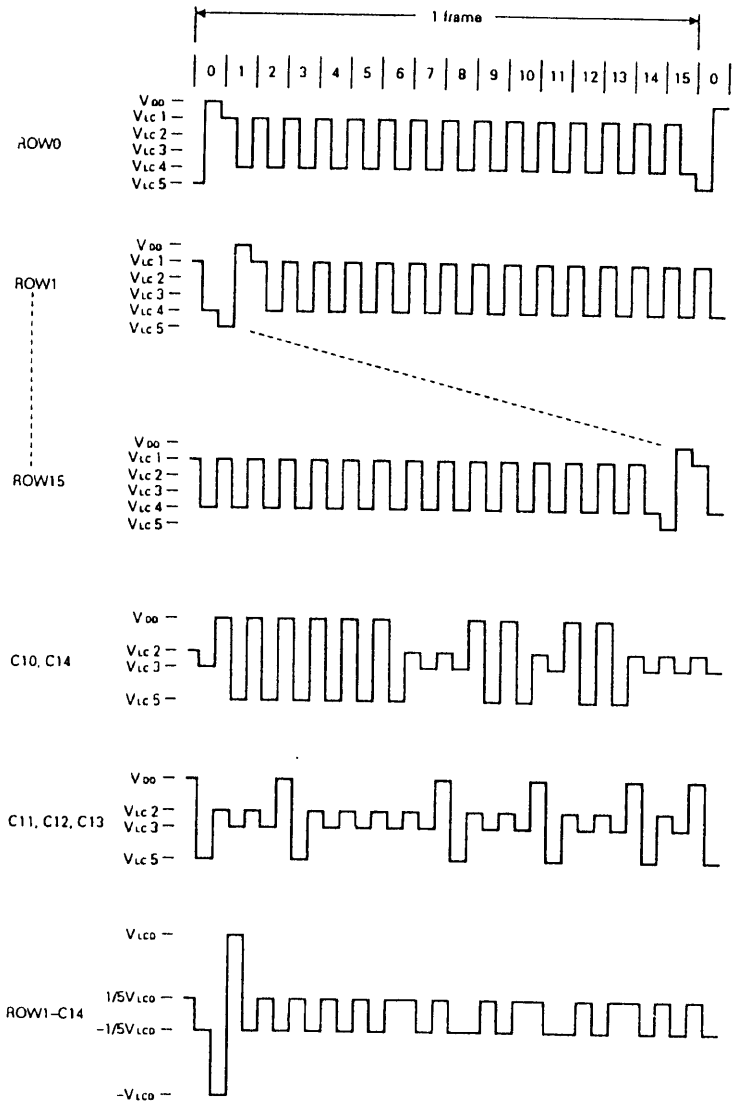


Fig. 15 16 Time-Sharings

7. EXAMPLES OF SYSTEM CONFIGURATION

This section shows the examples of single-chip and multi-chip configurations at 8 time-sharings and those of a multi-chip configuration at 16 time-sharings.

7.1 8 TIME-SHARINGS

i) When used in a single chip

- M2 to M0 = 2 or 3 is specified by the SMM command.
- The number of display dots = 8 × 40

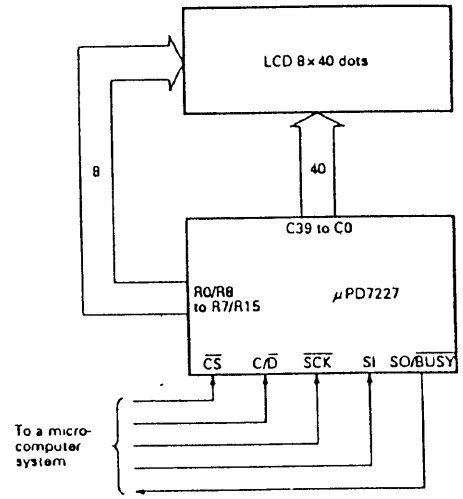


Fig. 16 Single Chip Configuration at 8 Time-Sharings

ii) When used in a multi-chip

- The SMM command specifies M_2 to M_0 = 2 or 3 of μPD7227 in case of No. 1 and M_2 to M_0 = 0 or 1 in case of No. 2 to No. n.
- The number of display dots = 8 × 40 × n

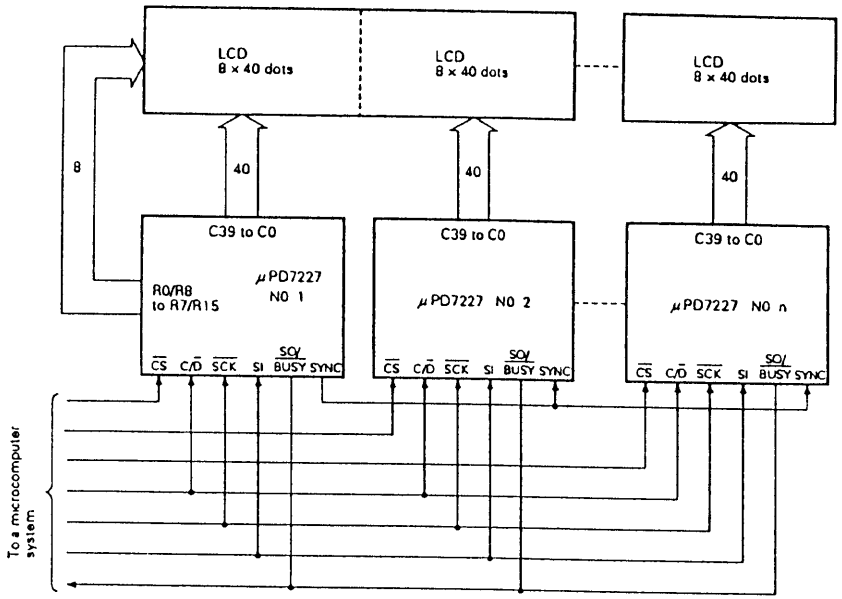


Fig. 17 The Multi-Chip Configuration at 8 Time-Sharings

7.2 MULTI-CHIP CONFIGURATION IN 16 TIME-SHARINGS

- The SMM command specifies M_2 to M_0 = 6 or 7 of μPD7227 in case of No. 1 and M_2 to M_0 = 4 or 5 in case of No. 2 to No. n.
- The number of display dots = 16 × 40 × n

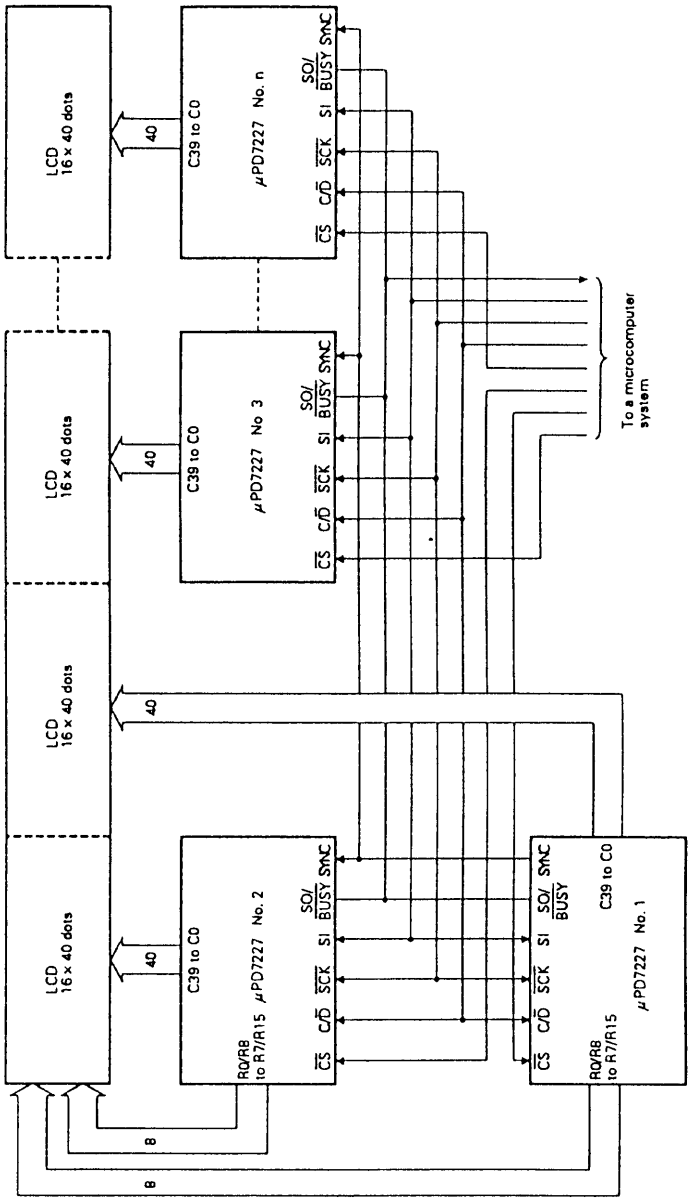


Fig. 18 The Multi-Chip Configuration in 16 Time-Sharings

8. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATING (T_a = 25°C)

Item	Sign	Condition	Rating	Unit
Power Supply Voltage	V_{DD}		−0.3 to +7.0	V
Input Voltage	V_I		−0.3 to V_{DD} +0.3	V
Output Voltage	V_O		−0.3 to V_{DD} +0.3	V
Operating Temperature	T_{opt}		−10 to +70	°C
Storage Temperature	T_{stg}		−65 to +150	°C

DC CHARACTERISTICS (T_a = −10 to +70°C, V_{DD} = 5 V ± 10%)

Item	Sign	Condition	Standard Value			Unit
			MIN	TYP.	MAX.	
High Level Input Voltage	V_{IH}		0.7V_{DD}		V_{DD}	V
Low Level Input Voltage	V_{IL}		0		0.3V_{DD}	V
High Level Input Leak Current	I_{LIH}	V_I = V_{DD}			10	μA
Low Level Input Leak Current	I_{LIL}	V_I = 0 V			−10	μA
High Level Output Voltage	V_{OH1}	SO/$\overline{BUSY}$, I_{OH} = −400 μA	V_{DD}−0.5			V
	V_{OH2}	SYNC, I_{OH} = −100 μA	V_{DD}−0.5			V
Low Level Output Voltage	V_{OL1}	SO/$\overline{BUSY}$, I_{OL} = 1.7 mA			0.45	V
	V_{OL2}	SYNC, I_{OL} = 100 μA			0.45	V
High Level Output Leak Current	I_{LOH}	V_O = V_{DD}			10	μA
Low Level Output Leak Current	I_{LOL}	V_I = 0 V			−10	μA
LCD Drive Voltage	V_{LCD}	8 time-sharing drive*	3.0		V_{DD}	V
Low Output Impedance	R_{ROW}			4	8	kΩ
Column Output Impedance	R_{COL}			10	15	kΩ
Power Supply Current	I_{DD}	f_c = 400 kHz		200	400	μA

Remarks: *: V_{DD} = V_{LCD} in case of 16 time-sharings

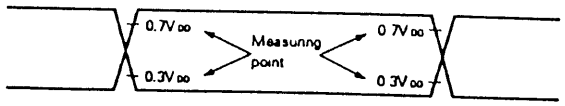
CAPACITANCE (T_a = 25°C, V_{DD} = 0 V)

Item	Sign	Condition	Standard Value			Unit
			MIN	TYP	MAX.	
Input Capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.			10	pF
Output Capacitance	C_{OUT}				25	pF
Input/Output Capacitance	C_{IO}				15	pF

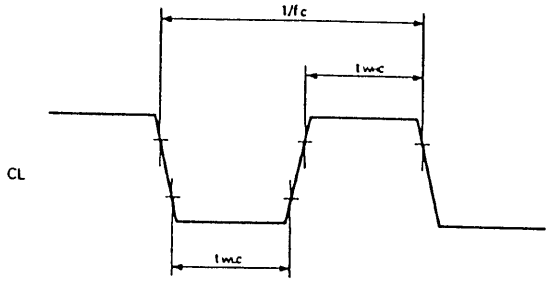
AC CHARACTERISTICS (T_a = −10 to +70°C, V_{DD} = +5 V ± 10%)

Item	Sign	Condition	Standard Value			Unit
			MIN.	TYP.	MAX	
Clock Operation Frequency	f_c		100		1000	kHz
High Level Clock Pulse Width	t_{WHC}		400			ns
Low Level Clock Pulse Width	t_{WLC}		400			ns
$\overline{SCK}$ Cycle	t_{CYK}		0.9			μs
High Level $\overline{SCK}$ Pulse Width	t_{WHK}		400			ns
Low Level $\overline{SCK}$ Pulse Width	t_{WLK}		400			ns
High Level $\overline{SCK}$ Hold Time from $\overline{BUSY}$↑	t_{HSK}		0			ns
SI Setup Time to $\overline{SCK}$↑	t_{SIK}		100			ns
SI Hold Time from $\overline{SCK}$↑	t_{HKI}		250			ns
SO Delay Time from $\overline{SCK}$↓→	t_{DKO}	C_L = 50 pF			320	ns
SO Delay Time from C/$\overline{D}$↓→	t_{DDO}	C_L = 50 pF			2	μs
High Level $\overline{SCK}$ Hold Time from C/$\overline{D}$↓	t_{HDK}		2			μs
$\overline{BUSY}$ Delay Time from 8th $\overline{SCK}$↑→	t_{DKS}	C_L = 50 pF			3	μs
$\overline{BUSY}$ Delay Time from C/$\overline{D}$↑→	t_{DDS}	C_L = 50 pF			2	μs
$\overline{BUSY}$ Delay Time from $\overline{CS}$↓→	t_{DCSS}	C_L = 50 pF			2	μs
$\overline{BUSY}$ Low Level Time	t_{WLS}	C_L = 50 pF	18		64	1/f_c
C/$\overline{D}$ Setup Time to 8th $\overline{SCK}$↑	t_{SDK}		2			μs
C/$\overline{D}$ Hold Time from 8th $\overline{SCK}$↑	t_{HKD1}		2			μs
Low Level C/$\overline{D}$ Hold Time from 8th $\overline{SCK}$↑	t_{HKD2}		2			μs
$\overline{CS}$ Hold Time from 8th $\overline{SCK}$↑	t_{HKCS}		2			μs
High Level $\overline{CS}$ Pulse Width	t_{WHCS}		2/f_c			μs
$\overline{BUSY}$ Float Delay Time from $\overline{CS}$↑→	t_{DCSF}	C_L = 50 pF			2	μs
SYNC Load Capacitance	C_{LSY}				100	pF

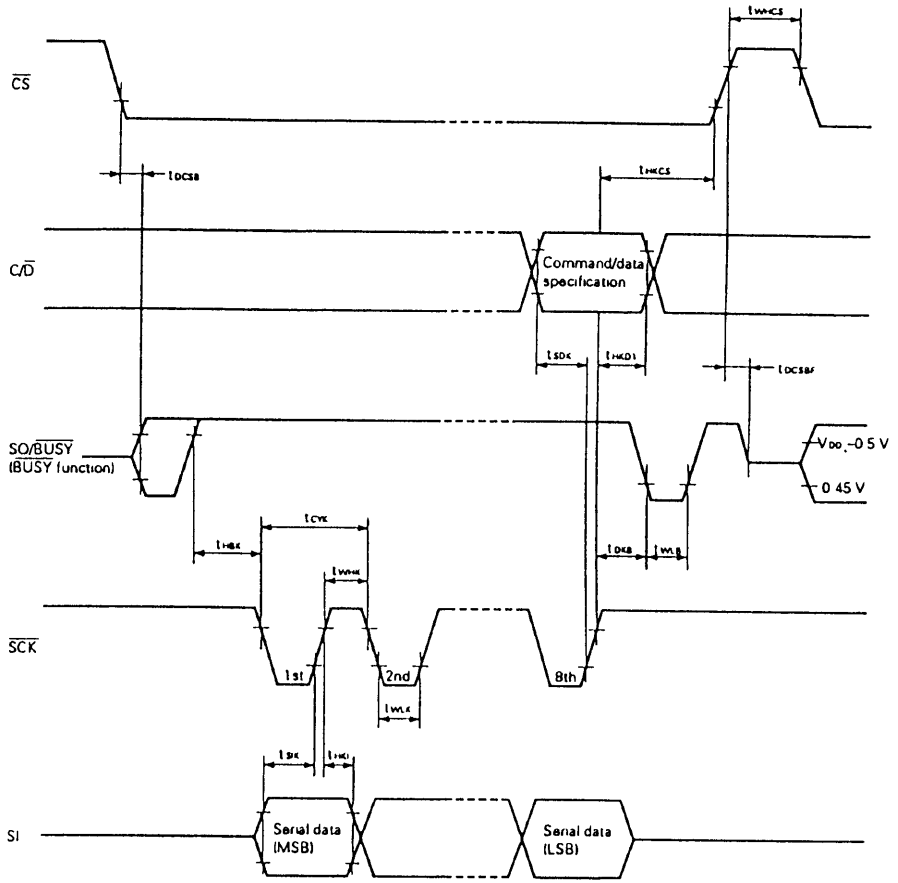
AC TIMING MEASUREMENT VOLTAGE



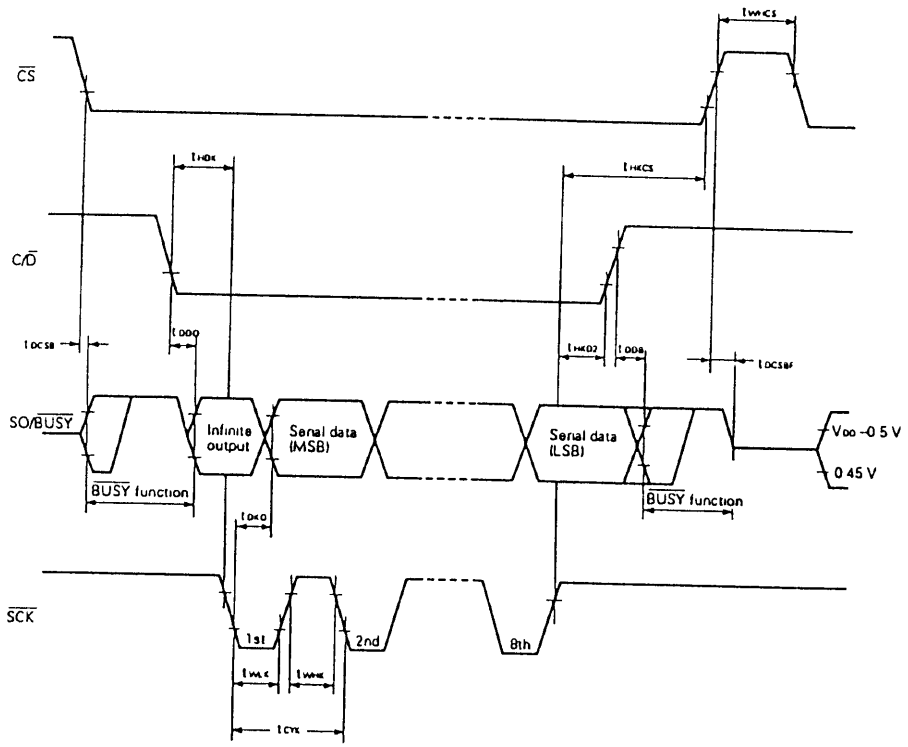
TIMING WAVEFORM



WRITE TIMING

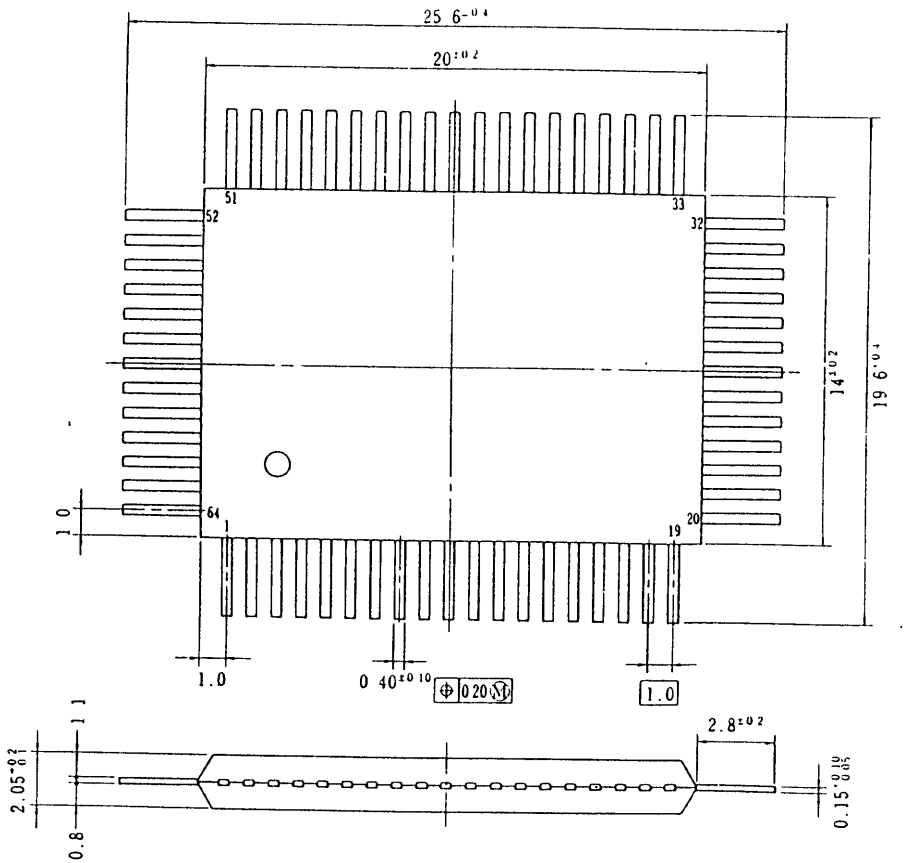


READ TIMING



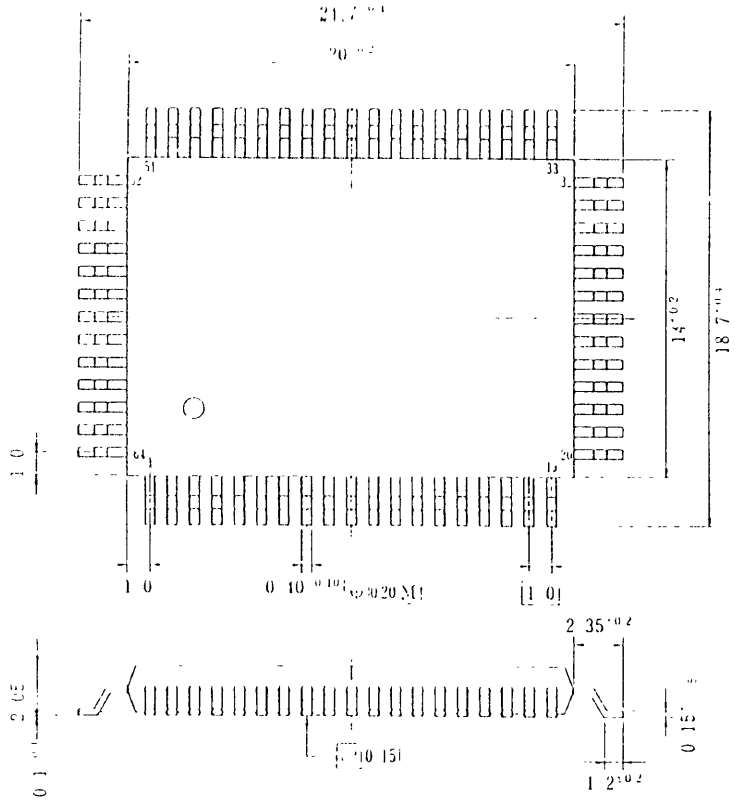
9. PACKAGE DRAWINGS

64-Pin Plastic QFP (Unit: mm)



P64G-100-11

64 Pin Plastic QFP (Bent Leads) (Unit: mm)



P64G-100-12