

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The μPA2751GR is asymmetrical dual N-Channel MOS Field Effect Transistor designed for DC/DC converters of notebook computers and so on.

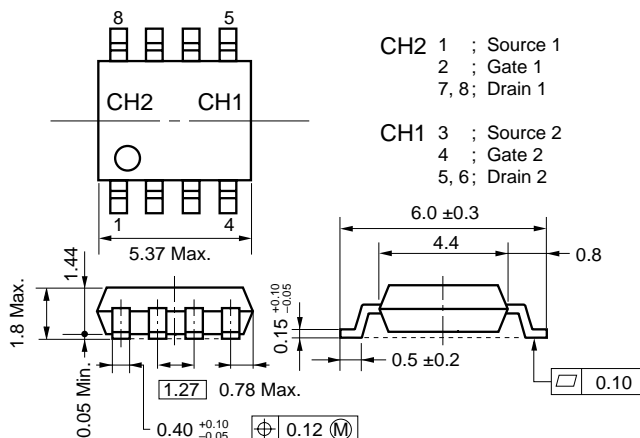
FEATURES

- Asymmetric dual chip type
- Low on-state resistance, Low C_{iss}
CH1: R_{DS(on)2}: 21.0 mΩ MAX. (V_{GS} = 4.5 V, I_D = 4.5 A)
C_{iss} = 1040 pF TYP. (V_{DS} = 10 V, V_{GS} = 0 V)
CH2: R_{DS(on)2}: 35.0 mΩ MAX. (V_{GS} = 4.5 V, I_D = 4.0 A)
C_{iss} = 480 pF TYP. (V_{DS} = 10 V, V_{GS} = 0 V)
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2751GR	Power SOP8

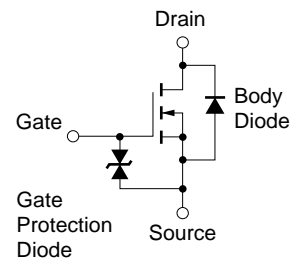
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V _{GS} = 0 V)	CH1/CH2	V _{DS}	30	V
Gate to Source Voltage (V _{DS} = 0 V)	CH1/CH2	V _{GS}	±20	V
Drain Current (DC)	CH1	I _{D(DC)}	±9.0	A
	CH2	I _{D(DC)}	±8.0	A
Drain Current (pulse) ^{Note1}	CH1	I _{D(pulse)}	±36	A
	CH2	I _{D(pulse)}	±32	A
Total Power Dissipation (1 unit) ^{Note2}	CH1/CH2	P _T	1.7	W
Total Power Dissipation (2 unit) ^{Note2}	CH1/CH2	P _T	2.0	W
Channel Temperature	CH1/CH2	T _{ch}	150	°C
Storage Temperature	CH1/CH2	T _{stg}	-55 to + 150	°C
Single Avalanche Current ^{Note3}	CH1	I _{AS}	9.0	A
Single Avalanche Energy ^{Note3}	CH1	E _{AS}	8.1	mJ
Single Avalanche Current ^{Note3}	CH2	I _{AS}	8.0	A
Single Avalanche Energy ^{Note3}	CH2	E _{AS}	6.4	mJ

EQUIVALENT CIRCUIT (1/2 circuit)



- Notes 1.** PW ≤ 10 μs, Duty cycle ≤ 1%
2. T_A = 25°C, Mounted on ceramic substrate of 2000 mm² x 1.6 mm
3. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω, V_{GS} = 20 → 0 V

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

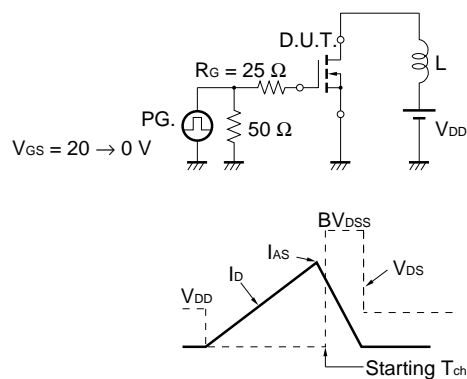
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ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

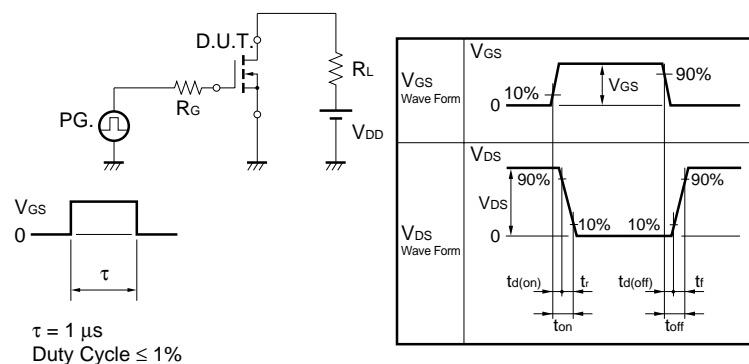
CH1

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 4.5 A	5	11		S
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 4.5 A		12.5	15.5	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 4.5 A		16.0	21.0	mΩ
	R _{DS(on)3}	V _{GS} = 4.0 V, I _D = 4.5 A		17.9	23.9	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V		1040		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		390		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		130		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 4.5 A		13		ns
Rise Time	t _r	V _{GS} = 10 V		10		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		43		ns
Fall Time	t _f			9		ns
Total Gate Charge	Q _G	V _{DD} = 24 V		21		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		3.3		nC
Gate to Drain Charge	Q _{GD}	I _D = 9.0 A		5.1		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 9.0 A, V _{GS} = 0 V		0.84		V
Reverse Recovery Time	t _{rr}	I _F = 9.0 A, V _{GS} = 0 V		34		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		34		nC

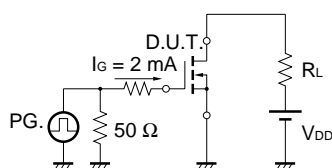
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE

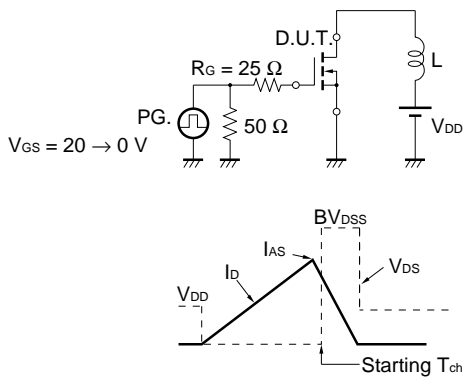


ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

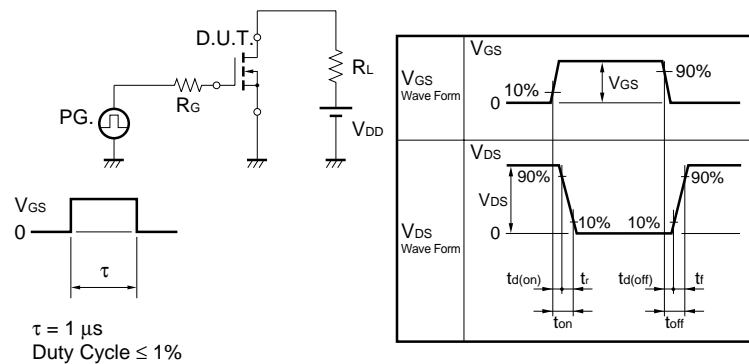
CH2

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±18 V, V _{DS} = 0 V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 4.0 A	3.5	7		S
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 4.0 A		18.0	23.0	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 4.0 A		25.0	35.0	mΩ
	R _{DS(on)3}	V _{GS} = 4.0 V, I _D = 4.0 A		28.5	41.0	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V		480		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		190		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		70		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 4.0 A		9.9		ns
Rise Time	t _r	V _{GS} = 10 V		6.2		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		25		ns
Fall Time	t _f			5.8		ns
Total Gate Charge	Q _G	V _{DD} = 24 V		10		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		1.9		nC
Gate to Drain Charge	Q _{GD}	I _D = 8.0 A		2.6		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 8.0 A, V _{GS} = 0 V		0.81		V
Reverse Recovery Time	t _{rr}	I _F = 8.0 A, V _{GS} = 0 V		28		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		23		nC

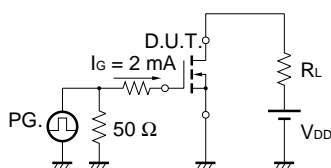
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



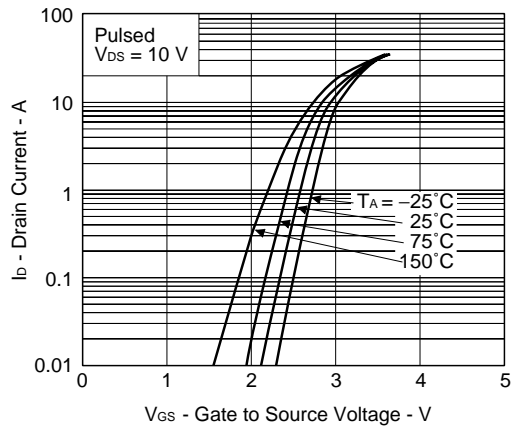
TEST CIRCUIT 3 GATE CHARGE



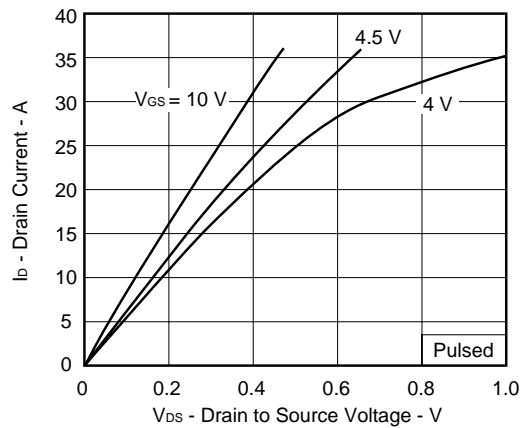
TYPICAL CHARACTERISTICS (T_A = 25°C)

A) CH1

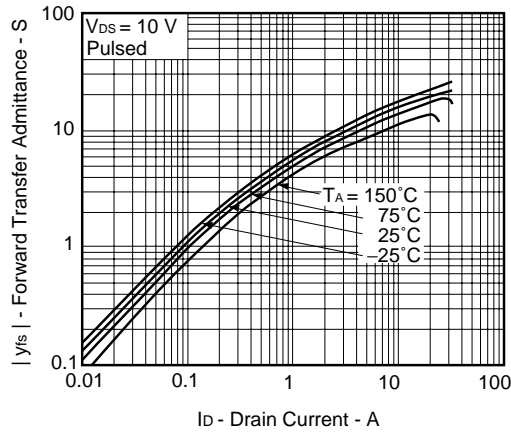
FORWARD TRANSFER CHARACTERISTICS



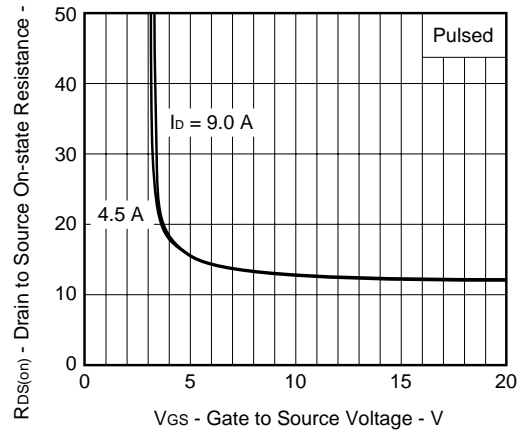
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



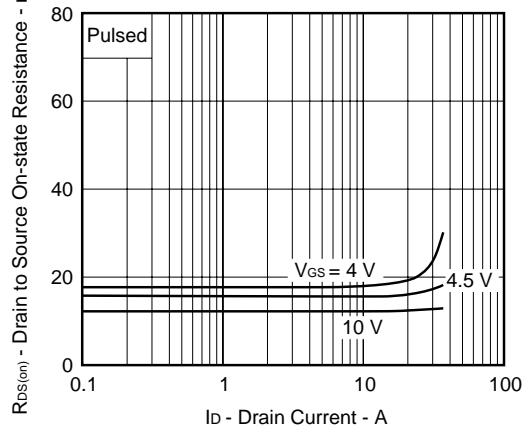
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



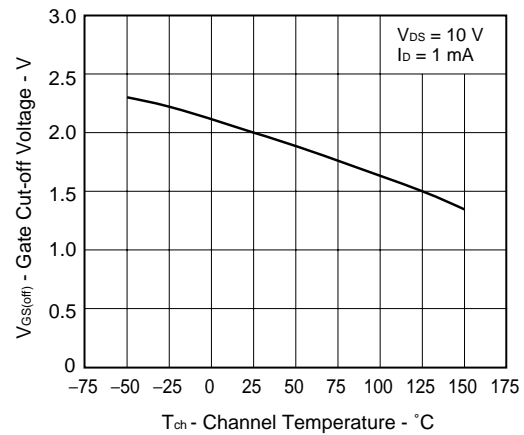
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



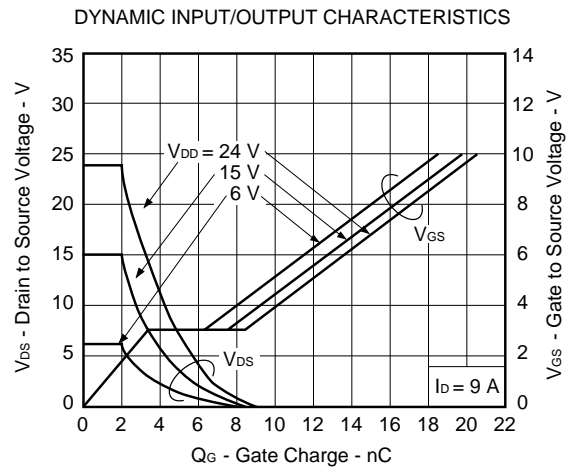
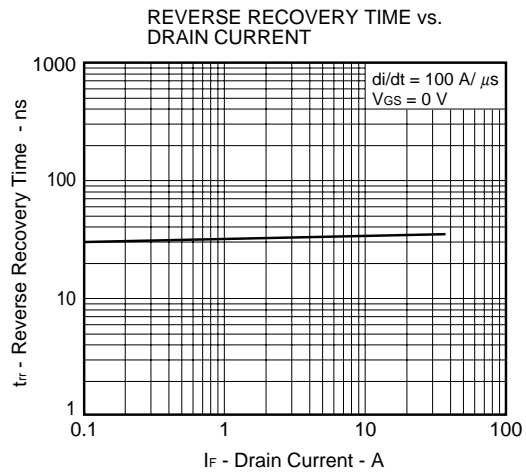
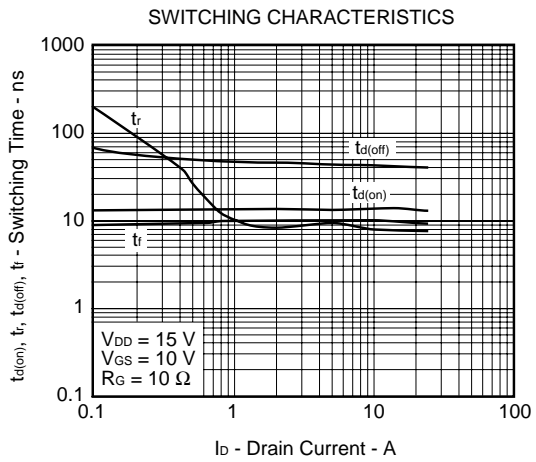
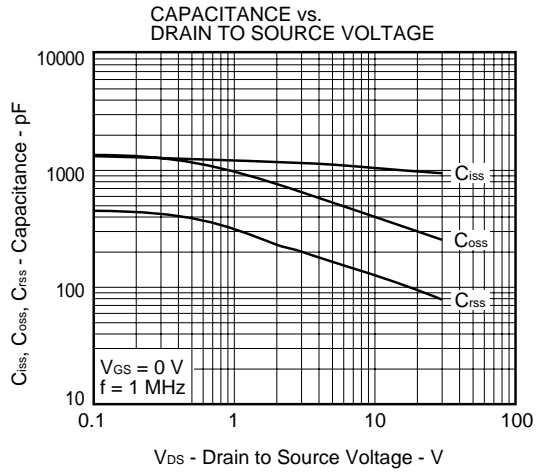
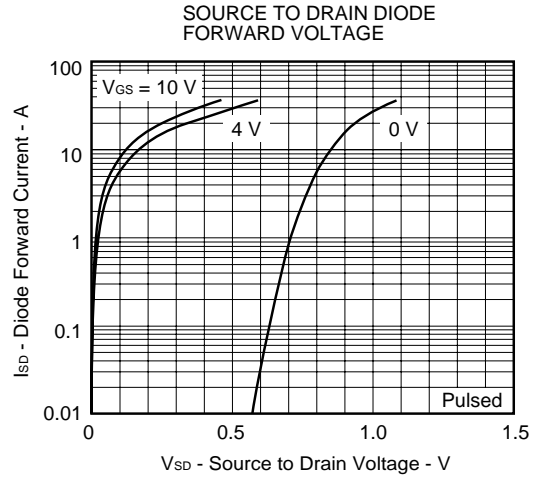
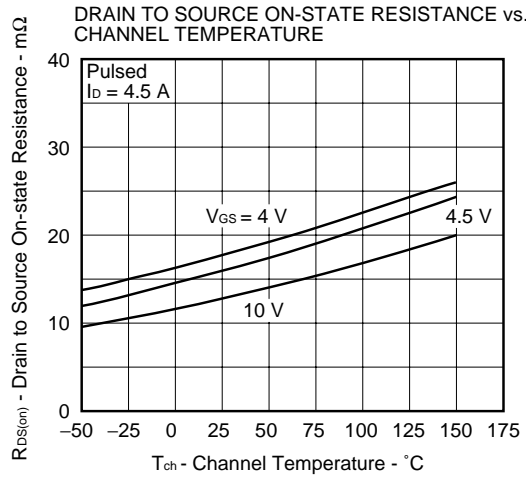
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

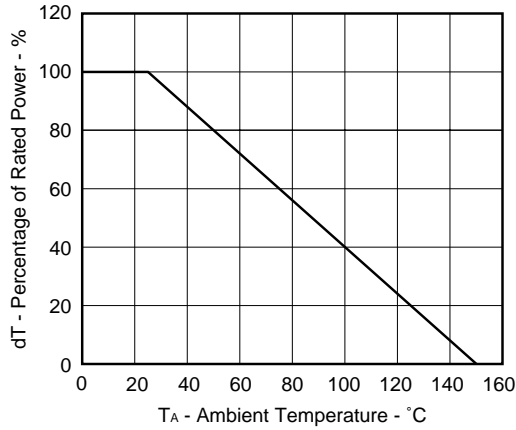


A) CH1

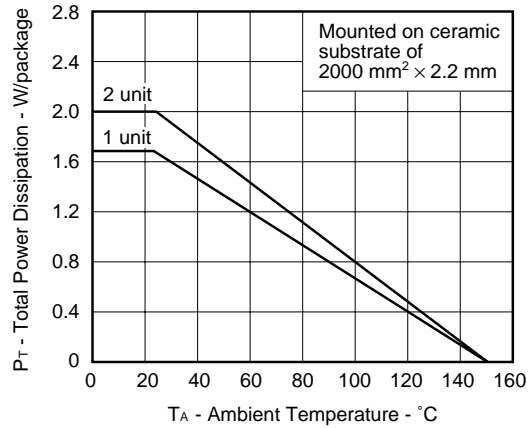


A) CH1

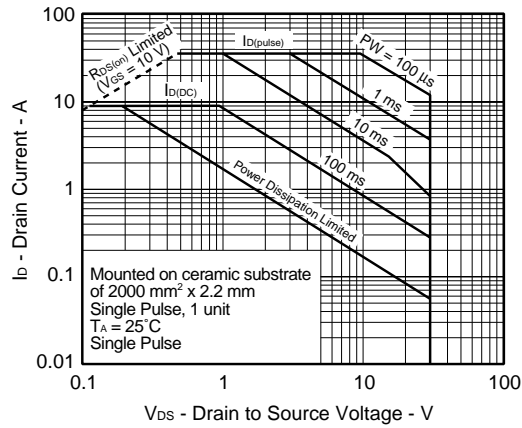
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



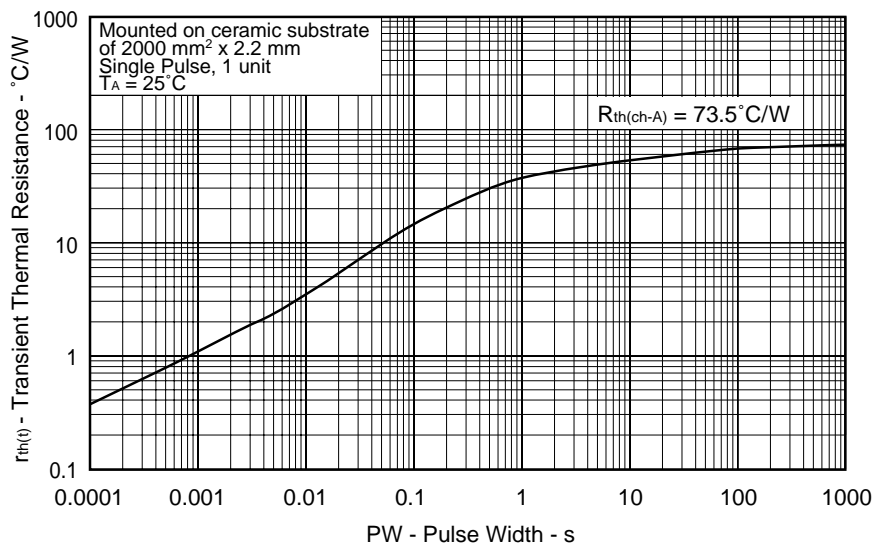
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



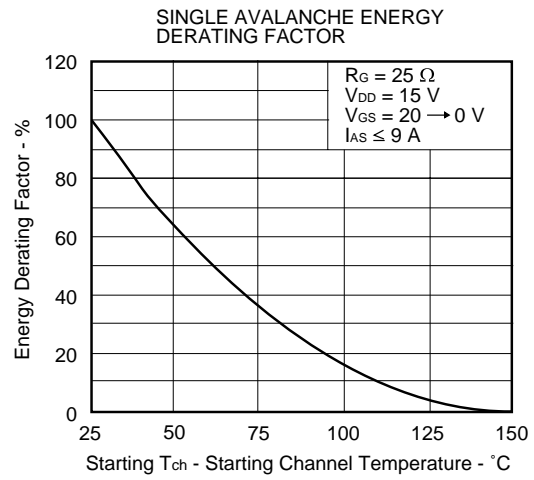
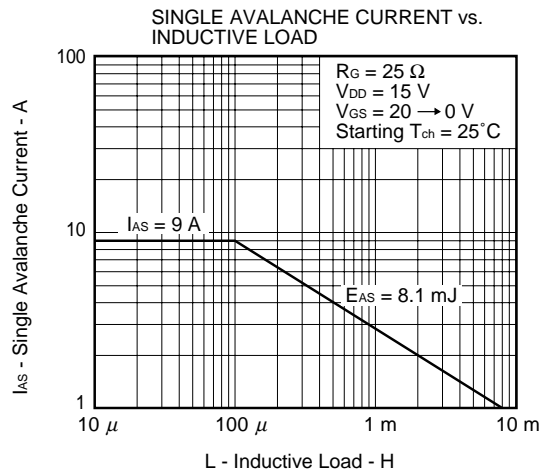
FORWARD BIAS SAFE OPERATING AREA



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



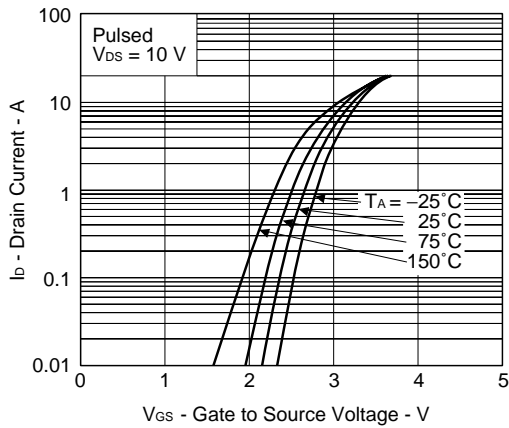
A) CH1



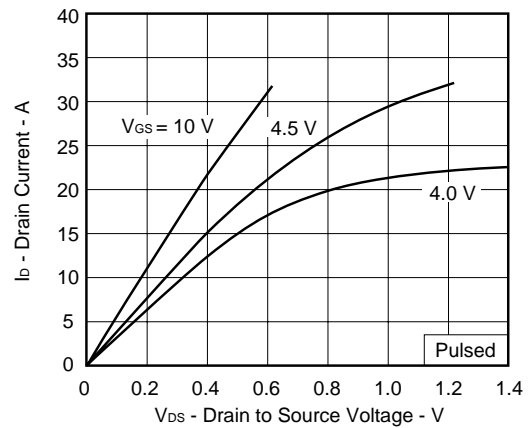
TYPICAL CHARACTERISTICS (TA = 25°C)

B) CH2

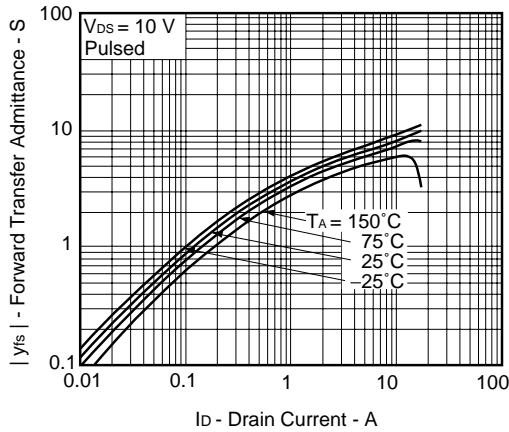
FORWARD TRANSFER CHARACTERISTICS



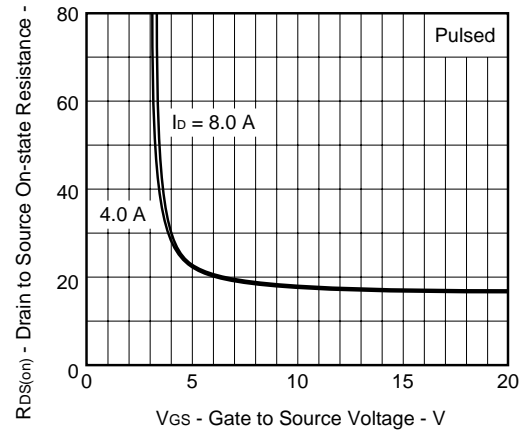
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



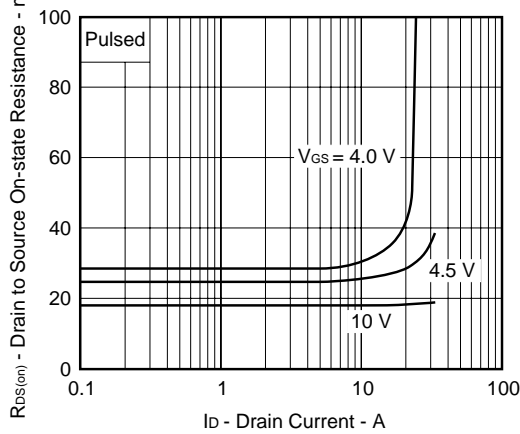
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



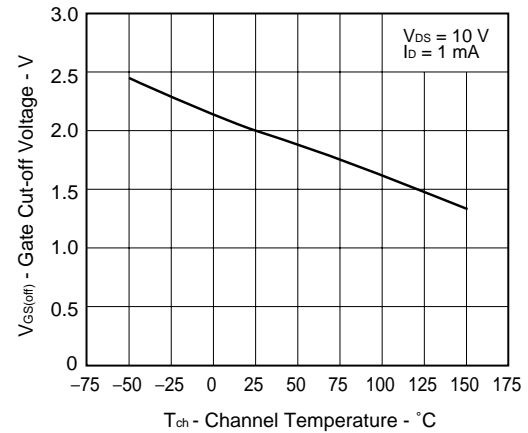
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



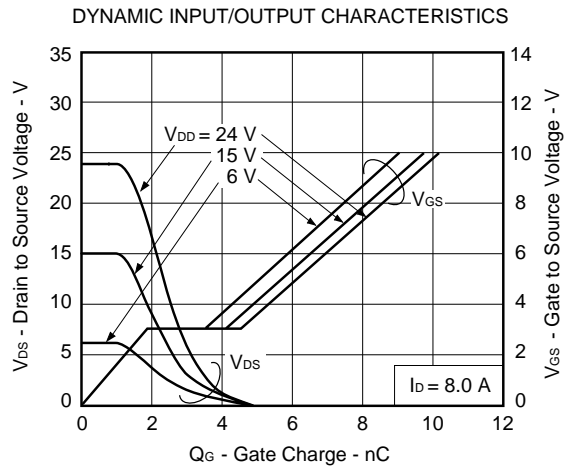
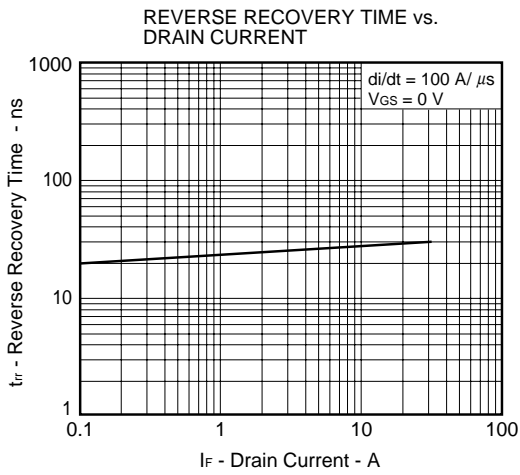
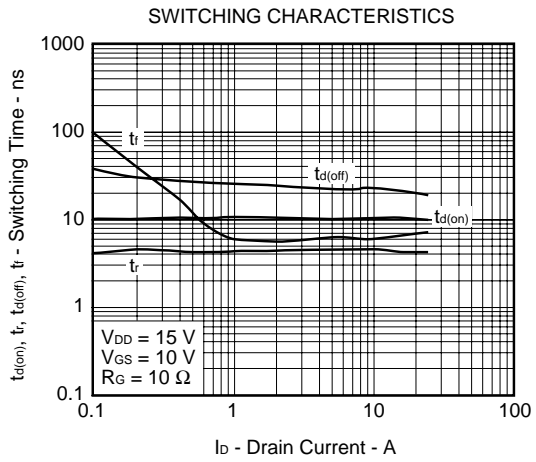
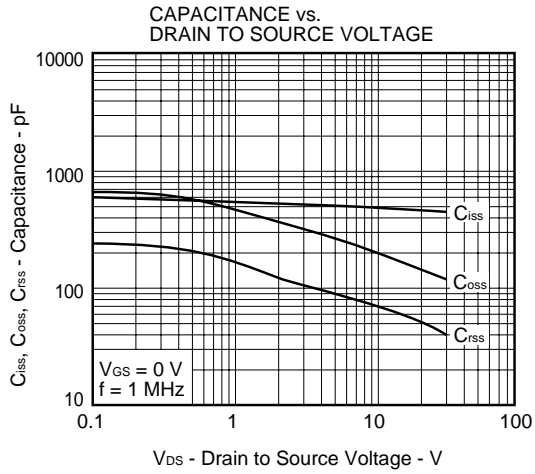
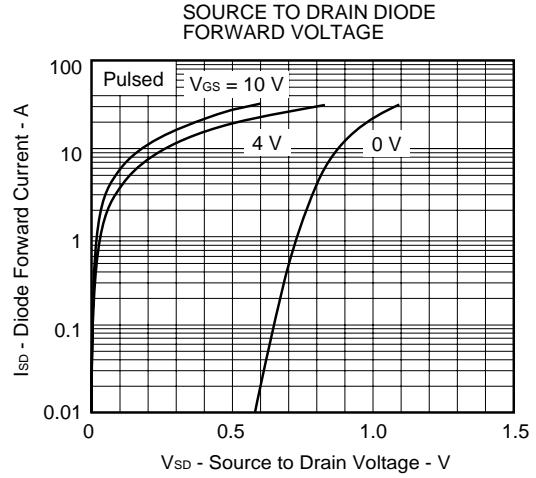
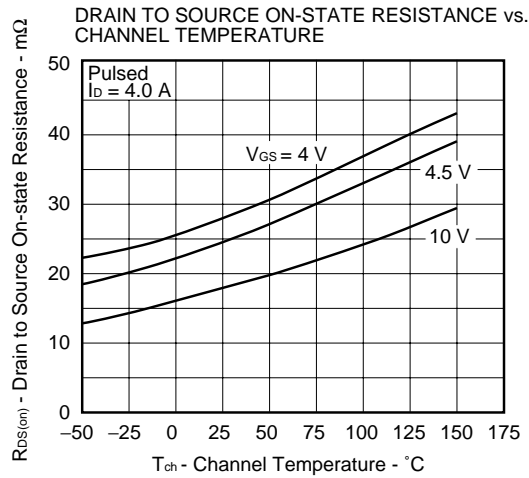
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



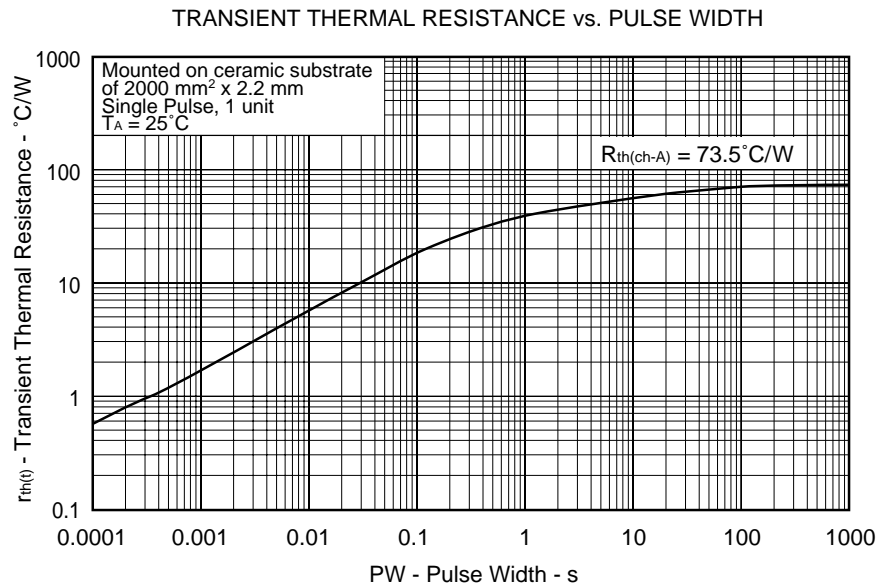
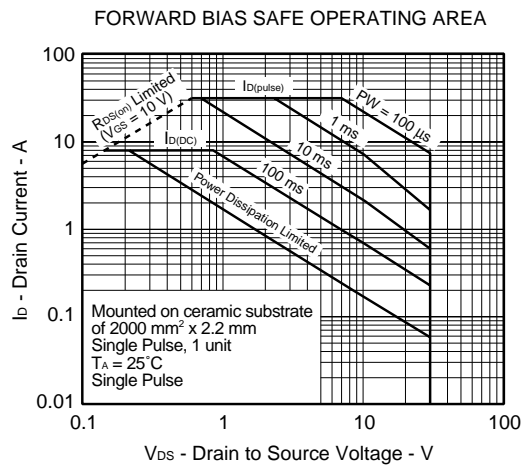
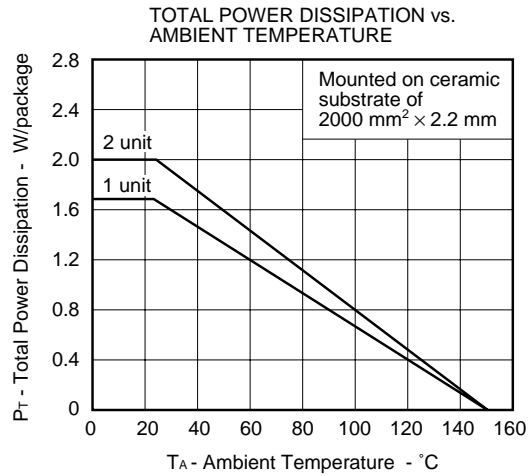
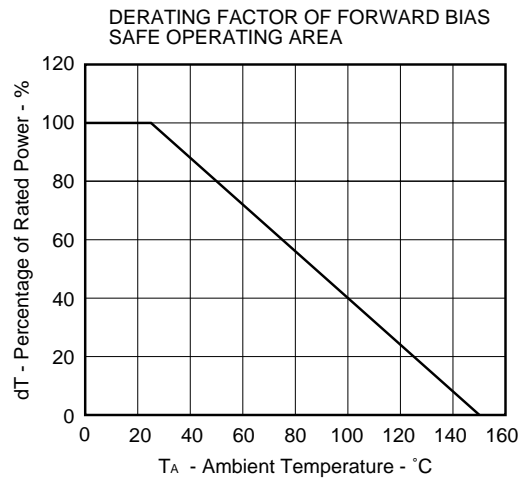
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



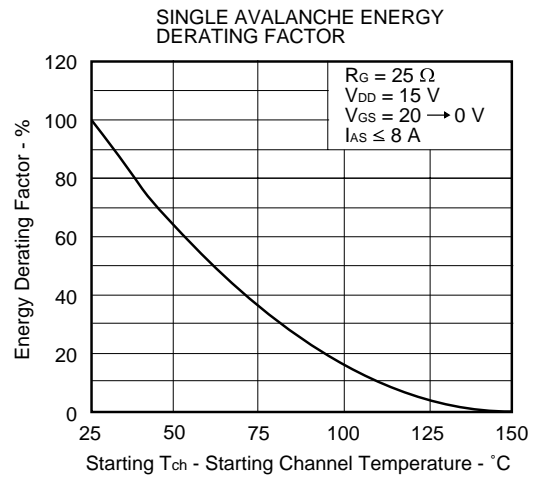
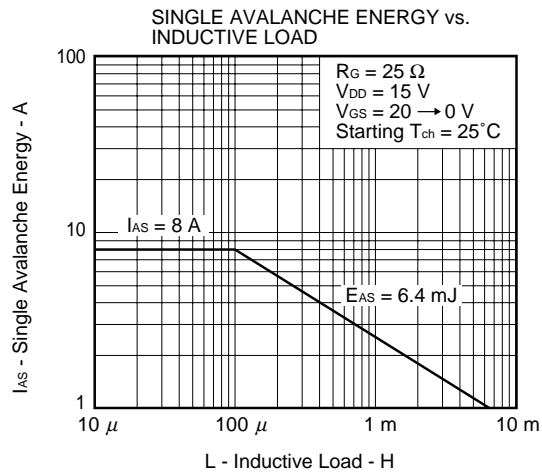
B) CH2



B) CH2



B) CH2



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