UM83C022

PRELIMINARY

AT HDC Interface

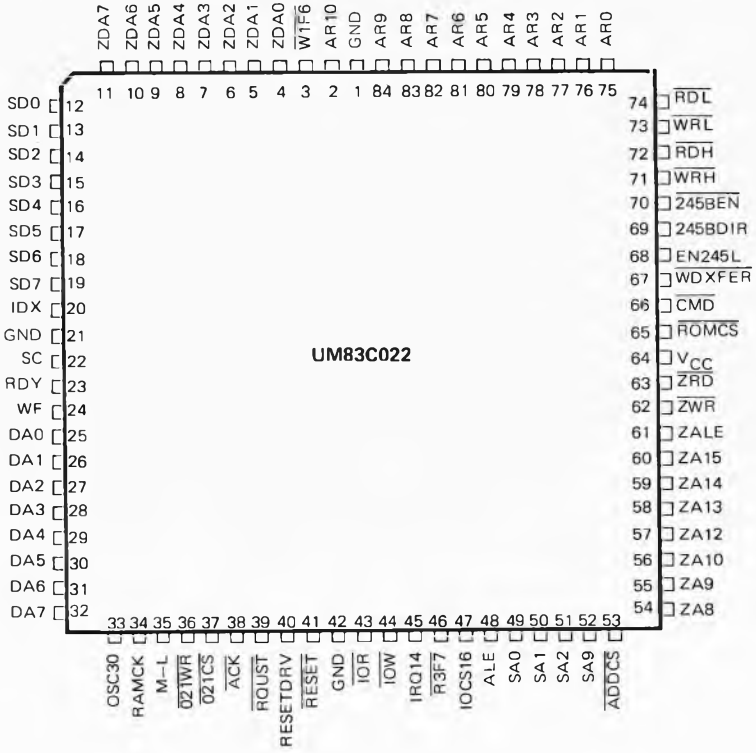
Features

- IBM PC/AT interface compatible
- Jumper selectable for RLL/MFM disk interface
- 1:2 interleave
- Buffer size 4k bytes
- Sector size 512 bytes
- 84-pin PLCC package

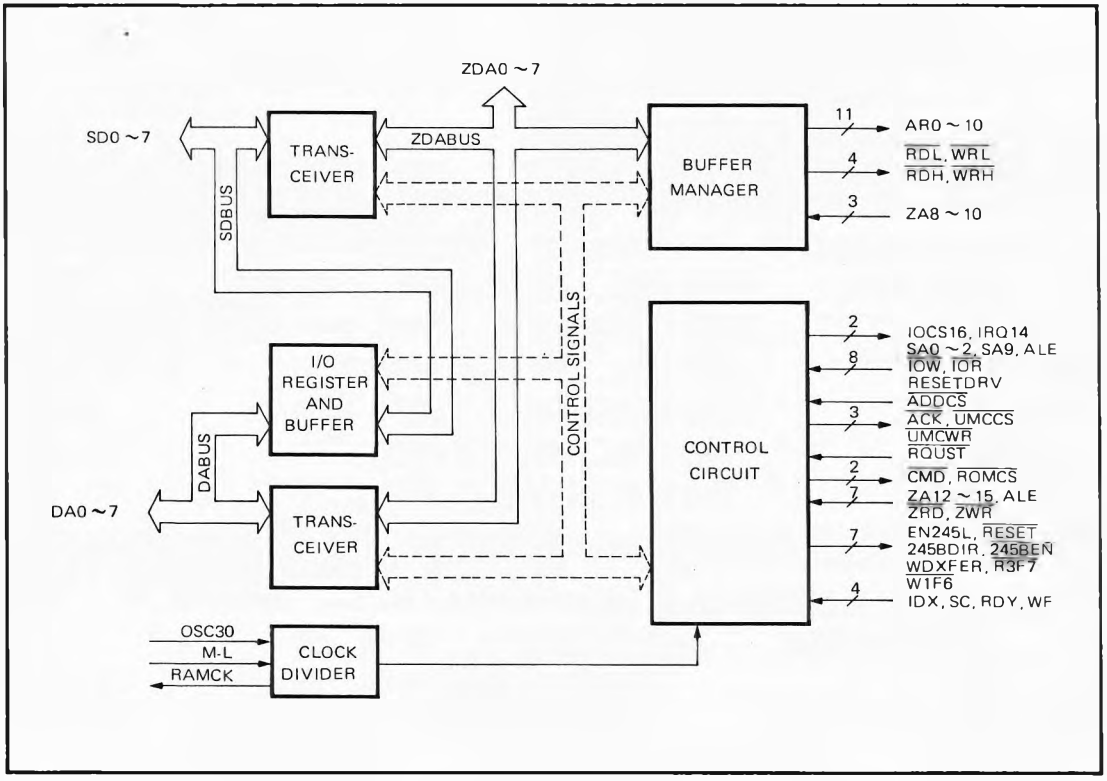
General Description

UM83C022 is a component for Winchester disk controller interface applications. It is designed to attach two 5.0/7.5 Mbit/sec MFM/RLL encoded ST-506 (ST-412) Winchester disk drives to IBM PC/AT compatible personal computers. The controller implements the host interface and the command set compatible to the original IBM PC/AT Disk Controller. UM83C022 supports the 4K-byte sector buffers, and track formats compatible to IBM PC/AT hard disk formats.

Pin Configuration



Block Diagram



Absolute Maximum Ratings *

Power Supply Voltage, V_{DD} . . . . . −0.5 to +7.0V

Input Voltage, V_I . . . . . −0.5V to V_{DD} + 0.5V

Operating Temperature, T_{OPT} . . . . . −40 to +85°C

Storage Temperature, T_{STG} . . . . . −65 to +150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to 70°C, V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{IL}	Input Low Voltage	–	0.8	V	
V_{IH}	Input High Voltage	2.0	–	V	V_{DD} = 5V V_{IN} = 0 – 5V
I_I	Input Leakage Current	–	± 50	μA	All others pin = 0V
V_{OL}	Output Low Voltage	–	0.4	V	I_{OL} = 8 mA V_{DD} = 5V
V_{OH}	Output High Voltage	2.4	–	V	I_{OH} = −8 mA V_{DD} = 5V

AC Characteristics (T_A = 0°c to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Min.	Max.	Unit	Conditions
T1	Address setup to EN245L low		25	ns	
T2	Address setup to EN245L high		25	ns	
T3	$\overline{IOR}$/$\overline{IOW}$-pulse width	100		ns	
T4	$\overline{IOR}$ setup to $\overline{RDL}$, $\overline{RDH}$ low		25	ns	
T5	$\overline{IOR}$ setup to $\overline{RDL}$, $\overline{RDH}$ high		20	ns	
T6	$\overline{IOW}$ setup to $\overline{WRL}$, $\overline{WRH}$ low		25	ns	
T7	$\overline{IOW}$ setup to $\overline{WRL}$, $\overline{WRH}$ low		20	ns	
T8	Address setup to IOCS16 low		25	ns	
T9	Address setup to $\overline{WDXFEF}$ low		25	ns	
T10	RAMCK setup to $\overline{ACK}$ low		20	ns	
T11	RAMCK setup to $\overline{WRL}$ low or to $\overline{RDL}$ low		20	ns	
T12	RAMCK setup to $\overline{WRL}$ high or $\overline{RDL}$ high		20	ns	
T13	RAMCK setup to $\overline{WRH}$ low or to $\overline{RDH}$ low		20	ns	
T14	RAMCK setup to $\overline{WRH}$ high or $\overline{RDH}$ high		20	ns	

Pin Description

Pin No.	Symbol	I/O	Description
2	AR10	O	Address 10 for buffer address decoding.
3	$\overline{W1F6}$	O	Write I/O port 1F6H/176H to select hard disk drive.
4-11	ZDA0 ~ 7	I/O	Data (address) bus for translation among HOST interface, CONTROLLER, and BUFFER.
12-19	SD0 ~ 7	I/O	System data bus provides bits 0 through 7 for PC bus.
20	IDX	I	INDEX pin provided by drive to indicate the beginning of a track.
22	SC	I	This signal, seek complete, goes active when the R/W head settles on the desired track at the end of a seek command.
23	RDY	I	Ready, when this signal and SC are active, it indicates the drive is ready to Read, Write, and Seek and the I/O signals are ready.
24	WF	I	Write fault, the signal means an improper operation of the disk at the driver.
25-32	DA0 ~ 7	I/O	These signals are provided for 8031 to control the address and data used.
33	OSC30	I	Provides 30 MHz oscillation signal.
34	RAMCK	O	This signal provides 10/15 MHz clock for UM83021 and 8031 to synchronize all CPU and DMA operations.
35	M-L	I	This signal is used to identify MFM (high) or RLL (low) drive operation.
36	$\overline{021WR}$	O	This signal is driven by the 8031 address decoder to indicate whether a register read or write is to be performed in the UM83C021.
37	$\overline{021CS}$	O	UM83C021 chip selection, this signal is driven by 8031's address port to enable the registers of the UM83C021 to be read or written. The address port is 4000H-5FFFH.
38	$\overline{ACK}$	O	Acknowledge, this signal is driven low to response UM83021 DMA transferring request.
39	$\overline{RQUST}$	I	This request signal is used in conjunction with the $\overline{ACK}$ signal for handshaking during the UM83C021 DMA transferring.
40	RESETDRV	I	This signal is active high to clear the system status.
41	$\overline{RESET}$	O	This signal provides external logic reset capability.
43	$\overline{IOR}$	I	PC-BUS I/O read operation control.
44	$\overline{IOW}$	I	PC-BUS I/O write operation control.

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
45	IRQ14	O	Interrupt request to HOST.
46	$\overline{R3F7}$	O	Read I/O port 3F7H/377H control.
47	IOCS16	O	This signal indicates the present operation is a 16-bit data transfer I/O cycle.
48	ALE	I	This signal latches the valid addresses from the HOST.
49-52	SA0 ~ 3 SA9	I	This signal indicates the present operation is a 16-bit data transfer I/O cycle.
53	$\overline{ADDRCS}$	I	Address chip select decoded from SA3 ~ 8.
54-60	ZA8 ~ 10 ZA12 ~ 15	I	Local address bus from 8031 to be used as high-byte address and control pins.
61	ZALE	I	Local address latch from 8031.
62	$\overline{ZWR}$	I	Looal write enable from 8031.
63	$\overline{ZRD}$	I	Local read enable from 8031.
65	$\overline{ROMCS}$	O	This signal is used to enable the external ROM of the 8031 from 0000H-1FFFH.
66	$\overline{CMD}$	O	This signal is used to interrupt the 8031 when the HOST issues the command execution request.
67	$\overline{WDXFER}$	O	This signal indicates the 16-bit data transfer operation.
68	EN245L	O	Enables low-byte data bus to be transferred between the PC-BUS and UM83C022.
69	245BDIR	O	This signal determines whether the data flow is from the high-byte buffer or from the low-byte buffer.
70	$\overline{245BEN}$	O	This signal enables the transfer between ZDA0 ~ 7 and high-byte buffer.
71	$\overline{WRH}$	O	Write high-byte data to SRAM buffer.
72	$\overline{RDH}$	O	Read high-byte data from SRAM buffer.
73	$\overline{WRL}$	O	Write low-byte data to SRAM buffer.
74	$\overline{RDL}$	O	Read low-byte data from SRAM buffer.
75-84	AR0 ~ 9	O	These signals are provided for the external SRAM buffer addresses.
1, 21, 42	GND	I	Ground.
64	V_{CC}	I	Power supply +5V.

Functional/Register Description

A. HOST CONTROLLER/DRIVE STATUS REGISTER (Read Only)

This register specifies the status of the controller/drive. This register may be accessed by the HOST at any time, however, when the BUSY bit is set, no other bits in the register are valid. Also by reading this register, I/O address 1F7H/166H, any pending interrupts to the HOST are cleared.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BUSY	RDY	WF	SC	DRQ	CORD	IDX	ERROR

Bit 0 ERROR: This bit is set when an error has occurred on the last command or power up diagnostics. The error code is stored in the buffer with address 27F9H and can be accessed by the HOST with I/O address 1F1H.

Bit 1 INDEX: This bit reflects the status of INDEX signal (I/P Pin 20) from the selected disk drive. This signal goes active once per revolution of the disk. This bit will not be set if the drive is not ready (i. e. if Bit 6 is reset).

Bit 2 ECC CORRECTION DATA: This bit is set whenever (on the previous read sector transfer) a sector read off the disk had a correctable ECC error which was corrected.

Bit 3 DATA REQUEST: This bit is set for data transfer to/from the sector buffer. This includes both sector and ECC data. The controller is considered "busy" whenever the DRQ or BUSYL bits are set.

Bit 4 SEEK COMPLETE: This bit indicates the state of the Seek Complete signal (I/P Pin 22) from the selected disk drive. This bit is set when the drive is not seeking.

Bit 5 WRITE FAULT: This bit reflects the state of the Write Fault Signal (I/P Pin 24) from the selected disk drive. When this bit is set, it indicates that the drive is unsafe for read/write transfer.

Bit 6 READY: This bit reflects the state of the Ready signal (I/P Pin 23) from the selected disk drive. When this bit is set, the drive is present, but may not be ready for read/write transfer.

Bit 7 BUSY: When this bit is set, the controller is executing a command. Also, when this bit is set, the HOST may not read or write any other task files except the AT HOST CONTROLLER/DRIVE STATUS REGISTER.

B. HOST FIXED DISK REGISTER (Write Only)

This fixed disk register is used by the HOST to control some of the internal functions. Its I/O port address is 3F6H/376H.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	HS3EN	RST	INTEN	X

Bit 0, 4 ~ 7: Don't care.

Bit 1 INTERRUPT ENABLE: This bit, when reset, enables the IRQ14 (Pin 45) output. When this bit is set, the IRQ14 output is tri-state, regardless of the presence or absence of a pending interrupt. The internal signal and the status will still be valid.

Bit 2 SOFTWARE RESET: Writing a 1 to this bit will cause this IC to be reset. The reset output will be asserted and will remain asserted until this bit is written back to 0.

Bit 3 HEAD SELECT 3 ENABLE: When this bit is set, the Head Select 3 will be output by the local micro controller. When this bit is reset, the Reduce Write Current will be output by the local microcontroller.

C. MICROCONTROLLER STATUS REGISTER (Read Only)

This register is used to indicate the status of operation and drive for the microcontroller. It's I/O address is 6000H.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	WF	HS3ENB	HS3EN	RDY	SC	ML	DRQ

Bit 1 MFM or RLL mode: When set, it indicates the drive is a MFM recorded drive.

Bit 4, 5 HEAD SELECT 3 ENABLE: These two bits are used to select the Head Select 3 or the Reduce Write Current Operation. The bit 4 reflects the bit 3 of host fixed disk register.

Others are the same as the HOST CONTROLLER/DRIVE STATUS REGISTER.

D. MICROCONTROLLER COMMAND REGISTER (Write Only)

This register is used to control the data operation and sends out the status of the operation. Its I/O address is 8000H sent from the microcontroller.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SBUSY	SETINT	SDRQB	DMAWRB	CRESETB	LONG	CORD	ERROR

Bit 0 ERROR: This bit indicates that a non-recoverable error has occurred. The error information is stored in the buffer and this bit is connected to the bit 0 of HOST CONTROLLER/DRIVE STATUS Register.

Bit 1 ECC CORRECTION DATA: This bit is connected to the bit 2 of HOST CONTROLLER/DRIVE STATUS REGISTER as a report for the data correction.

Bit 2 LONG: When this bit is set, it is used to indicate the Long Command for the read/write operation. This bit must be set before transferring data between Host and buffer for read/write LONG command.

Bit 3 ACKNOWLEDGE RESET: This bit is used to set the Acknowledge signals for the read/write operations of the HDC.

Bit 4 DMA READ/WRITE CONTROL: This bit is set for the read operation of HDC from the drive. When reset, it indicates a write operation of HDC to the drive.

Bit 5 SET DATA REQUEST: This bit, when reset, sets the DRQ bit in Status Register.

Bit 6 SET INTERRUPT: When changed from low to high, this bit is used to set the interrupt request to the HOST.

Bit 7 SBUSY: This bit is used to set the BUSY bit of the HOST CONTROLLER/DRIVE STATUS REGISTER to indicate that the μC is busy except when DRQ is asserted.

E. MICROCONTROLLER READ/WRITE I/O PORT

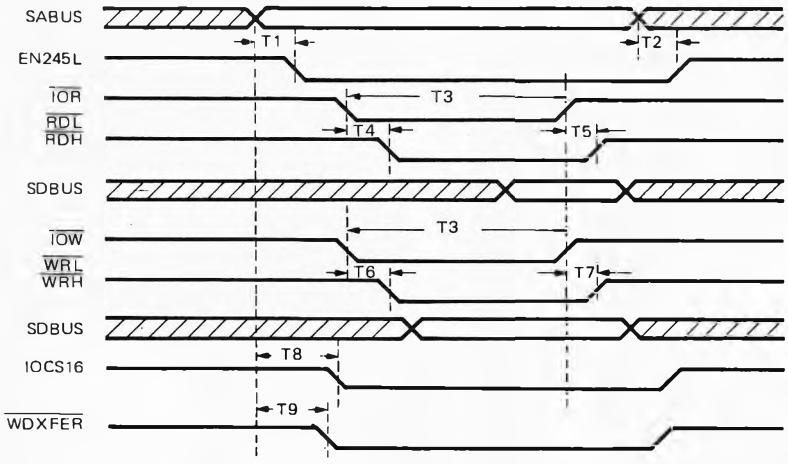
Writing to the A000H port will clear the bit 7 (BUSY) of the HOST CONTROLLER/DRIVE STATUS REGISTER if the SBUSY bit is reset.

Reading from the A000H port will generate a low-active pulse to initiate the buffer (SRAM) control signals.

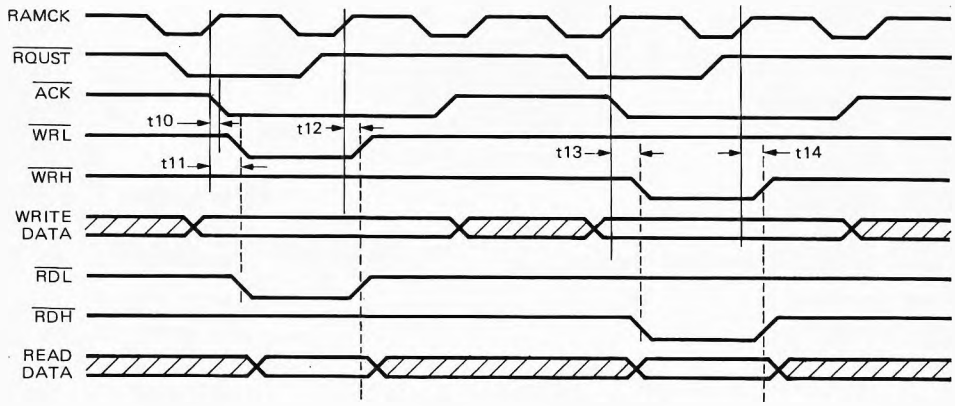
Writing to the C000H port will reset the bit 3 (DRQ) of the HOST CONTROLLER/DRIVE STATUS REGISTER and clear the internal interrupt (IRQ14) to the host.

Writing to the E000H port will set the bit 3 (DRQ) of the HOST CONTROLLER/DRIVE STATUS REGISTER.

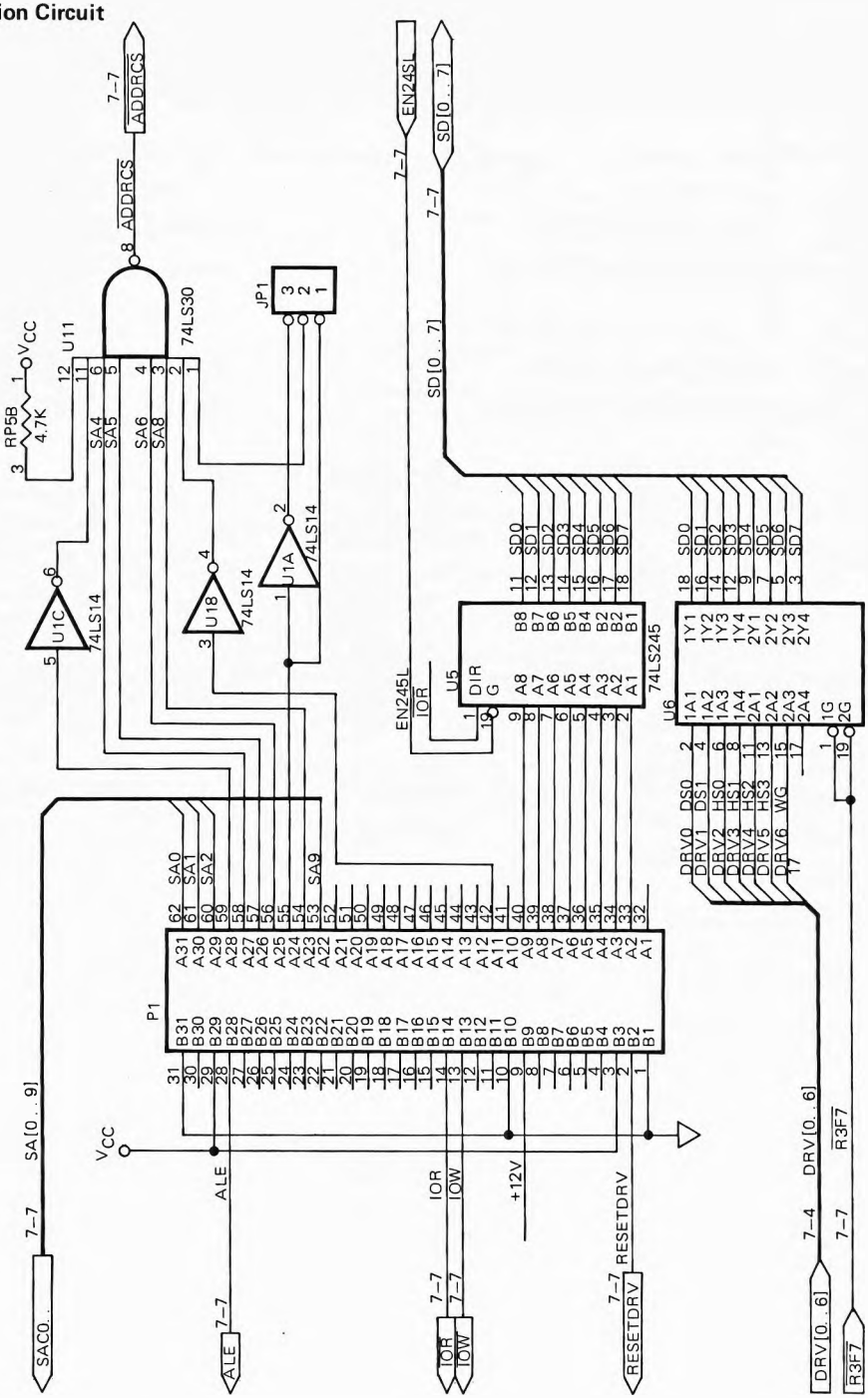
Host Interface Timing



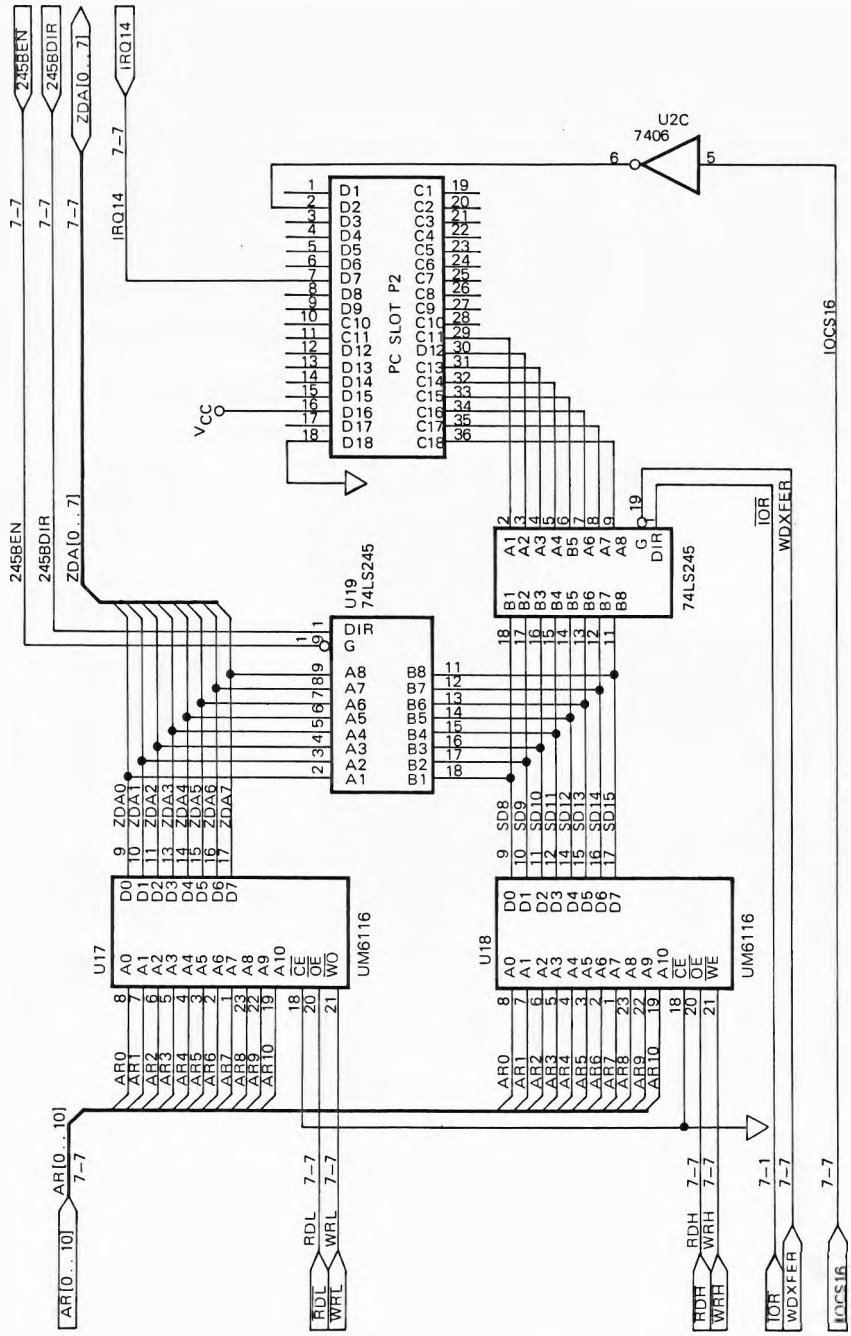
DMA Read/Write Timing



Application Circuit



Application Circuit (Continued)



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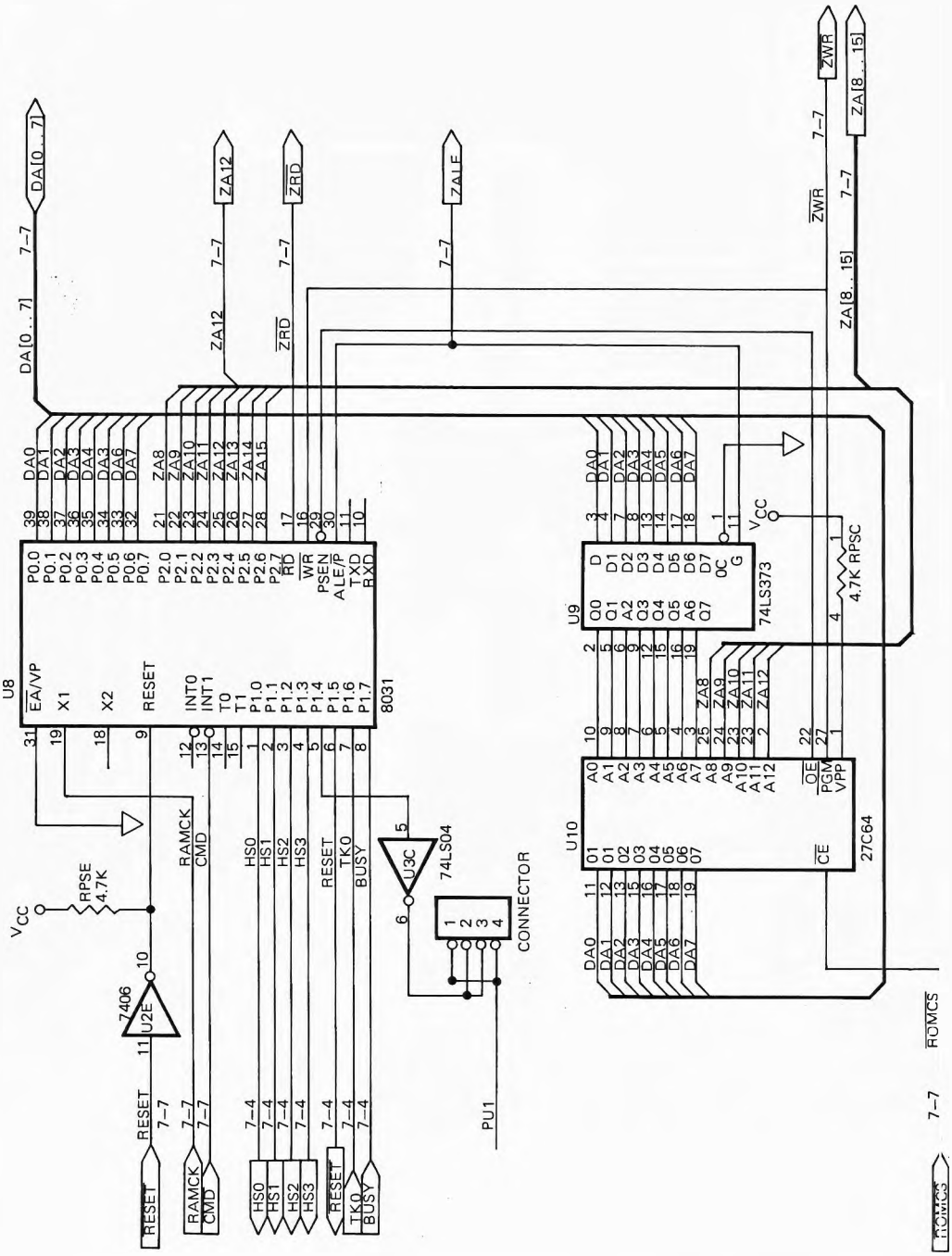

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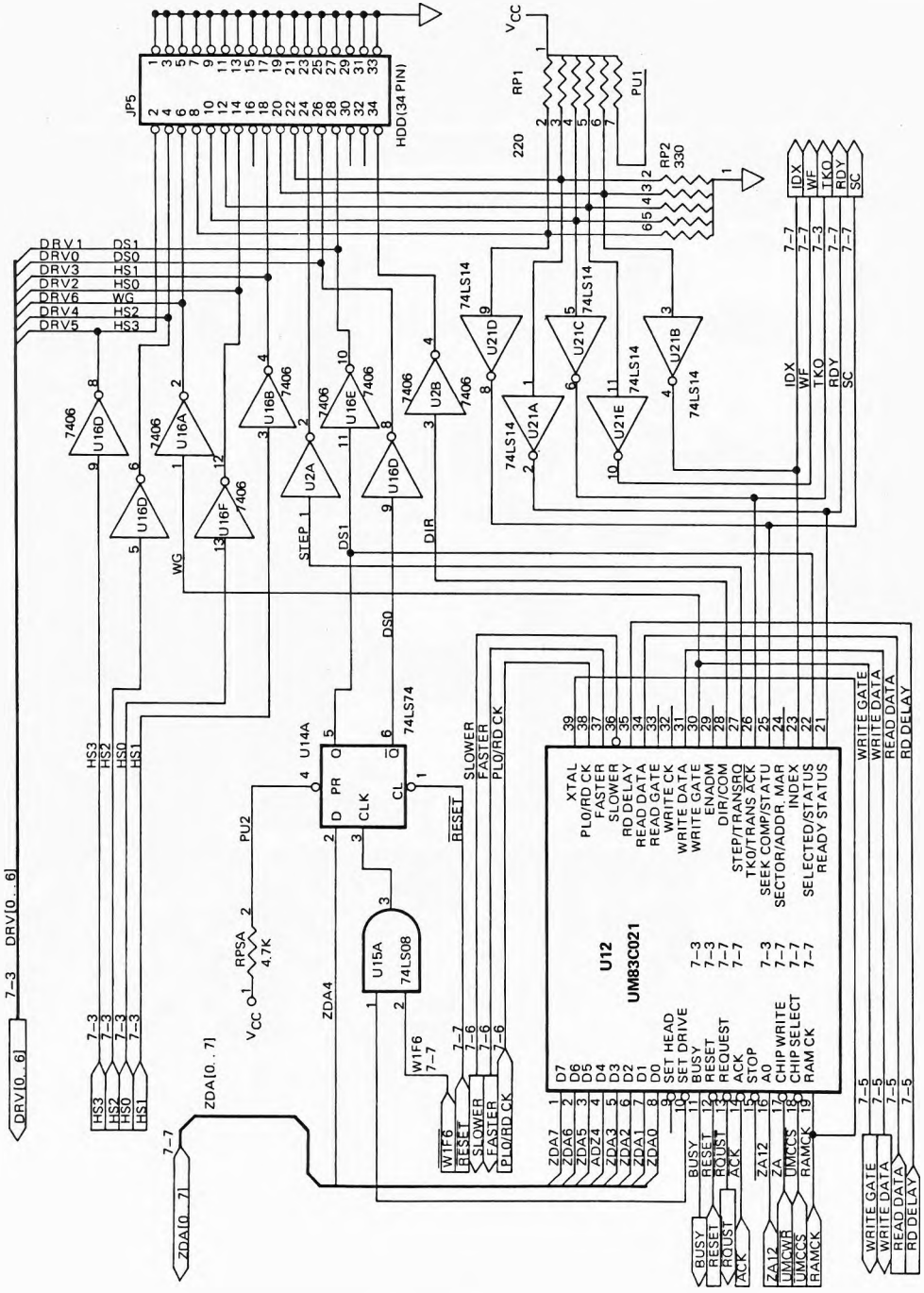

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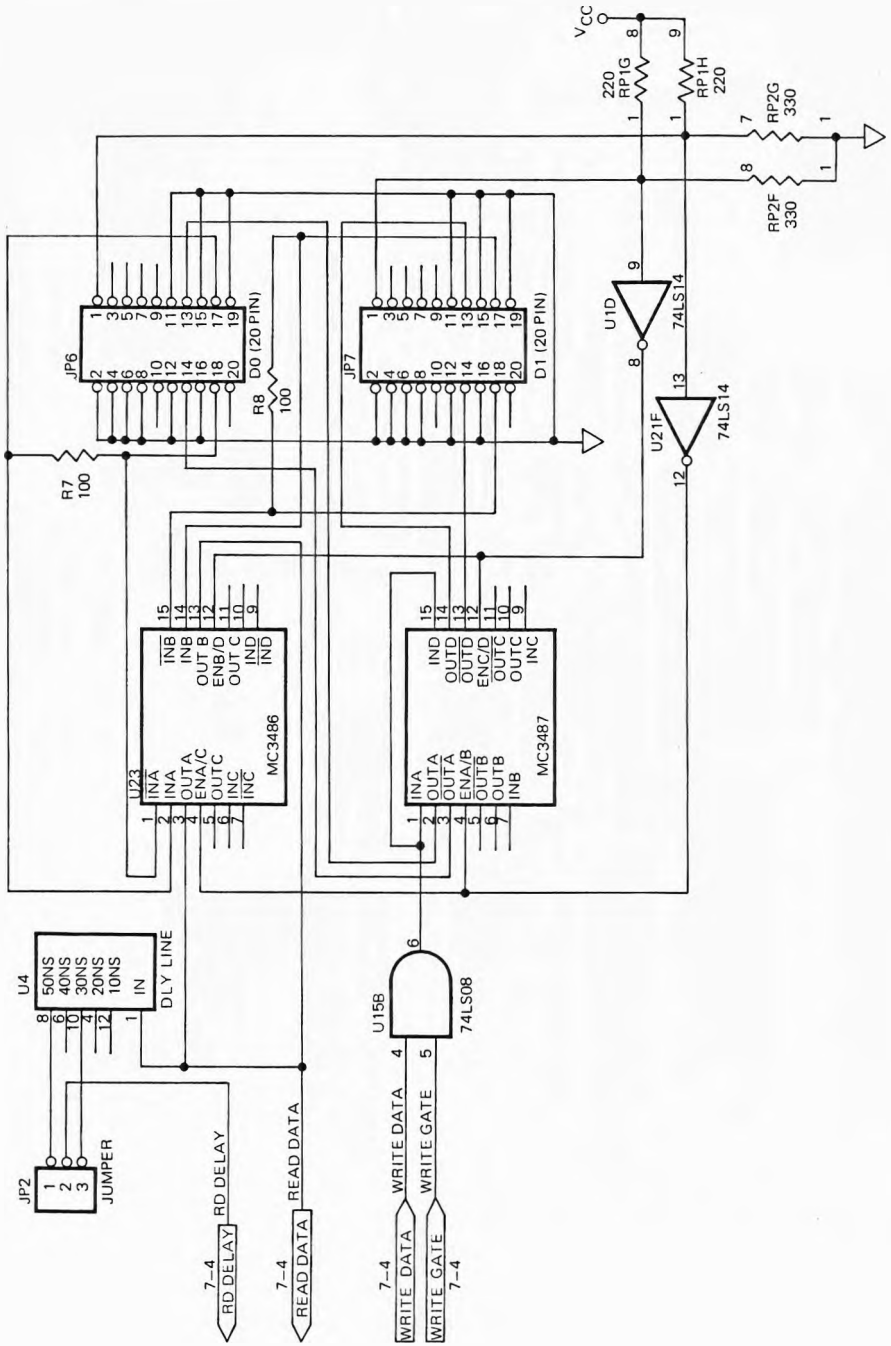
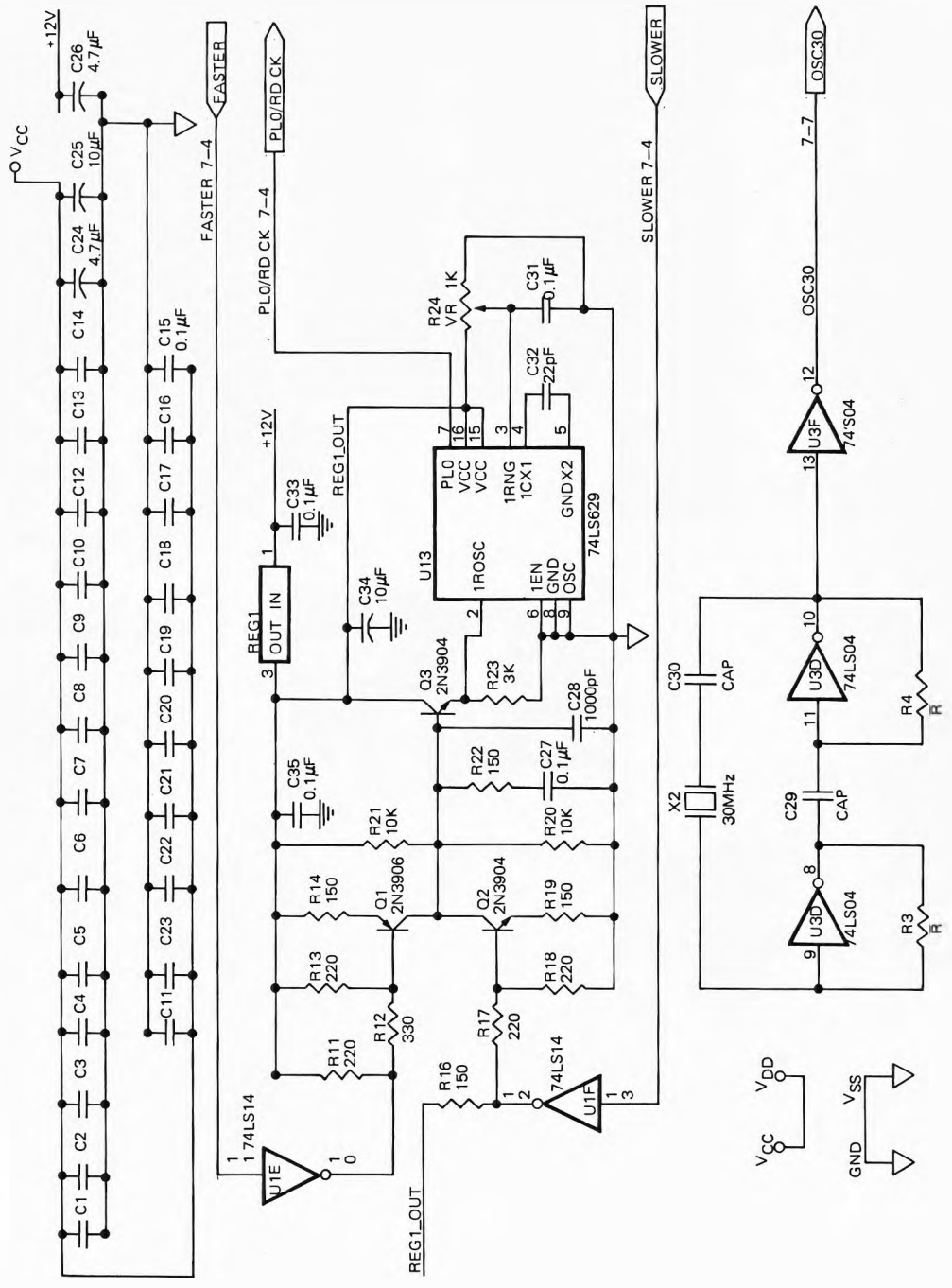
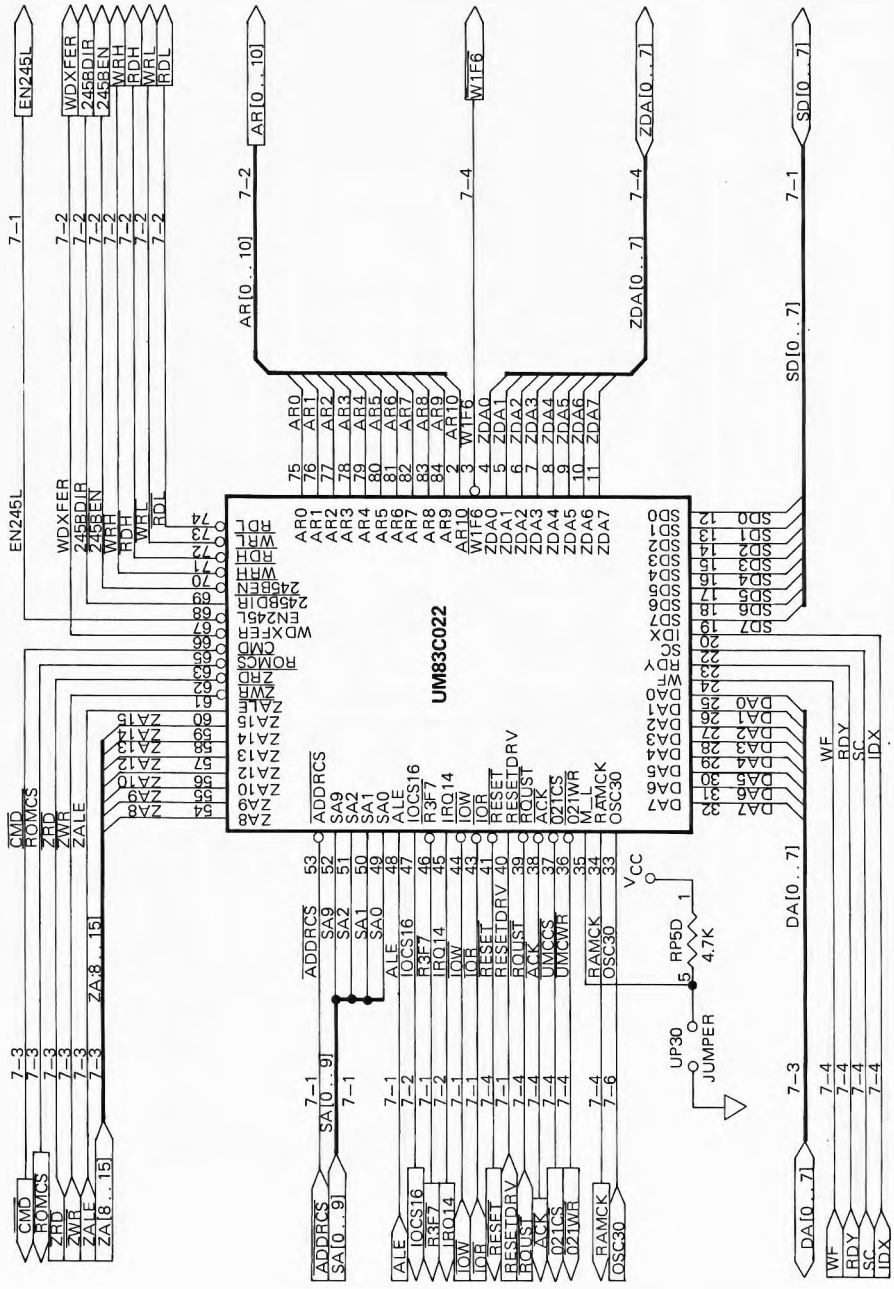


Application Circuit (Continued)



Application Circuit (Continued)



B. AT Interface I/O port

Task file – primary 1F0H to 1F7H (Secondary 170H to 177H) and 3F6H to 3F7H (Secondary 376H to 377H)

Primary	Secondary	$\overline{\text{Addrcs}}$	SA9	SA2	SA1	SA0	Read Port Function	Write Port Function
1F0H	170H	0	0	0	0	0	Read data (16 bits)	Write data (16 bits)
1F1H	171H	0	0	0	0	1	Error register	Write precomp cylinder
1F2H	172H	0	0	0	1	0	Sector count	Sector count
1F3H	173H	0	0	0	1	1	Sector number	Sector number
1F4H	174H	0	0	1	0	0	Cylinder number low	Cylinder number low
1F5H	175H	0	0	1	0	1	Cylinder number high	Cylinder number high
1F6H	176H	0	0	1	1	0	SDH	SDH
1F7H	177H	0	0	1	1	1	Status Register	Command register
3F6H	376H	0	1	1	1	0	Alternate status register	Fixed disk register
3F7H	377H	0	1	1	1	1	Digital input register	Not used

C. Microcontroller Task File Read/Write Port

HEX	READ PORT FUNCTION	WRITE PORT FUNCTION
27F9	write precomp register	error register
27FA	sector count	sector count
27FB	sector number	sector number
27FC	cylinder number low	cylinder number low
27FD	cylinder number high	cylinder number high
27FE	SDH	SDH
27FF	host command register	not used

D. Constraints

The PC/AT HDC supports two ST-506/412 Winchester disk drives. The host bus has to be IBM PC/AT BUS or compatible. The BIOS command set must be compatible to the original BIOS of IBM PC/AT. If RLL encoded drive is used, the BIOS must also contain RLL drive type or user defined drive type. If running on network environment, it might not be compatible to WD's HDC.