UM82C852

PRELIMINARY

Multi I/O For XT

Features

- Supports game port
- Supports 2nd serial port
- Centronics printer interface
- Independent control of transmit, receive, line status and data set interrupts
- Individual modem control signals
- Programmable serial interface characteristics:
  - 5, 6, 7, or 8 bit characters
  - Even, odd or no-parity bit generation and detection
  - 1, 1½, or 2 stop bit generation
- Milliseconds through month counters for real time clock
- 56 bits of RAM with comparator to compare the real time counter to the RAM data
- POWER DOWN input that disables all inputs and outputs
- Disables the chip from the reset of the system for standby low power operation by use of a POWER DOWN input
- 32,768 Hz crystal for real time clock
- Four-year calendar (no leap year)
- 24-hour clock

General Description

The Multi-I/O chip, UM82C852 is an integrated chip of UM82C450, UM82C11, UM82C8167. This chip is a Multi-I/O for PC/XT and PS2 model 30.

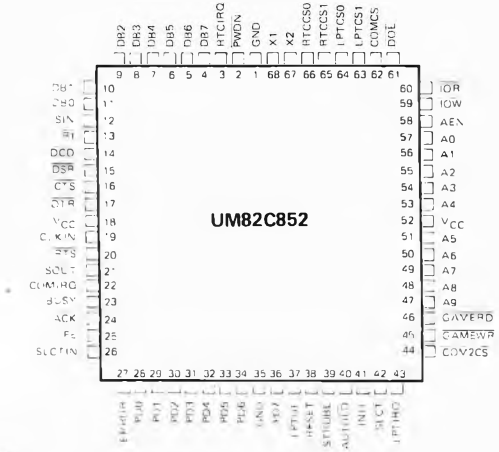
The UM82C450 asynchronous communications element (ACE) performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion of data characters transmitted by the CPU. The complete status of the ACE can be read at any time during functional operation by CPU. The information obtained includes the type and condition of the transfer operations being performed and error conditions.

The UM82C11 parallel port provides the user with a bi-directional parallel data port that fully supports the parallel Centronics type printer.

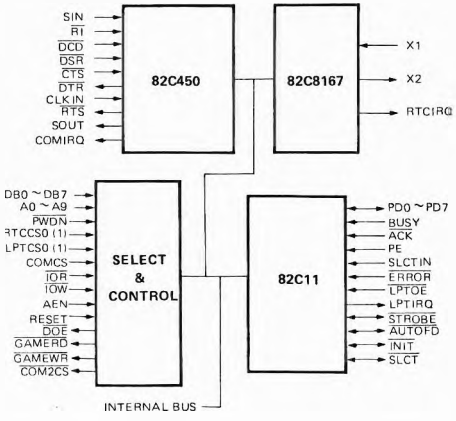
The UM82C8167 real time clock includes an addressable real time counter, 56 bits of static RAM with an on chip oscillation circuit which can generate the 32,768 Hz time base.

The UM82C852 is packaged in a 68-pin plastic leaded chip carrier.

Pin Configuration



Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
2	$\overline{PWDN}$	I	POWER DOWN – This input disables all inputs and outputs.
3	RTCIRQ	O	RTC INTERRUPT REQUEST – This is a RTC interrupt request when a RAM/real time counter comparison occurs.
4 ~ 11	DB 0 ~ DB7	I/O	DATA BUS – This data bus provides I/O lines for the transfer of data between CPU and the chip.
12	SIN	I	SERIAL INPUT – This line is used to receive serial data from the communication line.
13	$\overline{RI}$	I	RING INDICATOR – When low, indicates that a telephone ringing signal has been received by the MODEM or data set.
14	$\overline{DCD}$	I	DATA CARRIER DETECT – When low, indicates that the data carrier has been detected by the MODEM or data set.
15	$\overline{DSR}$	I	DATA SET READY – When low, indicates that the MODEM or data set is ready to establish the communication.
16	$\overline{CTS}$	I	CLEAR TO SEND – When low, indicates that the MODEM or data set is ready to receive data.
17	$\overline{DTR}$	O	DATA TERMINAL READY – When low, informs the MODEM or data set that the ACE is ready to communicate.
19	CLKIN	I	CLOCK INPUT – The external clock for UM82C450.
20	$\overline{RTS}$	O	REQUEST TO SEND – When low, informs the MODEM or data set that the ACE is ready to transmit data.
21	SOUT	O	SERIAL OUTPUT – Composite serial data output to the communications link.
22	COMIRQ	O	COM INTERRUPT REQUEST – ACE interrupt request.
23	BUSY	I	BUSY STATE – When high, printer can't receive data.
24	$\overline{ACK}$	I	ACKNOWLEDGE – When low, indicates that the data has been received and the printer is ready to accept other data.
25	PE	I	PAPER END – When high, indicates that the printer is out of paper.
26	SLCTIN	I	SELECT IN – This is always high unless the printer is down.
27	$\overline{ERROR}$	I	ERROR – When low, the printer has encountered an error condition.
28 ~ 34, 36	PD0 ~ PD7	I/O	PARALLEL DATA BUS – This bus provides a byte-wide bi-direction data port to the system.
37	$\overline{LPTOE}$	I	LINE PRINTER OUTPUT ENABLE – When low, the printer data output (PD0 ~ PD7) enables.
38	RESET	I	When high, forces the 82C450 and 82C11 to an idle state.
39	$\overline{STROBE}$	I/O	DATA STROBE – When low, the printer reads in the data on printer data bus PD0 ~ PD7, open collector output.
40	$\overline{AUTOFD}$	I/O	AUTO FEED – When low, the printer adds line-feed after a line is printed, open collector output.
41	$\overline{INIT}$	I/O	INITIAL – When low, the printer buffer is cleared, open collector output.

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
42	$\overline{SLCT}$	I/O	PRINTER SELECT – When low, the printer is selected, open collector output.
43	LPTIRQ	O	PRINTER INTERRUPT REQUEST – Printer interrupt request.
44	$\overline{COM2CS}$	O	COM2 CHIP SELECT – When low, COM2 is selected.
45	$\overline{GAMERD}$	O	GAME READ – When low, game port read enables.
46	$\overline{GAMEWR}$	O	GAME WRITE – When low, game port write enables.
47 ~ 51 53 ~ 57	A0 ~ A9	I	ADDRESS BUS – These address lines are used to select chip and internal register during CPU cycle.
58	AEN	I	DMA ADDRESS ENABLE – When high, DMA cycle. When low, CPU cycle.
59	$\overline{IOW}$	I	I/O WRITE – When low, CPU write data to data bus.
60	$\overline{IOR}$	I	I/O READ – When low, CPU read data from data bus.
61	$\overline{DOE}$	O	DATA OUTPUT ENABLE – When low, CPU read/write data to this chip.
62	COMCS	I	COM SELECT – COM address select.
63 ~ 64	LPTCS0 ~ LPTCS1	I	PRINTER SELECT – Printer address select.
65 ~ 66	RTCCS0 ~ RTCCS1	I	RTC SELECT – RTC address select.
67 ~ 68	X1, X2	I	32.768 KHz real time clock crystal input.
18, 52	V_{CC}	I	Power supply.
1, 35	GND	I	Ground.

Function Description:

(a) I/O Port Address:

(i) Parallel port:

LPTCS1	LPTCS0	Address	Comment
0	0	3BC ~ 3BE	LPT1
0	1	378 ~ 37A	LPT2
1	0	278 ~ 27A	LPT3
1	1	–	Disable

(ii) Asynchronous communication port:

COMCS	COM1 Address	COM2 Address
0	3F8 ~ 3FF	2F8 ~ 2FF
1	2F8 ~ 2FF	3F8 ~ 3FF

(iii) Real time clock:

RTCCS1	RTCCS0	Address	Comment
0	0	240 ~ 25F	RTC1
0	1	340 ~ 35F	RTC2
1	0	0E0 ~ 0EF 0B0 ~ 0BF	RTC3
1	1	–	Disable

(iv) Game port:

Address
201

(b) Serial Channel Registers

Three types of internal registers are used in the serial channel of the UM82C852. They are used in the operation of the device and are the control status and data registers. The control registers are the Bit Rate Select Register DLL (Divisor Latch LSB) and DLM (Divisor Latch MSB). Line Control Register Interrupt Enable Register and the Modem Control registers while the status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and the Transmitter Holding Register. The Address Read and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register [LCR (7)] to select the register to be written or read (see Table 1). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. An example LCR (7) refers to Line Control Register Bit 7.

The Transmitter Buffer Register and Receiver Buffer Register are data registers holding from five to eight bits of data. If less than eight data bits are transmitted data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The UM82C852 data registers are double-buffered so that read and write operations can be performed at the same time the UART is performing the parallel-to-serial and serial-to-parallel conversion.

The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory. The contents of the LCR are described as follows:

LCR (0) Word Length Select Bit 0 (WLS0)
LCR (1) Word Length Select Bit 1 (WLS1)
LCR (2) Stop Bit Select (STB)
LCR (3) Parity Enable (PEN)
LCR (4) Even Parity Select (EPS)
LCR (5) Stick Parity
LCR (6) Set Break
LCR (7) Divisor Latch Access Bit (DLAB)

LCR (0) and LCR (1) word length select bit 1: The number of bits in each serial character is programmed as shown in the following chart:

LCR (1)	LCR (0)	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

LCR (2) Stop Bit Select: LCR (2) specifies the number of stop bits in each transmitted character. If LCR (2) is a logic 0, one stop bit is generated in the transmitted data. If LCR (2) is a logic 1 when a 5-bit word length is selected, 1.5 stop bits are generated. If LCR (2) is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The receiver checks for two stop bits if programmed.

LCR (3) Parity Enable: When LCR (3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

Table 1. Serial Channel Internal Registers

DLAB	A2	A1	A0	Mnemonic	Register
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status Register
X	1	1	1	SCR	Scratch Register
1	0	0	0	DLL	Divisor Latch (LSB)
1	0	0	1	DLM	Divisor Latch (MSB)

X = "Don't Care" 0 = Logic Low 1 = Logic High

LCR (4) Even Parity Select: When parity is enabled (LCR (3) = 1). LCR (4)-0 selects odd parity, and LCR (4) = 1 selects even parity.

LCR (5) Stick Parity: When parity is enabled (LCR (3) = 1), LCR (5) = 1 causes the transmission and reception of a parity bit to be in the opposite state from that indicated by LCR (4). This allows the user to force parity to a known state and for the receiver to check the parity bit in a known state.

LCR (6) Break Control: When LCR (6) is set to a logic "1", the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by setting LCR (6) to a logic "0". The Break Control bit acts only on SOUT and has no effect on the transmitter logic. Break Control enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all "0" pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the transmitter to be idle (TEMT = 1, and clear break when normal transmission has to be restored.

LCR (7) Divisor Latch Access Bit (DLAB): LCR (7) must be set high (logic "1") to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR (7) must be input low to access the Receiver Buffer the Transmitter Holding or the Interrupt Enable Registers.

The Line Status Register (LSR) is a single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the serial channel of the UM82C852.

Three error flags OE, FE, and PE provide the status of any error conditions detected in the receiver circuitry. During reception of the stop bits the error flags are set high by an error condition. The error flags are not reset by the absence of an error condition in the next received character. The flags reflect the last character only if no overrun occurs. The Overrun Error character in the Receiver Buffer Register has been over-written by a character from the Receiver Shift Register before being read by the CPU. The character is thereby lost. Framing Error (FE) indicates that the last character received contained incorrect (low) stop bits. This is caused by the absense

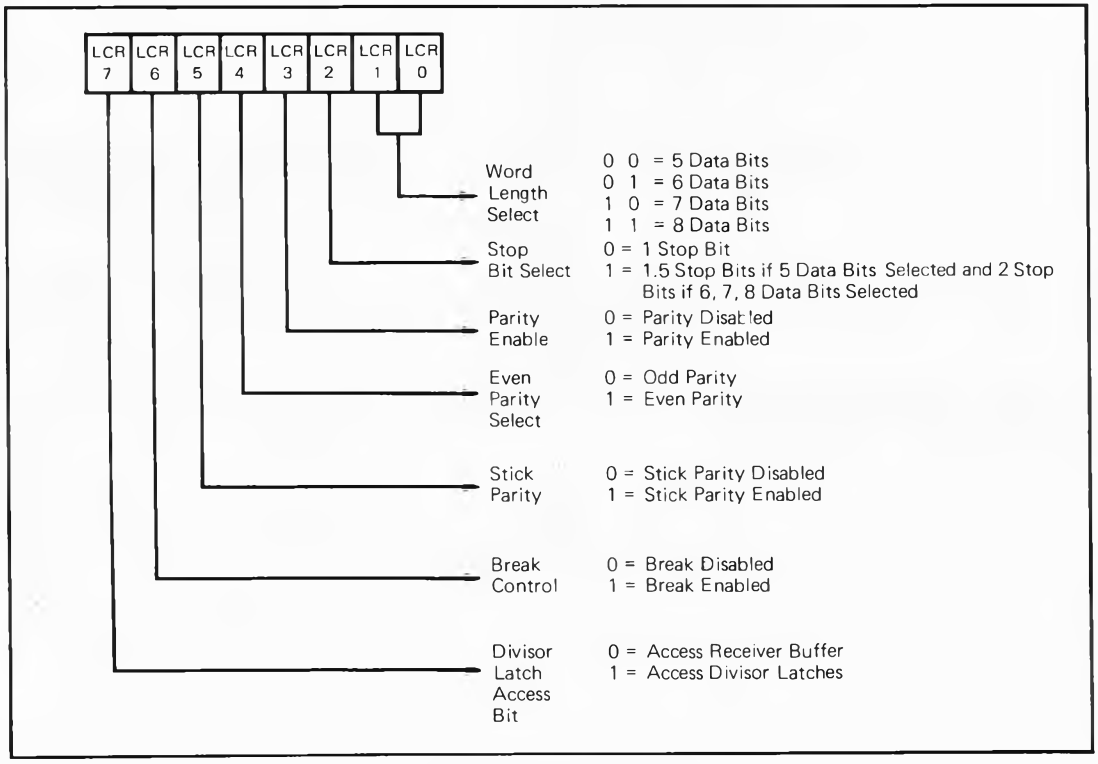


Figure 1. Line Control Register

of the required stop bit or by a stop bit too short to be detected. Parity Error (PE) indicates that the last character received had a parity error based on the programmed and calculated parity of the received character.

The Break Interrupt (BI) status bit indicates that the last character received was a break character. A break character is an invalid data character. However, it is an entire character including parity and stop bits.

The Transmitter Holding Register Empty (THRE) bit indicates that the THR register is empty and may receive another character. The Transmission Shift Register Empty (TEMT) bit indicates that the Transmitter Shift Register is empty and the serial channel has completed transmission of the last character to be sent. If the interrupt is enabled [IER (1)] an active THRE causes an interrupt (INTRPT).

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Reading the LSR clears LSR (1)-LSR (4). (OE, PE, FE, and BI).

The contents of the Line Status Register shown in Table 2 are described below:

LSR (0) Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR (0) is reset low by a CPU read of the data in the Receiver Buffer Register.

LSR (1) Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR (2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit [LCR (4)]. The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

LSR (3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR (3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR.

LSR (4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start bit + data bits + parity ÷ stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

LSR (1)-LSR (4) are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER(2) = 1 in the Interrupt Enable Register.

LSR (5) Transmitter Holding Register Empty (THRE) THRE: indicates that the UM82C852 is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register LSR (5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR (5) is not reset by a CPU read of the LSR.

When the THRE interrupt is enabled (IER (1) = 1). THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR (6) Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the

Table 2. Line Status Register Bits

LSR Bits		Logic 1	Logic 0
LSR (0)	Data Ready (DR)	Ready	Not Ready
LSR (1)	Overrun Error (OE)	Error	No Error
LSR (2)	Parity Error (PE)	Error	No Error
LSR (3)	Framing Error (FE)	Error	No Error
LSR (4)	Break Interrupt (BI)	Break	No Break
LSR (5)	Transmitter Holding Register Empty (THRE)	Empty	Not Empty
LSR (6)	Transmitter Empty (TEMT)	Empty	Not Empty
LSR (7)	Not Used		

Transmitter Shift Register (TSR) are both empty. LSR (6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR.

LSR (7): This bit is always 0.

The Modem Control Register (MCR) controls the interface with the modem or data set as described in Table 3. MCR can be written and read. The $\overline{RTS}$ and $\overline{DTR}$ outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins. MCR Bits 0, 1, 3, and 4 are shown below:

MCR (0): When MCR (0) is set high the $\overline{DTR}$ output is forced low. When MCR (0) is reset low, the $\overline{DTR}$ output is forced high. The $\overline{DTR}$ output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR (1): When MCR (1) is set high, the RTS output is forced low. When MCR (1) is reset low, the RTS output is forced high. The $\overline{RTS}$ output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR (3): When MCR (3) is set high, the INT output is enabled.

MCR (4): MCR (4) provides a local loopback feature for diagnostic testing of the channel. When MCR (4) is set high, Serial Output (SOUT) is set to the marking (logic "1") state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The three modem control inputs ($\overline{CTS}$, $\overline{DSR}$, and $\overline{RI}$) are disconnected. The modem control outputs ($\overline{DTR}$ and $\overline{RTS}$) are internally connected to the four modem control inputs. The modem control output pins are forced to their inactive state (high).

In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel. Bits MCR (5)-MCR (7) are permanently set to logic 0.

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs by accessing the data bus interface of the UM82C852. In addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines for each channel are $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$ and $\overline{DCD}$, MSR (4) - MSR (7) are status indications of these lines. The status indications follow the status of the input lines. If the modem status interrupt in the Interrupt Enable Register is enabled [IER (3)], a change of state in a modem input signal will be reflected by the modem status bits in the IIR register, and an interrupt (INTRPT) is generated. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described in Table 4. Note that the State (high or low) of the status bits are inverted versions of the actual input pins.

MSR (0) Delta Clear to Send (DCTS): DCTS indicates that the $\overline{CTS}$ input to the serial channel has changed state since the last time it was read by the CPU.

Table 3. Modem Control Register Bits

MCR Bits		Logic 1	Logic 0
MCR (0)	Data Terminal Ready (DTR)	$\overline{DTR}$ Output Low	$\overline{DTR}$ Output High
MCR (1)	Request to Send (RTS)	$\overline{RTS}$ Output Low	$\overline{RTS}$ Output High
MCR (2)	0		
MCR (3)	Interrupt (INT) Enable	INT Enabled	INT Disabled
MCR (4)	Loop	Loop Enabled	Loop Disabled
MCR (5)	0		
MCR (6)	0		
MCR (7)	0		

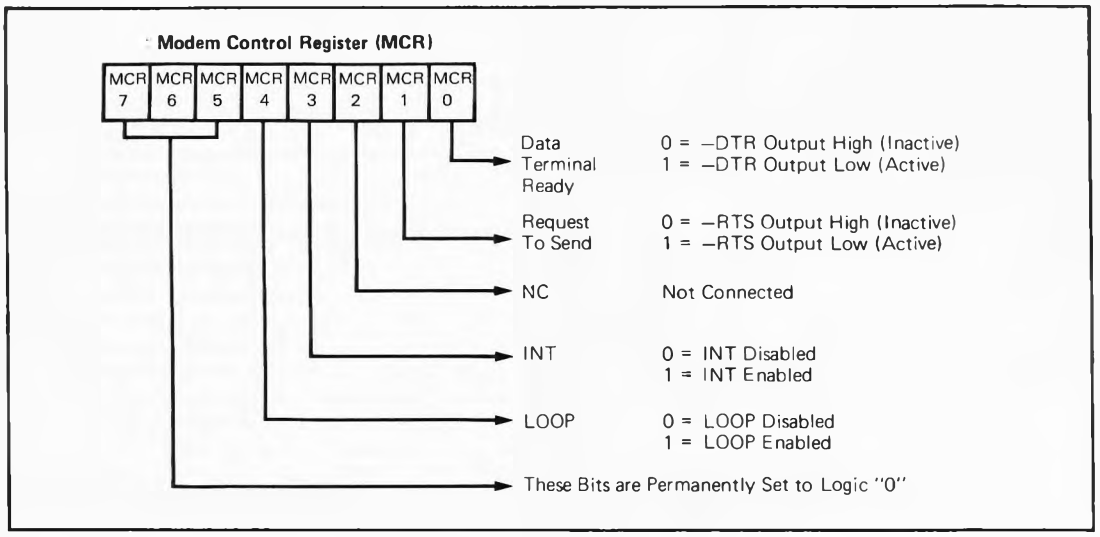


Figure 2. Modem Control Register

Table 4. Modem Status Register Bits

MSR Bit	Mnemonic	Description
MSR (1)	DDSR	Delta Data Set Ready
MSR (2)	TERI	Trailing Edge of Ring Indicator
MSR (0)	DCTS	Delta Clear to Send
MSR (3)	DDCD	Delta Data Carrier Detect
MSR (4)	$\overline{CTS}$	Clear To Send
MSR (5)	$\overline{DSR}$	Data Set Ready
MSR (6)	$\overline{RI}$	Ring Indicator
MSR (7)	$\overline{DCD}$	Data Carrier Detect

MSR (1) Delta Data Set Ready (DDSR): DDSR indicates that the $\overline{DSR}$ input to the serial channel has changed state since the last time it was read by the CPU.

MSR (2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the $\overline{RI}$ input to the serial channel has changed state from high to low since the last time it was read by the CPU. Low to high transitions on $\overline{RI}$ do not activate TERI.

MSR (3) Delta Data Carrier Detect (DDCD): DDCD indicates that the $\overline{DCD}$ input to the serial channel has changed state since the last time it was read by the CPU.

MSR (4) Clear to Send (CTS): Clear to Send (CTS) is the status of the $\overline{CTS}$ input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter, output (SOUT). If the serial channel is in loop mode [MSR (4) = 1]. MSR (4) is equivalent to $\overline{RTS}$ in the MCR.

MSR (5) Data Set Ready (DSR): Data Set Ready (DSR) is a status of the $\overline{DSR}$ input from the modem to the serial channel which indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the channel is in the loop mode [MCR (4) = 1], MSR (5) is equivalent to DTR in the MCR.

MSR (6) Ring Indicator: Indicates the status to the RI input (pin 39). If the channel is in the loop mode [MCR (4) = 1], MSR (6) is not connected in the MCR.

MSR (7) Data Carrier Detect: Data Carrier Detect indicates the status of the Data Carrier Detect ($\overline{DCD}$) input. If the channel is in the loop mode [MCR (4) = 1], MSR (4) is equivalent to OUT2 of the MCR.

The modem status inputs (RI, $\overline{DCD}$, $\overline{DSR}$, and $\overline{CTS}$) reflect the modem input lines with any change of status. Reading the MSR register will clear the delta modem status indications but has no effect on the status bits. The status bits reflect the state of the input pins regardless of the mask control signals. If a DCTS, DDSR, TERI, or DDCD are true, and a state change occurs during a read operation ($\overline{IOR}$), the state change is not indicated in the MSR. If DCTS, DDSR, TERI, or DDCD are false, and a state change occurs during a read operation, the state change is indicated after the read operation.

For LSR and MSR, the setting of status bits ($\overline{IOR}$) is inhibited during status register read operations. If a status condition is generated during a read operation. ($\overline{IOR}$), the status bit is not set until the trailing edge of the read ($\overline{IOR}$).

If a status bit is set during a read $\overline{IOR}$ operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read $\overline{IOR}$ instead of being set again.

The UM82C852 serial channel contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 3.1 MHz) by any divisor from 1 to $2^{16}-1$ (see also BRG description). The output frequency of the Baud Generator is 16X the data rate [divisor # = clock ÷ (baud rate x 16)]. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These Divisor Latch registers must be loaded during initialization. Upon loading either of the Divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

The receiver circuitry in each serial channel of the UM82C852 is programmable for 5, 6, 7, or 8 data bits per character. For words of less than 8 bits, the data is right justified to the least significant bit LSB = Data Bit 0 [RBR (0)]. Data Bit 0 of a data word [RBR (0)] is the first data bit received. The unused bits in a character less than 8 bits are output low to the parallel output by the serial channel.

Received data at the SIN input pin is shifted into the Receiver Shift Register by the 16X clock provided at the CLKIN input. This clock is synchronized to the incomplete data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. The DR flag in the LSR register is set.

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the serial channel, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in the RBR before complete reception of the next character results in the loss of the data in the Receiver Register. The OE flag in the LSR register indicates the overrun condition.

RBR Bits 0 thru 7:

RBR (0)	Data Bit 0
RBR (1)	Data Bit 1
RBR (2)	Data Bit 2
RBR (3)	Data Bit 3
RBR (4)	Data Bit 4
RBR (5)	Data Bit 5
RBR (6)	Data Bit 6
RBR (7)	Data Bit 7

The Transmitter Holding Register (THR) holds parallel data from the data bus (D0-D7) until the Transmitter Shift Register is empty and ready to accept a new character for transmission. The transmitter and receiver word length and number of stop bits are the same. If the character is less than eight bits, unused bits at the microprocessor data bus are ignored by the transmitter.

Data Bit 0 [THR (0)] is the first serial data bit transmitted. The THRE flag [LSR (5)] reflects the status of the THR. The TEMT flag [LSR (5)] indicates if both the THR and TSR are empty.

THR Bits 0 thru 7

THR (0)	Data Bit 0
THR (1)	Data Bit 1
THR (2)	Data Bit 2
THR (3)	Data Bit 3
THR (4)	Data Bit 4
THR (5)	Data Bit 5
THR (6)	Data Bit 6
THR (7)	Data Bit 7

The Scratchpad Register is an 8-bit Read/Write register that has no effect on either channel in the UM82C852 It is intended to be used by the programmer to hold data temporarily.

SCR Bits 0 thru 7

SCR (0)	Data Bit 0
SCR (1)	Data Bit 1
SCR (2)	Data Bit 2
SCR (3)	Data Bit 3
SCR (4)	Data Bit 4
SCR (5)	Data Bit 5
SCR (6)	Data Bit 6
SCR (7)	Data Bit 7

Interrupts

The Interrupt Identification Register (IIR) in the serial channel of the UM82C852 has interrupt capability for interfacing to current microprocessors. In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver Line Status (priority 1)
2. Received Data Ready (priority 2)
3. Transmitter Holding Register Empty (priority 3)
4. Modem Status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the interrupt Identification Register (IIR). When addressed during

chip select time, the IIR indicates the highest priority interrupt pending. No other interrupts are acknowledged until the interrupt is serviced by the CPU. The logic equivalent of the interrupt control circuit is shown in Figure 3. The contents of the IIR are indicated in Table 5 and are described below.

IIR (0): IIR (0) can be used in either a hard-wired prioritized or polled environment to indicate whether an interrupt is pending. When IIR (0) is low, an interrupt is pending, and IIR contents may be used as a pointer to the appropriate interrupt service routine. When IIR (0) is high, no interrupt is pending.

IIR (1) and IIR (2) are used to identify the highest priority interrupt pending as indicated in Table 5.

IIR (3)-IIR (7): These five bits of the IIR are logic 0.

The Interrupt Enable Register (IER) is a Write register used to independently enable the four serial channel interupts which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER (0)-IER (3) of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The content of the Interrupt Enable Register is described in Table 6 and below.

IER (0): When programmed high [IER (0) = Logic 1], IER (0) enables Received Data Available Interrupt.

IER (1): When programmed high [IER (1) = Logic 1], IER (1) enables the Transmitter Holding Register Empty interrupt.

IER (2): When programmed high [IER (2) = Logic 1], IER (2) enables the Receiver Line Status interrupt.

IER (3): When programmed high [IER (3) = Logic 1], IER (3) enables the Modem Status Interrupt.

IER (4)-IER (7): These four bits of the IER are logic 0.

Transmitter

The serial transmitter section consists of a Transmitter Holding Register (THR), Transmitter Shift Register (TSR), and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Shift Register Empty (TEMT) are two bits in the Line Status Register which indicate the status of THR and TSR. To transmit a 5 to 8-bit word, the word is written through DB0-DB7 to the THR. The microprocessor should perform a write operation only if THRE is high. The THRE is set high when the word is automatically transferred from the THR to the TSR during the transmission of the start bit.

When the transmitter is idle, THRE and TEMT are high. The last word written causes THRE to be reset to 0. After the transfer, THRE returns high. TEMT remains low for at least the duration of the transmission of the data word. If a second character is transmitted to the THR, the THRE is reset low. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty, THRE remains low until the TSR has completed sending the word. When the last word has been transmitted out of the TSR, TEMT is set high. THRE is set high one THR to TSE transfer time later.

Receiver

Serial asynchronous data is input into the SIN pin. The idle state of the line providing the input into SIN is high. A start bit detect circuit continually searches for a high to low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16X clock to 71/2, which is the center of the start bit. The start bit is valid if the SIN is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character (LCR (0), LCR (1)), number of stop bits LCR (2), if parity is used LCR (3), and the polarity of parity LCR (4). If Status for the receiver is provided in the Line Status Register to the Receiver Buffer Register when the Data Received indication in LSR (0) is set high, the CPU reads the Receiver Buffer Register through D0-D7. This read resets LSR (0). If D0-D7 are not read prior to a new character transfer from the RSR to the RBR, the overrun error status indication is set in LSR (1). The parity check tests for even or odd parity on the parity bit, which precedes the first stop bit. If there is a parity error, the parity error is set in LSR (2). There is circuitry which tests whether the stop bit is high. If it is not, a framing error indication is generated in LSR (3).

The center of the start bit is defined as clock count 7 1/2. If the data into SIN is a symmetrical square wave, the center of the data cells will occur within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16X clock cycle prior to being detected.

Baud Rate Generator (BRG)

The BRG generates the clocking for the UART function,

providing standard ANSI/CCITT bit rates. The clock driving the BRG is provided by the CLKIN input.

The data rate is determined by the Divisor Latch registers DLL and DLM and the external frequency. The bit rate is selected by programming the two divisor latches, Divisor Latch Most Significant Byte and Divisor Latch Least Significant Byte. Setting DLL = 1 and DLM = 0 selects the divisor to divide by 1 (divide by 1 gives the maximum baud rate for a given input frequency at the CLKIN input.

The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 2.4576 MHz, and 3.072 MHz. With these frequencies, standard bit rates from 50 to 38.5 kbps are available. Tables 7, 8, and 9 illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

Reset

After power up, the UM82C852 RESET input should be held high for 500 ns to reset the UM82C852 circuits to an idle mode until initialization. A high on RESET causes the following:

1. Initializes the transmitter and receiver internal clock counters.
2. Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. The Line Control Register (LCR), Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not affected.

Following removal of the reset condition (Reset high), the UM82C852 remains in the idle mode until programmed.

A hardware reset of the UM82C852 sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a reset on the UM82C852 is given in Table 10.

Programming

Each serial channel of the UM82C852 is programmed by the control registers LCR, IER, DLL and DLM, and MCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface. While the control register can be written in any order, the IER should be written to last because it controls the interrupt enables. Once a serial channel is programmed and operational, these registers can be updated any time the UM82C852 serial channel is not transmitting or receiving data.

The control signals required to access each serial channel's internal registers are shown below.

Software Reset

A software reset of the serial channel is a useful method for returning to a completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches, and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

Clock Input Operation

The maximum input frequency of the external clock of the UM82C852 is 3.1 MHz.

(c) Parallel Port Registers

The UM82C852's parallel port interfaces the device to a Centronics-style printer. When parallel port address selected ($\overline{IOR}$) and write ($\overline{IOW}$) pin are as shown, the Read Data Register allows the microprocessor to read the information on the parallel bus. The Read Status Register allows the microprocessor to read the status of the printer in the five most significant bits. The status bits are Printer Busy (BUSY). Acknowledge (ACK) which is a handshake function. Paper Empty (PE), Printer Selected (SLCT), and Error. (ERROR). The Read Control Register allows the state of the control lines to be read. The Write Control Register sets the state of the control lines.

They are LPTIRQ Enable (IRQ ENB). Select in (SLIN). Initialize the Printer (INIT). Autofeed the Paper (AUTOFD). Strobe (STROBE), which informs the printer of the presence of a valid byte on the parallel bus. The Write Data Register allows the microprocessor to write a byte to the parallel bus.

The parallel port is completely compatible with the parallel port implementation used in the IBM Serial/Parallel Adaptor.

Table 5. Interrupt Identification Register

Interrupt Identification				Interrupt Set and Reset Functions		
Bit 2	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Flag**	**Interrupt Source**	**Interrupt Reset Control**
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE FE, or BI	LSR Read
1	0	0	Second	Received Data Available	Received Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is the Interrupt Source or THR Write
0	0	0	Fourth	Modem Status	–CTS, –DSR –RI, –DCD)	MSR Read

X = Not Defined.

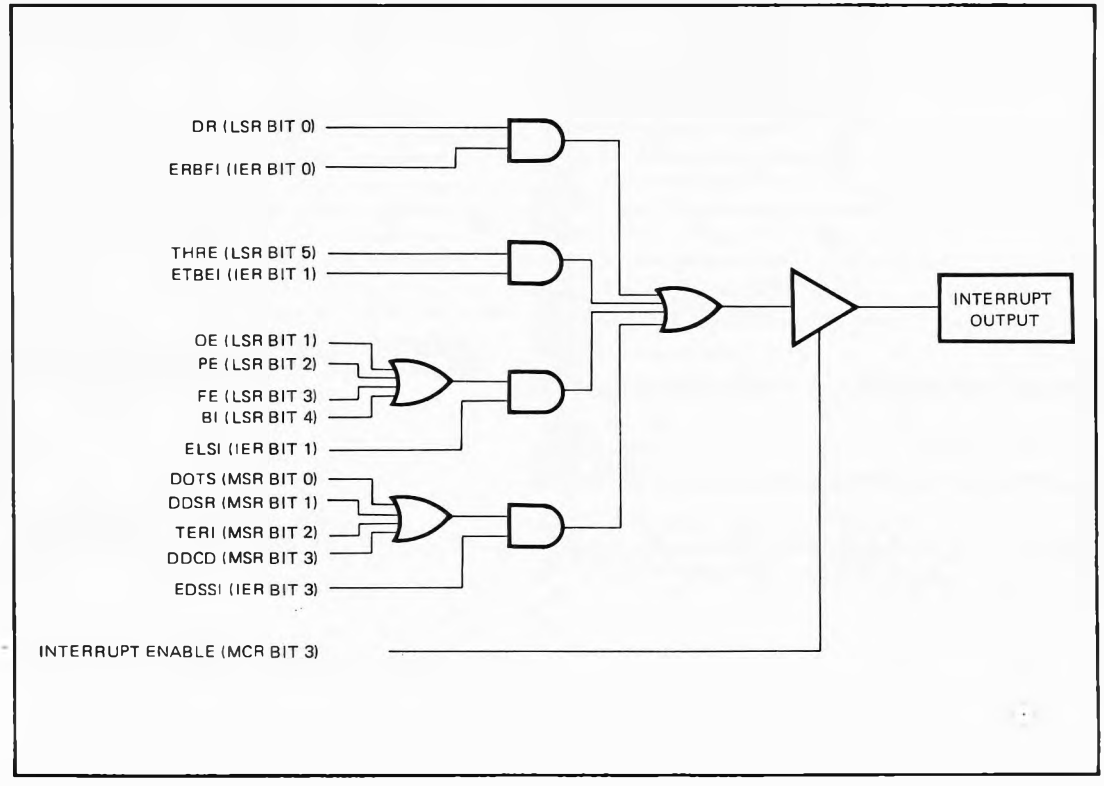


Figure 3. Interrupt Control Logic

Table 6. Serial Channel Accessible Registers

Register Mnemonic	Register Bit Number							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)*
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Interrupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Received Data Available Interrupt
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit (1)	Interrupt ID Bit (0)	"0" 1F Interrupt Pending
LCR	(DLAB) Divisor Latch Access Bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	(WLSB0) Word Length Select Bit 0
MCR	0	0	0	Loop	Out 2	Out 1	(RTS) Request To Send	(DTR) Data Terminal Ready
LSR	0	(TEMT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun Error	(DR) Data Ready
MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Ready Set	(CTS) Clear to Send	(DDCD) Delta Data Carrier Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

*LSB Data Bit 0 is the first bit transmitted or received.

Table 7. Baud Rates (1.8432 MHz Clock)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

Table 8. Baud Rates (2.4576 MHz Clock)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3072	–
75	2048	–
110	1396	0.026
134.5	1142	0.0007
150	1024	–
300	512	–
600	256	–
1200	128	–
1800	85	0.392
2000	77	0.260
2400	64	–
3600	43	0.775
4800	32	–
7200	21	1.587
9600	16	–
19200	8	–
38400	4	–

Table 9. Baud Rates (3.072 MHz Clock)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

(d) Real Time Counter

The real time counter is divided into 4-bit digits with 2 digits being accessed during any read or write cycle. Each digit represents a BCD number and is defined in Table 13. Any unused bits are held at a logical zero and ignored during a write. An unused bit is any bit not necessary to provide a full BCD number. For example, tens of hours can not legally exceed the number 2, thus only 2 bits are necessary to define the tens of hours. The other 2 bits in the tens of hours digit are unused. The unused bits are designated in Table 1 as dashes.

The addressable portion of the counter is from milliseconds to months. The counter itself is a ripple counter. The ripple delay is less than 60μs above 4.0V and 300μs at 2.0V.

RAM

56 bits of RAM are contained on-chip. These can be used for any necessary power down storage or as an alarm latch for comparison to the real time counter. The data in the RAM can be compared to the real time counter on a digit basis. The only digits that are not compared are the unit ten thousandths of seconds and tens of days of the week (these are unused in the real time counter). If the two most significant bits of any RAM digit are ones then this RAM location will always compare.

Table 10. Reset Control of Register and Pinout Signals

Register/Signal	Reset Control	Reset Status
Interrupt Enable Register	Reset	All Bits low
Interrupt Identification Register	Reset	Bit 0 is high and Bits 1-7 are low
Line Control Register	Reset	All Bits low
Modem Control Register	Reset	All Bits low
Line Status Register	Reset	Bits 5, 6 are high, others are low
Modem Status Register	Reset	Bits 0-3 are low, Bits 4-7 are input signal
SOUT	Reset	High
RTS DTR	Reset	High
COMIRQ	Reset	High-Impedance
STB, AFD, SLIN	Reset	High
INIT	Reset	Low

Table 11. Parallel Port Registers

Register	Register Bits							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Read Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	BUSY	ACK	PE	SLCT	ERROR	1	1	1
Read Control	1	1	1	LPTIRQ ENB	SLIN	INIT	AUTOFD	STROBE
Write Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	1	1	1	LPTIRQ ENB	SLIN	INIT	AUTOFD	STROBE

Table 12. Parallel Port Register Select

Control Pins				Register Selected
$\overline{IOR}$	$\overline{IOW}$	A1	A0	
0	1	0	0	Read Data
0	1	0	1	Read Status
0	1	1	0	Read Control
1	0	0	0	Write Data
1	0	0	1	Invalid
1	0	1	0	Write Control

The RAM is formatted the same as the real time counter. 4 bits per digit, 14 digits, however there are no unused bits. The unused bits in the real time counter will compare only to zeros in the RAM.

Interrupts and Comparator

There is one interrupt output. The most flexible is the RTCIRQ OUTPUT (a true high signal). This output can be programmed to provide 8 different output signals. They are: 10 Hz, 1 Hz, once per minute, once per hour, once a day, once a week, once a month, and when a RAM/real time counter comparison occurs. To enable the output a one is written into the interrupt control register at the bit location corresponding to the desired output frequency (Figure 4). Once one or more bits have been set in the

Table 13. Real Time Counter Format

Counter Addressed		Units D0	D1	D2	D3	Max. BCD Code	Tens D4	D5	D6	D7	Max. BCD Code
1/10,000 of Seconds	(00H)	–	–	–	–		D4	D5	D6	D7	9
Hundredths and Tenths Sec	(01H)	D0	D1	D2	D3	9	D4	D5	D6	D7	9
Seconds	(02H)	D0	D1	D2	D3	9	D4	D5	D6	–	5
Minutes	(03H)	D0	D1	D2	D3	9	D4	D5	D6	–	5
Hours	(04H)	D0	D1	D2	D3	9	D4	D5	–	–	2
Day of the Week	(05H)	D0	D1	D2	–	7	–	–	–	–	0
Day of the Month	(06H)	D0	D1	D2	D3	9	D4	D5	–	–	3
Month	(07H)	D0	D1	D2	D3	9	D4	–	–	–	1

(–) Indicates unused bits

interrupt control register, the corresponding counter's rollover to reset state will clock the interrupt status register and cause the interrupt output to go high. To reset the interrupt and to identify which frequency caused the interrupt, the interrupt status register is read. Reading this register places the contents of the status register on the data bus. The interrupt frequency will be identified by a one in the respective bit position. Removing the read will reset the interrupt.

The comparator is a cascaded exclusive NOR. Its output is latched 61μs after the rising edge of the 1KHz clock signal (input to the ten thousandth of seconds counter). This allows the counter to ripple through before looking at the comparator. For operation at less than 4.0V, the

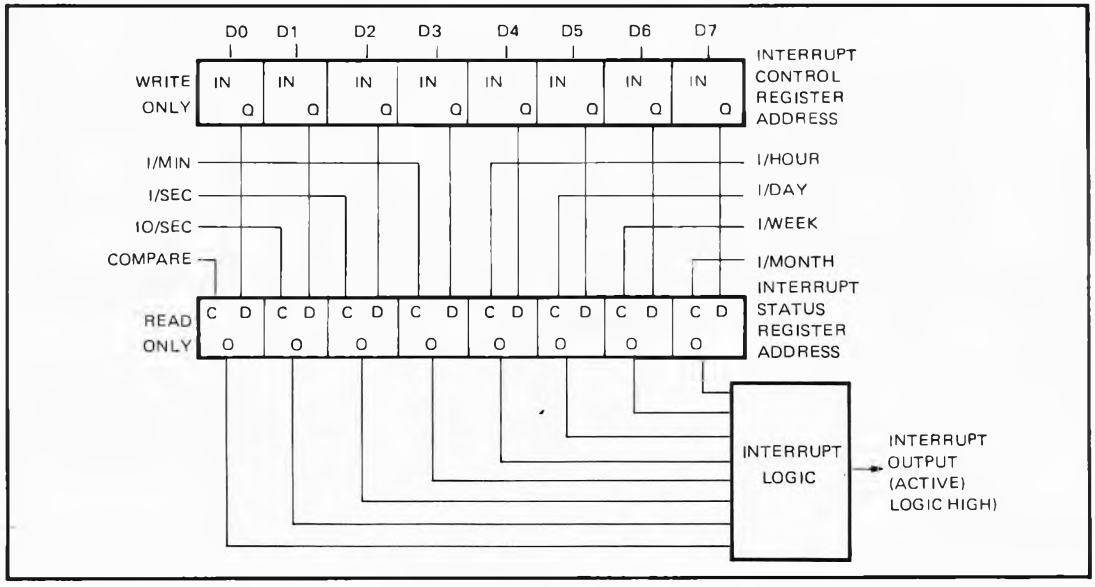


Figure 4. Interrupt Register Format

Table 14. Address Codes and Functions

A4	A3	A2	A1	A0	Function
0	0	0	0	0	Counter – Thousandths of Seconds
0	0	0	0	1	Counter – Hundredths and Tenths of Seconds
0	0	0	1	0	Counter – Seconds
0	0	0	1	1	Counter – Minutes
0	0	1	0	0	Counter – Hours
0	0	1	0	1	Counter – Day of the Week
0	0	1	1	0	Counter – Day of the Month
0	0	1	1	1	Counter – Months
0	1	0	0	0	Latches – Thousandths of Seconds
0	1	0	0	1	Latches – Hundredths and Tenths of Seconds
0	1	0	1	0	Latches – Seconds
0	1	0	1	1	Latches – Minutes
0	1	1	0	0	Latches – Hours
0	1	1	0	1	Latches – Day of the week
0	1	1	1	0	Latches – Day of the Month
0	1	1	1	1	Latches – Months
1	0	0	0	0	Interrupt Status Register
1	0	0	0	1	Interrupt Control Register
1	0	0	1	0	Counter Reset
1	0	0	1	1	Latch Reset
1	0	1	0	0	Status Bit
1	0	1	0	1	"GO" Command
1	0	1	1	0	Standby Interrupt
1	1	1	1	1	Test Mode

All others unused.

Table 15. Counter and Latch Reset Format

D0	D1	D2	D3	D4	D5	D6	D7	Counter or Latch Reset
1	0	0	0	0	0	0	0	Thousandths of Seconds
0	1	0	0	0	0	0	0	Hundredths and Tenths of Seconds
0	0	1	0	0	0	0	0	Seconds
0	0	0	1	0	0	0	0	Minutes
0	0	0	0	1	0	0	0	Hours
0	0	0	0	0	1	0	0	Day of the Week
0	0	0	0	0	0	1	0	Day of the Month
0	0	0	0	0	0	0	1	Months

For Counter Reset A4–A0 Must be 10010
For Latch Reset A4-A0 Must Be 10011

thousandth of seconds counters should not be included in a compare because of the possibility of having a ripple delay greater than 61μs. (For output timing see interrupt timing).

Tables 14 and 15 are referred for the address input codes and functions and for the counter and latch reset format.

Power Down Mode

The POWER DOWN input is essentially a second chip select. It disables all inputs and outputs. When this input is at a logic zero, the device will not respond to any external signals. (The programming must be down before the POWER DOWN input goes to a logic zero). When switching V_{DD} to the standby or power down mode, the POWER DOWN input should go to a logic zero at least 1μs before V_{DD} is switched. When switching V_{DD} all other inputs must remain between V_{SS}−0.3V and V_{DD} + 0.3V. When restoring V_{DD} to the normal operating mode, it is necessary to insure that all other inputs are at valid levels before switching the POWER DOWN input back to a logic one. These precautions are necessary to insure that no data is lost or altered when changing to or from the power down mode.

Counter and RAM Resets: Go Command

The counter's and RAM can be reset by writing all 1's (FF) at addresses 12H or 13H respectively.

A write pulse at address 15H will reset the thousandths hundredths, tenths, units and tens of seconds counters. This GO command is used for precise starting of the clock, the data on the data bus is ignored during the writing. If the seconds counter is at a value greater than 39 when the GO is issued the minute counter will increment: otherwise the minute counter is unaffected. This command is not necessary to start the clock but merely a convenient way to start precisely at a given minute.

Status Bit

The status bit is provided to inform the user the clock is in the process of rolling over when a counter is read. The status bit is set if this 1 KHz clock occurs during or after any counter read. This tells the user that the clock is rippling through the real time counter. Because the clock is rippling, invalid data may be read from the counter. If the status bit is set following a counter read, the counter should be read.

The status bit appears on D0 when address 14H is read. All the other data lines will be zero. The bit is set when a logical one appears. This bit should be read every time a counter read or after a series of counter reads are done. The trailing edge of the read at address 14H will reset the status bit.

Oscillator

The oscillator is the standard parallel resonant oscillator. Externally, 2 capacitors, a 20M Ohm resistor and the crystal are required. The 20M Ohm resistor is connected between X1 and X2 to bias the internal inverter in the linear region. For micropower crystals a resistor in series with the oscillator output may be necessary to insure the crystal is not overdriven. This resistor should be approximately 200K Ohms. The capacitor values should be typically 300pF. The crystal frequency is 32,768 Hz.

The oscillator input can be externally driven, if desired. In this case the output should be left floating and the input level should be within 0.3V of the supplies.

Test Mode

The test mode is merely a mode for production testing. It allows the counters to count at a higher than normal rate. In this mode the 32 KHz oscillator input is connected directly to the ten thousandths of seconds counter. The chip select and write lines must be low and the address must be held at 1 FH.

(e) GAME PORT:
Game: 201

I/O Write:

7	6	5	4	3	2	1	0	Function
							x	A Paddle Coordinate
						x		B Paddle Coordinate
					x			C Paddle Coordinate
				x				D Paddle Coordinate
			x					Status of A Paddle Button
		x						Status of B Paddle Button
	x							Status of C Paddle Button
x								Status of D Paddle Button

I/O Read:

7	6	5	4	3	2	1	0	Function
							x	A Joystick X Coordinate
						x		A Joystick Y Coordinate
					x			B Joystick X Coordinate
				x				B Joystick Y Coordinate
			x					Status of A Joystick Button 1
		x						Status of A Joystick Button 2
	x							Status of B Joystick Button 1
x								Status of B Joystick Button 2

Absolute Maximum Ratings *

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . –55°C to 150°C
All Output Voltages . . . . . –0.5V to +7V
All Input Voltages . . . . . –0.5V to +7V
Supply Voltage V_{CC} . . . . . 5V ± 10%
Power Dissipation 0.5W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{CC}	Supply Voltage	4.5		5.5	V	Output Enable
V_{CC}	Supply Voltage	2.0		5.5	V	Power Down
V_{IL}	Input Low Voltage	–0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 6 mA
						I_{OL} = 12 mA, (PD0 ~ PD7)
V_{OH}	Output High Voltage	2.4			V	I_{OH} = 2 mA
						I_{OH} = 4 mA, (PD0 ~ PD7)
V_{IHR} ~ V_{ILR}	Schmitt Trigger Hysteresis	0.25			V	RESET, CLKIN RTCCS0(1), COMCS LPTCS0(1)
I_{CC}	Power Supply Current			20	μA	Power Down
				50	mA	Output Enable

AC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%)

Input Requirement

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit
1	t_{AW}	$\overline{IOW}$ Delay Time from Address	50			ns
2	t_{WA}	Address Hold Time from $\overline{IOW}$	20			ns
3	t_{DS}	Data Setup Time to $\overline{IOW}$	40			ns
4	t_{DH}	Data Hold Time from $\overline{IOW}$	40			ns
5	t_{AR}	$\overline{IOR}$ Delay Time from Address	50			ns
6	t_{RA}	Address Hold Time from $\overline{IOR}$	20			ns

Output Response

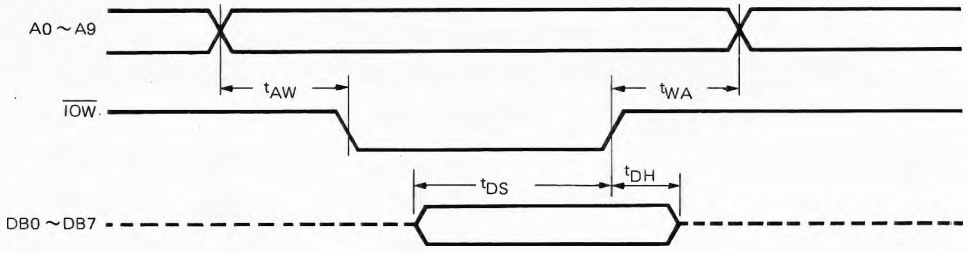
7	t_{RD}	Data Delay Time from $\overline{IOR}$			125	ns
8	t_{HZ}	Data Floating Time from $\overline{IOR}$	0		100	ns

AC Characteristics (Continued)

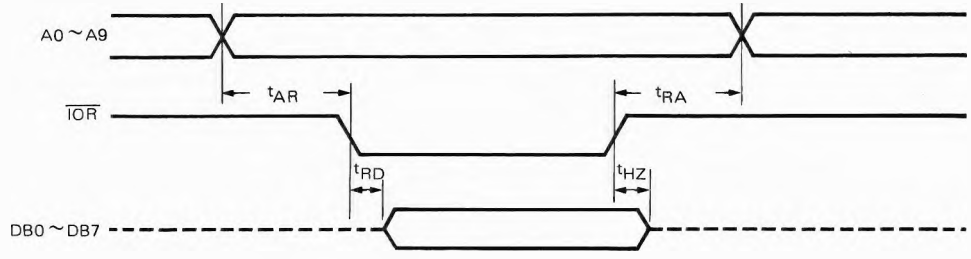
No.	Symbol	Parameter	Min.	Typ.	Max.	Unit
9	t_{SINT}	Set Interrupt Delay Time from Stop Bit	1		1	CLK cycle
10	t_{RINT}	Reset Interrupt Delay Time from RD RBR/LSR			1	μs
12	t_{IRS}	Transmit Start Delay Time from Initial INTR	8		24	CLK cycle
13	t_{SI}	Set Interrupt Delay Time from Initial write	16		32	CLK cycle
14	t_{STI}	Set Interrupt Delay Time from Stop Bit	8		8	CLK cycle
15	t_{IR}	Reset Interrupt Delay from RD IIR			250	ns
16	t_{MDO}	MODEM Output Delay Time from WR MCR			200	ns
17	t_{SIM}	Set Interrupt Delay Time from MODEM Input			200	ns
18	t_{RIM}	Reset Interrupt Delay Time from RD MSR			250	ns
19	t_{PPW}	Parallel Port Delay Time from WR PDR or PCR			300	ns
20	t_{SIAK}	Set Interrupt Delay Time from ACK			200	ns
21	t_{GMRW}	Game Command Delay Time from RD/WR Game Port			150	ns

Timing Waveforms

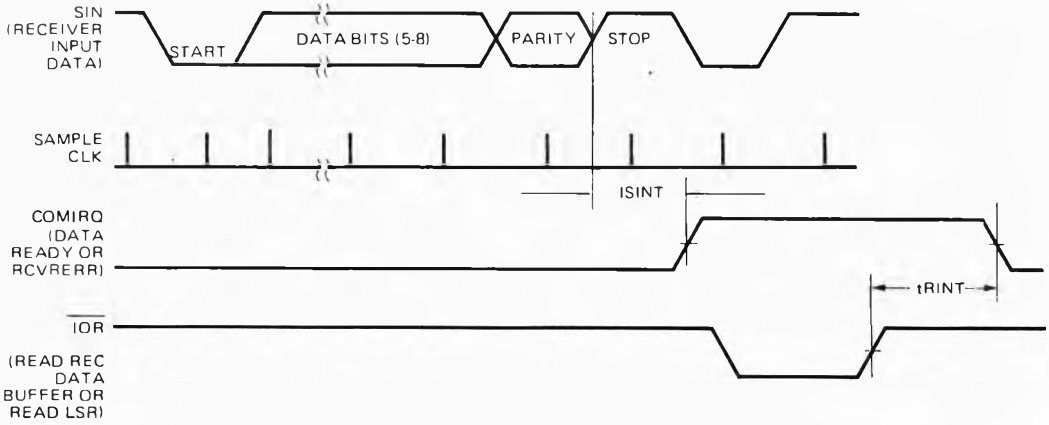
Write Cycle Timing



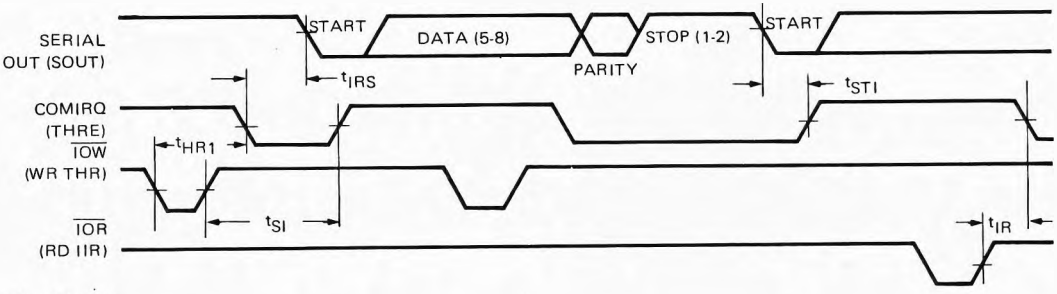
Read Cycle Timing



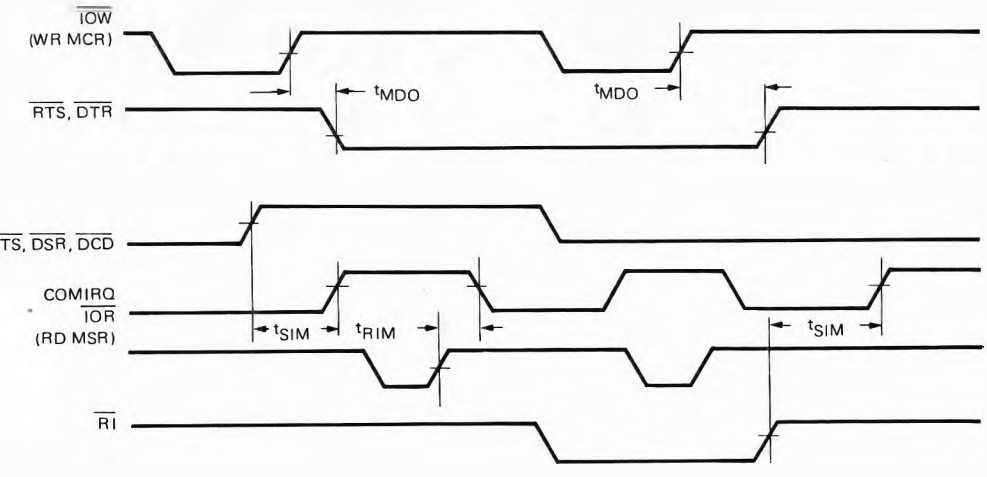
Timing Waveforms (Continued)



Transmitter Timing

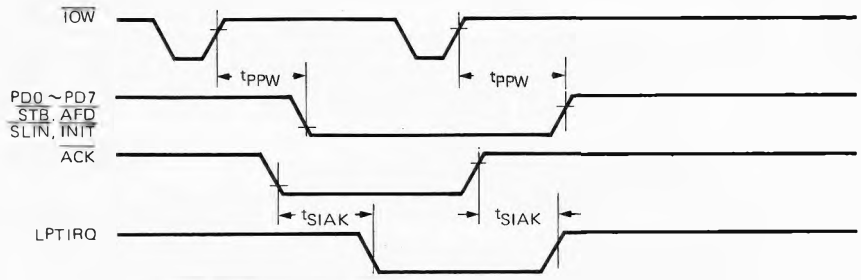


Modem Timing



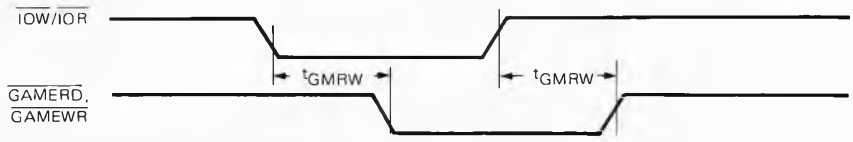
Timing Waveforms (Continued)

PARALLEL PORT TIMING



** Outputs of $\overline{STB}$, $\overline{AFD}$, $\overline{SLIN}$ and $\overline{INIT}$ are pulled up by 1K ohms resisters.

Game Port Timing



Application Circuit