UMC

UM587

PRELIMINARY

VGA Controller

Features

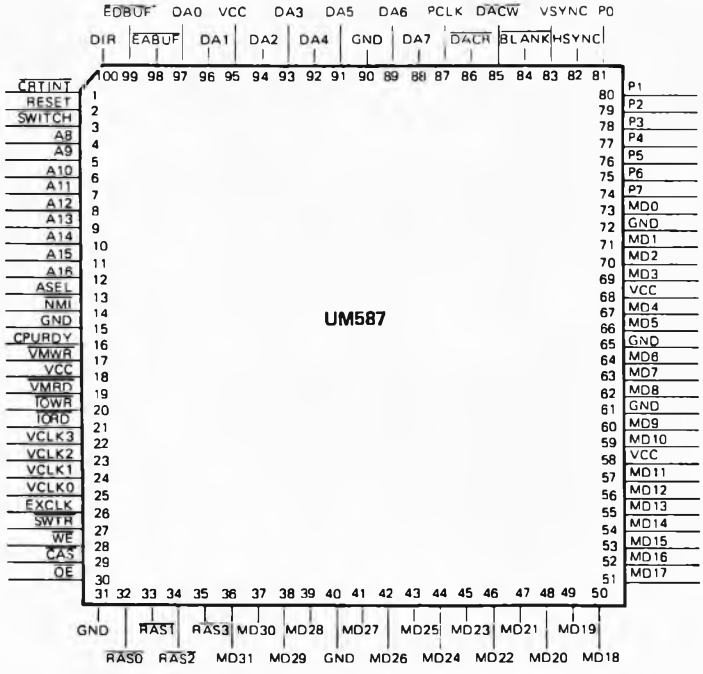
- Single chip VGA video graphics device fully compatible in the following systems:
  - IBM PC/AT, PC/XT, PS/2
  - IBM VGA (All modes)
  - IBM BIOS (Basic input/output system)
- Provides 800 x 600 element high-resolution graphics with 16 colors
- Flicker-free operation in all video modes
- Supports 132-column text modes
- Supports both digital and analog monitors

General Description

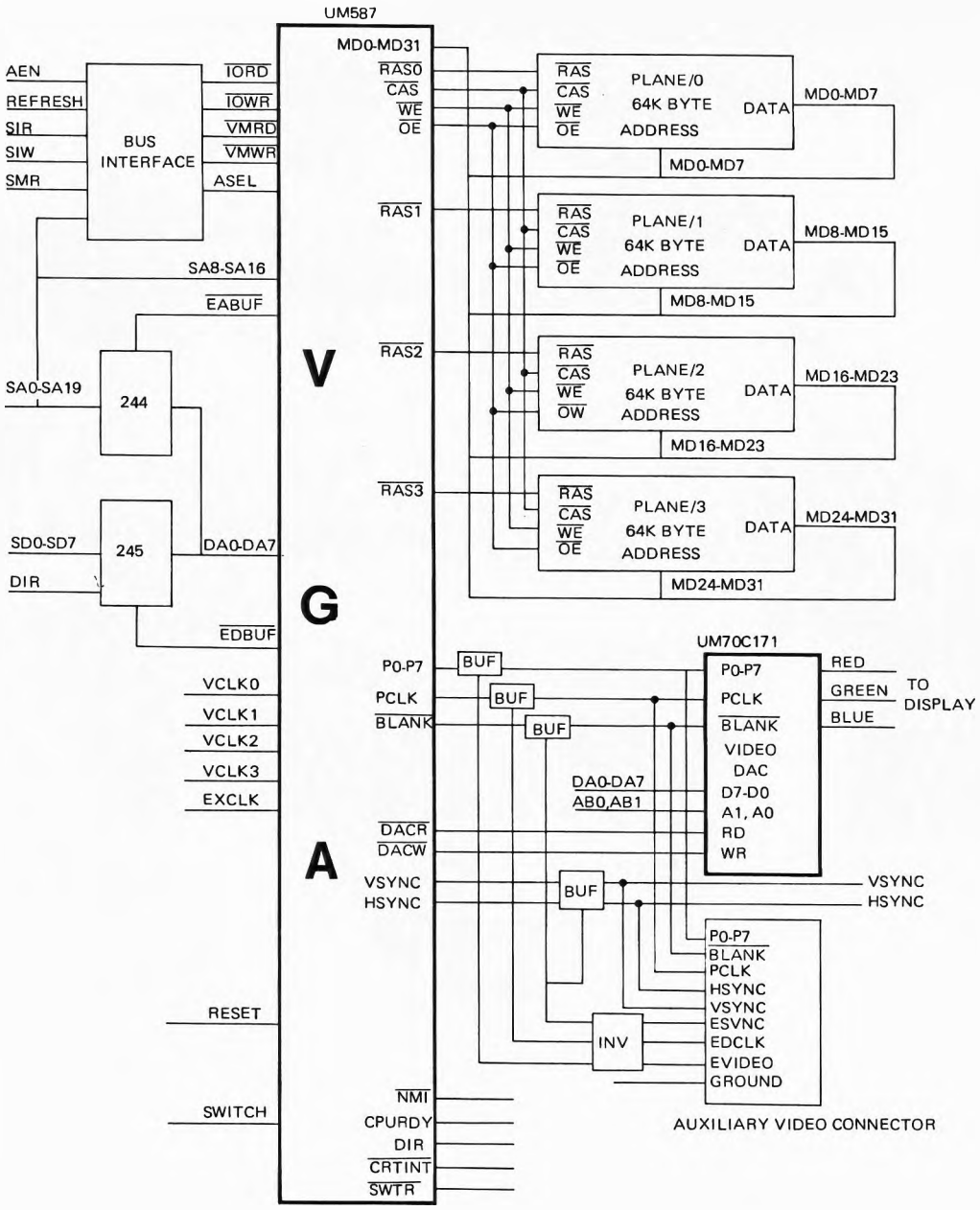
The UM587 is a single chip, high-integration, high resolution graphics device designed for use in IBM PS/2 model 30, PC/AT and PC/XT compatible systems. It provides high resolution graphics of 800 x 600 elements with 16 colors.

The UM587 also is fully compatible with IBM VGA (all modes). Hercules graphics, EGA, CGA, MDA and IBM BIOS. It is flicker free in all modes and supports an external digital-to-analog look-up table.

Pin Configuration



System Block Diagram



MODE TABLE

Mode	Type	Col x Row	Colors	Pages	Map Addr	CharBox
(HEX)					(HEX)	
00	Text	40 x 25	16	8	B800	8 x 8
01	Text	40 x 25	16	8	B800	8 x 8
02	Text	80 x 25	16	8	B800	8 x 8
03	Text	80 x 25	16	8	B800	8 x 8
00*	Text	40 x 25	16	8	B800	8 x 14
01*	Text	40 x 25	16	8	B800	8 x 14
02*	Text	80 x 25	16	8	B800	8 x 14
03*	Text	80 x 25	16	8	B800	8 x 14
00+	Text	40 x 25	16	8	B800	9 x 16
01+	Text	40 x 25	16	8	B800	9 x 16
02+	Text	80 x 25	16	8	B800	9 x 16
03+	Text	80 x 25	16	8	B800	9 x 16
07	Text	80 x 25	2	8	B000	9 x 14
07+	Text	80 x 25	2	8	B000	9 x 16
04	APA	320 x 200	4	1	B800	8 x 8
05	APA	320 x 200	4	1	B800	8 x 8
06	APA	640 x 200	2	1	B800	8 x 8
0D	APA	320 x 200	16	8	A000	8 x 8
0E	APA	640 x 200	16	4	A000	8 x 8
0F	APA	640 x 350	2	2	A000	8 x 14
10	APA	640 x 350	16	2	A000	8 x 14
11	APA	640 x 480	2	1	A000	8 x 16
12	APA	640 x 480	16	1	A000	8 x 16
13	APA	320 x 200	256	1	A000	8 x 8
50	Text	132 x 25	16	8	B800	8 x 14
51	Text	132 x 43	16	5	B800	8 x 8
52	Text	800 x 600	16	8	A000	8 x 8

Remarks. (1) Modes 0, 1, 2, 3 0*, 1*, 2*, 3* 0+, 1+, 2+, 3+ differ in CharBox size and display scan lines.

(2) Mode 3+ or 7+ is the default mode at power-up time.

Pin Description

Pin No.	Symbol	I/O	Description
1	$\overline{\text{CRTINT}}$	O	Display vertical retrace interrupt. An active low open collector.
2	RESET	I	System reset signal, active high.
3	SWITCH	I	Signal that detects the type of monitor.
4-12	A8-A16	I	CPU address bus bits 8 through 16.
13	ASEL	I	Active high, to select VGA address to decode.
14	$\overline{\text{NM}}$	O	Non maskable interrupt. An active low open collector.
16	CPURDY	O	An open collector active high output. Signals processor that it is ready for memory access.
17	$\overline{\text{VMWR}}$	I	Active low, video memory write signal.
19	$\overline{\text{VMRD}}$	I	Active low, video memory read signal.
20	$\overline{\text{IOWR}}$	I	Active low, I/O write signal.
21	$\overline{\text{IORD}}$	I	Active low, I/O read signal.
22	VCLK3	I	35.5 MHz input clock signal.
23	VCLK2	I	Reserved
24	VCLK1	I	28.322 MHz input clock signal.
25	VCLK0	I	25.175 MHz input clock signal.
26	EXCLK	I	External clock signal.
27	$\overline{\text{SWTR}}$	O	Read DIP switch control signal.
28	$\overline{\text{WE}}$	O	Video memory write enable. An active low signal.
29	$\overline{\text{CAS}}$	O	Column address strobe to all planes. An active low signal.
30	$\overline{\text{OE}}$	O	Output enable signal to memory. It is active low.
32-35	$\overline{\text{RAS0}}$, $\overline{\text{RAS3}}$	O	Row address strobe to planes 0-3. An active low signal.
36-39, 41-44	MD31-24	I/O	Display memory address/data time multiplexed bus line 7-0, interface to video memory plane 3.
45-52	MD23-16	I/O	Display memory address/data time multiplexed bus line 7-0, interface to video memory plane 2.
53-57, 59, 60, 62	MD15-8	I/O	Display memory address/data time multiplexed bus line 7-0, interface to video memory plane 1.
63, 64, 66, 67, 69-71, 73	MD7-0	I/O	Display memory address/data time multiplexed bus line 7-0, interface to video memory plane 0.
74-81	P7-P0	O	Video color look up table address bits 7-0.
82	HSYNC	O	Horizontal SYNC signal for monitor.
83	VSYNC	O	Vertical SYNC signal for monitor.
84	$\overline{\text{BLANK}}$	O	An active low blanking signal to external palette chip.
85	$\overline{\text{DACW}}$	O	An active low I/O write signal for external palette chip (256 color look up table).

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
86	$\overline{DACR}$	O	An active low I/O read signal for external palette chip (256 color look up table).
87	PCLK	O	Pixel clock signal for external palette chip (256 color look up table).
88, 89, 91-94 96, 97	DA7-DA0	I/O	Multiplexed address/data bus bits 7 through 0.
98	$\overline{EABUF}$	O	Active low, enable external address buffer.
99	–EDBUF	O	Active low, enable external data buffer.
100	DIR	O	Control signal for bidirectional data bus transceiver.
18, 58 68, 95	VCC		Power: +5V
15, 31, 40, 61 65, 72, 90	GND		Ground

Functional Description

Introduction

The single chip VGA is a standard video graphic controller for PS/2 model 30 and PC/XT/AT systems. Compared to earlier version video graphic controllers, several new features have been added, including higher resolution (640 x 480), new video mode, 256 color support for 320 x 200 graphics mode, up to 64 shades of grey display for monochrome monitors, and eight fonts loaded into video RAM simultaneously.

The host can access both VGA registers and video memory by setting the bus address and read/write commands to read or write 8-bit data. Video RAM and screen refresh activities occur concurrently and independently by assigning appropriate memory access cycles to each of them.

Most registers are readable so that BIOS and driver software are able to determine current state of video. In the basic configuration, 256K bytes of memory are needed as the display buffer. Four planes of video memory are controlled by four different-RAS (Row Address Strobe) signals and one-CAS (Column Address Strobe), one $\overline{WE}$ (Write Enable), one $\overline{OE}$ (Output Enable) Signal. The Video data bus is time multiplexed with the video address bus in a way that outputs RAS and CAS address early in the memory cycle and inputs 8-bit data for read or outputs 8-bit data for write late in the memory cycle.

NMI (Non-Maskable Interrupt) is generated by trapping some particular I/O ports so that backward compatibility can be done through the BIOS. The VGA chip will provide a 'DIRectional' signal to control the data flow to the system data bus for CPU Read or Write.

Major Components

There are four major components of the UM587 contained in a single 100-pin plastic flatpack. They are described below:

CRT Controller

The UM587 CRT Controller provides synchronization control, timing generation and supplies video memory address to display memory. Flexible timing configuration options are allowed by accessing I/O registers through software control. During the blanking period, an 8-bit refresh counter is placed on the memory address lines. A split screen feature is also provided to allow two windows.

Sequencer

The UM587 Sequencer takes care of basic memory timing for the display memory and the character clock for the control of memory fetches.

The intelligent state machine in the Sequencer automatically assigns appropriate memory access cycles to both the CPU and CRT Controller during active display period. The sequencer can also protect the entire memory plane by selectively masking out planes through the Mask re-

gister.

Graphics Controller

The Graphics Controller provides a data path for both CPU Read/Write and CRT Read access to the display memory. For CRT access it directs data to the Attribute Controller while the CPU access directs data to the system bus instead. It handles two basic modes: alphanumeric and graphics. In the alphanumeric mode, the data is sent in parallel directly to the Attribute Controller. In the graphics mode the memory data is shifted out serially to the Attribute Controller. The data formatting and manipulation are implemented for various modes. Color comparator is provided for fast color comparison in the application of color painting modes. Since the Graphics Controller can process 32-bit data (8-bits from each plane) at a time, a fast color presetting and area fill operation can be achieved.

Attribute Controller

The UM587 Attribute Controller provides video shifting, attribute processing and an internal palette of 16 colors selectable from a possible 64 colors. Pixel panning is also provided for both graphics and text modes. Underline, cursor and blinking logic are interpreted and manipulated here. The final output of the Attribute Controller is an 8-bit wide color data that is sent to the external color look-up table for final color mapping.

Memory and Clock Consideration

In basic configuration, eight 64K x 4-bit dynamic RAM's should be used to configure 256K bytes of video memory. The supported DRAM and CLOCK speeds are related to the graphics resolution as shown in Table 1.

Table 1. Resolution Requirements

Dram	120 ns	120 ns	100 ns
Clock	28 MHz	25 MHz	36 MHz
Resolution	720 x 400	640 x 480	800 x 600
Colors	16	16	16

VGA Registers

All registers in the VGA can be categorized into six groups for the different function blocks in the hardware. In the UM587 VGA chip, the system microprocessor data latches are readable for faster save and restore of the VGA state in the VGA BIOS. The VGA also provides the system microprocessor interface for the video DAC (external color palette chip). The DAC has one address register which can be accessed through address hex 03C7 for read, and hex 03C8 for write. Table 2 lists the registers and the I/O address where they are located. It also lists whether or not they are Read/Write, Read-Only, or Write Only.

Note that the PEL Mask Register must not be written to by application code or destruction of the color look-up table may occur.

Table 2. VGA Registers

Register Group	R/W	Mono Emulation	Color Emulation
General Registers			
Miscellaneous	W	03C2	03C2
	R	03CC	03CC
Input Status 0	RO	03C2	03C2
Input Status 1	RO	03BA	03DA
Feature Control	W	03BA	03DA
	R	03CA	03CA
VGA Enable	RW	03C3	03C3
DAC State	R	03C7	03C7
Sequencer Registers			
Address Register	RW	03C4	03C4
Data Registers	RW	03C5	03C5
CRTC Registers			
Address Register	RW	03B4	03D4
Data Registers	RW	03B5	03D5
Graphics Registers			
Address Register	RW	03CE	03CE
Data Registers	RW	03CF	03CF
Attribute Registers			
Address Register	RW	03C0	03C0
Data Registers	W	03C0	03C0
	R	03C1	03C1
Extended Registers			
Address Register	RW	03DE	03DE
Data Registers	RW	03DF	03DF
DAC Registers			
PEL Address (Write)	RW	03C8	03C8
PEL Address (Read)	WO	03C7	03C7
PEL Data Registers	RW	03C9	03C9
PEL Mask	RW	03C6	03C6

General Registers

This section describes all the general registers. The output is controlled by bit 0 of the Miscellaneous Output Register.

Miscellaneous Output Register

Read-03CC **Write-03C2**

Bit	Description
7	Vertical Sync Polarity
6	Horizontal Sync Polarity
5	Page Bit for Odd/Even
4	Reserved
3	Clock Select bit 1
2	Clock Select Bit 0
1	Enable RAM
0	I/O Address Select

Table 3. General Registers

Name	Read Port	Write Port	Index
Miscellaneous Output	03CC	03C2	–
Input Status 0	03C2	–	–
Input Status 1	03?A	–	–
Feature Control	03CA	03?A	–
VGA Enable	03C3	03C3	–
DAC State	03C7	–	–

Table 4. Registers (Continued)

Bit 7	Bit 6	Vertical Size
0	0	Reserved
0	1	400 lines
1	0	350 lines
1	1	480 lines

Bits 7, 6 The Polarity of Vertical/Horizontal Sync is used to select the vertical size as shown in Table 4.

Bit 5 Selects between two pages of memory when in the Odd/Even modes (modes 0-5, 7). A logic 0 selects the low page of memory; a logic 1 selects the high page of memory. This bit is provided for diagnostic use.

Bit 4 Reserved

Bits 3, 2 These two bits select the clock source. In UM587 VGA the third bit is defined in extended register and used with these two bits to select a wider range of clock sources for different video modes. See Table 5.

Bit 1 A logic 0 disables Video RAM address decode from the system microprocessor; a logic 1 enables Video RAM to the system microprocessor

Bit 0 A logic 0 sets CRTC addresses to Hex 03BX and Input Status Register 0's address to 03BA for Monochrome emulation. A logic 1 sets CRTC addresses to Hex 03DX and Input Status Register 0's address to Hex 03DA for color emulation.

Table 5. Registers (Continued)

CSEL2	CSEL1	CSEL0	Clock
0	0	0	25.175 MHz
0	0	1	28.322 MHz
0	1	0	External Input Clock
0	1	1	Reserved
1	0	0	14.318 MHz
1	0	1	16.257 MHz
1	1	0	Reserved
1	1	1	35.5 MHz

Input Status Register 0

Read-Only **Address = 03C2**

Bits	Description
7	CRT Interrupt
6, 5	Reserved
4	Switch Sense Bit
3-0	Reserved

Bit 7 A logic 1 indicates a vertical retrace interrupt is pending. A logic 0 indicates the vertical retrace interrupt is cleared.

Bit 6, 5 Reserved

Bit 4 This bit allows the power-on initialization to determine if a monochrome or color monitor is connected to the system.

Bit 3-0 Reserved

Input Status Register 1

Read-Only **Address = 03?A**

Bit	Description
7, 6	Reserved
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
2, 1	Reserved
0	Display Enable

Bits 7, 6 Reserved

Bits 5, 4 These two bits are used for diagnostics. They are connected to two of the eight color out-

puts of the Attribute Controller. The two bits defined in the Color Plane Enable Register to control the multiplexer for color output wiring as described in Table 6.

Bit 3 A logic 1 occurs during a vertical retrace interval. A logic 0 shows the video information is being displayed.

Bits 2, 1 Reserved

Bit 0 A logic 1 indicates a horizontal or vertical retrace interval. A logic 0 indicates that the internal Display Enable Signal is active. To avoid glitches in the display, some programs use this status bit to restrict screen updates to de-activate display intervals. The VGA has been designed to eliminate this software requirement, so display screen updates may be made at any time.

Table 6. Register Bits

Color Plane Register		Input Status 1 Register	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

Feature Control Register

Read = 03CA **Write = 03?A**

Bit	Description
7-4	Reserved
3	Vertical Sync Select
2-0	Reserved

Bits 7-4 Reserved

Bits 3 This bit should always be set to 0 to enable normal vertical sync output to the monitor; when bit 3 = 1, the "vertical sync" output is the logical OR of "vertical sync" and "vertical display enable".

Bits 2-0 Reserved

Video Subsystem Enable Register

Read-03C3 **Write-03C3**

Bit	Description
7-1	Reserved
0	Video Subsystem Enable

Bits 7-1 Reserved

Bit 0 A logic 1 enables video I/O and memory address decoding. A 0 disables the video I/O and memory address decoding.

Sequencer Registers

This section describes registers in the Sequencer Control block. See Table 7.

Table 7. Sequencer Registers

Register Name	I/O Port	Index
Sequencer Address	03C4	–
Reset	03C5	00
Clocking Mode	03C5	01
Map Mask	03C5	02
Character Map Select	03C5	03
Memory Mode	03C5	04

Sequencer Address Register

Read-03C4 **Write-03C4**

Bit	Description
7-3	Reserved
2-0	Sequencer Address

Bits 7-3 Reserved

Bits 2-0 A binary value pointing to the register where data is to be written or read.

Reset Register

Port = 03C5 **Index 0**

Bit	Description
7-2	Reserved
1	Synchronous Reset
0	Asynchronous Reset

Bits 7-2 Reserved

Bit 1 A logic 0 directs the sequencer to synchronously clear and halt. Bits 1 and 0 must be 1 to allow the sequencer to operate. This bit must be set to 0 before changing either bit 3 or bit 0 of the Clocking Mode register, or bit 3 or bit 2 of the Miscellaneous Output Register, or bit 5, bit 4 or bit 3 of the Bandwidth Control Register.

Bit 0 A logic 0 directs the sequencer to asychronously clear and halt. Bits 1 and 0 must both be 1 to allow the sequencer to operate. Resetting the sequencer with this bit can cause data loss in dynamic RAMs.

Clocking Mode Register

Port = 03C5 **Index 1**

Bit	Description
7, 6	Reserved
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load
1	Reserved
0	8/9 Dot Clocks

Bits 7, 6 Reserved

Bit 5 When set to 1, this bit turns off the video screen and assigns maximum memory bandwidth to the system CPU. A logic 0 puts the screen into normal operation. When this bit is set the screen is blanked. The synchronization pulses are maintained. This bit is used for fast full-screen updates.

Bit 4 When set to 1, the internal shift load registers are loaded every fourth character clock. When set to 0, they are loaded every character clock. When 32 bits are fetched each cycle and used together in the shift registers, this mode is useful.

Bit 3 A logic 0 selects normal dot clock directly from the sequencer master clock input. A logic 1 will select master clock divided by two as dot clock. Normally, dot clock divided by two is used for 320 and 360 horizontal resolution modes.

Bit 2 When set to 1, the internal shift load registers are loaded every other character clock. When set to 0, and bit 4 is set to 0, the internal shift load registers are loaded every character clock. This mode is useful when 16 bits are fetched per cycle and chained together in the shift load registers.

Bit 1 Reserved

Bit 0 A logic 0 directs the sequencer to generate nine dot wide character clocks. A logic 1 generates eight dot wide character clocks from the sequencer. Nine dots are selected for alphanumeric modes only. For nine dot modes, the ninth dot equals the eighth dot for ASCII codes C0 through DF hex. Also, see the Line Graphics bit in Mode Control Register in the Attribute section.

Map Mask Register

Port = 03C5 **Index = 02**

Bit	Description
7-4	Reserved
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

Bits 7-4 Reserved

Bits 3-0 A logic 1 enables the CPU to write to the corresponding memory map. These bits are used to write protect any memory map. When all four bits are logic 1, a 32-bit write operation can be performed by the CPU with only one memory cycle. This is useful for intensive screen updates in graphics modes. For odd/even modes, maps 0 and 1, and maps 2 and 3 should have the same map mask value. When chain 4 mode is selected, all maps should be enabled. This is a read-modify-write operation for CPU write.

Table 8. Map Select (1)

Bit 5	Bit 3	Bit 2	Map	Table Location
0	0	0	0	1st 8K of Map 2
0	0	1	1	3rd 8K of Map 2
0	1	0	2	5th 8K of Map 2
0	1	1	3	7th 8K of Map 2
1	0	0	4	2nd 8K of Map 2
1	0	1	5	4th 8K of Map 2
1	1	0	6	5th 8K of Map 2
1	1	1	7	8th 8K of Map 2

Table 9. Map Select (2)

Bit 4	Bit 1	Bit 0	Map	Table Location
0	0	0	0	1st 8K of Map 2
0	0	1	1	3rd 8K of Map 2
0	1	0	2	5th 8K of Map 2
0	1	1	3	7th 8K of Map 2
1	0	0	4	2nd 8K of Map 2
1	0	1	5	4th 8K of Map 2
1	1	0	6	6th 8K of Map 2
1	1	1	7	8th 8K of Map 2

Character Map Select Register

Port = 03C5 **Index = 03**

Bit	Description
7, 6	Reserved
5	Character Map Select High Bit A
4	Character Map Select High Bit B
3, 2	Character Map Select A

1, 0 Character Map Select B

Bits 7, 6 Reserved

Bits 5,3,2 Selects font table from map 2 according to Table 8 when attribute bit 3 is a 1.

Bits 4,1,0 Selects font table from map 2 according to Table 9 when attribute bit 3 is a 0.

Note: Bit 3 of the attribute byte normally controls the ON/OFF of the foreground intensity in text modes. This bit however, may be redefined as a switch between character sets. For this feature to be enabled, the following statement must be true:

The setting value of Character Map Select A does not equal the value of Character Map Select B.

Memory Mode Register

Port = 03C5 **Index = 04**

Bit	Description
7-4	Reserved
3	Chain 4
2	Odd/Even
1	Extended Memory
0	Reserved

Bits 7-4 Reserved

Bit 3 A logic 0 enables the CPU to access data sequentially within a bit map by use of the Map Mask Register. A logic 1 causes two low-order address bits (A0, A1) to select the map that will be accessed in Table 10.

For read operation from the CPU, these two bits are also used to select the read maps in the graphics section.

Bit 2 A logic 0 directs even CPU addresses to access maps 0 and 2, while odd CPU addresses access maps 1 and 3, A logic 1 causes access to data within a bit map sequentially.

Bit 1 A logic 1 shows that greater than 64K bytes of video memory is being used. This is set to permit the VGA to use the 256K bytes of video memory. This also enables the character map selection. (See Character Map Select Register.)

Bit 0 Reserved

Table 10. Map Select (3)

A1	A0	Map Selected
0	0	Map 0
0	1	Map 1
1	0	Map 2
1	1	Map 3

CRT Controller Registers

This section describes all the registers in the CRT Controller. See Table 11.

Table 11. CRT Controller Registers

Register Name	Port	Index
CRT Controller Address Register	03?4	–
Horizontal Total	03?5	00
Horizontal Display Enable End	03?5	01
Start Horizontal Blanking	03?5	02
End Horizontal Blanking	03?5	03
Start Horizontal Retrace	03?5	04
End Horizontal Retrace	03?5	05
Vertical Total	03?5	06
Overflow	03?5	07
Preset Row Scan	03?5	08
Maximum Scan Line	03?5	09
Cursor Start	03?5	0A
Cursor End	03?5	0B
Start Address High	03?5	0C
Start Address Low	03?5	0D
Cursor Location High	03?5	0E
Cursor Location Low	03?5	0F
Start Vertical Retrace	03?5	10
End Vertical Retrace	03?5	11
Vertical Display Enable End	03?5	12
Offset	03?5	13
Underline Location	03?5	14
Start Vertical Blank	03?5	15
End Vertical Blank	03?5	16
CRTC Mode Control	03?5	17
Line Compare	03?5	18

? = B of D in accordance with Bit 0 of Miscellaneous Output register.

CRT Controller Address Register

Port = 3?4

Bit	Description
7-6	Reserved
5	Test Bit, must = 0
4-0	CRTC Address

Bits 7, 6 Reserved

Bit 5 Test bit, must remain 0.

Bit 4-0 Binary value programmed in these bits selects one of the CRT Controller registers where data is to be accessed.

Note: All CRT Controller Registers are Read/Write registers.

Horizontal Total Register

Port = 03?5 **Index = 0**

Bit	Description
7-0	Horizontal Total (-5)

In the CRT Controller, there is a horizontal character counter which counts character clock inputs generating from the Sequencer and compares against the value of the horizontal registers to provide horizontal timings. The horizontal total defines the total number of characters in the horizontal scan interval including the retrace time.

Bits 7-0 The total number of characters minus 5.

Horizontal Display Enable End Register

Port = 03?5 **Index = 01**

Bit	Description
7-0	Horizontal Display Enable End (−1)

This register defines the length of the horizontal display enable signal. It determines the number of displayed character positions per horizontal line.

Bits 7-0 Total number of displayed characters minus 1.

Start Horizontal Blanking Register

Port = 03?5 **Index = 02**

Bit	Description
7-0	Start Horizontal Blanking

Bit 7-0 These 8-bit values determine when to start the internal horizontal blanking output signal. When the internal character counter reaches this value, the horizontal blanking signal becomes active.

End Horizontal Blanking Register

Port = 03?5 **Index = 03**

Bit	Description
7	Test Bit
6-5	Display Enable Skew Control
4-0	End Blanking

Bit 7 Test Bit

Bits 6, 5 Bits 6 and 5 indicate the magnitude of display enable skew. Display enable skew control is necessary to give adequate time for the CRT Controller to interrogate the display buffer in order to obtain a character and attribute code. It must also access the character generator font, and subsequently access the Horizontal PEL Panning register in the Attribute Controller. The display enable signal must be skewed one character clock unit for every access. This allows the video output to be in synchronization with the horizontal and vertical retrace signals. See Table 12.

Bits 4-0 A binary value programmed in these bits is compared to the six least-significant bits of the horizontal character counter to determine the status of the horizontal blanking signal. The comparison is equal at the time the horizontal blanking signal becomes inactive. Use the following algorithm to calculate the width W of blanking signal:

Value of Start Blanking register + width of blanking signal in character clock units = 6-bit result to be programmed into these bits. Bit number 5 is located in the End Horizontal Retrace register.

Table 12. Skew

Bit 6	Bit 5	Amount of Skew
0	0	Zero
0	1	One
1	0	Two
1	1	Three

Start Horizontal Retrace Register

Port = 03?5 **Index = 04**

Bit	Description
7-0	Start Horizontal Retrace

Bits 7-0 This register is used to center the screen horizontally and to specify the character position at which the Horizontal Retrace Pulse becomes active. The value programmed is a binary count of the character position number at which the signal becomes active.

End Horizontal Retrace Register

Port = 03?5 **Index = 05**

Bit	Description
7	End Horizontal Blanking, bit 5
6, 5	Horizontal Retrace Delay
4-0	End Horizontal Retrace

This register specifies the character position at which the Horizontal Retrace Pulse becomes inactive.

Bit 7 This is bit number 5 of End Horizontal Blanking. The first four bits are located in the End Horizontal Blanking register (index hex 03).

Bits 6, 5 These bits control the skew of the Horizontal Retrace signal. See Table 12.

Bits 4-0 A value programmed here is compared to the five least-significant bits of the horizontal character counter. When they are equal, the horizontal retrace signal becomes inactive. Use the following algorithm to calculate the width W of the retrace signal:

Value of Start Horizontal Retrace Register + Width of Horizontal Retrace signal in character clock units = 5-bit result to be programmed into the End Horizontal Retrace Register.

Vertical Total Register

Port = 03?5 **Index = 06**

Bit	Description
7-0	Vertical Total (−2)

The 8-bit binary value gives the number of horizontal scan lines on the CRT screen, minus 2, including vertical retrace. This is the low-order 8-bits of a 10-bit register. Bit 8 or this register is located in the CRT Controller Overflow register (hex 07, bit 0). Bit 9 of this register is located in the CRT Controller Overflow register (hex 07, bit 5).

Bits 7-0 Total number of horizontal scan lines, minus 2.

Overflow Register

Port = 03?5 **Index = 07**

Bit	Description
7	Start Vertical Retrace Bit 9
6	Vertical display Enable End Bit 9
5	Vertical Total Bit 9
4	Line Compare Bit 8
3	Start Vertical Blank Bit 8
2	Start Vertical Retrace Bit 8
1	Vertical display Enable End Bit 8
0	Vertical Total Bit 8

Bit 7 Bit 9 of the Start Vertical Retrace register.

Bit 6 Bit 9 of the Vertical display Enable End Register.

Bit 5 Bit 9 of the Vertical Total Register.

Bit 4 Bit 8 of the Line Compare Register.

Bit 3 Bit 8 of the Start Vertical Blank Register.

Bit 2 Bit 8 of the Start Vertical Retrace Register.

Bit 1 Bit 8 of the Vertical Display Enable End Register.

Bit 0 Bit 8 of the Vertical Total Register.

Preset Row Scan Register

Port = 03?5 **Index = 08**

Bit	Description
7	Reserved
6, 5	Byte Panning Control
4-0	Starting Row Scan Count after a Vertical Retrace

Bit 7 Reserved

Bits 6, 5 Bits 6 and 5 control byte panning when programmed as multiple shift modes. (This is currently not used.) The PEL Panning register in the attribute section allows panning of up to eight single PELs. When in single byte shift modes the CRT Controller start address is increased by one, while attribute panning is reset to 0. This is done to pan the next higher PEL. When used for multiple shift modes, the byte pan bits are extensions to the attribute PEL Panning register. In this manner, panning across the width of the video output shift is achieved. In the 32-bit shift mode, the byte pan and PEL panning bits provide up to 31 bits of panning capability. To pan from position 31 to 32, the CRT Controller start address is incremented and PEL and byte panning is reset to 0. These bits should normally be set to 0.

Bits 4-0 A binary value to specify the starting row scan count after a vertical retrace. The row scan counter increments each horizontal retrace time until a maximum row scan occurs.

Table 13. Clock Skew

Bit 6	Bit 5	Function
0	0	Zero-character clock skew
0	1	One-character clock skew
1	0	Two-character clock skew
1	1	Three-character clock skew

At maximum row scan compare time, the row scan is cleared (not preset).

Maximum Scan Line Register

Port = 03?5 **Index = 09**

Bit	Description
7	200 → 400 Line Conversion
6	Line Compare Bit 9
5	Start Vertical Blank Bit 9
4-0	Maximum Scan Line

Bit 7 A logic 1 causes the clock to the row scan counter to be divided by 2 and enables 200 to 400 line conversion. This allows the older 200-line modes to be displayed as 400 lines on the display (i. e. each line is displayed twice). When this bit is a 0, the clock to the row scan counter is equal to the horizontal scan rate.

Bit 6 Bit 9 of the Line Compare Register.

Bit 5 Bit 9 of the Start Vertical Blank Register.

Bit 4-0 These bits specify the number of lines per character row. The number to be programmed is the maximum row scan number minus 1.

Cursor Start Register

Port = 03?5 **Index = 0A**

Bit	Description
7, 6	Reserved
5	Cursor Off
4-0	Cursor Starts

Bits 7, 6 Reserved

Bit 5 A logic 1 turns off the cursor, a logic 0 turns on the cursor.

Bits 4-0 The value of these five bits tells the row scan line of a character where cursor is to begin.

Note that when Cursor Start is programmed with a value greater than the Cursor End, no cursor is generated.

Cursor End Register

Port = 03?5 **Index = 0B**

Bit	Description
7	Reserved
6, 5	Cursor Skew Control
4-0	Cursor Ends

Bit 7 Reserved

Bits 6, 5 These bits control the skew of the cursor signal. Cursor skew delays the cursor by the selected number of clocks. Each additional skew moves the cursor right one position on the screen. See Table 13.

Bits 4-0 These bits specify the row scan line of a character where the cursor is to end.

Start Address High Register

Port = 03?5 **Index = 0C**

Bit	Description
7-0	High Order 8-bit Start Address

Bits 7-0 These are the high order 8 bits of the start address. The 16-bit value, from the high-order and low-order Start Address Registers, is the first address after the vertical retrace on each screen refresh.

Start Address Low Register

Port = 03?5 **Index = 0D**

Bit	Description
7-0	Low Order Start Address

Bits 7-0 These are the low-order 8 bits of the start address.

Cursor Location High Register

Port = 03?5 **Index = 0E**

Bit	Description
7-0	High Order Cursor Location

Bits 7-0 These are the high-order 8 bits of the cursor location.

Cursor Location Low Register

Port = 03?5 **Index = 0F**

Bit	Description
7-0	Low Order Cursor Location

Bits 7-0 These are the low-order 8 bits of the cursor location.

Start Vertical Retrace Register

Port = 03?5 **Index = 10**

Bit	Description
7-0	Low Order 8-bit Vertical Retrace Pulse

Bits 7-0 These are the low-order 8 bits of the vertical retrace pulse start position in horizontal scan lines. Bits 8 and 9 are in the CRTC Overflow register.

End Vertical Retrace Register

Port = 03?5 **Index 11**

Bit	Description
7	Protect R0-R7
6	Select 5 Refresh Cycles
5	0 = Enable Vertical Interrupt

4	0 = Clear Vertical Interrupt
3-0	End Vertical Retrace
Bit 7	A logic 0 enables writing to CRTC registers 0-7. A logic 1 disables writing these registers. Note that the line comparing bit 4 in register 07 is not protected.
Bit 6	A logic 0 selects three refresh DRAM cycles. A logic 1 selects five refresh cycles per horizontal line. Five refresh cycles are used for slow (15.75 KHz) sweep rate displays.
Bit 5	A logic 0 enables a vertical retrace interrupt. This occurs on IRQ2. Since this may be a "shared" interrupt level, the Input Status register 0, bit 7, must be checked to determine if the VGA caused the interrupt to occur.
Bit 4	A logic 0 clears a vertical retrace interrupt. An interrupt handler has to reset an internal flip-flop by writing a 0 to this bit, then setting the bit to 1 so that the flip-flop does not hold interrupts inactive. Note that you do not change the other bits in this register when changing this bit. Read this register first before resetting this flip-flop so that the value of the other bits can be determined and saved for later use.
Bits 3-0	These bits determine the horizontal scan count value when the vertical retrace output signal becomes inactive. Use the following algorithm to calculate the width of vertical retrace signal: Value of Start Vertical Retrace register + width of vertical retrace signal in horizontal scan line units = 4-bit result to be programmed into the End Vertical Retrace register.

Vertical Display Enable End Register

Port = 03?5 **Index = 12**

Bit	Description
7-0	Low Order Vertical Display Enable End (−1)
Bits 7-0	These are the low-order 8 bits of a 10-bit register that determines the vertical display enable end position. Bits 8 and 9 of this register are contained in the CRT Controller Overflow register bits 1 and 6 respectively.

Offset Register

Port = 03?5 **Index = 13**

Bit	Description
7-0	Logic Line Width of the Screen
Bits 7-0	This register defines the logic line width of the screen. Starting memory address for the next character row is larger than the current character row by a factor of 2X or 4X this value. A word address programs the Offset Register. This word address may be a word or double word address, determined by the means of clocking the CRT Controller.

Underline Location Register

Port = 03?5 **Index = 14**

Bit	Description
7	Reserved
6	Doubleword Mode
5	Count by 4
4-0	Horizontal row scan where underline will occur
Bit 7	Reserved
Bit 6	A logic 1 enables double-word mode for memory addresses. Also, see the description of the CRT Controller Mode Control register bit 6.
Bit 5	When this bit is set to 1, the memory address counter is clocked with the character clock divided by 4. This bit is used when double-word addresses are used.
Bits 4-0	This register determines the horizontal row scan of a character row where an underline occurs. The scan line number desired is a value one greater than the number programmed.

Start Vertical Blanking Register

Port = 03?5 **Index = 15**

Bit	Description
7-0	Start Vertical Blanking (−1)
Bits 7-0	These are the low-order 8 bits of a 10-bit register. The value of this register determines when the vertical blanking signal becomes active. Bit 8 is located in the CRT Controller Overflow register bit 3. Bit 9 is contained in the CRT Controller Maximum Scan Line register bit 5. The horizontal scan line count (at which the vertical blanking signal becomes active) is one greater than the value of these 10 bits.

End Vertical Blanking Register

Port = 03?5 **Index = 16**

Bit	Description
7-0	End Vertical Blanking
Bits 7-0	This register defines the horizontal scan count value at the time the vertical blank output signal goes inactive. The register must be

programmed in whole units of horizontal scan lines. Use the following algorithm to obtain the width of the vertical blank signal.

(Value of Start Vertical Blank register−1) + width of vertical blank signal in horizontal scan unit = 8-bit result to be programmed into the End Vertical Blank register.

CRTC Mode Control Register

Port = 03?5 **Index = 17**

Bit	Description
7	Hardware Reset
6	Word/Byte Mode
5	Address Wrap
4	Reserved
3	Count by Two
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	CMSO

Bit 7 A logic 0 clears horizontal and vertical retrace. A logic 1 enables horizontal and vertical retrace. This bit does not reset any other registers or outputs.

Bit 6 A logic 0 selects the word address mode which shifts all memory address counter bits down one bit, and the most significant bit of the counter appears on the least significant bit of the memory address output. A logic 1 selects the byte address mode. Note that bit 6 of the Underline Location register also controls the addressing. When it is a 0, bit 6 of this register has control. When it is a 1, the addressing is forced to be shifted by two bits.

Bit 5 This bit selects the memory address counter bit MA13 or bit MA15, and it appears on the MA0 of CRT address output in the word address mode. A logic 1 selects MA15. MA13 is selected for the case where only 64K memory is installed. Since 256K memory is always installed for UM587, MA15 should be selected in odd/even mode.

Bit 4 Reserved

Bit 3 A logic 0 causes the memory address counter clocked with the normal character clock input. A logic 1 clocks the memory address counter with the character clock input divided by 2. This bit is used to create either a byte or word refresh address for the display buffer.

Bit 2 A logic 0 selects normal horizontal retrace. A logic 1 selects horizontal retrace divided by 2 as the clock that controls the vertical timing counter. This bit can be used to effectively double the vertical resolution capability of the CRT Controller. The 10-bit vertical counter has a maximum of 1024 scan lines. If the vertical counter is clocked with the horizontal retrace divided by 2, then the vertical resolution is doubled to 2048 horizontal scan lines.

Bit 1 A logic 0 selects row scan counter bit 1 for CRT memory address bit MA14. A logic 1 selects MA14 counter bit for CRT memory address bit MA14.

Bit 0 When this bit is a logic 0, row scan address bit 0 is substituted for memory address bit 13 during active display time. A logic 1 enables memory address bit 13 to appear on the memory address output bit 13 of the CRT Controller.

Table 14. Register Modes

Memory Address	Byte Mode	Word Mode	Double-word Mode
MA0/RFA0	MA0	MA15/MA13	MA12
MA1/RFA1	MA1	MA0	MA13
MA2/RFA2	MA2	MA1	MA0
MA3/RFA3	MA3	MA2	MA1
MA4/RFA4	MA4	MA3	MA2
MA5/RFA5	MA5	MA4	MA3
MA6/RFA6	MA6	MA5	MA4
MA7/RFA7	MA7	MA6	MA5
MA8/RFA8	MA8	MA7	MA6
MA9	MA9	MA8	MA7
MA10	MA10	MA9	MA8
MA11	MA11	MA10	MA9
MA12	MA12	MA11	MA10
MA13	MA13	MA12	MA11
MA14	MA14	MA13	MA12
MA15	MA15	MA14	MA13

Line Compare Register

Port = 03?5 **Index = 18**

Bit	Description
7-0	Line Compare Target

Bits 7-0 This register is the lower byte of the line compare target. When the vertical counter achieves this value, the internal start of the line counter is reset. This causes an area of the screen to not be affected by scrolling. Bit 9 is in the Maximum Scan Line register. Bit 8 of this register is in the Overflow Register.

Graphics Controller Registers

This section describes all the registers located in the Graphics Controller. See Table 15.

Table 15. Graphics Controller Registers

Register Name	Port	Index
Graphics Address	03CE	–
Set/Reset	03CF	00
Enable Set/Reset	03CF	01
Color Compare	03CF	02
Data Rotate	03CF	03
Read Map Select	03CF	04
Graphics Mode	03CF	05
Miscellaneous	03CF	06
Color Don't Care	03CF	07
Bit Mask	03CF	08

Graphics Address Register

Port = 03CE

Bit	Description
7-4	Reserved
3-0	Graphics Address

Bits 7-4 Reserved

Bits 3-0 A binary value in these bits points to the other registers in the Graphics Controller section.

Set/Reset Register

Port = 03CF **Index = 00**

Bit	Description
7-4	Reserved
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bits 7-4 Reserved

Bits 3-0 During CPU memory write with write mode 0, the value of these bits will be written to all eight bits of the respective memory map if Set/Reset mode is enabled for the corresponding map.

Enable Set/Reset Register

Port = 03CF **Index = 01**

Bit	Description
7-4	Reserved
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bits 7-4 Reserved

Bits 3-0 A logic 1 enables the Set/Reset function. When enabled, the respective memory map is written with the value of the Set/Reset register, if write mode 0 is selected. However, when write mode is 0 and Set/Reset is not enabled on a map, that map is written with the value of the system microprocessor data.

Color Compare Register

Port = 03CF **Index = 02**

Bit	Description
7-4	Reserved
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bits 7-4 Reserved

Bits 3-0 These bits represent a 4-bit color value to be compared if the system microprocessor sets read mode 1 and does a memory read, the data returned from the memory cycle will be a 1 in each bit position where the four maps equal the color compare register.

The color compare bit is the value that all bits of the corresponding map's byte are compared with. Each of the eight bit positions of the selected byte are then compared across the four maps and a 1 is returned in each bit position where the bits of all four maps equal their respective color compare values.

Data Rotate Register

Port = 03CF **Index = 03**

Bit	Description
7-5	Reserved
4	Function Select
3	Function Select
2	Rotate Count 2
1	Rotate Count 1
0	Rotate Count 0

Bits 7-5 Reserved

Bits 4, 3 Data in the system microprocessor latches can operate logically with data written to memory. If rotate function is selected, it is applied before the logic function. See Table 17.

Bits 2-0 These bits specify the number of positions to right-rotate the system microprocessor data bus during system microprocessor memory writes. This operation is done when the write mode is 0. To write nonrotated data, the bits should be set to 0. See Table 17.

Table 16. Data Functions

Bit 4	Bit 3	Function
0	0	Data unmodified
0	1	Data ANDed with latched data
1	0	Data ORed with latched data
1	1	Data XORed with latched data

Table 17. Rotate Functions

Bit 2	Bit 1	Bit 0	Function
0	0	0	No Rotate
0	0	1	Rotate 1 Position
0	1	0	Rotate 2 Positions
0	1	1	Rotate 3 Positions
1	0	0	Rotate 4 Positions
1	0	1	Rotate 5 Positions
1	1	0	Rotate 6 Positions
1	1	1	Rotate 7 Positions

Read Map Select Register

Port = 03CF **Index = 04**

Bit Description
7-2 Reserved
1 Map Select 1
0 Map Select 0

Bits 7-2 Reserved

Bits 1, 0 These bits select the memory map number from which the system microprocessor reads data. This register has no effect on the color compare read mode. In odd/even modes the value may be 00 or 01 (10 or 11) for chained maps 0, 1 (2, 3). See Table 18.

Table 18. Map Data

MS1	MS0	Function
0	0	Read data from Map 0
0	1	Read data from Map 1
1	0	Read data from Map 2
1	1	Read data from Map 3

Graphics Mode Register

Port = 03CF **Index = 05**

Bit Description
7 Reserved
6 256 Color Mode
5 Shift Register Mode
4 Odd/Even
3 Read Type
2 Reserved
1, 0 Write Mode

Bit 7 Reserved

Bit 6 A logic 0 permits bit 5 to handle the loading of the Shift Registers. A logic 1 supports the 256 color mode (only for 320x200 320x 400 resolution).

Bit 5 A logic 1 instructs the Shift Registers in the graphic section to format the serial data with odd-numbered bits from both maps on the odd-numbered maps and even-numbered bits from both maps on the even-numbered maps. This bit is also used in modes 4 and 5.

Bit 4 A logic 1 enables the odd/even addressing mode, which can emulate the IBM CGA compatible mode. The value programmed is the value of the Memory Mode register bit 2 of the Sequencer.

Bit 3 A logic 0 causes the system microprocessor to read data from the memory map selected by the Read Map Select register unless chain 4, link 4, or link 8 is set to 1. In this case the Read Map Select register has no effect. When this bit is a logic 1, the system microprocessor reads the results of the comparison of the four memory maps and the Color Compare register.

Bit 2 Reserved

Bits 1, 0 Write Mode (See Table 19.)

Miscellaneous Register

Port = 03CF **Index = 06**

Table 19. Function Decode

Bit-1	Bit-0	Function
0	0	The system microprocessor data is rotated by the number or counts in the Rotate Register that each memory map is written with, unless Set/Reset is enabled for the map. When the map Set/Reset is enabled, they are written with 8-bits of the value in the Set/Reset Register for that map.
0	1	The contents of the system microprocessor latches are written to each memory map. A system read operation loads these latches.
1	0	8-bits of the value of data bit n fills memory map n (0-3).
1	1	The maps are written by the 8-bits contained in the Set/Reset Register for that specific map (Enable Set/Reset Register is a "don't care"). Rotated system microprocessor data is logically ANDed with Bit Mask Register data and forms an 8-bit value. This is the function that the Bit Mask Register performs in write modes 0 and 2. (See Bit Mask Register.)

Note that the logic function specified by the Function Select register is applied to data being written to memory following modes 0, 2, and 3 described above.

Bit	Description
7-4	Reserved
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bits 7-4 Reserved

Bits 3, 2 These bits control the mapping between regenerative buffer and the CPU address space. The bit functions are defined in Table 20.

Bit 1 When set to a logic 1, this bit instructs the system microprocessor address bit 0 to be replaced by a higher-order bit. The odd/even maps will be selected with odd/even values of the system microprocessor A0 bit, respectively.

Bit 0 This is the text mode addressing control. A logic 1 enables the graphics mode. The character generator address latches are disabled, when set to graphics mode.

Table 20. Byte Select

Bit 3	Bit 2	Function
0	0	Hex A0000 for 128K bytes
0	1	Hex A0000 for 64K bytes
1	0	Hex B0000 for 32K bytes
1	1	Hex B8000 for 32K bytes

Color Don't Care Register

Port = 03CF **Index = 07**

Bit	Description
7-4	Reserved
3	Map 3 = Don't Care
2	Map 2 = Don't Care
1	Map 1 = Don't Care
0	Map 0 = Don't Care

Bits 7-4 Reserved

Bit 3 1 - Do the color compare for map 3.
0 - Don't Care for map 3.

Bit 2 1 - Do the color compare for map 2.
0 - Don't Care for map 2.

Bit 1 1 - Do the color compare for map 1.
0 - Don't Care for map 1.

Bit 0 1 - Do the color compare for map 0.
0 - Don't care for map 0.

Bit Mask Register

Port = 03CF **Index = 08**

Bit Description

7-0 Bit Mask for 8-bits of data

Bits 7-0 Bits programmed to a 1 allow writes to the corresponding bits in the maps. A logic 0 permits the corresponding bit n in each map to be locked at its current state, providing the location being written was the final location read by the system's microprocessor.

Note that the bit mask applies to write modes 0 and 2. To preserve bits using the bit mask, data must be latched internally by reading the location. When data is written to preserve the bits, the most current data in the latches is written in those positions. The bit mask applies to all maps simultaneously.

Attribute Controller Registers

This section describes all the registers located in Attribute Controller section. See Table 21.

Table 21. Attribute Controller Registers

Register Name	Port	Index
Address Register	03C0	–
Palette Registers	03C0	00-0F
Attribute Mode Control Register	03C0	10
Overscan Color Register	03C0	11
Color Plan Enable Register	03C0	12
Horizontal PEL Panning Register	03C0	13
Color Select Register	03C0	14

Attribute Address Register

Port = 03C0

Bit	Description
7, 6	Reserved
5	Palette Address Source
4-0	Attribute Address

Bits 7, 6 Reserved

Bit 5 Bit 5 must be cleared to 0 before loading the Color Palette registers. Normal operation of the Attribute Controller requires that bit 5 be set to 1. This allows the video memory data to access the palette registers.

Bits 4-0 A binary value in these bits points to the Attribute Data register where data is to be written.

The Address and Data registers can not be selected by the Attribute Controller register. An internal address flip-flop controls this selection. To initialize the flip-flop, an I/O Read instruction must be sent to the Attribute Controller at address 03BA or 03DA. This clears the flip-flop, and then selects the Address register. The Address register is then loaded with an I/O Write to 03C0. The following I/O Write instruction to 03C0 loads the Data register. The flip-flop changes state each time an I/O Write instruction is sent to the Attribute Controller. It does not change when an I/O Read to 03C1 occurs.

Palette Registers

Write-03C0 Read-03C1 Index-00-0F

Bit	Description
7, 6	Reserved
5	P5
4	P4
3	P3
2	P2
1	P1
0	P0

Bits 7, 6 Reserved

Bits 5-0 The attribute byte of text or graphic color value is indexed to these 16 Color Palette registers. The contents of the pointed Palette registers are then used as values sent off the chip to the video DAC, where they in turn serve as addresses into the DAC internal registers. A logic 1 selects the appropriate color.

The Palette registers should be modified only during the vertical retrace interval to avoid problems with the displayed image.

Attribute Mode Control

Port - 03C0(R), 03C1(W) **Index = 10**

Bit	Description
7	P5, P4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved
3	Select Background Intensity or Enable Blink
2	Enable Line Graphics Character Code
1	Mono Emulation
0	Graphics/Alphanumeric Mode

Bit 7 A logic 0 selects the output of the Palette register as P5, P4. A logic 1 selects bits 1, 0 of the Color Select register as P5, P4 which are digital video bits that go off the chip.

Bit 6 A logic 1 causes the video pipeline to be sampled so that eight bits are available to select a color in the 256 color mode (hex 13). This bit must be a logic 0 in all other modes.

Bit 5 A logic 0 makes line compare and has no effect on the output of the PEL Panning register. A logic 1 causes a line compare

in the CRTC to force the output of the PEL Panning register to 0. When VSYNC occurs, the output reverts to its programmed value. This bit allows part of the screen to be panned.

Bit 4 Reserved

Bit 3 This bit is set to 1 for blinking graphics modes. A logic 1 enables the blink function in alphanumeric modes. A logic 0 selects the background intensity of the input. Previously, this mode was on the MDA and CGA modes.

Bit 2 A logic 1 enables the special line graphics character codes for the Monochrome emulation mode. A logic 0 causes the ninth dot the same as the background. When this bit is enabled it forces the ninth dot of a line graphic character to be the same as the eighth dot of a line graphic character. Graphics character codes are hex C0 through hex DF. For character fonts that do not use the line graphics character codes in this range (hex C0 through hex DF) bit 2 should be a 0. If not, unwanted video information will be shown on the CRT screen.

Bit 1 A logic 1 sets monochrome emulation mode. A logic 0 sets color emulation mode.

Bit 0 A logic 0 selects text mode. A logic 1 selects graphics mode.

Overscan Color Register

Port = 03C0(R), 03C1(W) **Index = 11**

Bit	Description
7	P7
6	P6
5	P5
4	P4
3	P3
2	P2
1	P1
0	P0

Bits 7-0 A binary value in this register determines the border color displayed on the CRT screen. The border color is displayed right after the Display Enable signal goes low and before the start of blanking period. The border is not supported in the 40-column text modes or the 320-PEL graphics modes, except for mode hex 13.

Color Plane Enable

Port = 03C0(R), 03C1(W) **Index = 12**

Bit	Description
7, 6	Reserved
5, 4	Video Status MUX
3-0	Enable Color Plane

Bits 7, 6 Reserved

Bits 5, 4 Two of the eight color outputs will be selected, according to these two bits, to reflect the real time status on bits 4 and 5 of Input Status Register 1. See Table 22.

Bits 3-0 A logic 1 for each bit enables the respective display memory color plane. A logic 0 disables color plane.

Table 22. Color Plane And Status

Color Plane Register Bit 5	Color Plane Register Bit 4	Input Status Register 1 Bit 5	Input Status Register 1 Bit 4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

Horizontal PEL Panning

Port = 3C0(W), 3C1(R) **Index = 13**

Bit	Description
7-4	Reserved
3-0	Horizontal PEL Panning

Bits 7-4 Reserved

Bits 3-0 These four bits select the number of pixels that will shift the video data to the left. PEL panning is available in both graphics and text modes. In modes 0+, 1+, 2+, 3+, 7 and 7+, the maximum shift is eight pixels. Mode 13 allows a maximum of three pixels. In the rest of the modes, the image can be shifted a maximum of seven pixels. The order for shifting the image is shown in Table 23.

Table 23. PEL Register

PEL Panning Register Value	Number of PELs Shifted to the Left: 0+, 1+, 2+ 3+, 7, 7+	Number of PELs Shifted to the Left: All Other Modes	Number of PELs Shifted to the Left: Mode 13
0	1	0	0
1	2	1	–
2	3	2	1
3	4	3	–
4	5	4	2
5	6	5	–
6	7	6	3
7	8	7	–
8	0	–	–

Color Select Register

Port = 03C0(W), 03C1(R) **Index = 14**

Bit	Description
7-4	Reserved
3	Select Color 7
2	Select Color 6
1	Select Color 5
0	Select Color 4

Bits 7-4 Reserved

Bits 3, 2 These bits are the two high-order bits of the 8-bit digital color value sent off-chip in all modes except the 256 color graphics. In the 256 color modes, the 8-bit attributes are stored in video memory. This becomes the 8-bit digital color value to be sent off-chip to the video DAC. These bits are also used to switch quickly among sets of colors in the video DAC.

Bits 1, 0 These two bits can be used to replace the P4 and P5 bits from the Attribute Palette registers to form the 8-bit digital color value sent off-chip. This is controlled by bit 7 of Attribute Mode Control register. By using this feature, sets of colors can be rapidly switched in the video DAC.

Extended Registers

A set of new registers have been added into the basic version of the VGA to perform new features. They are grouped under the assignment of I/O ports 3DE and 3DF for address and data access respectively. All, except the NMI Data Cache registers, have both read and write access. A summary of new registers is given in Table 24.

Table 24. Extended Registers

Port	Index	R/W	Bits	Register
3DE	–	R/W	5	Extension Address Register
3DF	D	R/W	6	Bandwidth Control
3DF	E	R/W	4	I/O Trap Control
3DF	F	R	8	NMI Data Cache (FIFO)
3DF	10	R	8	Read DIP Switch

3DE-Extension Address Register

Bit	Description
0-4	5-bit index pointer to the extension data registers.
5-7	Reserved

The contents of this register need to be programmed before the data register is accessed. The I/O port assigned is 3DE for both read and write access.

3DF-Bandwidth Control

Index D

Bit	Description
0-2	Reserved
3-4	Bandwidth Control (See Table 25.)
5	Clock select bit 2 (CSEL2).

Used with bits 2 and 3 of Miscellaneous Register. One of eight different clock inputs can be selected. (See Table 26.)

Table 25. Bandwidth

Bit 4	Bit 3	Bandwidth
0	0	1-4
1	0	1-7
0	1	1-9
1	1	Reserved

Table 26. Clock

CSEL2	CSEL1	CSEL0	Clock
0	0	0	25.175 MHz
0	0	1	28.322 MHz
0	1	0	External Input Clock
0	1	1	Reserved
1	0	0	14.318 MHz
1	0	1	16.257 MHz
1	1	0	Reserved
1	1	1	35.5 MHz

3DF-I/O Trap Control **Index E**

Bit	Description
0	When set to 1, the trap is activated and generates NMI for downward compatibility emulation. When set to 0, the NMI logic is turned off.
1-2	Backward Compatibility Mode (See Table 27.)
3-6	Reserved = 0
7	Graphics Latch read compatibility.

Table 27. Graphics Mode

Bit 2	Bit 1	Mode
0	0	VGA
0	1	EGA
1	0	CGA
1	1	MCGA (MDA & HERC)

3DF - NMI Data Cache **Index F**

Bit	Description
0-7	First read of this register gets the address of the trapped I/O. Second read gets the data of the trapped I/O. The size of the cache is two bytes wide and five rows deep. Each read causes the read pointer to autoincrement resets at the end of information. Note that only the first 8-bits of I/O address are saved into cache. That means the first digit "3" is ignored. The trapped software should take care of this after receiving the address from cache. Since bit 7 of the first read of this register is always 1 if there is an address saved at this position, the trapped software should check this bit to determine whether this is a last read or not. Note that this is a read only register.

3DF - Read DIP Switch **Index 10**

Bit	Description
7	Reserved
6	DIP Switch 6
5	DIP Switch 5
4	DIP Switch 4
3	DIP Switch 3
2	DIP Switch 2
1	DIP Switch 1
0	DIP Switch 0

These bits will be read in during BIOS initialization to determine the type of monitor currently attached.

AC Characteristics: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, GND = 0V

I/O Read/Write, DAC Read/Write, Switch Read (See Figures 1, 2, 8, 9 & 10.)

Symbol	Parameter	Min.	Max.	Unit	Conditions
tACS	Address Setup Time	60	–	ns	
tCCS	ASEL Setup Time	30	–	ns	
tCAH	Address Hold Time	0	–	ns	
tCCH	ASEL Hold Time	0	–	ns	
tCPW	Command Pulse Width (Note)	200	–	ns	
tDWD	Write Data Delay	–	80	ns	
tDWH	Write Data Hold Time	0	–	ns	
tCED	$\overline{EDBUF}$ and $\overline{EABUF}$ Delay	–	50	ns	
tRDD	Read Data Valid Delay	–	120	ns	
tRDH	Read Data Hold Time	10	–	ns	
tRDIRD	Read to DIR Delay	–	45	ns	
tDRDD	$\overline{DACR}$ Delay	–	50	ns	
tDWDD	$\overline{DACW}$ Delay	–	50	ns	
tRDACD	Read to DAC Read Delay	–	40	ns	
tWDACD	Write to DAC Write Delay	–	40	ns	
tRSWTR	Read to Switch Read Delay	–	40	ns	

Memory Read/Write (See Figures 3 & 4.)

Symbol	Parameter	Min.	Max.	Unit	Conditions
tACS	Address Setup Time	60	–	ns	
tCCS	ASEL Setup Time	30	–	ns	
tCAH	Address Hold Time	0	–	ns	
tCCH	ASEL Hold Time	0	–	ns	
tDWD	Write Data Delay	–	80	ns	
tDWH	Write Data Hold Time	0	–	ns	
tCED	$\overline{EDBUF}$ and $\overline{EABUF}$ Delay	–	50	ns	
tRDIRD	Read to DIR Delay	–	45	ns	
tMRIOLD	Command to CPURDY Low Delay	–	40	ns	
tMRIOHD	RD Data to CPURDY High Delay	–	15	ns	
tVDH	Valid RD Data Hold Time	–	45	ns	

Clock and Video (See Figure 5.)

Symbol	Parameter	Min.	Max.	Unit	Conditions
tCLK	CLKIN/DOTCLK Cycle	28	–	ns	
tPEL	P0-P7 Delay	–	80	ns	
tBNK	$\overline{BLANK}$ Delay	–	80	ns	
tSYNC	HSYNC/VSYNC Delay	–	80	ns	
tPCLK	CLKIN to PCLK Delay	–	60	ns	

DRAM Read/Write (See Figures 6 & 7.)

Symbol	Parameter	Min.	Max.	Unit	Conditions
tRS	Row Address Setup	10	–	ns	
tRH	Row Address Hold Time	0.5 tCLK	–	ns	
tRPW	$\overline{RAS}$ Low Time	4 tCLK - 10	–	ns	
tRPC	$\overline{RAS}$ High Time	3 tCLK	–	ns	
tCS	Column Address Setup Time	10	–	ns	
tCH	Column Address Hold Time	tCLK	–	ns	
tCPW	$\overline{CAS}$ Low Time	4.5 tCLK	–	ns	
tCPC	$\overline{CAS}$ High Time	2.5 tCLK - 10	–	ns	
tROED	$\overline{RAS}$ to $\overline{OE}$ Delay	2.5 tCLK - 10	–	ns	
tRWE	$\overline{RAS}$ to $\overline{WE}$ Delay	2.5 tCLK - 10	–	ns	
tWER	$\overline{WE}$ to $\overline{RAS}$ High	tCLK	–	ns	
tRC	$\overline{RAS}$ to $\overline{CAS}$ Reference	1.5 tCLK - 10	–	ns	
tDWS	Data to $\overline{WE}$ Setup Time	10	–	ns	
tDWH	Data to $\overline{WE}$ Hold Time	tCLK	–	ns	

Timing Waveforms

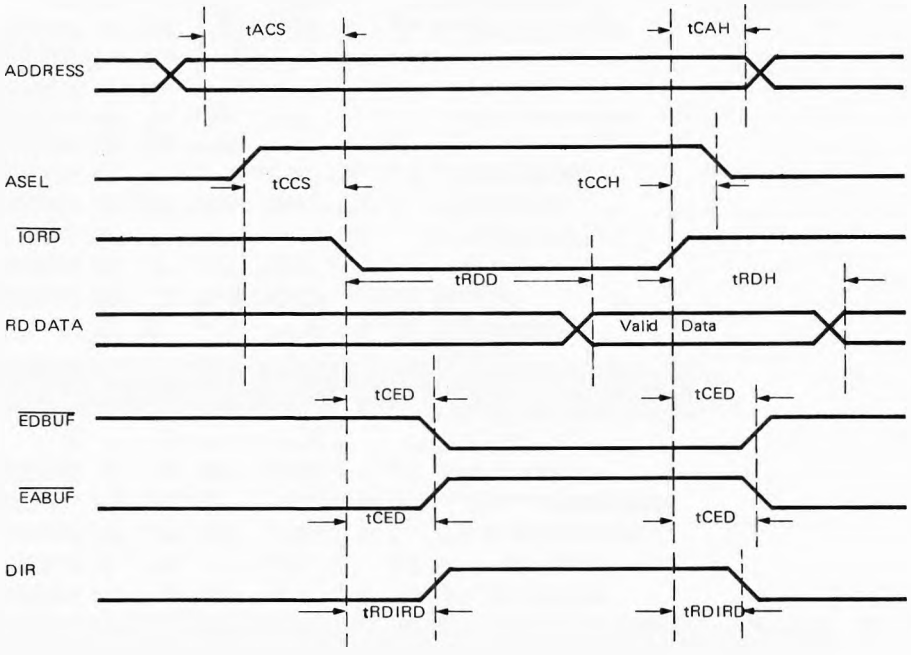


Figure 1. I/O READ TIMING

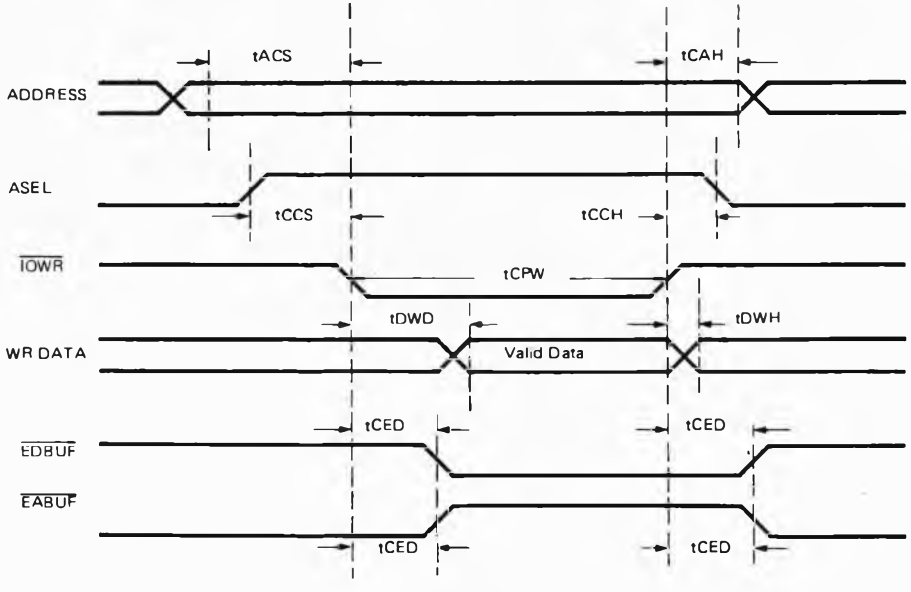


Figure 2. I/O WRITE TIMING

Timing Waveforms (Continued)

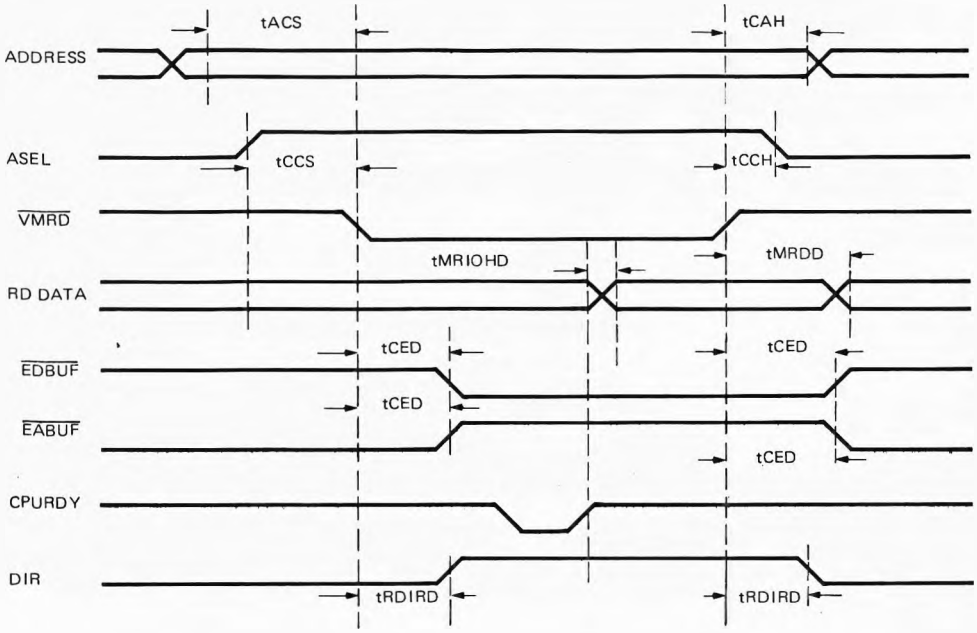


Figure 3. MEMORY READ TIMING

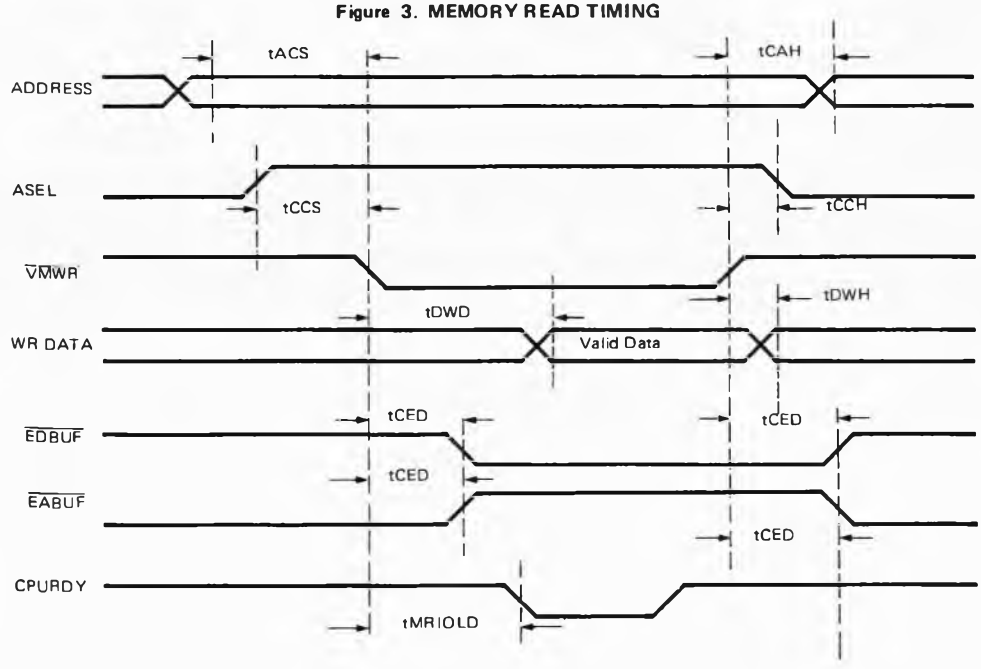


Figure 4. MEMORY WRITE TIMING

Timing Waveforms (Continued)

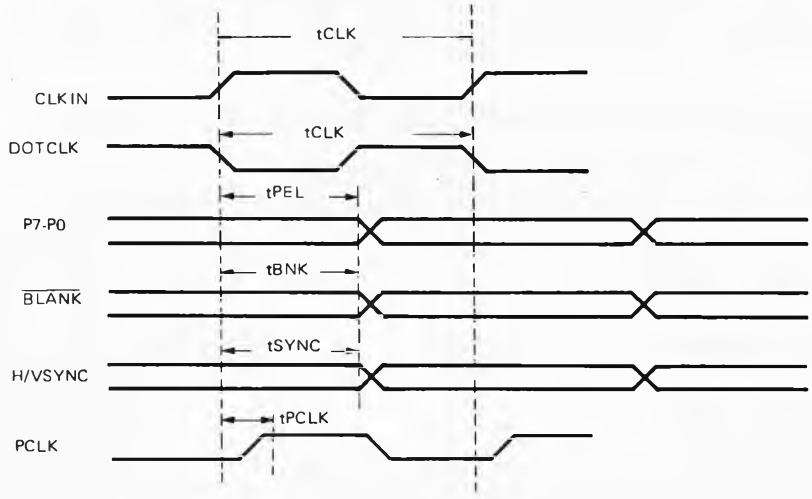


Figure 5. CLOCK AND VIDEO TIMING

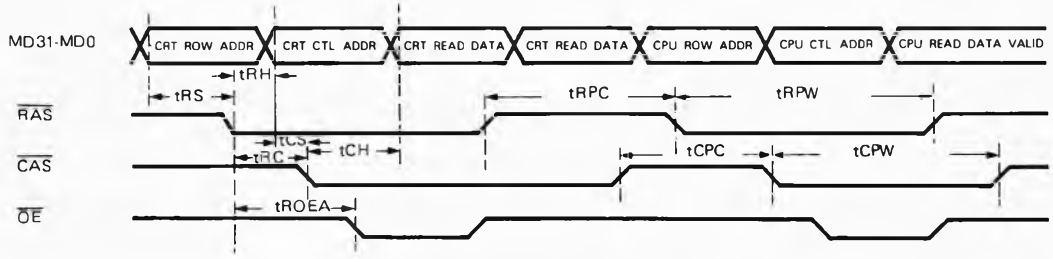


Figure 6. DRAM READ TIMING

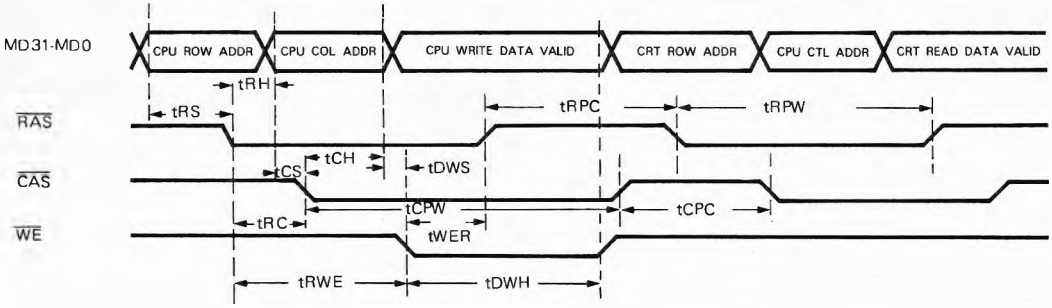


Figure 7. DRAM WRITE TIMING

Timing Waveforms (Continued)

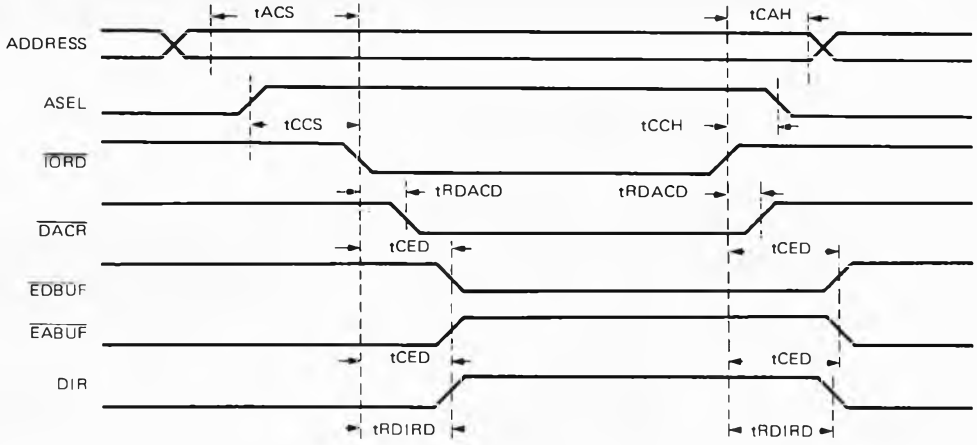


Figure 8. DAC Read Timing

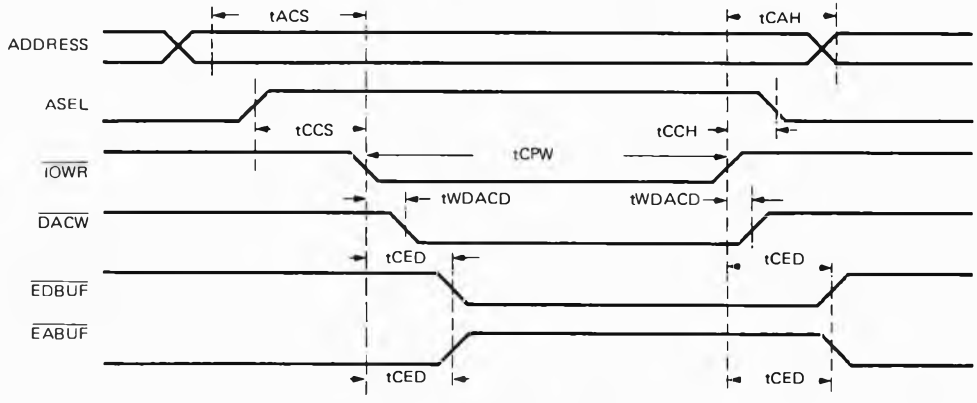


Figure 9. DAC Write Timing

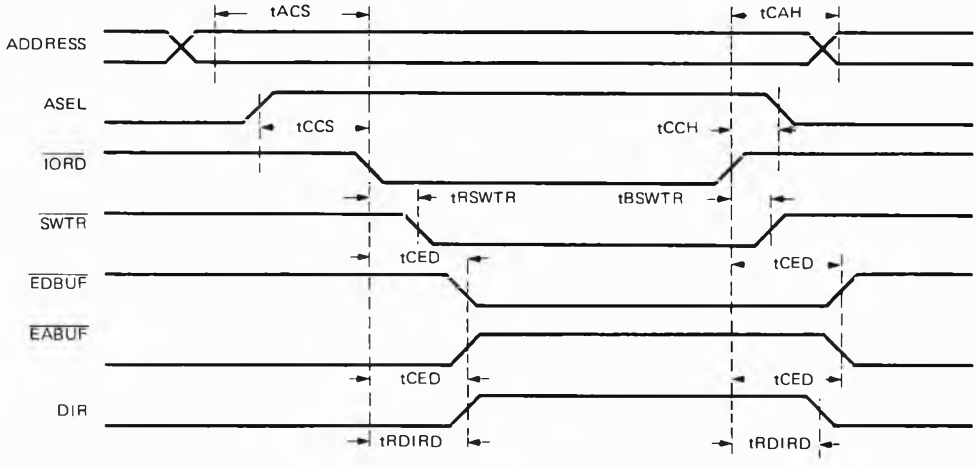


Figure 10. Switch Read Timing

Absolute Maximum Ratings *

Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Supply Voltage to Ground Potential
. . . . . −0.5V to V_{CC} +7.0V
Applied Input Voltage . . . . . −0.5V to V_{CC} +7.0V

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics: T_A = 25°C, V_{CC} = 5V ± 5%, GND = 0V

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 400 μA
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 20 mA, Note 1
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 12 mA, Note 1
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 8 mA, Note 1
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 4 mA, Note 1
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2 mA, Note 1
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	TTL
V_{IL}	Input Low Voltage	−0.5	0.8	V	TTL
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
C_{IO}	Input/Output Capacitance		16	pF	
I_{LI}	Input Leakage Current	−10	10	μA	
O_{LI}	Output Leakage Current	−10	10	μA	
I_{CC}	Operating Supply Current		80	mA	VIN = V_{CC} or GND V_{CC} = 5.25V Outputs Unloaded

Note 1: 2 mA output pads: $\overline{EABUF}$, $\overline{EDBUF}$, DIR, $\overline{CRTINT}$, $\overline{NMI}$, CPURDY, $\overline{SWTR}$, HSYNC, VSYNC, $\overline{BLANK}$, $\overline{DACR}$, $\overline{DACW}$

4 mA output pads: P7-P0, DA7-DA0, MD31-MD0.

8 mA output pads: $\overline{RAS0}$, $\overline{RAS3}$, $\overline{WE}$

12 mA output pads: $\overline{OE}$

20 mA output pads: $\overline{CAS}$