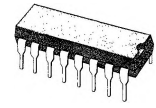
SGS-THOMSON MICROELECTRONICS

UAA4003

SWITCH MODE REGULATOR FOR DC MOTORS

- SOFT START
- DIRECT DRIVE OF THE SWITCHING TRANSISTOR (or darlington)
- SELF-REGULATED POSITIVE BASE CURRENT (peak 1.5 A)
- NEGATIVE BASE CURRENT PROVIDING FAST TURN-OFF, AND ALLOWING THE BEST USE OF THE SAFE OPERATING AREA (peak 1.5 A)
- SWITCHING TRANSISTOR PROTECTED AGAINST SATURATION FAILURE
- INSTANTANEOUS LIMITATION OF THE COLLECTOR CURRENT
- POWER SUPPLY MONITORING
- ON-CHIP THERMAL PROTECTION
- INCLUDES 2 µs MINIMUM CONDUCTING TIME (or no conduction) FOR USE OF A SNUBBER CIRCUIT

DIP-16/2
(Plastic)

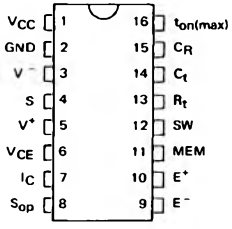


ORDER CODE : UAA4003DP

DESCRIPTION

The UAA4003 is a regulation and control device for the drive of DC motors.
Includes oscillator, PWM and error amplifier.

PIN CONNECTION



1 - Supply voltage
2 - Ground
3 - Negative supply (power stage)
4 - Power stage output
5 - Positive supply (power stage)
6 - $V_{CE(sat)}$ sensing
7 - Collector current monitoring
8 - Op. amp. output
9 - Op. amp. inverting input
10 - Op. amp. non-inverting input
11 - Memory input
12 - SW
13 - R_t resistor (oscillator)
14 - C_t capacitor (oscillator)
15 - Locked rotor
16 - Limit access

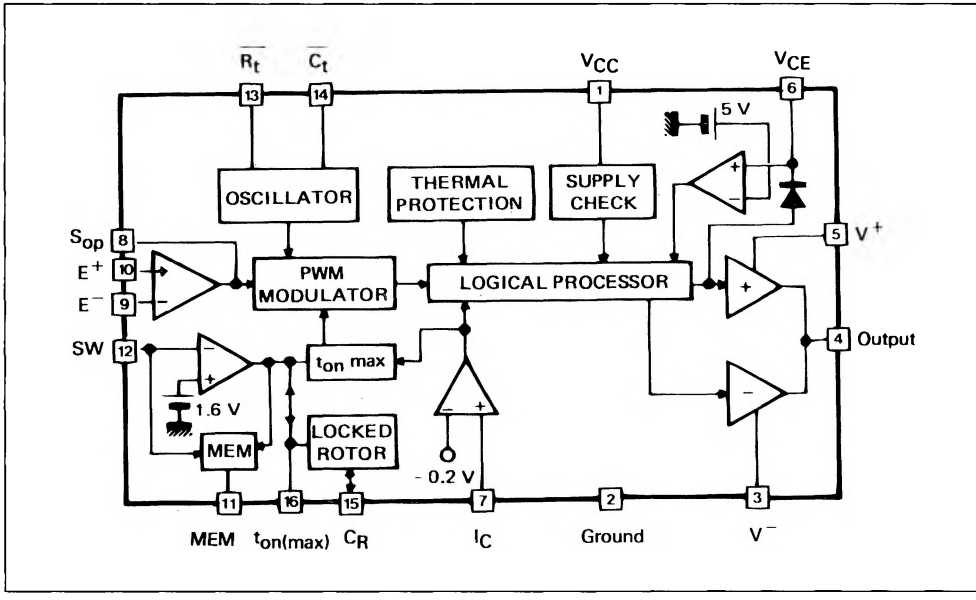
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+ 15	V
	Supply Voltages (power stage)		V
V^+	Positive	+ 15	
V^-	Negative	− 9	
$V^+ - V^-$	Voltage between Pin 5 and Pin 3	+ 18	V
I_O	Output Current	± 2	A
−	MEM Output Current	10	mA
−	Current into Input I_C (internal protection diodes)	± 5	mA
R_t	Minimum Value of Resistance R_t	10	kΩ
T_j	Junction Temperature Range	− 40 to + 150	°C
T_{stg}	Storage Temperature Range	− 40 to + 150	°C

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Maximum Junction–ambient Thermal Resistance	80	°C/W

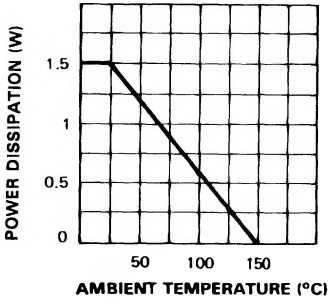
BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS T_{amb} = + 25 °C, V_{CC} = + 10 V, V^- = – 5 V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	6.2	–	14	V
I_{CC}	Supply Current (V_{CC} = + 10 V)	–	10	–	mA
V^+	Positive Supply Voltage (power stage)	4	–	14	V
V^-	Negative Supply Voltage (power stage)	0	–	– 8	V
$V_{I(th)}$	Threshold of Input I_C	– 0.260	– 0.2	– 0.140	V
–	I_C Input Current ($V_{(7)}$ = 0 V)	–	5	20	µA
A_V	Op. Amp. Open Loop Gain	60	–	–	dB
–	Op. Amp. Input Current	–	–	1	µA
–	Op. Amp. Offset Voltage	–	5	–	mV
–	Op. Amp. Common-mode Voltage	0	–	V_{CC} – 3	V
f_{osc}	Oscillator Frequency	–	$\frac{2}{R_t.C_t}$	50	kHz
R_t	Value of Resistance R_t	10	50	500	kΩ
–	Dead Time	–	5	–	µs
I_O	Output Current ($V_{(5)} - V_{(4)}$ = + 3 V)	± 1.5	–	–	A
–	Input Current into Pin 12 (SW) ($V_{(12)}$ = 0 V)	–	25	50	µA
–	MEM Output Current (open collector) ($V_{(11)}$ = + 0.3 V)	1.2	–	–	mA
–	"Locked Rotor" Time Constant (V_{CC} = + 10 V)	–	0.3	–	s/µF
–	V_{CE} Comparator Threshold Voltage	–	5	–	V
$t_{on(min)}$	Time Constant $t_{on(min)}$	–	2	–	µs

MAXIMUM POWER DISSIPATION



CIRCUIT DESCRIPTION

OSCILLATOR

It is a sawtooth generator whose fall time is much inferior to its rise time. The period is $T_{osc} = 0.5\ R_t.C_t$, R_t and C_t being tied between pins 13 and 14 respectively, and ground.

The voltage swing is about $V_{CC}/2$ and the low level is + 1.5 V.

The maximum working frequency is 50 kHz.

PULSE WIDTH MODULATOR (PWM)

A signal with a variable duty cycle is generated by a comparison between pin 14 voltage (oscillator) and pin 8 voltage (output of the error amplifier).

A second comparator limits the maximum conduction ratio by a comparison between the sawtooth and pin 16 voltage ($t_{on\ (max)}$). If $V_{(16)} = 0$, there is an internal fixed dead time (≈5 µs).

CURRENT LIMITATION

A level lower than – 0.2 V on pin 7 (I_C) involves two actions.

- A direct action through a logic processor which stops the drive until the end of the period.
- An indirect action through the $t_{on\ (max)}$ function. The change of state at the output of comparator I_C is applied to pin 16 as long as the current overload persists. By inserting capacitor C_B between pin 16 and V_{CC} (about 0.1 µF), the voltage at this point rises up by a quantity ΔV proportional to the duration and the frequency of the oversteps.

This will consequently lower the maximum conduction ratio, thus decreasing the frequency of the oversteps.

At the end of an overload state, capacitor C_B slowly charges through a 20 kΩ internal impedance, in order to return progressively to normal operation.

This capacitor also achieves a soft-start during power-up.

Note : It is possible to use direct action only provided pin 16 is tied to ground.
In this case, "locked rotor" and "memory" functions cannot be used.

LOCKED ROTOR

A voltage greater than + 1.5 V at pin 16 starts up the linear charge of a capacitor C_R connected between pin 15 and ground (3 µF/ s).

If V_{16} becomes lower than + 1.5 V again before $V_{(15)}$ reaches V_{CC}, capacitor C_R is quickly discharged.

In the fault persists, $V_{(15)}$ reaches V_{CC}, and the output is definitively cut. There are two possible ways to return to normal drive :

- Tie temporarily pin 12 (SW) to ground.
- Tie temporarily pin 15 to ground to discharge C_R.

If this function is not to be used, simply tie pin 15 to ground.

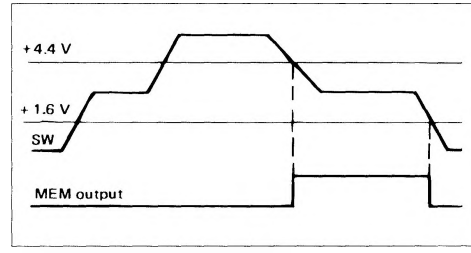
ERROR AMPLIFIER

This is an operational amplifier whose open loop gain is greater than 1000.

The input currents are lower than 1 µA, and the input offset voltage is typically 5 mV. The input common mode voltage can range from 0 V to ($V_{CC} - 3V$).

MEMORY AND INHIBITIION

Input SW (pin 12) senses a three-state logic signal. The response of the output MEM is represented here-under :



When the input signal is lower than + 1.6 V, there is an inhibition of the output drive through the $t_{on(max)}$ function. In this case the voltage on pin 16 remains close to V_{CC}.

If the input SW becomes greater than + 1.6 V, the voltage $V_{(16)}$ (between t_{on} and ground) falls. The restart is accomplished in a soft mode.

PROTECTION AGAINST DESATURATION

If, because of a too low base current or a too heavy load, voltage V_{CE} on the switching transistor rises above 4.5 V approximately, the output of comparator V_{CE} changes state, and the drive is interrupted.

POWER SUPPLY MONITORING

The drive is disabled if V_{CC} is less than + 6.2 V. Pin 3 should be connected to a voltage equal to or less than + 0.5 V.

Note that under no circumstances should this pin be left open.

THERMAL PROTECTION

This protection becomes active when the junction temperature reaches + 150 °C.

LOGIC PROCESSOR

A logic unit processes the information coming from the fault detectors, and ensures that the output signal fulfils two conditions :

- No double pulsing within a period : the occurence of a fault is memorized until the end of the period.
- To allow the discharge of a snubber network, the minimum width of the output pulse is set at 2 µs by an internal monostable. If this monostable is not triggered, there will be no conduction.

OUTPUT STAGE

ON-STATE

The positive drive achieves a very efficient drive of the switching transistor.

Its features are essentially :

- Direct drive (neither inductor nor transformer)
- The transistor stays in a quasi-saturation mode, and thus has a reduced storage time.
- The drive energy is strictly limited to the required amount.
- Easy implementation.

K_1 is closed to turn the positive stage on. The maximum value of the positive base current is set by the limitation resistor R.

Diode D maintains Q in a quasi-saturation mode : the more Q is saturated, the more diode D will shunt an important part of the drive current I_{B1}, through diode D_1.

Resistor R_B has a low value (about 1 Ω), and is used to stabilize the regulation loop.

For a good efficiency of the negative drive, the value of this resistor should be as low as possible (about 1 Ω).

Integrated Darlington T_1 is able to supply a peak current of 1.5 A with a 12 V saturation voltage.

The voltage V_{CE} on transistor Q is :
$V_{CE} = V_D + R_B I_{B1}$

OFF-STATE

The turn off is accomplished in two steps :

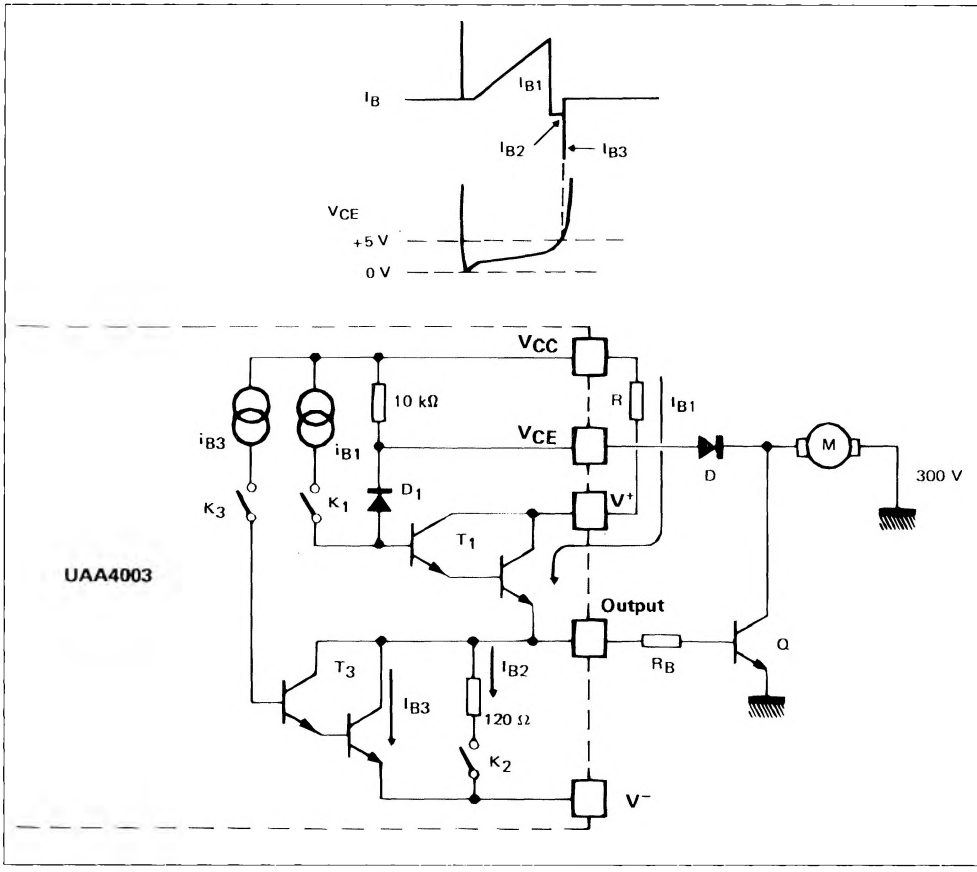
- An immediate action through K_2 which connects the base of the switching transistor to the negative supply through a 120 Ω integrated resistor (current I_{B2}).
- A delayed action through K_3 which is closed only after the desaturation of the external transistor.

This is detected by comparator V_{CE}, when collector to emitter voltage reaches 4.5 V.

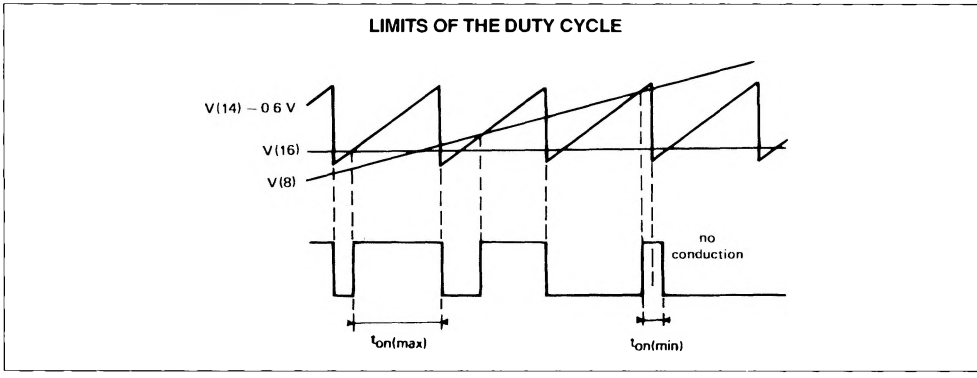
Darlington T_2 can supply 1.5 A with a 2 V saturation voltage (current I_{B3}).

NOTE : The negative drive I_{B3} for the removal of the stored charges is delayed in order to limit the slope dI_B/dt at the on-off transition. A high dI_B/dt might indeed lead to a destructive overheating of the base-collector junction (see "The power transistor in its environment" published by Thomson CSF Division Semiconducteurs Discrets).

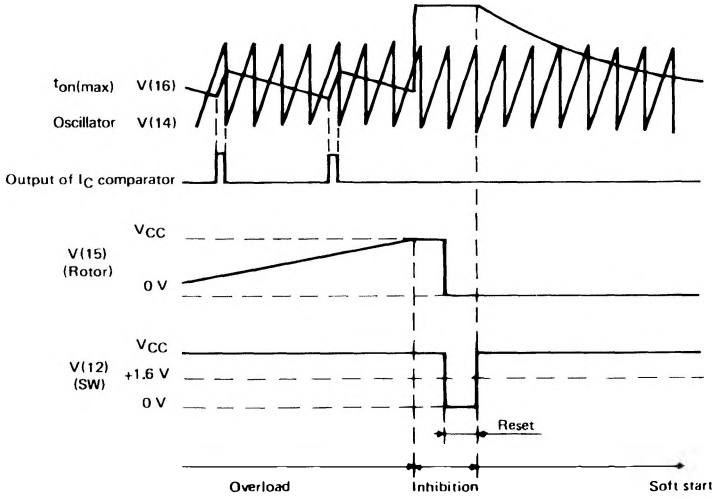
SELF REGULATED BASE CURRENT $I_B = f(V_{CE})$



TYPICAL WAVEFORMS



"CURRENT LIMITATION" AND "LOCKED ROTOR" OPERATION



SPEED REGULATOR 1.5 kW