SGS-THOMSON MICROELECTRONICS

TSGSM SERIES

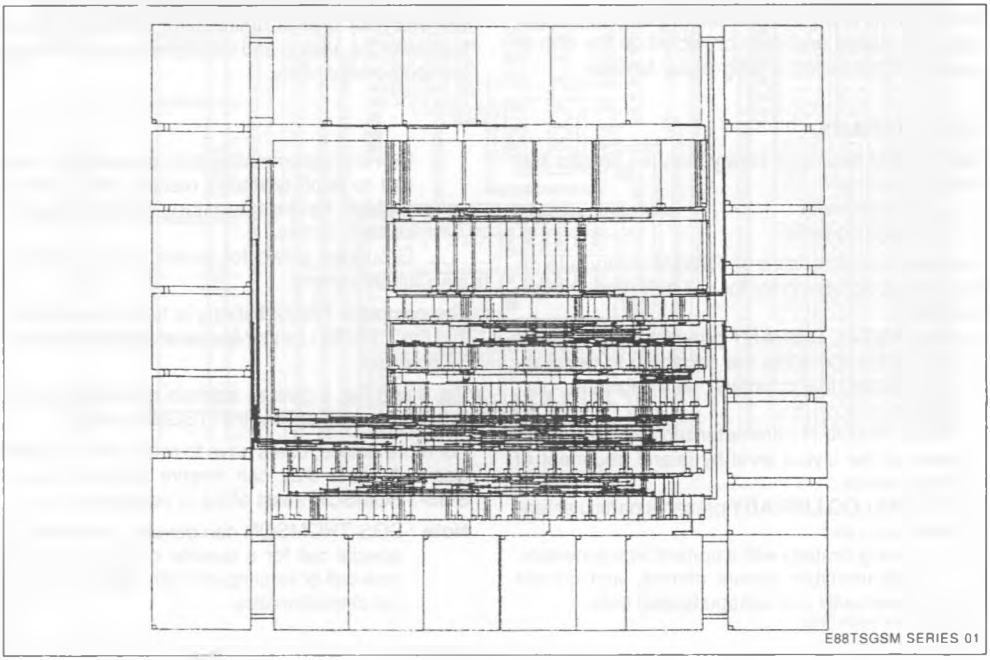
3.5µ/2 POLY / 1 METAL HCMOS MIXED ANALOG-DIGITAL STANDARD CELLS

- ADVANCED HCMOS TECHNOLOGY :
  - 3.5µ drawn channel length
  - 2 polysilicon layers
  - 1 metal layer
  - P well silicon gate CMOS process
- HIGH LATCH-UP IMMUNITY
- FULL ESD PROTECTION
- POWER SUPPLY
  Maximum ratings : - 0.5V to + 12V
  Operating conditions : 3 to 10V
- EXTENSIVE MACROCELL LIBRARY
  - 94 logic cells
  - 66 analog cells
    with programmable cells : soft macro cells, abuttable cells
- INPUT/OUTPUT CELLS
  Compatibility : TTL or CMOS levels
  Configurability : input/output/bidirectional i/o/analog I/O ...
- CAD SOFTWARE SUPPORT
  - ADS (Analog Design System)
  - Fully integrated (+ FILCAD™ for filter design)
  - Flexible design interfaces
- OPERATING TEMPERATURE RANGE
  COMMERCIAL : 0 TO + 70°C
  INDUSTRIAL : – 40 TO + 85°C
  MILITARY : – 55 TO + 125°C
- PACKAGE OPTIONS
  DIL : PLASTIC OR CERAMIC
  SMD : SO, PLCC, LCCC, QF

DESCRIPTION

The TSGSM Series, mixed analog-digital Standard Cell products from SGS-THOMSON Microelectronics, represents a major step allowing the system designer dealing with both digital and high level ana-

Figure 1 : Example of TSGSM Chip Layout.



log functions to benefit of the state of the art semi-custom circuit integration capabilities.

The large variety of predefined and precharacterized functions ranging :

- in digital from simple gates to counters, registers...
- in analog from single operational amplifier to A/D or D/A converters, switched capacitors filters ...

has been proven extremely efficient in the design of many mixed HCMOS Analog-Digital ASIC's circuits in such various applications as consumer, computer, industrial, military, telecommunications and automotive fields.

TSGSM ARCHITECTURE

TECHNOLOGY

TSGSM Series developed by SGS-THOMSON is using an advanced silicon gate P well, dual poly-silicon layer, single metal layer HCMOS technology.

The process is very well suited for the design and integration of high performance analog functions combined with digital. It achieves operating speeds up to 15MHz for the digital part of the TSGSM circuit.

Thanks to the 2 polysilicon layers, TSGSM Series can integrate high accuracy switched capacitors filters based on the same concept of TSGF Series, switched capacitor Filter Arrays (Refer to TSGF04/08/12 Data Sheet). True capacitors are realized with Poly 1 and Poly 2 layers.

CELLS

Predesigned and precharacterized Macrocells are selected, placed and interconnected on the chip to implement the mixed analog-digital function.

Digital and Analog Macrocells have different height, as shown on the chip layout of fig. 1. In addition some cells like A/D or D/A converters are designed as fixed blocks.

CHIP TOPOLOGY

The inputs and outputs of cells are interconnected by using 2 conductive layers : polysilicon and metal.

The chip layout is composed of cell rows, whose number is determined to optimize the die size, and of horizontal routing channels.

Peripheral cells surround the internal active chip area in order to interface it with its external environment.

Despite the row base architecture complex block functions can be placed and routed on the chip.

Generally for design optimization purpose, power busses of the analog and the digital parts of the chip are routed separately.

CELL LIBRARY

The TSGSM Macrocell library features around 160 different macros :

- 94 digital cells.
- 66 analog cells.

The main characteristics of TSGSM library is to offer users a high flexibility for cell definition and generation :

- The **DIGITAL LIBRARY** provides in addition of existing hard macros the capability to generate soft macros like counters, shift registers, dividers...
  These modulo N parameterized cells are generated at the layout level by lateral abutment of hard macros.
- The **ANALOG LIBRARY** presents particular features such as :
  - Biasing strategy with a current bias generator, programmable current mirrors, and current biased cells and voltage biased cells.
  - Use of programmable cells for capacitor fields (0.1 to 30pF typically), resistor fields (150 to 1.8MΩ), bipolar transistors, MOS transistors, current mirrors.
  - Grounded shield for power supply rejection improvement.

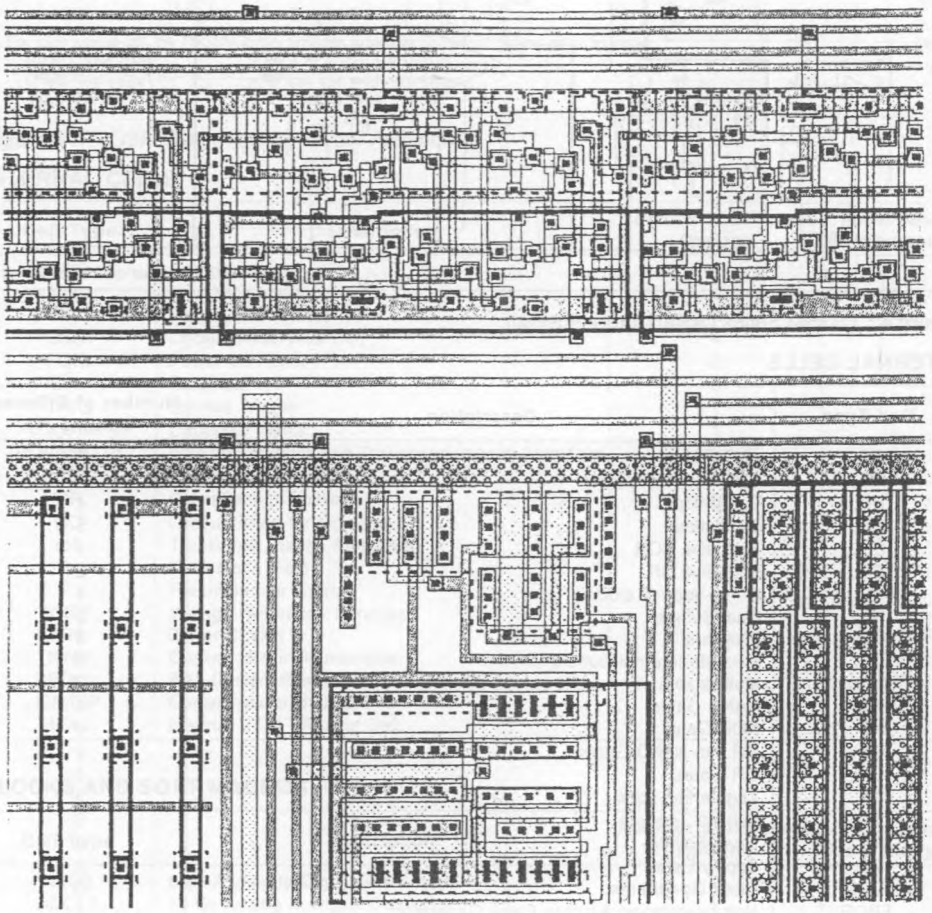
The complete TSGSM library is fully described within the TSGSM User's Manual of the SGS-THOMSON library.

Fig. 4 and Fig. 5 give an abstract of all available digital and analog cells within TSGSM' library.

For more details, users have to refer to the TSGSM User's Manual they can require to their nearest SGS-THOMSON sales office or representative.

Note : SGS-THOMSON can develop on request a special cell for a specific customer circuit : new cell or existing cell with different electrical characteristics.

Figure 2 : Example of Interconnection between Analog and Digital Cells.



E88TSGSM-SERIES-02

Figure 3 : Example of a Mixed Analog-Digital Function.

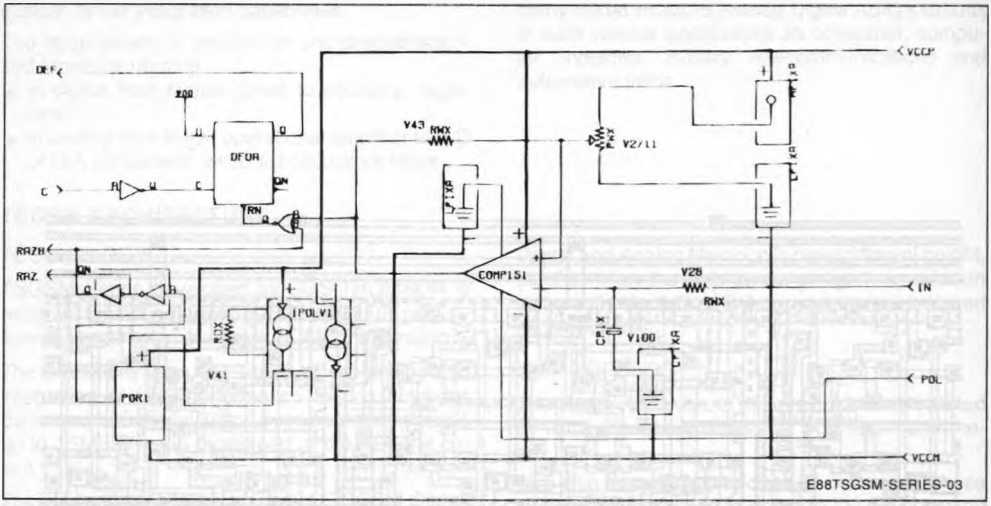


Figure 4 : TSGSM Series Digital Library Abstract.

INTERNAL CELLS

Cell Type	Description	Number of Different Options (1)
AA..	AND Gates	3
AN..	AND into NOR Gates	4
DF..	D Flip-flops	4
DL..	D Latches	5
EN..	Exclusive NOR	1
EO..	Exclusive OR	2
FF..	D Flip-flops (2 clocks)	4
II..	Dual Buffers	2
IN..	Inverters	5
IT..	Tri-state Internal Buffers	3
MU..	Multiplexers	3
NA..	NAND Gates	4
NO..	NOR Gates	4
ON..	OR into NAND Gates	2
OR..	OR Gates	3
TF..	Toggle Flip-flops	3
TG..	Schmitt Triggers	3
TT..	Level Shifters	3
ZZ..	Supply Cells	2
CCG	Clock Generators	3
FPCG	Non-overlapping 4-phase Clock Generator	1
TPCG	Non-overlapping 2-phase Clock Generator	1
INVL	Delay Inverter	1

(1) For each type of cell, the TSGSM library provides extensive number of options as for example

- NAND type cells : 2, 3, 4 or 6 input NAND s
- D flip-flop cells : with low set, with low reset .
- input buffers : TTL, CMOS, with pull-up.

Figure 4 (continued).

I/O CELLS

Cell Type	Description	Number of Different Options (1)
OB.	Output Buffers	4
PP..	Power Pads	3
OB..	Tri-state Output Buffers	4
IB..	Input Buffers	8
IO..	Bidirectional Buffers	5
OB..	Open-drain Output Buffers	4

(1) For each type of cell, the TSGSM library provides extensive number of options as for example :
- NAND type cells : 2, 3, 4 or 6 input NAND's
- D flip-flop cells : with low set, with low reset.
- input buffers : TTL, CMOS, with pull-up.

Figure 5 : TSGSM Series Analog Library Abstract.

INTERNAL CELLS

Cell Type	Description	Number of Different Options	Metal Mask Programmable
COMP.	Comparators	6	
MN...	N MOS Transistors	4	x
MP...	P MOS Transistors	4	x
OSC..	Oscillators (crystal RC)	4	
POR.	Power on Reset	2	
SW.	Switches	3	
TRIG	Schmitt Trigger	1	
CP..	Capacitor Fields	1	x
BOPA/BOTA	Bias for Op amps and Transconductance Amplifiers	3	
BIP	Bipolar Transistors	1	x
OP	Operational Amplifiers	5	
OO	Output Stage for Op Amp	1	
OT	Transconductance Amplifiers	2	
R..	Resistance Fields	3	x
P..	Potentiometer Fields	3	x
VREF	Voltage Reference Bandgap	1	
ZEN.	Zener Diodes	3	
IPNV	Current Mirror Source-sink	1	x
IPOL..	Bias Current Generator	2	x
ISN/ISP	Current Mirror Source/sink	4	x
HF/LF	Internal V^+/V^- Analog Cell	2	

BLOCKS AND SOFT MACROS

Cell Type	Description	Number of Different Options	Metal Mask Programmable
ADC8	8 Bit Analog to Digital Converters	2	
ADC12	12 Bit Analog to Digital Converter	1	
DAC8	8 Bit Digital to Analog Converter	1	
DBP/DS1	LCD Drivers	3	
SCF	Biquadratic 2nd Order Filter	1	x
VRLCD	LCD Voltage Reference	1	

ADS ANALOG DESIGN SYSTEM

The SGS-THOMSON TSGSM Series is fully supported by a complete Computer Aided Design (CAD) system. The SGS-THOMSON CAD system, ADS, is complete in that once a design is entered all the tools necessary to complete that design are available to the user in this one system.

These tools include schematic capture, logic and analog simulations, fault simulation, automatic place and route, parasitic delay extraction and test pattern generation.

ADS ANALOG DESIGN SYSTEM is available on DEC™ VAX™ computer systems.

In addition, the TSGSM library is implemented on CAE workstations :
- Mentor™
- Daisy™.

SGS-THOMSON developped direct interfaces between these CAE workstations and its ADS system.

The ADS package allows the development of analog and digital standard cell circuits so easily that each system designer can handle it.

The development of mixed analog and digital circuit is done with advanced concepts such as :
- parameterized cells (resistors, capacitors, current generators ...)
- metal mask programmable cells (switched capacitor filters ...)
- compiled cells (bit slice concept for digital functions like counters, dividers ...).

The main CAD tools available within ADS are :

■ SCHEMATIC GRAPHIC CAPTURE

SDS™ provides graphic capture of schematic circuit diagram. Designer can create blocks by using the 100% hierarchy of SDS™ and also can specify values of parameterized cells.

After the net list generation, the modules generated under SDS™ are oriented automatically thru logic or analog simulation.

■ LOGIC SIMULATION

HILO3™, hierarchical logic simulator, allows design verification and timing analysis of the circuit. A pre-layout timing analysis is run with calculated delays based on fanout, VDD, temperature and best, typical or worst case process conditions.

The 2 input files to HILO3™ are the net list generated from graphic capture and the input test pattern description.

HILO3™ simulator allows mixed analog and digital simulation for analog cells having an equivalent model described under HILO3™.

■ ANALOG SIMULATION

H3SPICE electrical simulator allows pre-layout or post-layout timing analysis of the analog blocks of the circuit.

H3SPICE input files are the net list and the input test pattern descriptions.

With the improvements brought by SGS-THOMSON to H3SPICE, the analog simulator becomes a powerful CAD tool :
- special level modelling for speed improvement on digital sub-circuits,
- fast execution on full analog part of TSGSM circuit, thanks to macro modelling, allows simulation of large analog blocks.

■ PLACEMENT AND ROUTING

CALMP™ software is an efficient standard cell automatic place and route whose main features are :
- use of different heights of cells on the chip
- interactive pre-placement of blocks, cells and I/O's for die size optimization
- capability to force priorities on nets for critical path routing
- capability to generate soft macros, blocks by cell abutment.

A check program performs at the end of the layout, design rule checking and verifies conformity of the graphic data base versus the schematics data base.

■ PARASITIC DELAY EXTRACTION

ADS is computing the exact parasitic delays brought by the placement and routing. Delays are based both on resistance and capacitance of each interconnect.

As soon as the parasitic RC delays are extracted, user can run a post layout simulation for accurate timing new analysis.

■ TEST GENERATION

According to the input test patterns already described, user can determinate the testability coverage ratio of its digital test sequence thanks to the fault simulator which is incorporated within HILO3™.

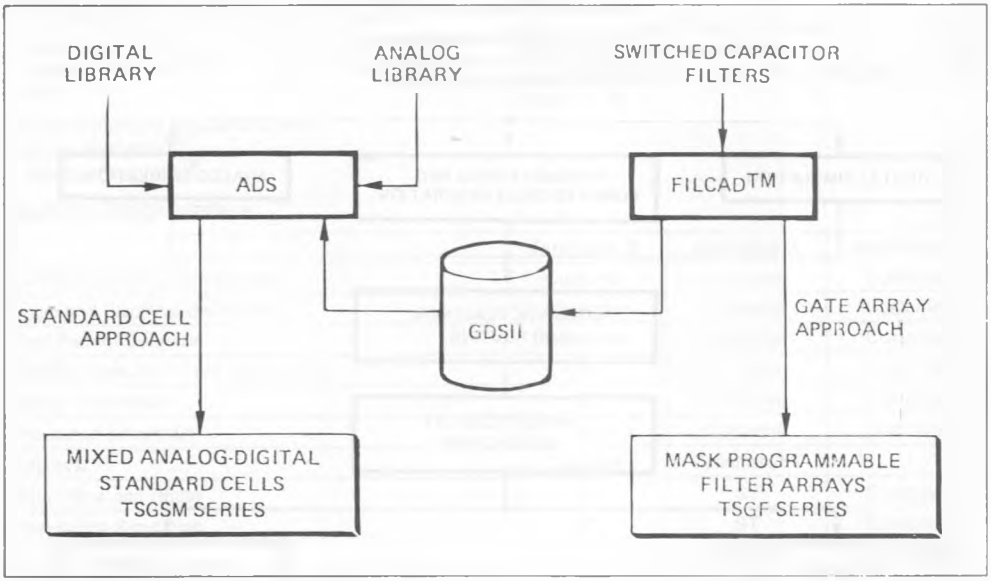
Depending of the fault simulator results user can generate new input test patterns in order to improve testability coverage.

ADS software converts automatically the post layout simulation (with parasitic delays) file into test patterns directly compatible with SGS-THOMSON test equipments.

At same time static and dynamic parameters are added to the functional test pattern file : all input/output levels are tested during the functional test sequence.

Fig. 6 outlines the SGS-THOMSON approach for the design of analog or mixed analog/digital circuits.

Figure 6 : SGS-THOMSON CAD Tools and Product for Analog and Mixed Analog-Digital Circuits.



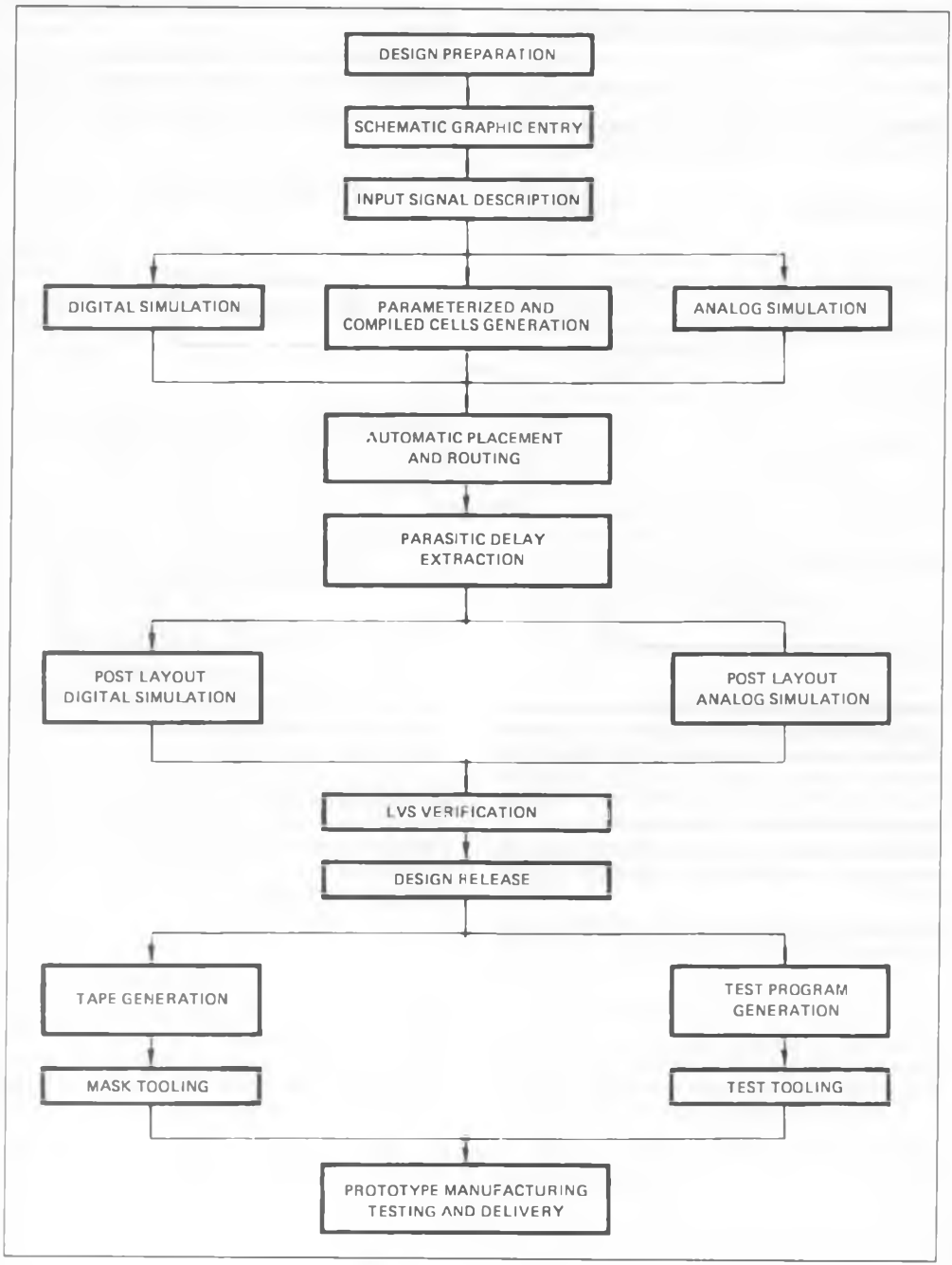
One of the particularities of TSGSM series is to provide switched capacitor filter integration capabilities. The filter cells available within TSGSM library are identical to those used on the SGS-THOMSON Analog Filter Arrays, TSGF Series, which are mask programmable switched capacitor filters.

For filter synthesis, simulation and layout, designers are given an efficient Filter CAD design tool : FILCAD™.

For more informations about SGS-THOMSON switched capacitor filter design solutions and CAD tools, please refer to TSGF04/08/12, 4th to 12th order switched capacitor filter arrays data sheet.

Fig. 7 shows the development phases of a TSGSM Series standard cell. The design translation phase up to the prelayout simulation can be done either on CAE workstations like Daisy Systems™ and Mentor Graphics™, or on VAX™ computer with ADS Analog Design System.

Figure 7 : TSGSM Series Development Flow.



CUSTOMER DESIGN INTERFACE

SGS-THOMSON has developed several interfaces for customers giving them easy and flexible design approaches for TSGSM 3.5µ/2 poly/1 metal HCMOS mixed Analog Digital Standard Cells series.

User can access ADS Analog Design System.
- via the SGS-THOMSON Design Centers.
- via connection to SGS-THOMSON CAD Center,
- via the SGS-THOMSON associated Design Centers.

CAE workstations capabilities are :
- Daisy Systems™.
- Mentor Graphics™.

In that case direct interfaces will be offered to user in order to make design implementation and test generation with ADS.

According to all of these design possibilities, SGS-THOMSON defined 3 main customer design interfaces.

Figure 8 outlines these interfaces. Each interface delineates the responsibilities of customer and SGS-THOMSON during circuit development flow shown in fig. 7.

Figure 8 : Design Interface.

	Interface 2	Interface 3	Interface 4
Definition of Circuit Specification	Customer	Customer	Customer
Logic and Electrical Description	Customer	Customer	Customer
Test Pattern Definition	Customer	Customer	Customer
Graphic Capture + Input Signal Entry	ST	Customer	Customer
Design Verification	ST	Customer	Customer
Pre-layout Simulation	ST	Customer	Customer
Approval	Customer	Customer/ST	
Auto Place and Route	ST	ST	Customer
Post-layout Simulation	ST	ST	Customer
Design Release	Customer	Customer/ST	Customer/ST
Test Program Generation - Test Tooling	ST	ST	ST
Mask Tooling	ST	ST	ST
Prototype Manufacturing and Testing	ST	ST	ST
Prototype Delivery	ST	ST	ST

With interface 3, design can be done either at SGS-THOMSON Microelectronics Design Center facilities or at customer location.

ABSOLUTE MAXIMUM RATINGS (note 1) T_{amb} = 25°C, voltage referenced to V_{SS}.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage	− 0.5	12.0	V
V_I, V_O	I/O Voltage	− 0.5	V_{DD} + 0.5	V
I_I, I_O	I/O Current	− 40	+ 40	mA
T_{stg}	Storage Temperature (ceramic)	− 65	+ 150	°C
	Storage Temperature (plastic)	− 40	+ 125	°C

Note : 1. Stresses above those listed order "maximum rating" may cause permanent damage to the device. This is a stress rating only and functional operation to the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS Voltage referred to V_{SS}

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Operating Supply Voltage	4.5 9.0	5.0 10.0	5.5 11.0	V
V_{DD}	Extended Supply Voltage (note 2)	3		12.0	V
T_{amb}	Operating Ambient Temperature Military Industrial Commercial	 – 55 – 40 0		 + 125 + 85 + 70	°C

Note : 2. For extended supply voltage please consult SGS-THOMSON Microelectronics.

DC GENERAL ELECTRICAL CHARACTERISTICS V_{DD} = 5V ± 10% or V_{DD} = 10V ± 10% (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High Level TTL Input Voltage	V_{DD} = 5V ± 10% T° = 0°C/= 70°C T° = – 40°C/+ 85°C T° = – 55°C/+125°C	 2.0 2.25 2.25			V
V_{IL}	Low Level TTL Input Voltage	V_{DD} = 5V ± 10% All Temp. Ranges			0.8	V
V_{IH} V_{IL}	High Level CMOS Input Voltage Low Level CMOS Input Voltage		70% V_{DD}		 30% V_{DD}	V
I_{OZH}	Tristate Output Leakage Current	V_O = V_{DD} T° = 0°C/+ 70°C T° = – 40°C/+ 85°C T° = – 55°C/+ 125°C			2.5 5 10	µA
I_{OZL}		V_O = V_{SS} T° = 0°C/+ 70°C T° = – 40°C/+ 85°C T° = 55°C/+ 125°C	 – 2.5 – 5.0 – 10.0			µA
I_{IH}	High Level Input Leakage Current	V_I = V_{DD} T° = 0°C/+ 70°C T° = – 40°C/+ 85°C T° = – 55°C/+ 125°C			 1.0 3.0 5.0	µA
I_{IL}	Low Level Input Leakage Current	V_I = V_{SS} T° = 0°C/+ 70°C T° = – 40°C/+ 85°C T° = – 55°C/+ 125°C	 – 1.0 – 3.0 – 5.0			µA
I_{CC}	Max Admissible Current per Pin : – Analog – Digital				 ± 20 + 40	mA

DIGITAL LIBRARY AC ELECTRICAL CHARACTERISTICS ABSTRACT V_{DD} = 10V ± 10%, $T_{amb.}$ = 25°C, Typical Process Standard Condition = 2 Loads + 1mm of Metal Interconnect

Cell Code	Description	V_{DD} = 10V ± 10%			Unit
		T_{PHL}	T_{PLH}	Other	
IN01	Standard Inverter	5.7	4.7		ns
NA02	2-input NAND	6.2	5.8		ns
NO02	2-input NOR	6.4	5.1		ns
DF08	Positive Edge D Flip-Flop from CKL to Q : T_{SH} T_H T_{WH} T_{WL}	10.6	6.1	 14.0 5.0 20.0 16.0	ns
OB2	TTL Inverting Output Buffer Capacitance Load = 50pF = 25pF = 15pF	 4.1 3.6 3.4	 5.0 4.3 4.0		ns
T02	Tri-state TTL Output Buffer Capacitance Load = 50pF = 25pF = 15pF	 4.1 3.6 3.4	 5.0 4.3 4.0		ns
IB021	CMOS Inverting Input Buffer	7.4	8.7		ns

Note : Refer to TSGSM User's Manual for more detailed informations.

ANALOG LIBRARY AC ELECTRICAL CHARACTERISTICS ABSTRACT V_{DD} = 10V ± 10%, unless otherwise specified T = 25°C, typical process.

Cell Code	Description	Parameter/conditions	Min.	Typ.	Max.	Unit
COMP	Static Comparator	Propagation Delay (overdrive = 10mV) Offset		1 ± 5	2 ± 15	µs mV
CP1X	Capacitor Fields	Unit Capacitance Capacitor Value Range Absolute Accuracy Matching (capacitor ratio)	0.08 0.1	0.1 0.5	0.12 50 ± 15 1.0	pF pF % %
	Resistors					
RPX/PPX	. Polysilicon	Resistor Value Range Absolute Accuracy Matching Temperature Coefficient	.15		20 ± 20 ± 1 0.15	kΩ % % %/°C
RDX/PDX	. P^+ Diffusion	Resistor Value Range Absolute Accuracy Matching Temperature Coefficient	.75		100 ± 20 ± 1 0.15	kΩ % % %/°C
RWX/PWX	. P^- Well	Resistor Value Range Absolute Accuracy Matching Temperature Coefficient Voltage Coefficient	5		2000 ± 20 ± 2 ± 1 5	kΩ % % %/°C %/V
	Switches					Ω
SWIX	. Analog Switch	R_{ON} Value Range		10k	30k	
MN1X/MP1X	. MOS Switch	R_{ON} Value Range	50		500	
IPOLxx + ISyy	Programmable Reference Current Generator	Current Current Step Supply Voltage Rejection (4V < V_{DD} < 10V)	1	 1 + 2	250	µA µA %/V
OPA2	General Purpose Operational Amplifier	Phase Margin Unit Gain Bandwidth (C_L = 100pF, R_L = 10kΩ) Offset		80 3.3 ± 5	 ± 10	deg MHz mV
OTA1	Transconductance Amplifier	Unit Gain Bandwidth (C_L = 3.5pF)	7	10.5		MHz
POR1	Static Power on Reset	Active Voltage (V_{DD} = 10V) (V_{DD} = 5V)		4.5 3.5		V V
VREF	Voltage Bandgap Reference	Output Voltage	1.15	1.18	1.20	V
ZENx	Zener Diode	Zener Voltage (bias current = 50µA)	5.3	5.6	5.9	V
OSC11	Crystal Oscillator	Frequency	0.1		12	MHz
OSC31	RC Timer	Frequency Stability Versus Temperature Stability Versus Supply Voltage		100 0.02 0.5	500	kHz %/°C %/V
ADC8Bx	8 Bits Analog to Digital Converter	Conversion Time Integral non Linearity			25 ± 0.5	µs LSB
ADC12B	12 Bits Analog to Digital Converter	Conversion Time Differential non Linearity			25 ± 0.7	µs LSB
SCFx	Biquadratic Filter Cell	Signal Frequency Order	 2		30 12	kHz

Note : Refer to TSGSM User's Manual for more detailed informations.

PACKAGING

SGS-THOMSON has a wide variety of package options available to the user :

- Dual in line packages (DIP)
  - Plastic
  - Cerdip
  - Side Braze
- Chip carriers
  - Plastic Leaded Chip Carriers (PLCC)
  - Ceramic Leadless Chip Carriers (CLCC)
  - Ceramic Leaded Chip Carriers (LDCC)
- Small outlines (SO)

Where different packaging requirements are needed, contact SGS-THOMSON Marketing. SGS-THOMSON Microelectronics can also supply standard cells products in dice form (chip tray or wafer form).

ORDER CODES

TS GSM 235 A V FN D

SGS-THOMSON

3.5µ /2 POLY/1 METAL MIXED ANALOG-DIGITAL STANDARD CELLS

CUSTOMER SPECIFICATION NUMBER

RELEASE LETTER

QUALITY LEVEL

-	Standard
D	Burn-in
B	MIL STD 883 Class B
G	NFC 96883 Class G

PACKAGE

P	Plastic DIP
J	Cerdip
E	CLCC
FN	PLCC
R	CPGA
C	Ceramic
FP	SO

TEMPERATURE RANGE

C	0 °C/+ 70 °C
I	- 25 °C/+ 85 °C
M	- 55 °C/+ 125 °C
T	- 40 °C/+ 105 °C
V	- 40 °C/+ 85 °C