SGS-THOMSON MICROELECTRONICS

TSGF SERIES

MASK PROGRAMMABLE FILTERS
ANALOG SWITCHED CAPACITOR FILTER ARRAYS

- HCMOS MASK PROGRAMMABLE SWITCHED CAPACITOR FILTERS : FAST DESIGN TURN-AROUND TIME (5 to 6 weeks average), THANKS TO GATE ARRAY APPROACH
- INTEGRATION OF ANY KIND OF CLASSIC, NON-CLASSIC FILTERS : BANDPASS, LOW-PASS, HIGHPASS, BAND REJECT...
- CAUER, CHEBYCHEV, BUTTERWORTH, LEGENDRE...
- FILTER ORDER : FROM 2ND TO 12TH
- CASCADABLE STRUCTURE : HIGHER ORDER ACHIEVABLE
- NO EXTERNAL COMPONENTS REQUIRED TO REALIZE THE FILTERING FUNCTION
- ADDITIONAL OPTIONS AVAILABLE ON CHIP :
  - UNCOMMITED OP-AMPS (for anti-aliasing and/or smoothing filters, half or full wave rectifiers...) ;
  - INTERNAL DIVIDER (sampling frequency generated from external clock) ;
  - OUTPUT SAMPLE-AND-HOLD
- TSGF SERIES PROVIDES :
  - LEAPFROG STRUCTURE FOR VERY LOW SENSITIVITY FILTERS ;
  - CASCADABLE BIQUADRATIC CELLS FOR NON-CLASSIC FILTER DESIGN
- TSGF SERIES FULLY SUPPORTED BY "FILCAD"® CAD SOFTWARE FROM FILTER SYNTHESIS AND SIMULATION UP TO LAYOUT
  - APPLICATION NOTES
  - EVALUATION BOARDS
  - INPUT SIGNAL FREQUENCY : 0 TO 30KHz
  - SIGNAL TO NOISE RATIO : 60 TO 85dB
- POWER SUPPLY : DUAL ± 5V
  SINGLE 0 - 10V
  SINGLE 0 - 5V
- ADJUSTABLE POWER CONSUMPTION : 0.5mW TO 20mW PER FILTER ORDER
- QUALITY FACTOR : UP TO 50
- PASS-BAND GAIN : UP TO 40dB
- INPUT SENSITIVITY : 1mVRMS (min)

DESCRIPTION

TSGF series is a family of Mask Programmable Filters (MPFs) developed by SGS-THOMSON Microelectronics.

The TSGF product range is composed of 3 switched capacitor filter base arrays, TSGF04, TSGF08 and TSGF12 providing filter integration capability from 2nd to 12th order.

TSGF04/08/12 are using "gate array" technique : the filter customization is achieved only by the final metallization mask.

Therefore TSGF series provide users with filter integration solutions with very fast design turn-around time : 5 to 6 weeks up to delivery of full tested prototypes.

TSGF04/08/12 base arrays provide on chip all necessary functions to realize all kind of filters :

- transconductance amplifiers
- switches
- capacitor fields
- sample-and-hold
- non overlapping phase generator

Additional on-chip integration capabilities are offered by TSGF products such as :

- prefiltering and post filtering functions antialiasing and smoothing filters)
- cosine filter
- output sample-and-hold driving
- power consumption adjustment
- output DC level adjustment.

TSGF series provide users a fast and complete design solution for their specific filter circuits resulting in highly accurate and reliable products thanks to switched capacitor technique.

But SGS-THOMSON filtering approach is not only limited to the Mask Programmable Filter (MPF) products.

TSGF SERIES PRODUCT RANGE

Part Number	Number of on-chips Filters	Filter Order	Uncommitted Op-amps	Clock	Output Sample-and Hold	Packages
TSGF04	1	2 to 4	1	Internal Oscillator* TTL/CMOS Levels	External* Driving	PDIP 8-14 Pins CDIP 14 Pins SO Wide 16 Pins
TSGF08	1	4 to 8	2	1 Clock Input TTL/CMOS Levels	Internal Driving	PDIP 8-16 Pins CDIP 16 Pins SO Wide 16 Pins
TSGF12	1 or 2	8 to 12	2	2 Clock Inputs TTL/CMOS Levels	External* Driving	PDIP 16-18-20 Pins CDIP 16-18-20 Pins SO Wide 18-24 Pins

* Optional.

Users are given :

- Standard Device Filters which are general purpose filters designed by SGS-THOMSON from the 3 TSGF base arrays.
  - TSG 87xx developed on TSGF04 filter array (2nd to 4th order)
  - TSG 85xx developed on TSGF08 filter array (4th to 8th order)
  - TSG 86xx developed on TSGF12 filter array (8th to 12th order).

Refer to data sheets of these standard filter products.

- "Gate Array" Filters which are the TSGF04, TSGF08, TSGF12 filter arrays described in this data sheet.
- "Standard Cell" Filters described in the TSGSM Series Data Sheet.

By offering TSGF-like macrocells in its library, the mixed analog/digital TSGSM Standard Cell family also provides filtering capabilities and then can extend integration possibilities offered by TSGF series.

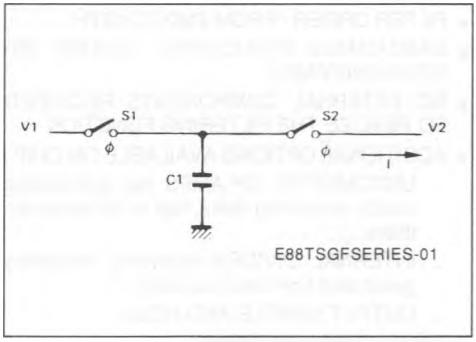
For example higher than 12th order filters or circuit combining filters with digital and analog functions on the same chip are achievable with TSGSM Standard Cells.

SWITCHED CAPACITOR TECHNIQUE

SGS-THOMSON TSGF products are active filters where resistors are replaced by capacitors which are switched at a frequency, named sampling frequency (F_i).

Figure 1 is showing the basic principle of switched capacitor technique.

Figure 1.



The 2 switches (S1 and S2) are controlled by 2 complementary and non overlapping clock phases.

During the phase $\varnothing = 1$ (S1 on, S2 off) the charge stored in C1 is :

$Q1 = C1.V1$ (1)

During the phase $\overline{\varnothing} = 1$ (S1 off, S2 on) the charge stored in C1 becomes :

$Q2 = C1.V2$ (2)

During a complete clock period $Ti = \frac{1}{Fi} = \varnothing + \overline{\varnothing}$

the transferred charge is :

$\Delta Q = Q1 - Q2 = C1\ (V1 - V2)$ (3)

During this Ti period, this charge flow is equivalent to a current, I :

$\Delta Q = C1\ (V1 - V2) = I.Ti$ (4)

$$I = C1.Fi\,(V1 - V2) = \frac{C1\,(V1 - V2)}{T_i} \quad (5)$$

Comparing (5) with Ohm's law applied to a resistance :

$$I = \frac{V1 - V2}{R} \quad (6)$$

The equivalent resistor is then :

$$Req = \frac{T_i}{C1} \quad (7)$$

Then, with (7), a RC product becomes :

$$Req.\,C = \frac{C}{C1}\,T_i \quad (8)$$

SWITCHED CAPACITOR FILTER BENEFITS

In active filters, the time constant is fixed by the RC product but the component values R and C used with the Op-amp are absolutely uncorrelated : so trimmings, tunings are very often needed to obtain an accurate template. On the other hand, with switched capacitor networks, only capacitor ratios are used. These ratios are obtained with capacitors integrated on the same chip. The available accuracy is 0.1% to 0.5% whatever the temperature condition may be.

As the time constant is fixed by capacitor ratio, fully integrated filters are achievable without trimming. In addition, as shown in (8) the time constant RC is proportional to the sampling period Ti : the filter cutoff frequency can be shifted by tuning the sampling clock frequency without any change on the shape of response curves.

SWITCHED CAPACITOR FILTER FEATURES

Key Points	Results
• Monolithic Filter. • The coefficients of the filter transfer function are completely determined by : – a single crystal controlled clock frequency – and ratioed capacitors • Fully HCMOS Integrated Filters • Switched capacitor filters are sampled-and-hold circuits.	• Board Size Reduction. • High Accuracy Template. • Stability in Temperature and Time. • High Order Filter Achievable. • No Adjustment. • Clock Tunable Cutoff Frequency. • Low Power. • No External Components. • Ease and Safety of Use. • Antialiasing prefiltering is required if the input signal is wide band. • Smoothing post filtering may be used to avoid spectral rays around the sampling frequency.

SWITCHED CAPACITOR FILTER ARRAY ARCHITECTURE

Analog switched capacitor filter arrays, TSGF series, are processed with a 3.5/2 polysilicon layer/1 metal layer HCMOS process.

SGS-THOMSON offers 3 filter base arrays, TSGF04, TSGF08 and TSGF12, providing filtering capabilities from 2nd to 12th order.

The 3 arrays are designed around a "Universal biquadratic filter cell", SGS-THOMSON patented. This cell consists of 2 adder integrators using a transconductance amplifier, switches, and capacitor fields. Fields of capacitors are composed of hundred unit capacitors (0.1pF) and then provide high and accurate capacitor values.

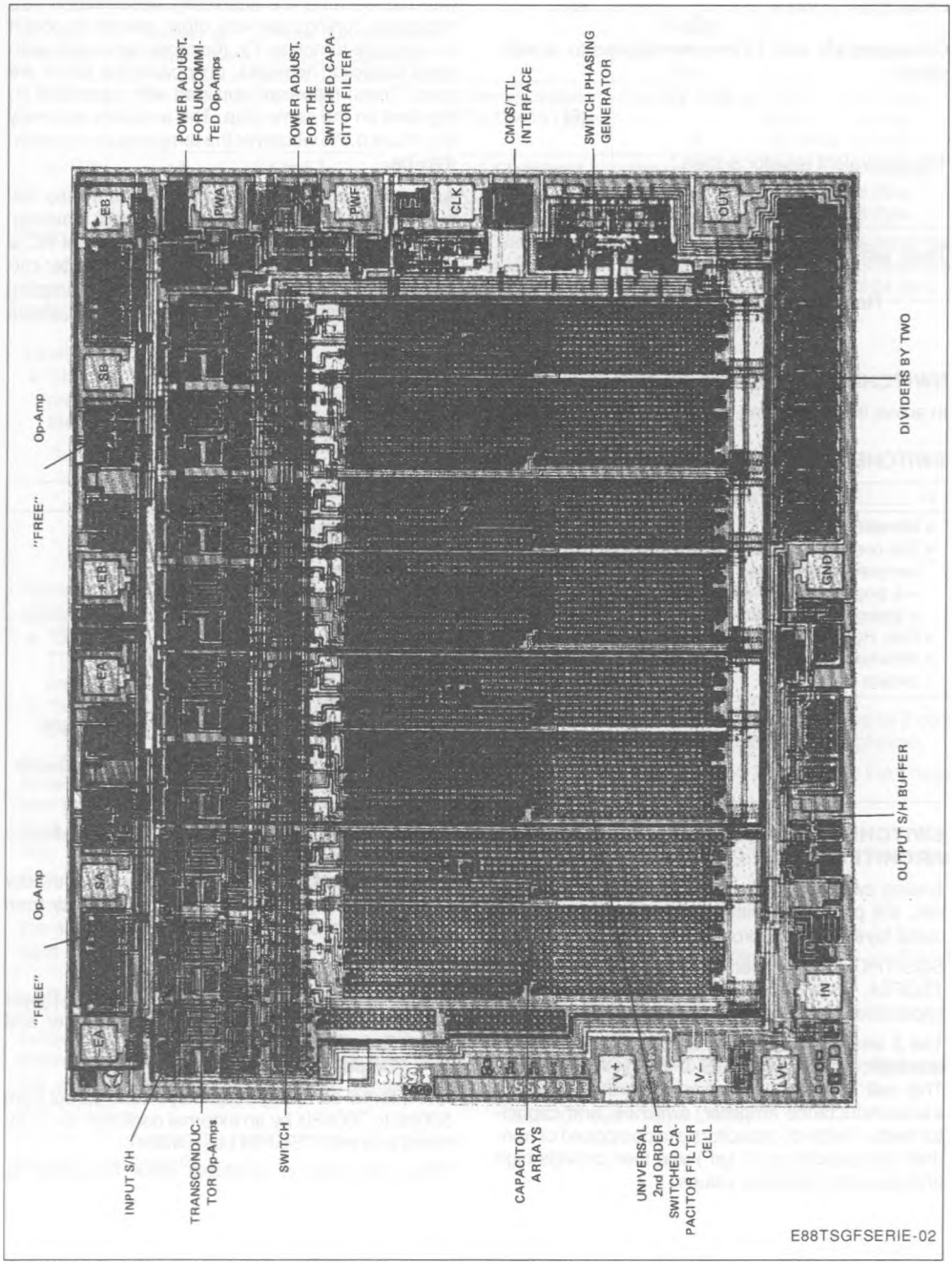
Figure 2 shows the TSGF08 chips, outlining all functions available on TSGF filter arrays :

- Universal 2nd order Filter Cell. Clock divider generating internal sampling frequency from external clock.
- Non overlapping phase generator.
- Input Sample-and-Hold.
- Uncommitted free Op-amps. Power consumption Adjustment cells for filter and Op-amps.
- Output Sample-and-Hold.

The internal sampling frequency Fi can be set from 500Hz to 700KHz by an external oscillator (or an internal one with TSGF04 base wafer).

When the external available clock frequency is

Figure 2 : TSGF08 CHIP.



higher than 700KHz, the set of Mask Programmable dividers by 2 is used to adapt the external clock frequency to the sampling frequency. In any case the external clock frequency must be lower than 5MHz.

As the ratio Fi/Fc between sampling frequency Fi and selected filter frequency Fc is a constant, designers can move the filter characteristics (central or cut-off frequency) only by tuning the clock.

A 10V power supply, either 0V and 10V, or - 5V and + 5V, gives the best performances : maximum output swing of 8V. The TSGF filters can also operate with a standard 0/5V power supply. In that case the maximum output swing is 2.2V.

Typical power consumption is 0.5mA per filter order. This power consumption is user adjustable between 0.1mA and 2mA with an external resistor, depending on the frequency range.

The power consumption adjustment is also provided to the uncommitted operational amplifiers : the bias current must be increased when a high gain - bandwidth product is required.

These uncommitted Op-amps give the designer the capability to create auxiliary circuits like voltage gain, prefiltering and post filtering functions half or full wave rectifier functions, or local oscillator (refer to application notes AN-061, AN-069, AN-070, AN-075).

The offset voltage of TSGF products is typically a few millivolts, with a 300mV max depending of the filter type.

Moreover, there is a possibility to adjust the filter output DC levels, thanks to an external bias voltage applied on "LVL" pin. Automatic offset compensation can be done by mean of one uncommitted on-chip operational amplifier, as indicated in Application note AN-069.

The TSGF products feature a high input impedance (typ. : 3MΩ) and a low output impedance (typ. : 10Ω) allowing then cascadable filter network in order to achieve higher than 12th order.

The output buffers are configurated as sample-and-hold amplifiers which can drive a 1KΩ load resistance and a 100pF load capacitance.

On the TSGF04 and TSGF12 an external sample-and-hold clocking allows to connect the filter output directly to an analog to digital converter (Optional ; see fig. 7).

In addition some particular switched capacitor cells have been implemented on the first 2 integrators of each chip allowing realization of special functions like :

- cosine filter
- complementary high pass filter
- exact bilinear leapfrog filter.

Figure 3a : TSG8512 : 7th Order Cauer Low pass Filter.

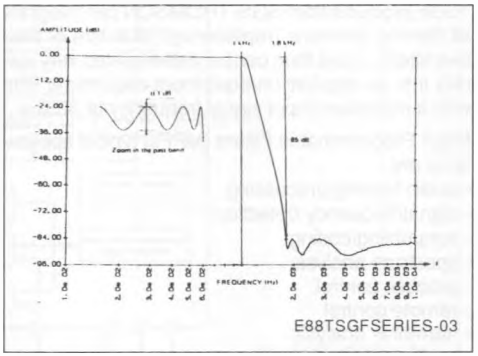
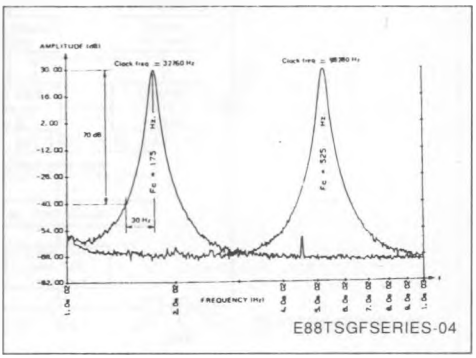


Figure 3b : TSG8551 : 8th Order High-Q Band pass Filter (Q = 35).



BENEFITS

With the TSGF series of SGS-THOMSON, designers are given unique "Gate Array" filter products for the replacement of their passive/active filters or the design of new filters.

The TSGF04/08/12 provide then with gate Array technique 3 complete arrays where all functions necessary to realize the filter function and its external circuit environment are available on chips.

The switched capacitor process permits the realization of very accurate and fully integrated filters and breaks down the equipment production costs by providing fully tested filters parts : tuning or adjustment of external components are no more ne-

cessary with TSGF series.

Figures 3A, 3B is showing 2 examples of Standard Filters designed with the TSGF08 matrix.

APPLICATIONS

TSGF products from SGS-THOMSON can integrate all filtering functions (replacement of active or passive filters...) and then can be implemented very quickly into an application/equipment requiring a filter with a maximum input signal frequency of 30KHz.

Mask Programmable Filters (MPFs) typical applications are :

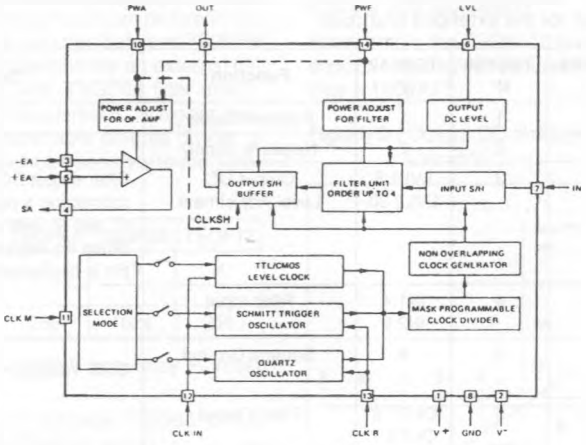
- audio filtering/processing
- signal/frequency detection
- scrambling/coding
- spectrum analysis
- process control
- remote control
- harmonic analysis
- equalization
- frequency tracking
- alarm systems
- robotics
- anti-knock system
- data acquisition (before A/D and after D/A converters)
- automatic answering
- inwarding
- speech processing
- security system (coding, recognition)
- sonar detection
- mobile radio
- modems

BLOCK DIAGRAMS

Figure 4 outlines the mean features and options offered by each of the 3 MPF arrays by showing TSGF04, TSGF08 and TSGF12 block diagrams.

Figure 4 : Block Diagrams.

TSGF04



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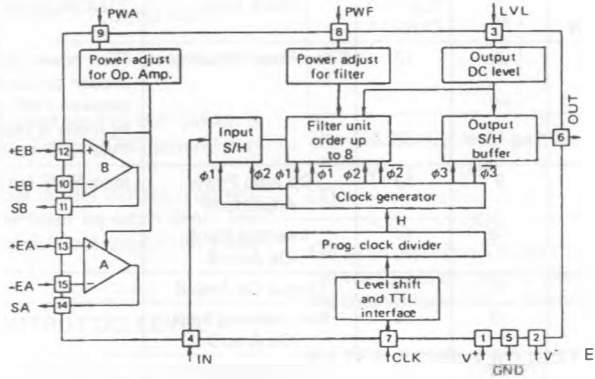
TSGF08



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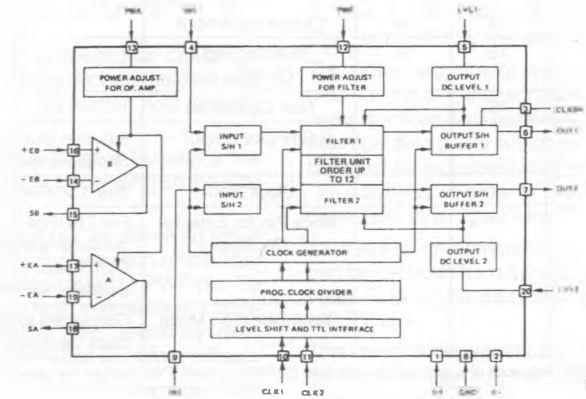
TSGF12



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PIN DESCRIPTION

The table below gives the pin description of the 3 MPF arrays, TSGF04 TSGF08 and TSGF12. The pin assignment is given for the extended and complete version of each array, it means with all the available on-chip options connected to the package.

Name	Pin Type	TSGF04 N°	TSGF08 N°	TSGF12 N°	Function	Description
V⁺	I	1	1	1	Positive Supply	
V⁻	I	2	2	2	Negative Supply	
LVL	I	6	3	LVL1 5 LVL2 20	Output DC Level Adjustment	Filter output DC level adjustment when connecting a potentiometer between V⁺ and V⁻ with its middle point to LVL. When no adjustment is needed, LVL pin is connected to GND.
IN	I	7	4	IN1 4 IN2 9	Filter Input	
GND	I	8	5	8	General Ground	GND Voltage = $\frac{V^+ + V^-}{2}$
OUT	O	9	6	OUT1 6 OUT2 7	Filter Output	
CLK	I	See CLKIN	7	CLK1 10 CLK2 11	Clock Input	TTL/CMOS Level Compatibility
PWF	I	14	8	12	Filter Power Adjustment	Filter power consumption can be chosen by connecting a resistor between PWF and GND (or V⁺). Stand by mode is obtained by connecting PWF to V⁻ (or non connected)
PWA	I	10*	9	13	Op Amp Power Adjustment	Idem PWF but for Op Amp (PWA)
–EB	I		10	14	Inverting Input Op Amp B	
SB	O		11	15	Output Op Amp B	
+EB	I		12	16	Non Inverting Input Op Amp B	
+EA	I	5	13	17	Non Iverting Input Op Amp A	
SA	O	4	14	18	Output Op Amp A	
–EA	I	3	15	19	Inverting Input Op Amp A	
NC			16		Non Connected	
CLKSH	I	10*		3	S/H Clock Input	External Driving Clock of Output Sample-and-hold
CLKIN	I	12			Clock Input	See TSGF04 Clock Oscillator Section
CLKR	O	13			Clock Pin for External Oscillator	For TSGF04, external RC or crystal oscillator are connected to CLKIN and CLKR pins. See TSGF04 clock oscillator section
CLKM	I	11			Clock Selection Mode	Connected to GND or V⁻ see TSGF04 clock oscillator section

* For TSGF04 when external driving clock of output sample-and-hold (CLKSH) is used. PWF realizes the power adjustment of both uncommitted Op-amp and filter.

Note : For other packing pin-out, refer to package drawings and pin-out at the end of data sheet.

FUNCTIONAL DESCRIPTION

INTERNAL CLOCK DIVIDER (CLK)

The internal sampling frequency F_i can be fixed from 500Hz to 700KHz (F_i can be used between 700KHz and 1MHz with some limitations) by an external oscillator (or internal one with TSGF04 filter array). When the external clock frequency F_e, is higher than 700KHz, a mask programmable on-chip divider is used to adapt available clock frequency to the sampling rate.

	TSGF04	TSGF08	TSGF12
Number of Divide by 2 Available Per Chip	8	10	8
Max. F_e/F_i Ratio	256	1024	256

In any case, the external clock frequency F_e must be less than 5MHz.

Example : The TSG8510 features (TSG8510 is a standard filter based on TSGF08 array) :

F_e max = 1.5MHz and F_i max = 750KHz then

$$\frac{F_e}{F_i} = 2$$

only one divider by 2 is used for this filter (which is the case of most of SGS-THOMSON' general purpose filters).

Note : As the internal clock divider is mask programmable, the ratio F_e/F_i is fixed for each filter. The change of this ratio is possible but results into a new part number.

ADJUSTMENT OF OUTPUT DC LEVEL (LVL)

The output DC offset voltage can be removed thanks to an external bias voltage applied on "LVL" pin, as shown on figure 8.

However automatic offset compensation can be implemented by using one of the uncommitted on-chip Op-amps, as indicated in application note AN-069 (see fig. 9 in AN-069).

The offset voltage of TSGF filters is typically a few millivolts, with a 300mV max, depending on the type of the filter.

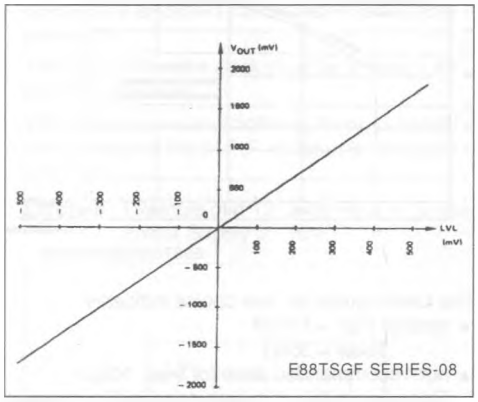
A drift of this offset voltage can be observed when user increases the power consumption of the filter with an external resistor connected to PWF pin. So when the filter operates at high frequencies, a compromise exists between the filter frequency response performance and its output DC offset voltage.

When no DC output level adjustment is required, LVL pin has to be connected to the GND voltage.

The level gain, LG, of each filter can be deduced from the curve representing $V_{OUT} = f(LVL)$. This curve is filter dependent.

For example the TSG8510 presents following curve shown in figure 5 (measured with F_e = 256KHz, I_{PWF} = 100µA) :

Figure 5 : Output DC Voltage Adjustment from LVL Pin.



The TSG8510's level gain is :

$$LG = \frac{V_{OUT}}{LVL} \cong \frac{1000}{300} \cong 3.3$$

For example if one TSG8510 presents a 100mV offset voltage at its output, user must apply an external bias voltage LVL = 30mV to compensate it.

FILTER POWER ADJUSTMENT (PWF)

The filter power consumption can be chosen by connecting an external resistor, R_{PWF} between PWF and GND (or V+) pins.

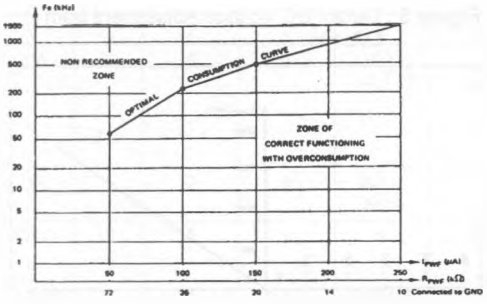
This power adjustment operates the variation of the bias current of the integrators used in the switched capacitor filter. This current, I_{PWF}, can be low when filter operates at low cut-off frequencies ($F_c \cong 1$KHz), but must be increased at high cut-off frequencies ($F_c \cong 20$KHz), in order to charge and discharge the capacitors at a higher rate.

As a result, an optimal choice of I_{PWF} bias current can be deduced from the curve representing $I_{PWF} = f(F_e)$, F_e being the external clock frequency applied on CLK pin.

This curve is dependent on the filter. For example, as shown in figure 6, the TSG8510 presents following characteristics :

Example : if the cutoff frequency of the low pass TSG8510 filter has to be set at 3.4KHz, user must apply the external clock frequency F_e = 75.3 x 3.4 = 256KHz.

Figure 6 : TSGF10 user's Guide for IPWFand RPWF Choise.



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The User's guide for I_{PWF} choice indicates :

- optimal I_{PWF} = 100µA
  R_{PWF} = 35kΩ
- non recommanded zone for I_{PWF} 100µA
  Operation within this area can lead to increase the ripple in the pass band and to decrease the stop band attenuation.
- zone of correct functioning with over consumption for I_{PWF} > 100µA.

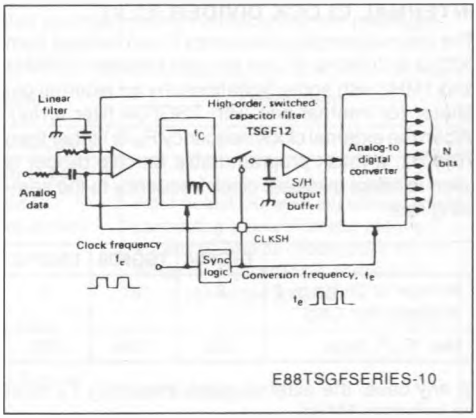
Note : Power consumption choice has to be prioritized when major concern in TSGF design is the frequency response (gain versus frequency). The output DC offset voltage comes in 2nd position in that case.

EXTERNAL DRIVING OF OUTPUT SAMPLE-AND-HOLD

This facility allows the filter output to be connected directly to an analog-to-digital converter, as illustrated in figure 7.

The clock signal which enters on the CLKSH pin must be synchronous with the sampling frequency. As a result, the external clock frequency F_e must be the sampling frequency F_i (the on-chip divider does not have to be used).

Figure 7 : External Driving of Output Sample and Hold (example).



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The clock signal applied on CLKSH pin has to be optimized in order to read a settled signal issued from the switched capacitor filter.

On the example shown in figure 7, a 12th order low pass filter makes an ideal antialiasing filter to precede data conversion. The filter precludes the need for oversampling when driving the A/D converter.

CLKSH option is only available on TSGF04 and TSGF12 arrays.

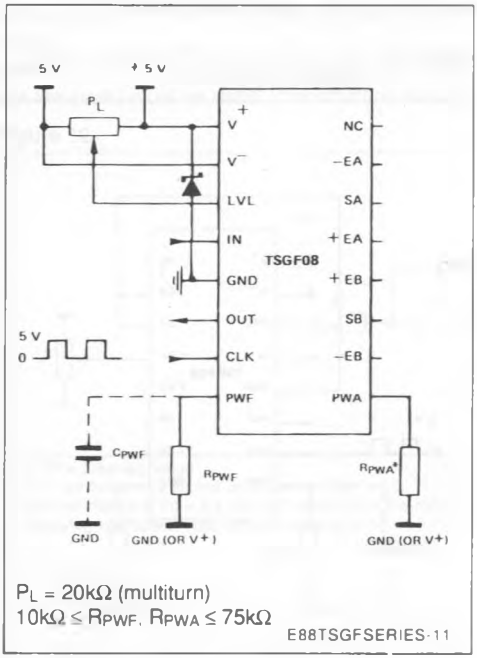
USE OF THE MPF WITH - 5V/+5V DUAL POWER SUPPLY

The adjustment of the DC output level of the M.P.F. is achieved by an external voltage source (for example, a bridge divider connected between the positive and the negative power supplies and whose the middle point is connected to the LVL pin of the M.P.F.). If no output DC adjustment is required, the LVL pin can be directly connected to GND.

The consumption of the filter can be also adjusted by means of an external resistance connected between GND (or V^+) and the PWF pin of the circuit.

The consumption can thus be chosen to match the particular application.

Figure 8 : Example of a TSGF08 Fed in Dual Supply : +5V, 0, -5V.



If the Op-Amps are not used, RPWA has not to be connected between PWA and GND

The stand-by mode is obtained by strapping the PWF pin to V⁻ (or non connected).

The adjustment of the power consumption of the two operational amplifiers can be achieved exactly like for the previous case, but via the PWA pin of the circuit. The stand-by mode is also obtained by strapping the PWA pin to V⁻ (or non connected).

The clock levels are TTL, but CMOS levels are accepted. With these previous conditions, the output linear dynamic range of the M.P.F. is about 8V, between - 4.5V and + 3.5V.

A capacitor C_{PWF} can be added in parallel with R_{PWF} in order to improve the clock feedthrough rejection : (Typical value C_{PWF} = 33pF).

As for all CMOS circuits operating with dual power supply (- 5V, 0, + 5V), it is advised to use clamping diodes (Threshold voltage less than 0.6V) (Schottky is preferrable) in order to avoid transients during power up which could drive TSGF circuits over their maximum ratings. Only 1 Schottky diode between GND and V+ is sufficient for TSGF products.

USE OF THE MPF WITH 0/10V SINGLE POWER SUPPLY

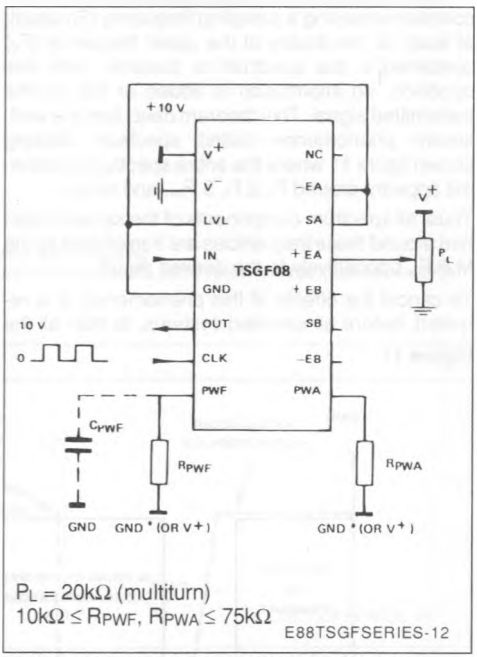
In this case, V⁻ is the reference ground of the circuit and GND must be adjusted to + 5V by means of the potentiometer P_L (V+ - V⁻)/2), or by using a simple bridge divider. But in that case small resistors values (2kΩ) have to be used in order to set GND at a low impedance value.

The adjustments of the DC output level of the M.P.F. of the power consumptions of the filter and of the operational amplifiers can be achieved exactly like previously.

The high level of the clock must be at least 1.4V upper the GND level.

With these previous conditions, the output linear dynamic range of the M.P.F. is about 8V between 0.5 and 8.5V.

Figure 9 : Example of a TSGF08 FED, in Single Power Supply 0 - 10V.



* GND is used, when the user provides the 5V voltage.

USE OF THE MPF WITH 0/5V SINGLE POWER SUPPLY

In this case, V⁻ is the reference ground of the circuit

and GND must be adjusted to + 2.5V by means of the potentiometer P_L ($(V+ - V^-)/2$), and one Op-amp used as buffer in order to provide a low impedance on GND reference.

Otherwise, without Op-amp, a simple bridge divider is sufficient, but small resistor values (2kΩ) have to be used in order to set GND at a low impedance value.

The other adjustments are achieved exactly like previously except for bias resistance of the filter and of the operational amplifiers (R_{PWF} and R_{PWA}), whose must be exclusively to V+.

The clock levels must be CMOS levels. With these previous conditions, the output linear dynamic range of the M.P.F. is about 2.2V, between 1.2 and 3.4V.

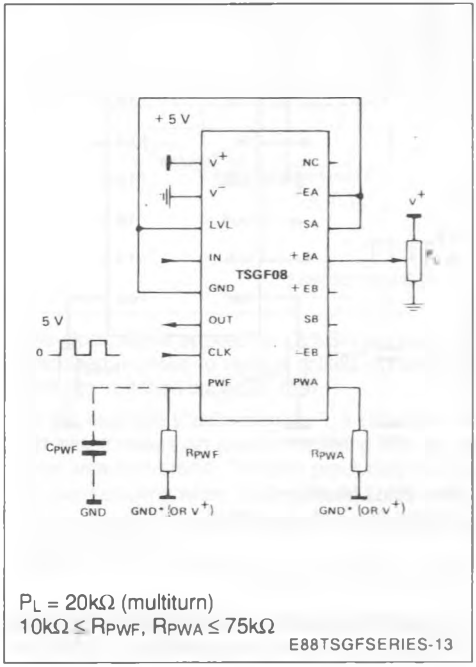
ANTI-ALIASING AND SMOOTHING

Anti-aliasing : The switched capacitor filters are sampled systems and must verify the SHANNON condition imposing a sampling frequency (F_i) equal, at least, to the double of the upper frequency (F_c) contained in the spectrum to transmit. With this condition, no information is added or lost on the transmitted signal. This theorem describes the well-known phenomenon called spectrum aliasing shown figure 11 where the entire spectrum to transmit appears around F_i, 2 F_i, 3 F_i... and so on.

Thus, all spectrum components of the signal contained around these frequencies are transmitted by the M.P.F., oppositively to the desired result.

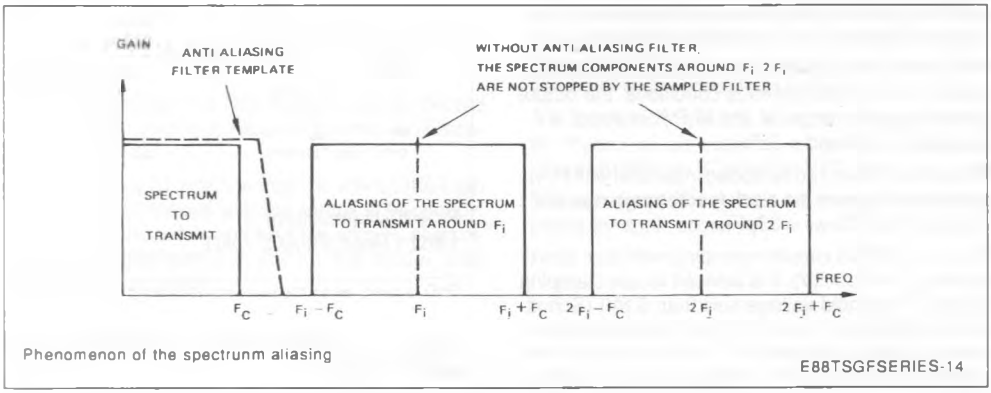
To cancel the effects of this phenomenon, it is required. before all sampled systems, to filter all the spectrum components of the intput signal upper than F_i - F_c. An analog filter, called "anti-aliasing filter", must be therefore applied before the M.P.F.

Figure 10 : Example of a TSGF08 FED in Single Power Supply 0-5V.



*GND is used, when the user provides the 2.5V Voltage.

Figure 11.



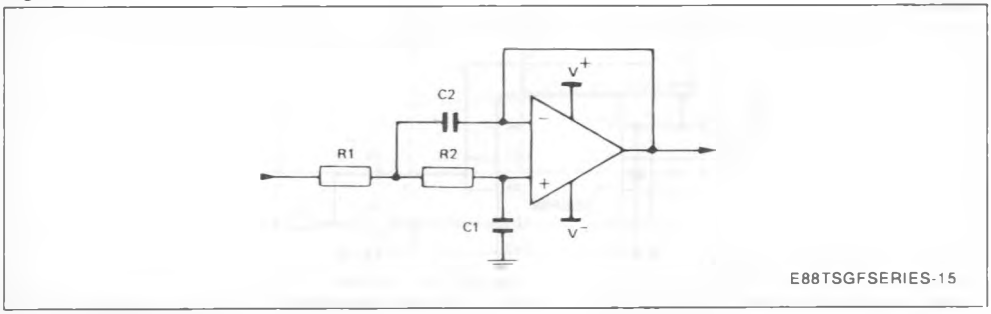
- Without anti-aliasing filter : Spectrum to transmit ≠ transmitted spectrum
- With anti-aliasing filter : Spectrum to transmit = transmitted spectrum

The selectivity of this filter depends upon the F_i/F_c ratio.

If F_i/F_c 200, a RC filter (first order low-pass) is sufficient.

If F_i/F_c 200, a SALLEN-KEY structure (second order low-pass) must be used. This structure and its relationships are described (figure 12). In these relationships, F_c is the cut-off frequency desired of the anti-aliasing filter and ξ its damping coefficient. For a cut-off as tight as possible and in order to correct the sin x/x effect, ξ must have a value around 0.7.

Figure 12.



R1 = R2 = arbitrary value
F_c = cut-off frequency for the antialiasing filter.
An optimal choice is Fc = 2 x cut-off frequency of the main filter
ξ = damping coefficient ; the optimal value is 0.7

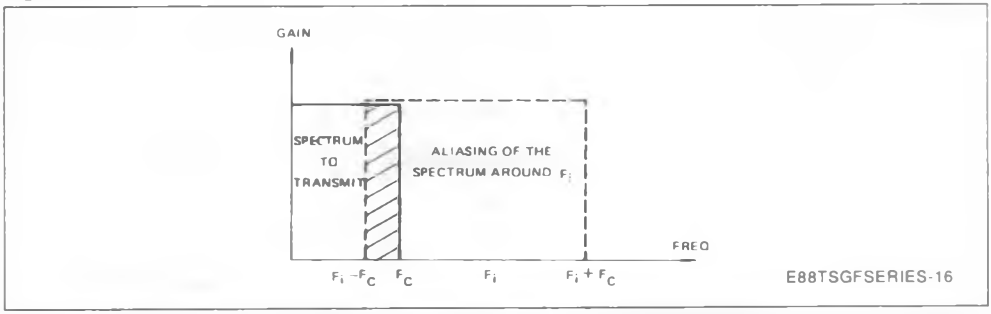
$$C1 = \frac{\xi}{2\pi R1 Fc}$$

$$(C1 = \xi 2 - C2)$$

$$C2 = \frac{1}{2\pi\xi R1 Fc}$$

SALLEN-KEY structure (second order low-pass Filter) for anti-aliasing and smoothing.
Note : If F_i/F_c 2 (figure 13), the spectrum to transmit and the spectrum aliased have a part in common and it becomes impossible to share the useful signals from the undesirable signals.

Figure 13.

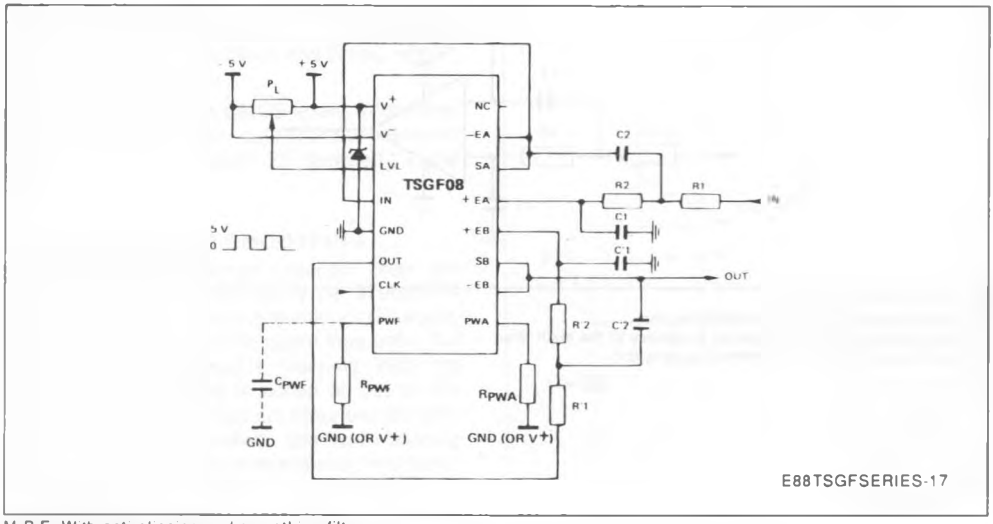


When Fi/Fc<2, the spectrum component included between Fi-Fc and Fc and which are due to spectrum aliasing are not stopped by the sampled filter.

- Smoothing : As the signal obtained at the output of the M.P.F. is a sampled and hold signal, it is often required to smooth it. This smoothing filter can be achieved from the SALLEN-KEY structure previously described (figure 12).
- Hardware implementation : In order to make easier anti-aliasing and smoothing. SGS-THOMSON has designed, on the TSGF chip one or, two general purpose operational amplifiers. A few external components are therefore sufficient to achieve these functions (figure 14).

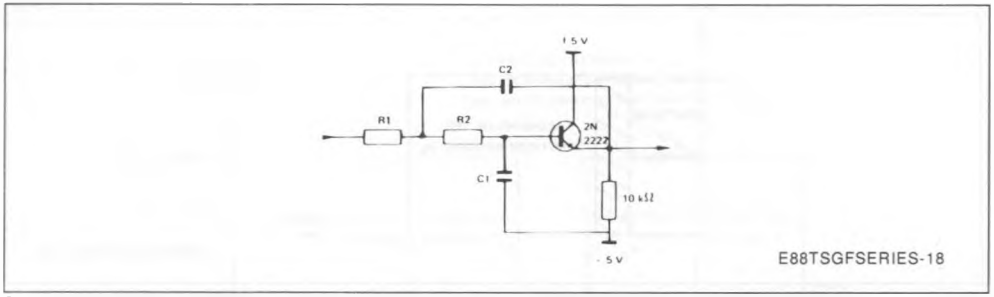
On the other hand, in the most of M.P.F.'s, a special integrated cell is included in the chip (cosine filter) to reduce the aliasing effects around F_i.

Figure 14.



M.P.F. With anti-aliasing and smoothing filters.
P_L = 20kΩ (multiturn)
$10k\Omega \leq R_{PWF}, R_{PWA} \leq 75k\Omega$
R1,R2,C1,C2 } See anti-aliasing
R'1, R'2,C'1,C'2 } and smoothing considerations

Figure 15.



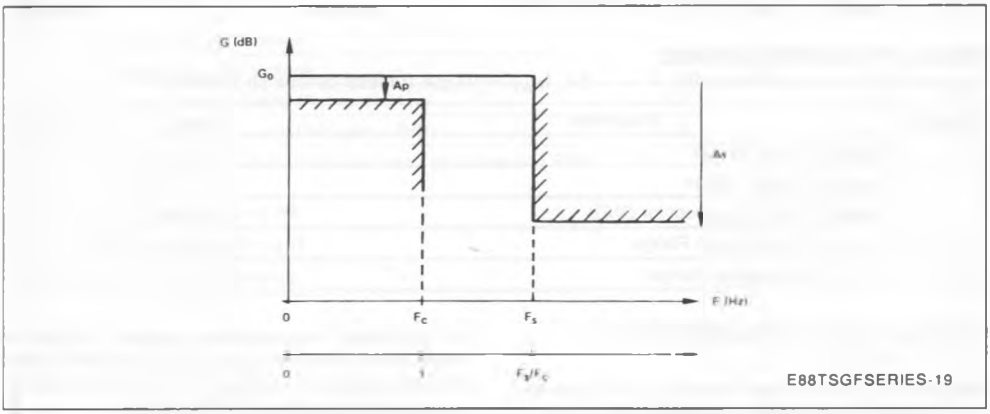
Second order low-pass Filter (SALLEN-KEY STRUCTURE) with a transistor replacing the operational amplifier.

Nonetheless, if the application allows it, these two operational amplifiers can be used to implement other functions (gain, comparator, oscillator...).

In this case, the circuit shown figure 15 can be used as anti-aliasing or smoothing filter. This structure is the same as the SALLEN-KEY structure described figure 12 (second order low-pass), in the same way as the corresponding relationships.

CUT-OFF FREQUENCY DEFINITION

Figure 16 : Design Specifications.



The cut-off frequency F_c is the passband limit frequency as defined on the design specifications above mentioned. The maximum value of the attenuation variation in the passband : Ap is 3dB for Butterworth. Bessel and Legendre filters (figure 17a), and is called passband ripple for Chebychev (figure 17b) and Cauer filters (figure 17c).

The passband ripple is design dependent and between 0.05dB and 0.2dB with TSGF standard filters. The parameters G_o called passband gain is the maximum value of the gain in the passband, and may have low variation from part to part.

Figure 17a.

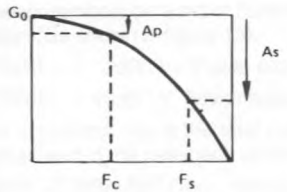


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Figure 17b.

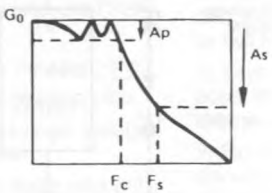

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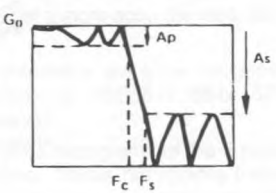
Figure 17c.



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ELECTRICAL SPECIFICATION

The following electrical characteristics are common to the 3 base filter arrays TSGF04, TSGF08 and TSGF12, because their structures are designed with the same basic components.

ABSOLUTE MAXIMUM RATINGS

T_{amb} = 25°C, V+ = 5V, GND = 0V, V– = – 5V, I_{PWF} = 100µA (unless otherwise specified)

Symbol	Parameter	Value	Unit
V+	Positive Supply Voltage	– 0.15 to + 7	V
V–	Negative Supply Voltage	– 7 to + 0.15	V
V	Voltage to any Pin (except for GND)	(V–) – 0.3 to (V+) + 0.3	V
T_{oper}	Operating Temperature Range	T_{min} – 5°C to T_{max} + 5°C	°C
T_{stg}	Storage Temperature Range	– 60 to + 150	°C

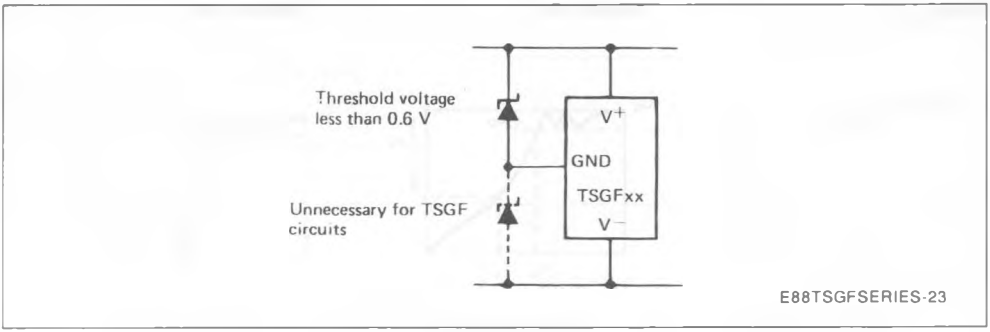
WARNING : DUAL POWER SUPPLY (- 5V, 0, + 5V)

Although TSGF circuits are internally gate protected to minimize the possibility of static damage, MOS handling and operating procedure precautions should be observed. Maximum rated supply voltages must not be exceeded. Use decoupling networks to remove power supply turn on/off transients, ripple and switching transients.

Do not apply independently powered signals or clocks to the chip with power off as this will forward bias the substrate. Damage may result if external protection precautions are not taken :

As for all CMOS circuits operating with three supply voltages (V+, GND, V-), it is advised to use clamping diodes (Schottky is preferable), in order to avoid transient during power up that would drive the circuit over its maximum ratings (see figure 18).

Figure 18 : Application Hint for CMOS ICs with Three Supply Voltages.



ELECTRICAL OPERATING CHARACTERISTICS

$V^+ = 5V$, GND = 0V, $V^- = -5V$, $T_{amb} = 25°C$, $I_{PWF} = 100\mu A$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+	Positive Supply Voltage	4	5	6	V
V^-	Negative Supply Voltage	– 6	– 5	– 4	V
V_{OUT}	Output Voltage Swing (*)	$(V^-) + 0.5$		$(V^+) - 1.5$	V_{PP}
V_{IN}	Input Voltage (*) (with filter gain = 0dB)	$(V^-) + 0.5$		$(V^+) - 1.5$	V_{PP}
I_{PWF}	Bias Current on PWF (stand-by mode by connecting PWF to V^-)	50		250	µA
V_{IL}	TTL Clock Input "0" (**)			+ 0.8	V
V_{IH}	TTL Clock Input "1" (**)	2			V
T_{CP}	Ext. Clock Pulse Width	80			ns
R_{IN}	Input Resistance	1	3		MΩ
C_{IN}	Input Capacitance			20	pF
R_{OUT}	Output Resistance		10		Ω
C_L	Load Capacitance			100	pF
R_L	Load Resistance	0.1	1		kΩ

Note : with supply (0, + 10V) : same specifications
with single supply (0, + 5V) : contact SGS-THOMSON sales office or representative.
(*) Depending on I_{PWF} current
(**) TTL levels are referenced to GND voltage

Other filter's characteristics, such as noise, power supply rejection ratio, total harmonic distortion... are filter dependent. As a result, for such characteristics, SGS-THOMSON can only guarantee the lower level of performance for each parameter, as indicated below. (this lower level has been determined from measurements on a set of hundred different TSGF filters, as shown in figure 19).

PSRR + > 2dB : V+ Power supply rejection ratio.

PSRR – > 10dB : V Power supply rejection ratio.

$V_n < 1mVrms$: V_n is the total output noise voltage measured in the passband of the filter.

SNR > 57dBm/600 Ohm : Signal to noise ratio with $V_{IN} = 775mVrms$.

SNR > 65dBV : signal to noise ratio with $V_{IN} = 2Vrms$.

THD < 0.1% : Total harmonic distortion.

As such characteristics are not predictable from simulation results, their typical values are provided from measurements of the customized filter prototypes. (These measurements could be performed by SGS-THOMSON on special request).

These typical values, obtained with TSGF products, are better than the lowest level guaranteed, and designers can get a more accurate idea about them by two means.

1) Such characteristics are given for general-purpose filters. Refer to TSG85xx, 86xx, 87xx data sheets.

2) Figure 19 gives histograms of the 5 parameters discussed above. These histograms indicate the distribution of the typical value of the considered parameter over a set of hundred different TSGF filters. (Note that the aim of these histograms indicate the dispersion of the considered characteristic for a given TSGF filter).

Figure 19 : Distribution of Typical Value Over a set of Hundred Different TSGF Filters.

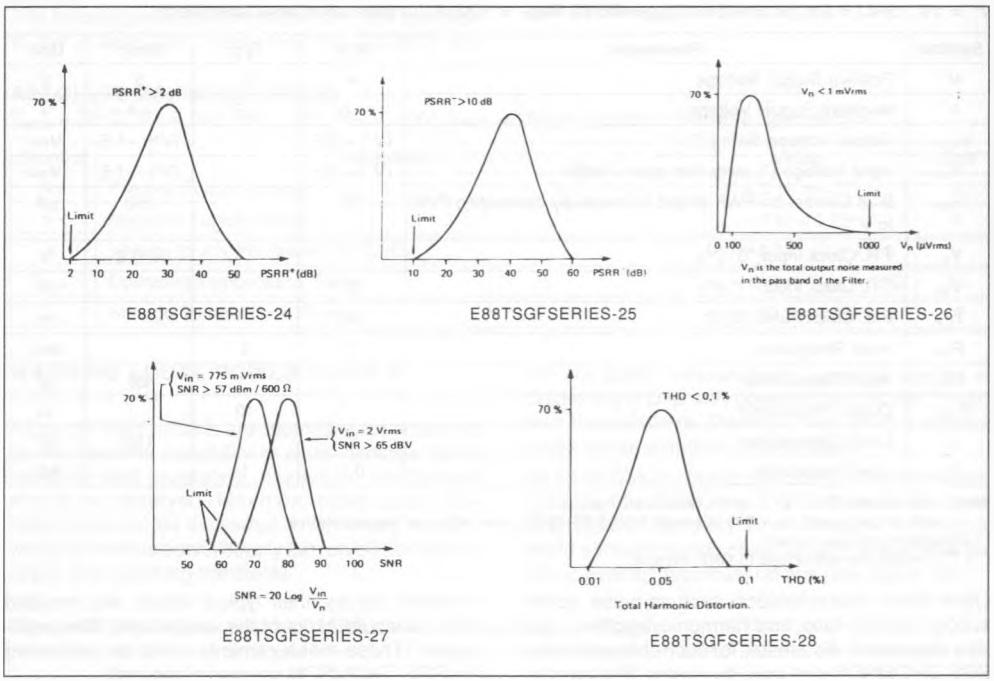
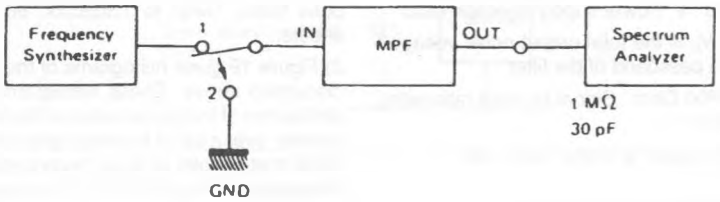


Figure 20 : Method of Noise Measurement.



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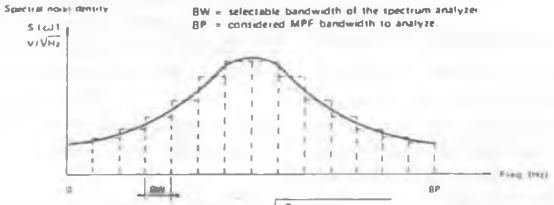
Position 1 : Calibration of the spectrum analyzer to 0dBV (1Vrms).
Position 2 : Measurement with filter input connected to GND.

Figure 20 : (continued).



We obtain theoretical noise voltage : $Vn(Vrms) = \sqrt{\int_0^{BP} S^2(\omega).d\omega}$

and measured noise voltage : $Vn(Vrms) = \sqrt{\sum_{k=1}^{BP/BW} S^2(k) . BW}$

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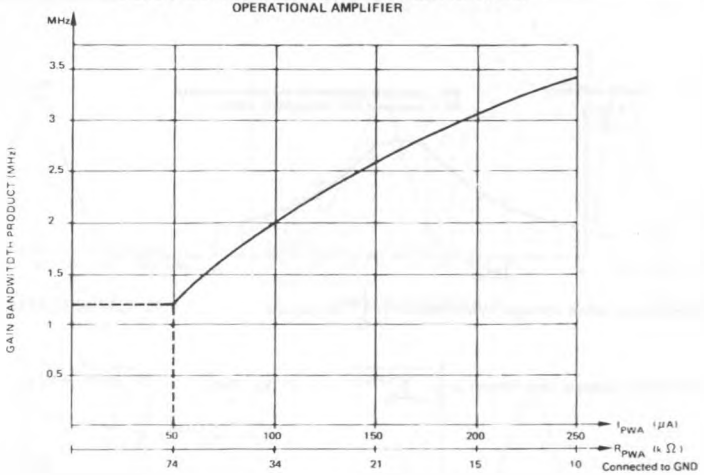
UNCOMMITTED ON-CHIP OPERATIONAL AMPLIFIERS

$V^+ = 5V$, $GND = 0V$, $V^- = -5V$, $T_{amb} = 25°C$, $RL = 2k\Omega$, $I_{PWA} = 100\mu A$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$G_0{}^+$ $G_0{}^-$	DC Open Loop Gain (without load)	60 60	75 75		dB dB
G_{BP}	Gain Bandwidth Product (without load)	1	2		MHz
V_{IO}	Input Offset Voltage (without load)		± 5	± 10	mV
$V_{OP}P$	Output Swing		− 4.5 3.5	− 4.7 3.7	V V
I_{IB}	Input Bias Current (without load)		± 5	± 10	nA
SVR	Supply Rejection (without load)	60	65		dB
CMR	Common Mode Rejection $V_{CM} = 1V$ (without load)	60	65		dB
R_O	Output Resistance		10		Ω
Ia^+ Ia^-	Supply Current		2.6 2.6	3.2 3.2	mA mA
SR^+ SR^-	Slew Rate	2 2	5 6		V/µs V/µs

USER'S GUIDE OF I_{PWA} AND R_{PWA} FOR UNCOMMITTED ON-CHIP OPERATIONAL AMPLIFIER



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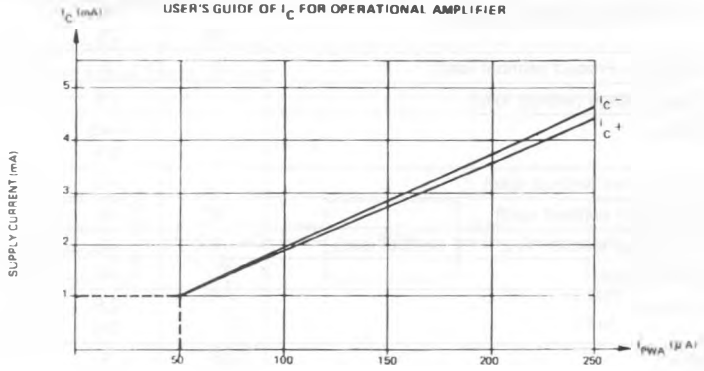
USER'S GUIDE OF I_C FOR OPERATIONAL AMPLIFIER



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CAD SOFTWARE : FILCAD

In order to take full advantage of its Mask Programmable filter TSGF approach for Semicustom applications, SGS-THOMSON has developed a comprehensive software package called FILCAD® to cover all the development steps, starting from the feasibility evaluation of the customer's specifications, up to the single-metal interconnection routing required for the MPF customization.

More specifically, the FILCAD system gives the de signer strong assistance during the following steps :

- Evaluation of MPF solutions well suited to specific filter circuit requirements,
- Filter synthesis, leading to a switched capacitor electrical schematic,
- MPF filter simulation (performed with MPF capacitor capabilities),
- Schematic capture and routing of the optional connections,
- Layout file generation, and final verification performed by accurate post-routing simulation.

All FILCAD modules run on VAX® under VMS operating System, and are linked toghether as shown in figure 21. All modules are fully described in the TSGF's User's manual (Vol. 5 of SGS-THOMSON ASIC User's Manuals).

The entry to FILCAD is the customer filter specification which can be provided to SGS-THOMSON in different forms :

- amplitude - phase - group delay templates
- poles and zeros
- biquadratic cell coefficients
- polynomial transfer functions

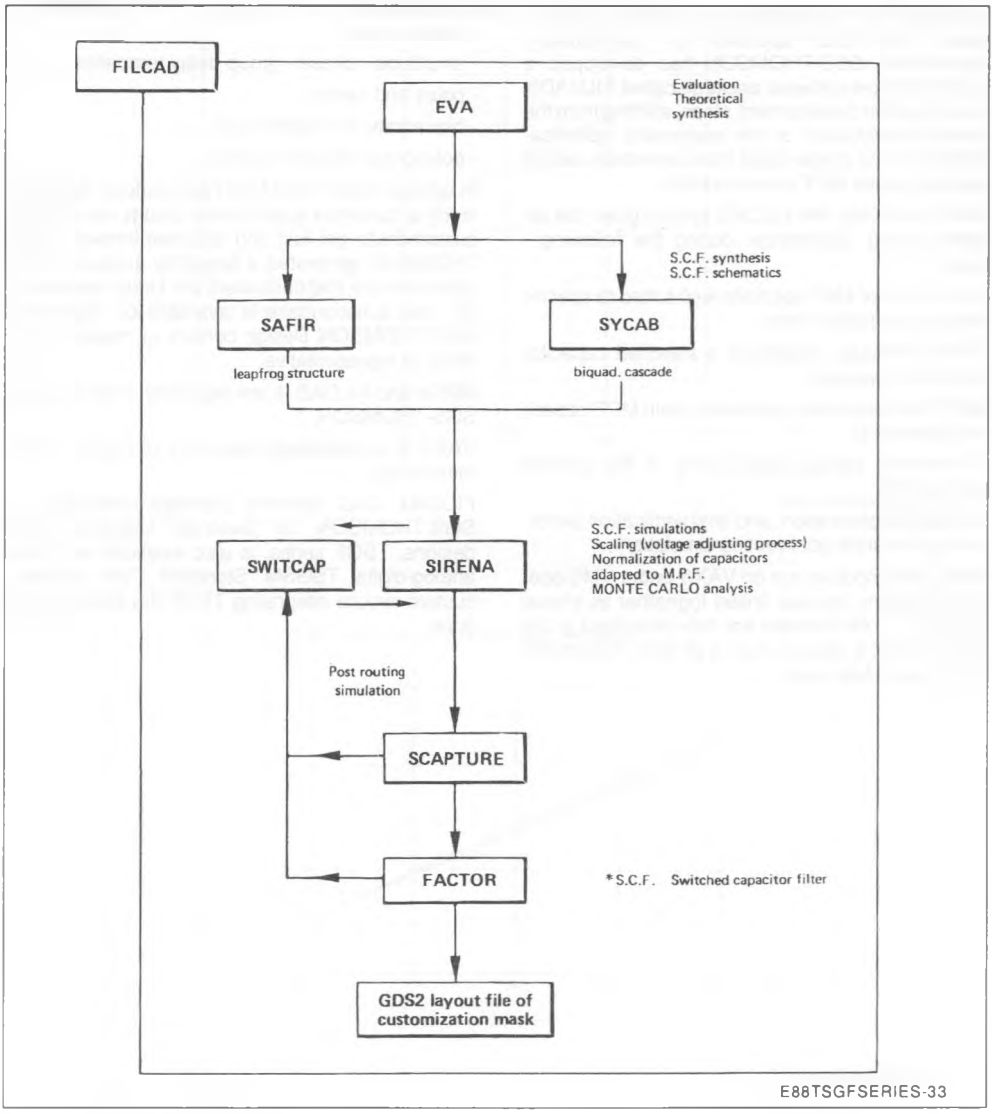
In addition SGS-THOMSON can perform feasibility study of customer specific filter circuits : in order for customers to get fast and accurate answer, SGS-THOMSON generated a feasibility analysis TSGF questionnaire that customers are kindly required to fill. This questionnaire is available on request at SGS-THOMSON Design centers or nearest sales office or representative.

MPF® and FILCAD ® are registered trademarks of SGS-THOMSON.

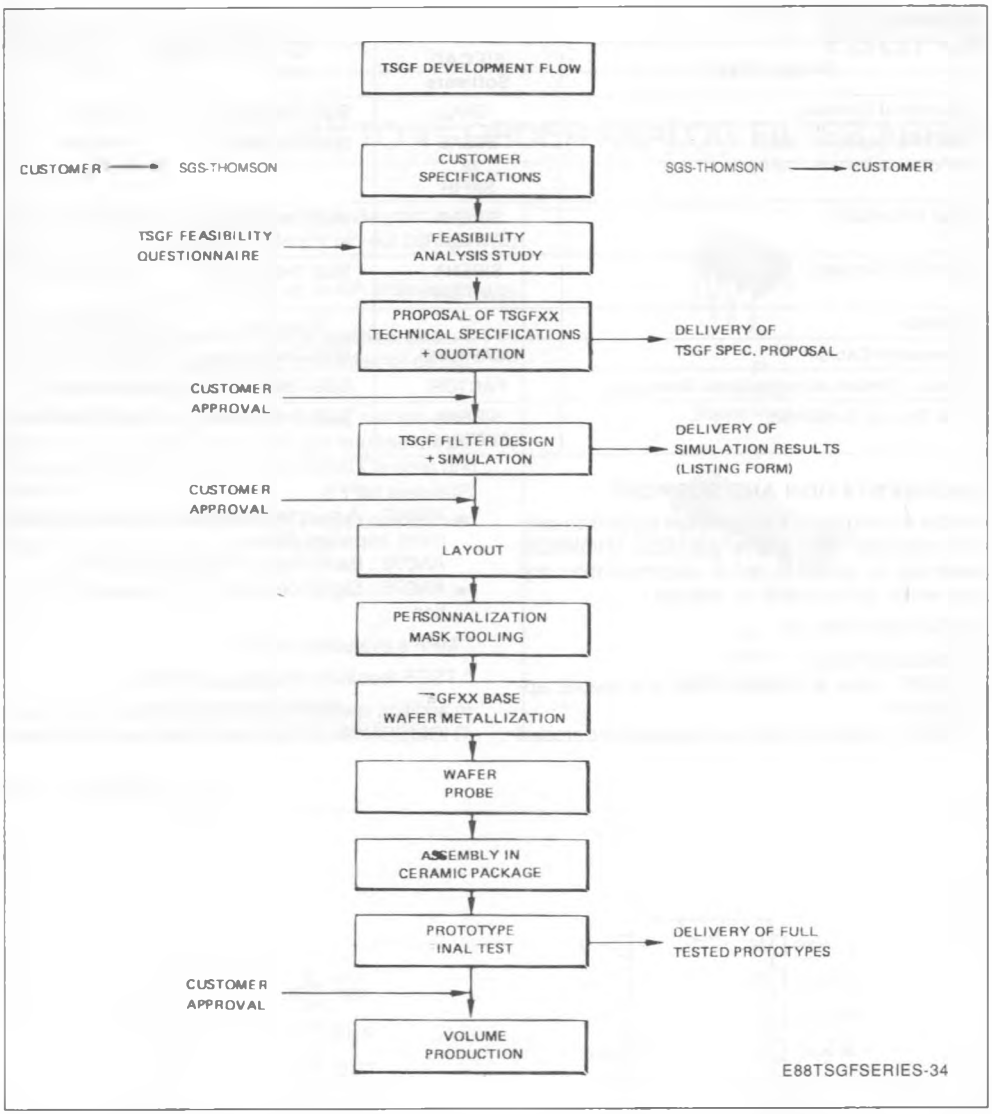
VAX® is a registered trademark of Digital Equipment Corp.

FILCAD, CAD software package developed by SGS-THOMSON for Switched Capacitor Filter designs, TSGF series, is also available for mixed analog-digital TSGSM Standard Cells or Full custom circuits integrating TSGF-like filtering functions.

Figure 21.



FILCAD is a trademark of SGS-Thomson
SWITCAP is a trademark of Columbia University



SGS-THOMSON proposes presently 2 design interfaces to customers for the design of their filter circuits with TSGF series :

- design entirely done by SGS-THOMSON within its Design Centers ;
- design done by customer up to simulation and then completed by SGS-THOMSON.

The table below outlines customer and SGS-THOMSON respective responsibilities for these 2 design interfaces.

DESIGN INTERFACES

Design Step	FILCAD Software	Int 2	Int 3
Theoretical Synthesis	EVA	SGS-THOMSON	Customer
Switched Capacitor Filters Schematics before Scaling	SYCAB or SAFIR	SGS-THOMSON	Customer
Final Schematics	SIRENA (SWITCAP)	SGS-THOMSON	Customer
Additional Simulation	SIRENA (SWITCAP)	SGS-THOMSON	Customer
Approval		Customer	SGS-THOMSON
Schematics Capture	SCAPTURE	SGS-THOMSON	SGS-THOMSON
Layout - Personnalization Mask Generation	FACTOR	SGS-THOMSON	SGS-THOMSON
Post Routing Simulation	SIRENA (SWITCAP)	SGS-THOMSON	SGS-THOMSON

DOCUMENTATION AND SUPPORT

In order to bring users the maximum support on switched capacitor TSGF filter arrays, SGS-THOMSON generated a complete set of documentation and tools which are available on request :

* TSGF User's Manual

* Application Notes
  - AN052 : How to choose a filter in a specific application
  - AN061 : implementation and applications around Standard MPFS
  - AN069 : A supplement to the utilization of switched capacitor filters.
    AN070 : Band Pass and Band Stop Filters.
  - AN075 : Signal detection and sinewave generation.

* MPF's evaluation boards.

* TSGF feasibility/analysis questionnaire.

In addition specialists can be contacted within SGS-THOMSON Microelectronics Filter Design Centers.