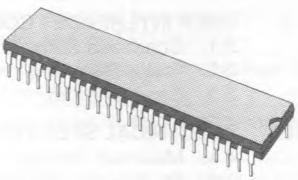
SGS-THOMSON MICROELECTRONICS

TS7532

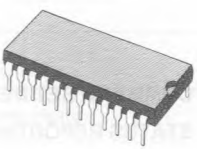
V. 32 MODEM CHIP SET

ADVANCE DATA

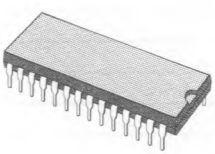
- CCITT V.32 COMPATIBLE MODEM CHIP SET [see ref 1 of Appendix D]
- INTEGRATED IMPLEMENTATION ON THREE DSP AND THREE MAFE CHIPS
- FULL DUPLEX OPERATION AT 9600 AND 4800 BPS
- FULL IMPLEMENTATION OF THE V.32 HANDSHAKE
- DYNAMIC RANGE : 43 dB
- TWO SATELLITE HOPS AND FREQUENCY OFFSET CAPABILITIES (10 Hz) FOR THE FAR END ECHO CANCELLER
- TRELLIS ENCODING AND VITERBI DECODING
- 12.5 % ROLL-OFF RAISED COSINE TRANSMITTER PULSE SHAPING
- HIGH PERFORMANCE PASSBAND FRACTIONALLY SPACED ADAPTIVE EQUALIZER
- SIGNAL QUALITY MONITORING
- PARALLEL INTERFACE TO STANDARD MICROPROCESSORS
- BIT RATE DATA CLOCKS PROVIDED FOR SYNCHRONOUS DATA TRANSFER
- FULL DIAGNOSTIC CAPABILITY
- DTMF GENERATION
- CALL PROGRESS TONE DETECTION
- FUTURE UPGRADE TO INCLUDE V.22 BIS, V.22, B212A AND FSK (TOTALLY PIN-COMPATIBLE)
- SOFTWARE LICENSE AND DEVELOPMENT TOOLS AVAILABLE FOR EASY CUSTOMIZATION



P
DIP48
(Plastic Package)
TS75320/1/2



P
DIP24
(Plastic Package)
TS68950



P
DIP28
(Plastic Package)
TS68951/2

(Ordering information at the end of the datasheet)

DESCRIPTION

The SGS-THOMSON Microelectronics V.32 chip set is a highly integrated modem engine, which can operate in full duplex at 9600 and 4800 bps. The modem hardware consists of three analog front end (MAFE) chips, three DSP processor chips and additional memory chips.

The three SGS-THOMSON analog front end chips (TS68950/1/2) are the transmit interface, the receive interface and the clock generator respectively.

The modem signal processing functions are implemented on three TS68930 programmable digital signal processors. TS75320 supports the echo canceller, TS75321 the transmitter, handshake and user's interface and TS75322 the receiver.

TABLE OF CONTENTS

TABLE OF APPENDICES

1. PIN DESCRIPTION

1.1. SYSTEM INTERFACE

TS75321 (DSP#1 Transmitter and Handshake)

Pin Name	Pin N°	Type	Signal Name	Description
AD0.AD7	27.34	I/O	D0H.D7H	System Data Bus : these lines are used for data transfer between the TS7532 mailbox and the host processor.
$\overline{CS}$	21	I	CSL	Chip Select : this input is asserted when the TS7532 is to be accessed by the host processor.
$\overline{RS}$	22	I	RSL	Register Select : this signal is used to control the data transfers between the host processor and the TS7532 mailbox.
$\overline{SDS}$	20	I	DSL	System Data Strobe : synchronizes the transfer between the TS7532 mailbox and the host processor.
SR/$\overline{W}$	19	I	RWL	System Read/Write : control signal for the TS7532 mailbox operation.
$\overline{IRQ}$	24	O	INTL	Interrupt Request : signal sent to the host processor to access the TS7532 mailbox.
$\overline{RESET}$	23	I	RSTL1	Master Reset of DSP#1

1.2. ANALOG INTERFACE

TS68950 (Analog Front End Transmitter)

Pin Name	Pin N°	Type	Signal Name	Description
AT0	15	AT0	AT0	Analog Transmit Output

TS68951 (Analog Front End Receiver)

Pin Name	Pin N°	Type	Signal Name	Description
RAI	16	I	RAI	Receive Analog Input
LEI	17	I	LEI	Local Echo Input. This signal is subtracted from signal RAI.

1.3. CLOCK INTERFACE

TS68952 (Clock Generator)

Pin Name	Pin N°	Type	Signal Name	Description
TxCLK	23	O	TxCLK	Transmit Bit Clock
TxRCLK	16	O	TxRCLK	Transmit Baud Clock
TxCCLK	24	O	TxCCLK	Transmit Conversion Clock
TxMCLK	18	O	TxMCLK	Transmit Multiplex Clock
RxCLK	22	O	RxCLK	Receive Bit Clock
RxRCLK	20	O	RxRCLK	Receive Baud Clock
RxCCLK	21	O	RxCCLK	Receive Conversion Clock
RxMCLK	19	O	RxMCLK	Receive Multiplex Clock
TxSCLK	11	I	TxSCLK	Transmit Synchro Clock : can be used to synchronize the transmitter on an external bit clock provided by the RS232C (or V.24) junction.

2. FUNCTIONAL DESCRIPTION

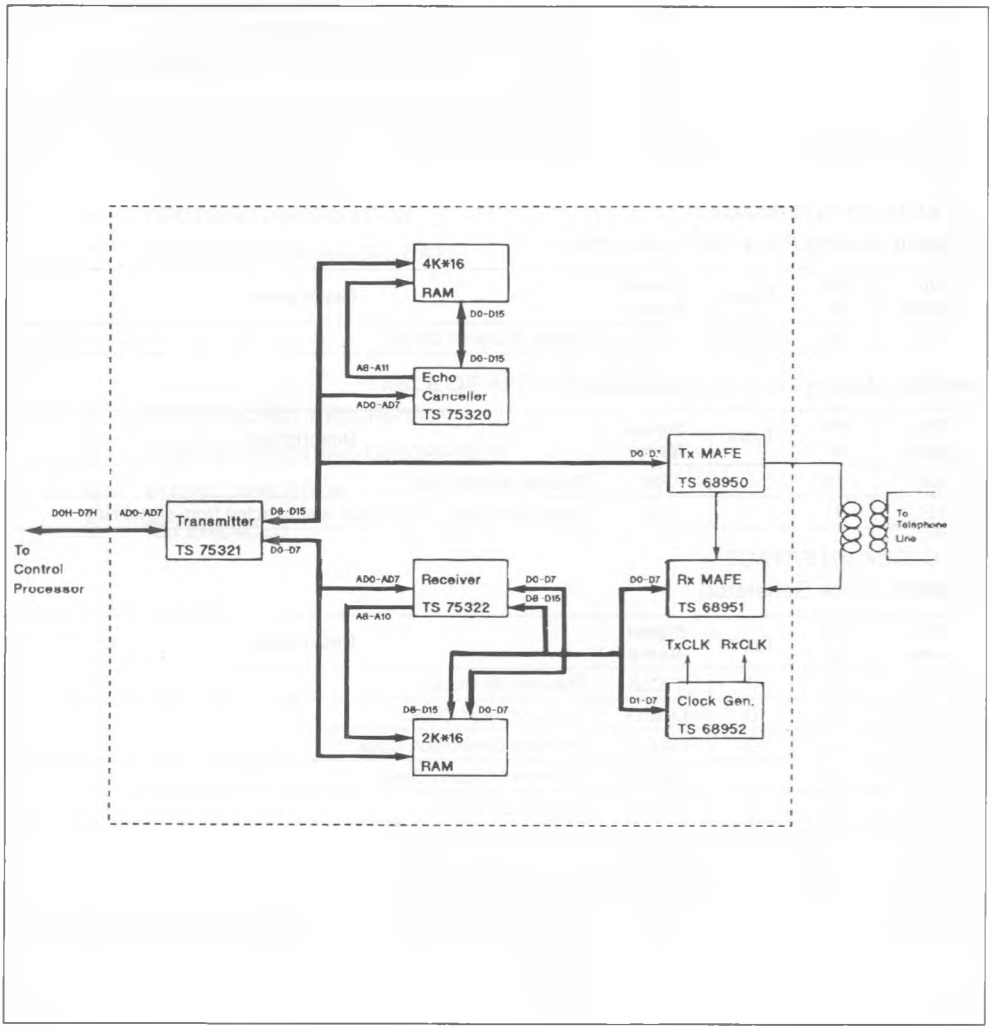
2.1. SYSTEM ARCHITECTURE

The SGS-THOMSON V.32 chip set is a highly integrated modem engine which provides the functionality and performance requirements for full-duplex 9600 bps modem solutions at a low cost and with a small circuit area. At the heart of the modem engine are three SGS-THOMSON DSPs which implement the complete signal processing and control functions. The analog front end of the modem engine consists of the SGS-THOMSON MAFE three-chip set which is designed to meet the requirements of high-speed modem applications and particularly V.32 modems. The only other components in the modem engine are the external RAM chips used for the far-end echo canceller delay line and the Viterbi decoder.

2.2 PROCESSOR AND MAFE CHIPS ARRANGEMENT

Figure 1 shows the interconnections between the MAFE and signal processors.

Figure 1 : Hardware Architecture.



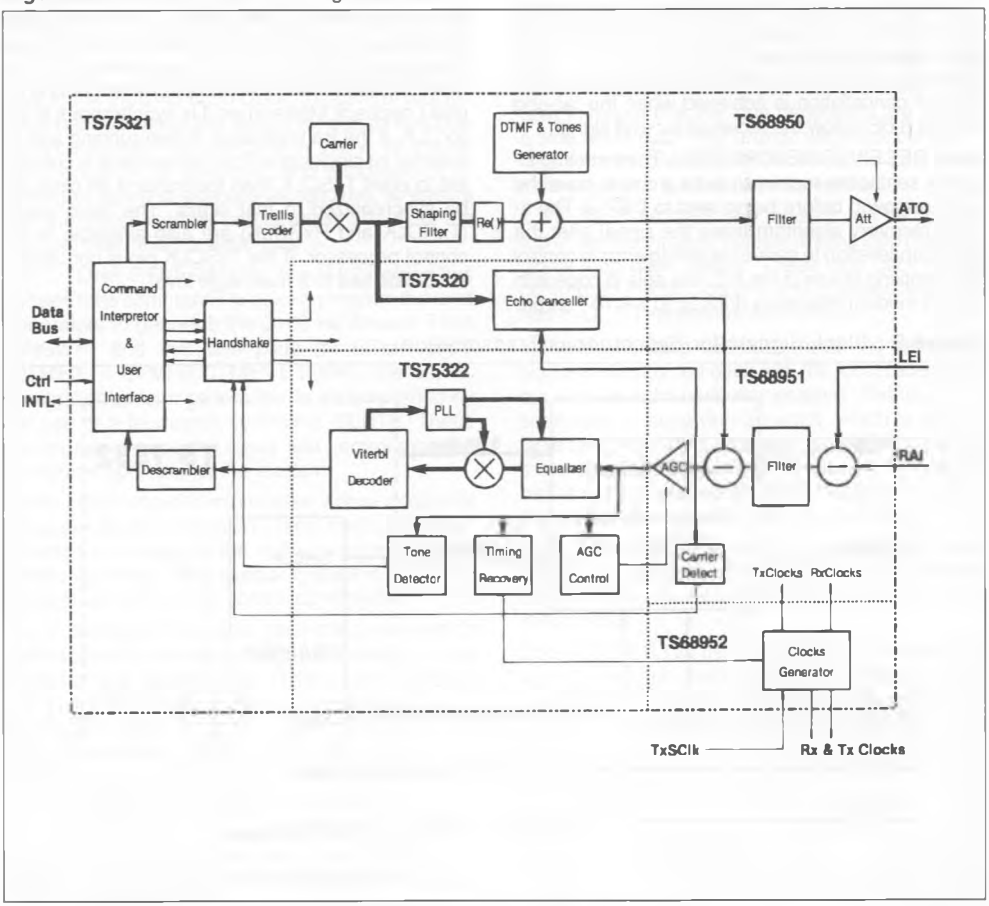
DSP 1 communicates with the control processor through its system bus, AD0-AD7. It is also connected to the two other DSPs through its D0-D7 and D8-D15 data buses to transfer data, to pass a control command to the DSPs and to get the modem operation status and then pass it to the control processor. The transmitter, V.32 handshake and part of the receiver algorithms are implemented in this processor. DSP 0 implements the echo cancellation function. 4Kx16 of RAM are connected to this processor to implement the data delay line for the far end echo cancellation. DSP 2 implements most of the receiver functions. 2Kx16 of RAM are attached to it due to the requirements of the Viterbi decoder.

The transmitter interface chip, TS68950 [see ref 5 of Appendix D], is connected to the 8 MSB's of the DSP 1 data bus. The echo replica is sent from DSP 1 to TS68950 then to the receiver interface chip, TS68951 [see ref 6 of Appendix D], after conversion to analog format. This chip and the clock generator chip, TS68952 [see ref 7 of Appendix D], are connected to the 8 MSB's of the DSP 2 data bus. The clock generator chip generates the A/D and D/A sampling clocks and the data bit and baud rate clocks.

2.3. OPERATION

2.3.1. MODES. The modem implementation is fully compatible with the CCITT recommendation V.32. It operates at two different bit rates, 9600 and 4800 bps. In the 9600 bps mode, the trellis encoder and the Viterbi decoder can be switched in or out. Both the bit rate and trellis options are determined during the initial modem handshake sequence.

Figure 2 : Functional Block Diagram.



2.3.2. SIGNAL SPECTRUM SHAPING. A square root of 12.5 percent roll-off raised cosine filter is implemented in the transmitter to properly shape the transmit signal pulse. This filter is chosen based on a compromise of two considerations. First, the signal should have a narrow spectrum to avoid severe distortion on the telephone line. Second, the signal spectrum should be made as wide as possible to facilitate timing recovery in receiver.

2.3.3. ECHO CANCELLATION. The echo canceller is implemented on a single DSP [see ref 8 of Appendix D] with its associated external RAM. It cancels both near-end and far-end echoes even in the presence of frequency offset in the far-end echo path. The near-end echo cancellation is better than 55 dB and the residual near-end echo is smaller than - 65 dBm with a near-end echo level of - 10 dBm at the receiver input and a far-end signal level of - 43 dBm.

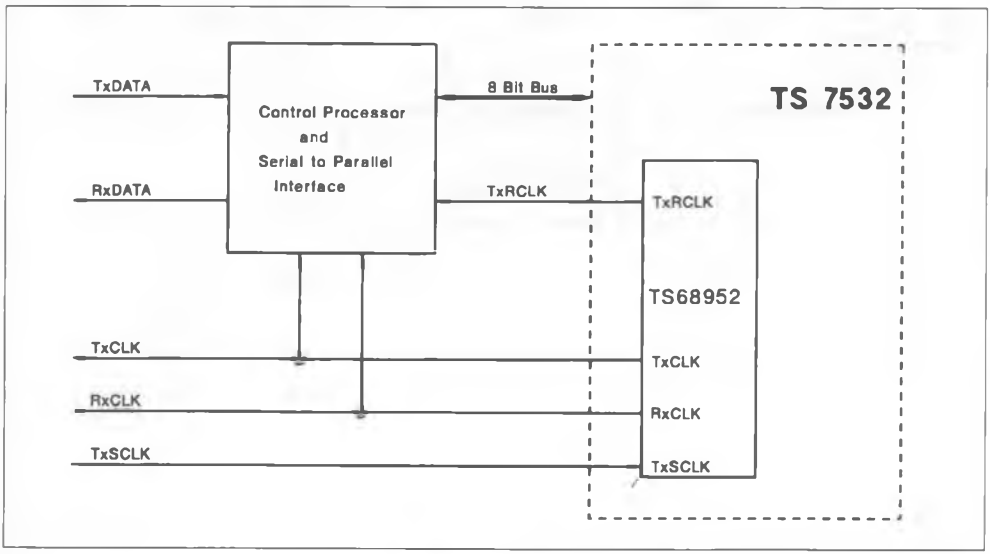
The combined near-end and far-end echo cancellers maintain the residual echo level 24 dB below the received signal even if the far-end echo signal path introduces up to 10 Hz of frequency offset. This level of cancellation is achieved when the far-end echo is 8 dB below the received far-end signal.

2.3.4. RECEIVER DESCRIPTION. The incoming signal is sent to the receiver interface chip to have the echo removed before being sent to DSP 2. The timing recovery algorithm takes the signal after the echo cancellation to derive the timing error to control the sampling phase of the A/D. It is able to cope with distant modem frequency drifts up to $\pm 2.10^{-4}$ as per CCITT rec. The A/D output samples are sent to the adaptive equalizer and the signal energy estimator for the gain control. The adaptive equalizer outputs a complex number every baud interval, which is then phase corrected by the carrier recovery loop. The Viterbi decoder makes hard decisions on the phase corrected samples for the adaptation of the equalizer and carrier recovery. It also makes soft decisions with an optimum decoding depth.

2.3.5. EQUALIZATION. The modem receiver has a passband T/3 fractionally spaced automatic adaptive equalizer which can compensate for the signal degradation caused by low quality line conditions.

2.3.6. SYNCHRONOUS AND ASYNCHRONOUS DATA TRANSFER. The V. 32 modem engine provides the control processor and the DTE with both the transmit and the receive bit clocks (Figure 3). These clocks are generated by the TS68952 and are independent of each other. The receive clock (RxCLK) is derived from the received data signal. The transmit clock (TxCLK) is free-running at the nominal bit rate (9600 or 4800 bps) except during Digital Loopback Mode when it is synchronous to the RxCLK. If the transmit clock is free-running and an external bit clock signal from the terminal is connected to point TxSCLK then the transmit bit clock will be synchronized to that signal. The baud clocks (TxRCLK and RxRCLK) are also available to the control processor. If the TxSCLK pin is not used, it should be tied to a fixed logic level.

Figure 3 : Clock Signals for Synchronous Transmission.



The control processor interface is synchronous with the transmit baud clock. Eight bits of data are transferred from the control processor to DSP 1 for each information exchange. At 9600 bps, the data is transmitted every 2 bauds and the data is transmitted every 4 bauds for 4800 bps. The received bits are also nominally transferred from DSP 1 to the control processor once every two transmit baud intervals. When the transmitter is not synchronized with the receiver, however, the receive baud interval may be slightly shorter or longer than the transmit baud interval. If it is shorter, it is necessary to periodically pass 16 received bits from DSP 1 to the control processor. If it is longer, then periodically, there will be no data transmitted from DSP 1 to the control processor. Since the received bits are being passed to the DTE at a fixed rate equal to the RxCLK, some buffering is necessary in the control processor.

For asynchronous transmission, the clocks are not required by the DTE. But since the control processor to DSP 1 interface is still synchronous with respect to the transmit baud clock, the control processor must implement the asynchronous to synchronous conversion (as specified in the V. 22 bis recommendation, for example). This will consist of inserting or deleting stop bits as required, to ensure that the transmitted bit rate is within 0.01 % of the nominal rate (9600 or 4800 bps).

2.3.7. TONE GENERATOR. The V.32 Engine has thirteen tone commands to quickly program the tone generators to generate the 2100 Hz Answer Tone (ANSWR) and the tone pairs for DTMF digits (DTMF0, ..., DTMF9, DTMF*, DTMF#). Silence, i.e. termination of tone generation, is accomplished by the use of a fourteenth command, SLNTS. These commands provide the tones and control required for normal operation of the modem.

Some circumstances might arise where additional tones are desired. For such cases, the V.32 Engine provides the user with the ability to generate such additional tones. This special feature is achieved through use of the tone control commands.

The V.32 Engine maintains a pair of locations which are reserved for tone generation parameters. These locations are denoted as TONE1 and TONE2. These locations may be programmed by the use of the define tone commands, DEFT1 and DEFT2. These commands provide the two tone generators with the phase increment of the tone to be generated with respect to the 7200 Hz sample rate.

The normal tone commands automatically program the tone generators. The DEFT1 and DEFT2 commands do not change the enabled or disabled state of the tone generators. If a tone is being generated when the DEFT command is received, the new tone will be generated without further action on the part of the user. If tone generation was not in progress it is not started.

Enabling the tone generators is accomplished by the tone control commands TGEN0, TGEN1, TGEN2, and TGEN12. Each of these commands affects both tone generators. TGEN0 disables both tone generators and TGEN12 enables both tone generators. To enable tone generator 1 and disable tone generator 2 the TGEN1 command is used. For the reverse condition, with generator 1 disabled and generator 2 enabled, the TGEN2 command is employed. if both tone generators are enabled, one of the tone levels can be scaled as specified by the control processor.

Refer to the command in appendix A for more detailed information.

Generation of special user tones is not part of the normal data communications operations of the modem. Use of this feature may interfere with data transfer operations. It is the responsability of the user to insure that the tone generators are used at a time when such interference will not occur and to disable both tone generators when the tone generation operations have been completed.

2.3.8. TEST MODES.The modem can be configured in two test modes, namely analog loop back and digital loop back modes. These loop back modes conform to the test loops 3 and 2 respectively defined in CCITT recommendation V.54.

In the local analog loop back mode, the transmitter signal is directly fed back into the local receiver input with the echo canceller enabled. The user is responsible for supplying a switch, which is controllable by the control processor, to enable or disable the analog loop back mode. The receiver descrambler is set as the inverse of the transmitter scrambler so that the receiver detects correct bits.

If the modem is configured in the digital loop back mode, the transmitter clock is locked to the receiver clock and the received bits are used as the transmitter input.

2.3.9. POWER ON INITIALIZATION. When the power is turned on, the transmitter interface sets the output signal attenuation to infinite. This avoids undesirable signal transmission on the telephone line [see ref 5 of Appendix D]. The gain of the AGC in the receive interface is set at the lowest level to avoid signal clipping during the initial handshake. The clock generator is programmed to generate all the necessary clocks for the 9600 bps mode. The clocks include the 7200 Hz sampling clock, the 2400 Hz baud rate clocks and the 9600 bps bit rate clocks. The

transmit clocks are free running when the TxSClk pin is tied to a fixed logic level. Otherwise, the transmit bit clock is synchronized to the frequency present at the TxSClk pin. DSP 1 is configured properly to receive commands from the control processor.

2.4. MODEM INTERFACE [Figure 4]

2.4.1. ANALOG INTERFACE. The transmit signal at the tip and ring is programmable over a 22 dB dynamic range by 2 dB steps in TS68950. The signal level can be further scaled to any value by setting a scaling factor in the DSP. The nominal Transmit level, at the ATO pin is – 5.7 dBm.

2.4.2. DIGITAL INTERFACE. The DSP and control processor interface complies with the system bus interface of the TS68930. The interface to the control processor is managed by DSP 1 as shown in Figure 1. The DSP signals which are presented to the interface, and a brief definition of the signals are tabulated in table 1.

Table 1 : Digital Interface Signals.

Interface Signals	Signal Definition
D0H	Data Bus (LSB)
D1H	Data Bus
D2H	Data Bus
D3H	Data Bus
D4H	Data Bus
D5H	Data Bus
D6H	Data Bus
D7H	Data Bus (MSB)
RWL	Write Signal
DSL	Data Strobe
INTL	Mailbox Handshake
CSL	DSP Select
RSL	Register Select
TxRCLK	Transmit baud rate clock
RxRCLK	Receive baud rate clock
TxCLK	Transmit bit rate clock
RxCLK	Receive bit rate clock
TxMCLK	Transmit multiplex clock
RxMCLK	Receive multiplex clock
TxSCLK	Transmit terminal clock

All information exchanges across this interface conform to the three byte mailbox structure [see ref 4 of Appendix D] and protocol of the DSP. As may be seen in the table, the DSP generates a control signal, INTL, which defines the mailbox handshake operation.

2.4.3. CONTROL PROCESSOR/DSP INTERFACE. As seen by the software in the user provided control processor, DSP 1 is a synchronous machine. It requires the attention of the control processor at regular intervals in order to perform properly. Any failure of the control processor to interact with the modem engine in a timely manner will result in reduced performance or improper operation.

Each interaction begins when the control processor sends a three byte command to the mailbox. Once the command has been written to the mailbox, the ownership of the mailbox is relinquished by the control processor. Upon acquisition of the mailbox, DSP 1 reads the command bytes and then sends a three byte response to the mailbox. Then, DSP 1 relinquishes the ownership of the mailbox back to the control processor. The received command is then decoded and the embedded data and/or operational parameters are extracted and acted upon as appropriate. The modem status information will be collected for the next mailbox exchange. The control processor handles the returned information as soon as it regains the ownership of the mailbox.

Because the control processor owns the mailbox initially, it may store a command at any time before it is required by DSP 1. After this, the mailbox becomes available to DSP1 and can be read by it when required.

2.4.4. MAILBOX DESCRIPTION.The mailbox located internally to the DSP contains 3-byte input (RIN) and 3-byte output (ROUT) shift registers. The DSP has an internal flag RDYOIN which indicates whether the DSP (RDYOIN = 0) or control processor (RDYOIN = 1) has access to the mailbox. The DSP can relinquish its accessability to the mailbox by setting RDYOIN but it can no longer regain access to the mailbox as RDYOIN is reset only after the control processor relinquishes its accessability to the mailbox. The access protocol and system bus transfers are controlled by an internal I/O sequencer within the DSP described as follows :

1. The mailbox is made available to the control processor by the DSP program which sets RDYOIN flag to 1. This action will cause INTL mailbox handshake signal to switch to the active (low) state.

2. The control processor detects INTL active and dummy reads the mailbox by forcing DSP Select (CSL) and Register Select (RSL) low along with write signal (RWL) high. The activated Data Strobe signal (DSL = 0) validates the above signals.

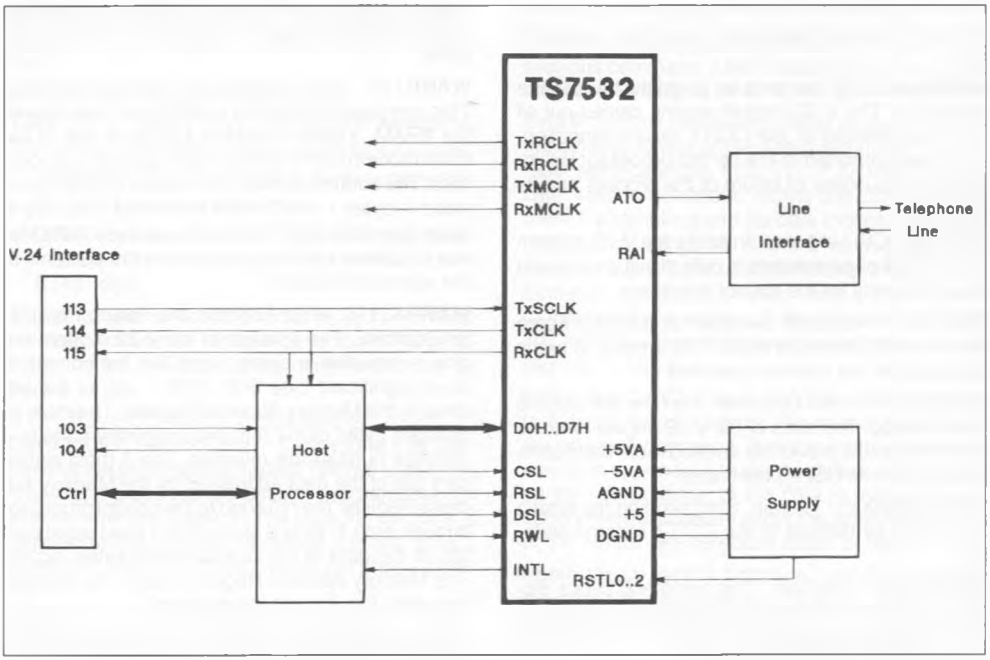
3. The DSP detects the dummy read of its mailbox via the control signals mentioned in 2 and negates INTL mailbox handshake signal within 800 ns.

4. The control processor detects the negation of INTL indicating that the DSP mailbox is available for data transfers. The control processor writes

three 8-bit bytes and/or reads three 8-bit bytes in the mailbox shift registers RIN, ROUT respectively.

5. The exchange protocol described above is terminated by the control processor performing a dummy read of the mailbox as in 2 but with RSL in the high state.
6. The RDYOIN flag within the DSP is cleared to 0 by the dummy read of the mailbox in step 5 and the DSP now has access to RIN and ROUT registers within the mailbox.

Figure 4 : Functional Interconnect Diagram.



3. USER INTERFACE - COMMAND SET

The command set has the following attractive features :

- user friendly with easy to remember mnemonics
- allows straightforward expansion with new commands to suit specific customization requirements
- fully compatible with other SGS-THOMSON DSP-based modem products.

The command set has been designed to provide the necessary functional control of the V.32 Engine. Each command falls into one of several groups, based on function and the presence or absence of parameters. The length of the OP code varies with instruction type, but in all cases, a command consists of three bytes.

The commands which pass parameters or data to DSP 1 have a short OP code format. Byte 0 forms the OP code portion of the command. Bytes 1 and 2 are data and/or parameters associated with each OP code. The meaning of the last two bytes is dependent on the specific instruction.

Other instructions command the V.32 Engine to perform certain specific tasks. These do not pass parameters or data to the V.32 Engine. These commands have an OP code which is a full 24 bits in length.

The command set of the V.32 Engine is summarized below. The descriptions are of the form :

MNEMONIC (OPCODE) : DESCRIPTION.

For detailed information and data format specifics of each command, please refer to appendix A.

3.1. COMMAND SUMMARY

3.1.1. OPERATIONAL CONTROL COMMANDS.

FREZ (14) : Freeze adaptive processes. Freeze the adaptive processes as specified by the data in bits 0 and 1 of byte 1. Bit 0 of byte 1 controls the adaptive equalizer. Freeze the equalizer if bit 0 of byte 1 is 1. A 0 in this bit will unfreeze the equalizer. Echo canceller adaptation is controlled by bit 1 of byte 1. if bit 1 is 1, the echo canceller adaptation is frozen. The echo canceller adaptation is unfrozen by a 0 in bit 1.

HSHK (040000) : Handshake. Begin the handshake sequence. The V.32 modem engine carries out all the steps defined in the CCITT recommendation. The status reported to the control processor will indicate the success or failure of the process and its progress.

INIT (0600C0) : Initialize. Initialize the V.32 modem engine. Set all parameters to default values and wait for commands for the control processor.

JMP (06) : Force code execution at address. Force the selected processor of the V.32 Engine to begin execution at the address specified.

NOP (000000) : No Operation. No new operation is commanded. The state of the V.32 engine remains unaltered and a previously invoked multi-baud command (such as HSHK) continues.

RTRA (050000) : Retrain. Start sending the retrain sequence as defined in the CCITT recommendation.

SETGN (02) : Set Gain. This command sets a global gain factor, which will be multiplied by all transmit samples before being sent to the TS68950. Bytes 1 and 2 store the gain factor.

3.1.2. DATA COMMUNICATIONS COMMANDS.

XMIT (03) : Transmit data. Transmit data to far end modem. The data is provided in byte 1 of the command, where the least significant bit is the first bit to be transmitted. The third byte of the command must be provided, but is not used. Hence, any value may be supplied.

XMITI (01) : Transmit data and Initiate additional cycle. Transmit data and inform the DSP to accept another command at the next transmit baud. If the next command requires an answer from DSP 1, the control processor has to keep issuing this command followed by a command which does not requires an answer until the answer has been received.

3.1.3. MEMORY. MANIPULATION COMMANDS.

SPAC (13) : Store Parameter And Count. Store parameter in addressed memory and increment the pointer. This command passes data in bytes 1 and 2, least significant byte in byte 1. It is used to write an arbitrary 16-bit value into the writable memory location currently specified by the Memory Address Register. The contents of the Memory Address Register are incremented by 1 at the completion of this command.

SPAM (12) : Store parameter in Addressed Memory. This command passes data in bytes 1 and 2, least significant byte in byte 1. It is used to write an arbitrary 16-bit value into the writable momory location currently specified by the Memory Address Register.

WARP (10) : Write Address and Return Parameter. This command allows the controller to read any of the XRAM, YRAM, ERAM or CROM of any of the three modem DSPs without interrupting the processors. The address to the V.32 modem engine is provided in bytes 1 and 2 of the command (least significant byte first). DSP 1 stores the address in the Memory Address Register and returns the contents of the addressed location.

WARPX (11) : Write Address and Return Parameter Complex. The address to the V.32 modem engine is provided in bytes 1 and 2 of the command (least significant byte first). DSP 1 stores the address in the Memory Address Register. The most significant bytes of the real and imaginary parts of a complex number are returned. The 8 most significant bits of the data addressed by the Memory Address Register are returned to the control processor through byte 1. Byte 2 stores the 8 most significant bits of the data at the location immediately higher. The Memory Address Register retains the address provided. (i.e. it is not incremented.)

3.1.4. CONFIGURATION CONTROL COMMANDS

CV32 (20) : Configure modem for V.32. Configure the modem as Originate / Answer, 9600/4800, Viterbi / No-Viterbi, Analog Loopback, Digital Loopback.

CV29 (21) / CV27T (22) / CV26T (23) / CV23 (24) / CV22B (25) / CV21 (26) / CB212 (27) / CB103 (28) / CGRP2 (29) : Configure the modem to the basic operating mode specified, as well as Originate/Answer, 9600/4800, Analog Loopback, Digital Loopback. These commands are not supported by the V.32 Engine. They are listed here only for reference (i.e. for future upgrade or other product).

3.1.5. MAFE MANIPULATION COMMANDS.

CMAFE (07) : Configure MAFE. The following two bytes of this command are written directly to the MAFE chip set (TS68950/1/2). This allows the control processor to configure parameters, such as the transmit level, the receiver analog front end, and the transmit and receive clocks.

RRR1 (080000) : Read Register 1. Causes the V.32

Engine to read and immediately return the 12 bit contents of the MAFE register RR1.

RRR2 (090000) : Read Register 2. Causes the V.32 Engine to read and immediately return the 12 bit contents of the MAFE register RR2.

WTR1 (0A) : Write Register 1. Causes the V.32 Engine to write the supplied data to the MAFE register TR1.

WTR2 (0B) : Write Register 2. Causes the V.32 Engine to write the supplied data to the MAFE register TR2.

3.1.6. TONE SELECT COMMANDS.

TONE (0C) : Select Tone. Program the tone generator(s) for the desired tone(s). Examples include :

- **ANSWR** (0C1000) : Program the tone generator for the 2100 Hz answer tone.
- **DTMF** (see appendix) : Program the tone generators for the tone pair which forms the specified DTMF digit.

This command selects the tones to be transmitted, but does not enable the tone generators. To transmit the tones, the tone control commands must be issued.

3.1.7. TONE CONTROL COMMANDS

DEFT1 (0E) : Define Tone 1. Define tone 1 as specified by the parameter provided. The two data bytes following the opcode are used to program, but not enable, tone generator 1. The data for the tone is represented as a phase offset per sample. Byte 1 stores the least significant byte of the phase increment.

DEFT2 (0F) : Define Tone 2. Define tone 2 as specified by the parameter provided. The two data bytes following the opcode are used to program, but not enable, tone generator 2. The data for the tone is represented as a phase offset per sample. Byte 1 stores the least significant byte of the phase increment.

SLNT (0D0000) : Silence the tone generators. Discontinue tone transmissions by disabling the tone generators.

TGEN (0D) : Tone Generator control. Enable or disable tone generator 1 and tone generator 2 according to parameter provided. If both tone generators are enabled, the level of tone 2 is 2 dB higher than that of tone 1. However, the user can change the relative levels by modifying the amplitude level of both tone generators.

3.2. STATUS REPORTING

Whenever DSP 1 owns the mailbox, it transmits the modem status to the control processor. The status consists of three bytes of information which are stored by DSP 1 in its ROUT register for access by the control processor. These three bytes may consist of received bits and modem status or they may contain the answers to the previous command, such as WARP and RRR1/2.

Data bits have higher priority than the answer to the previous command. If both data byte and command answer are ready to be sent, the data will be sent.

Byte 0 contains status flags. Refer to appendix B for the detailed format of the status response. The four most significant bits, F00, F01, F10 and F11, indicate various conditions during the call establishment, handshaking and the data modes. They have different meanings in different modes. The flag DAV1 and DAV2 are used to indicate the type of information contained in bytes 1 and 2. Bit H is used to indicate the condition of the handshake and bit 107 informs the control processor whether the 107 flag has to be set.

DAV1 and DAV2. If both DAV1 and DAV2 are set to 1, bytes 1 and 2 contain the data in response to the previous command. Refer to the relevant commands in appendix A to get the detailed information on the interpretation of the data in bytes 1 and 2. Otherwise, they contain either the received data bits or the handshake detection status or both.

If both bits are set to 0, both byte 1 and byte 2 contain the data bits, where the bits in byte 1 are received earlier in time. The least significant bit is the first bit received. The data bits are stored in byte 1 and the modem status is stored in byte 2 when DAV2 is 1 and DAV1 is 0. When DAV1 is 1 and DAV2 is 0, the control processor should ignore the data in byte 1 and get the detection status from byte 2.

During handshake operations the V.32 Engine reports the detection status regularly. When the rate sequence is received, it will be transferred in byte 1 of the response. Each bit in byte 2 indicates the detection of a specific event in the training sequence. It has different meanings for call and answer modems. For detailed information, refer to appendix B. During the data mode, byte 2 is always provided, but is used only when there are two bytes of data to transmit. This occurs occasionally when the receiver clock is running faster than the transmitter clock.

F00-F11 bits. During the call establishment operation, the V.32 Engine reports call progress tones through the F01 and F00 flags. F00 is set to 1 when the signal energy in frequency band 1 is above the threshold level. F01 is set to 1 when the signal energy in band 2 is above the threshold level. Detection of the 2100 Hz answer tone is indicated by setting the F10 flag to a 1.

During handshake operations, all four bits are used to indicate the line condition and some detection results. F00 is set to 0 if the line quality is good and 1 if it is bad. F01 is set to 1 if any segment in the training sequence is not detected within a time out. This bit can be used to indicate a non V.32 detection if either AA is not detected in the answer modem or the AC is not detected in the call modem. Both F00 and F01 are set to 1 when an illegal mode or a GSTN cleardown is received in the rate sequence.

The detection of the rate sequence is reported in the flags F11 and F10. When the modem is operating at 9600 bps without trellis coding, these bits are both set to 0. With trellis coding at 9600 bps, F11 is set to 1 and F10 is cleared to 0. For 4800 bps, 0 and 1 will be placed in F11 and F10, respectively. When both F11 and F10 are set to 1, the modem has negotiated with the far end modem and determined that the maximum negotiated operating speed is 2400 bps.

During data mode, the perceived line quality is reported in the flags F01 and F00. The line conditions are reported as either good (code 00), poor (code 01), or terrible (code 10). The code 10 should be interpreted as a local modem retrain request. Upon receipt of this code, the controller can issue the RTRA command to begin the retrain procedure. The code 11 is used when the remote modem begins a retrain sequence. The control processor is then responsible for manipulating the appropriate data communications interface signals.

H and 107 bits. When the V.32 Engine is commanded to perform the CCITT handshake sequence, the H bit will be set to 1 for the duration of the handshake operation. At the successful completion of the handshake operation the H flag will go to 0 and the control processor is then responsible for manipulating the appropriate data communications interface signals. e.g. 106 and 109. The 107 flag is set to a 1 to indicate that the controller should assert signal 107 on the data communications interface.

3.3. COMMAND LIST

OPERATIONAL CONTROL COMMANDS

Command Mnemonic	OP Code (HEX)	Description
uFzec	170000	Unfreeze Echo Canceller
Frezq	1B0000	Freeze the Equalizer Adaptation
Frezc	160000	Freeze the Echo Canceller Adaptation
uFzeq	1C0000	Unfreeze Equalizer
hshk	040000	Handshake with Other Modem
init†	0600C0	Initialize Modem
jmp†	06	Force Code Execution
nop	000000	No Operation
rtra	050000	Retrain
setgn†	02	Set the Scaling Factor for the Transmitter

DATA COMMUNICATIONS COMMANDS

Command Mnemonic	OP Code (HEX)	Description
xmit	03	Transmit Data
xmiti†	01	Transmit Data and Initiate Additional Transfer

† Future enhancement or other product reference.

MAFE MANIPULATION COMMANDS

Command Mnemonic	OP Code (HEX)	Description
cmafe†	07	Configure MAFE Chipset
rrr1†	080000	Read MAFE Reg RR1
rrr2†	090000	Read MAFE Reg RR2
wtr1†	0A	Write MAFE Reg TR1
wtr2†	0B	Write MAFE Reg TR2

TONE SELECT COMMANDS

Command Mnemonic	OP Code (HEX)	Description
answ	0C1000	Select 2100 Hz Answer Tone
dtmf 0	0C0000	Select DTMF Digit 0
dtmf 1	0C0100	Select DTMF Digit 1
dtmf 2	0C0200	Select DTMF Digit 2
dtmf 3	0C0300	Select DTMF Digit 3
dtmf 4	0C0400	Select DTMF Digit 4
dtmf 5	0C0500	Select DTMF Digit 5
dtmf 6	0C0600	Select DTMF Digit 6
dtmf 7	0C0700	Select DTMF Digit 7
dtmf 8	0C0800	Select DTMF Digit 8
dtmf 9	0C0900	Select DTMF Digit 9
dtmf *	0C0E00	Select DTMF Digit *
dtmf #	0C0F00	Select DTMF Digit #
tone	0C	Select Tone (s)

CONFIGURATION CONTROL COMMANDS

Command Mnemonic	OP Code (HEX)	Description
cv32	20	Configure Modem for V.32
cv29†	21	† Configure Modem for V.29
cv27t†	22	† Configure Modem for V.27t
cv26t†	23	† Configure Modem for V.26t
cv23†	24	† Configure Modem for V.23
cv22B†	25	† Configure Modem for V.22 / V.22 bis
cv21†	26	† Configure Modem for V.21
cb212†	27	† Configure Modem for Bell 212
cb103†	28	† Configure Modem for Bell 103
cgrp2†	29	† Configure Modem for Group 2 Fax

MEMORY MANIPULATION COMMANDS

Command Mnemonic	OP Code (HEX)	Description
spac†	13	Write MEM and Increment MEM Pointer
spam†	12	Write MEM
warp†	10	Write MEM Pointer & Read MEM
warpx†	11	Write MEM Pointer & Read MEM & MEM + 1

† Future enhancement or other product reference.

TONE CONTROL COMMANDS

Command Mnemonic	OP Code (HEX)	Description
deft1†	0E	Define Tone 1
deft2†	0F	Define Tone 2
slnt	0D0000	Transmit no Tone
tgen 0	0D0000	Tone Generators Disabled
tgen 1†	0D0100	Tone Generator 1 Enabled
tgen 2†	0D0200	Tone Generator 2 Enabled
tgen 3	0D0300	Tone Generators 1 & 2 Enabled

4. ELECTRICAL SPECIFICATIONS

4.1. MAXIMUM RATINGS :

TS75320/1/2

Symbol	Parameter	Value	Unit
V_{CC}*	Supply Voltage	– 0.3 to 7.0	V
V_{in}*	Input Voltage	– 0.3 to 7.0	V
T_A	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

* With respect to V_{SS}.

Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

TS68950/1/2

Symbol	Parameter	Value	Unit
	Supply Voltage between V + and AGND or DGND	– 0.3 to + 7	V
	Supply Voltage between V - and AGND or DGND	– 7 to + 0.3	V
	Voltage between AGND and DGND	– 0.3 to + 0.3	V
	Digital Input Voltage	DGND – 0.3 to V_{CC}^+ + 0.3	V
	Digital Output Voltage	DGND – 0.3 to V_{CC}^+ + 0.3	V
	Digital Output Current	– 20 to + 20	mA
	Analog Input Voltage	V_{CC}^- – 0.3 to V_{CC}^+ + 0.3	V
	Analog Output Voltage	V_{CC}^- – 0.3 to V_{CC}^+ + 0.3	V
	Analog Output Current	– 10 to + 10	mA
	Power Dissipation	500	mW
T_{oper}	Operating Temperature	0 to + 70	°C
T_{stg}	Storage Temperature	– 65 to + 150	°C

4.2. DC ELECTRICAL CHARACTERISTICS DGND = AGND = 0 V

Digital Supply

V_{CC} = 5.0 V ± 5 %, V_{SS} = 0, T_A = 0 to + 70°C (Unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IL}	Input Low Voltage	– 0.3		0.8	V
V_{IH}	Input High Voltage	2.4		V_{CC}	V
I_i	Input Extal Current	– 50		+ 50	µA
I_{in}	Input Leakage Current	– 10		10	µA
V_{OH}	Output High Voltage (I_{load} = – 300 µA) except $\overline{DTACK}$	2.7			V
V_{OL}	Output Low Voltage (I_{load} = 3.2 mA)			0.5	V
P_D	Total Power Dissipation		4.5	6.6	W
C_{in}	Input Capacitance		10		pF
I_{TSI}	Three State (off state) Input Current (0.4 V - 2.4 V)	– 20		– 20	µA
T_{amb}	Operating Temperature (note 1)	0		70	°C
$R_{\theta JA}$	Thermal Resistance Junction-ambient		28		°C/W

Note 1 : Case temperature T_C must be maintained below 100 °C.

Analog Supply

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+	Positive Power Supply	4.75		5.25	V
V^-	Negative Power Supply	– 5.25		– 4.75	V
I^+	Positive Supply Current			35	mA
I^-	Negative Supply Current	– 35			

4.3. AC ELECTRICAL SPECIFICATIONS

4.3.1. CLOCK AND CONTROL PINS TIMING

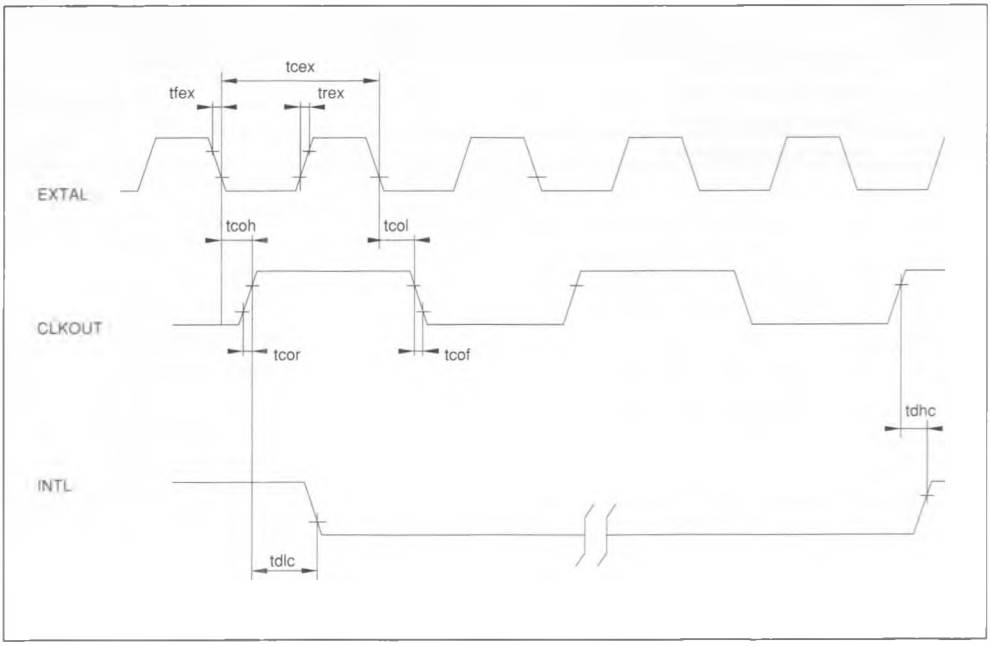
(V_{CC} = 5.0 V ± 5 %, T_A = 0° to + 70°C, see figure 5)
OUTPUT LOAD = 50 pF + DC characteristics I load

REFERENCE LEVELS : AC TESTING INPUTS ARE DRIVEN AT 2.4 V FOR A LOGIC "1" AND 0.4 V FOR A LOGIC "0".TIMING MEASUREMENTS ARE MADE AT 1.5 V FOR BOTH A LOGIC "1" AND "0".

tr, tf ≤ 5 ns for i nput signal

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{cex}	External Clock Cycle Time		40		ns
t_{fex}	External Clock Fall Time			5	ns
t_{rex}	External Clock Rise Time			5	ns
t_{coh}	EXTAL to CLKOUT High Delay		25		ns
t_{col}	EXTAL to CLKOUT Low Delay		25		ns
t_{cor}	CLKOUT Rise Time			10	ns
t_{cof}	CLKOUT Fall Time			10	ns
t_{dlc}	CLKOUT to Control Output Low (INTL)			50	ns
t_{dhc}	CLKOUT to Control High (INTL)			50	ns

Figure 5 : Clock and Control Pins Timing.



4.3.2. TS68952 : Clock Generator

CLRYSTAL OSCILLATOR INTERFACE

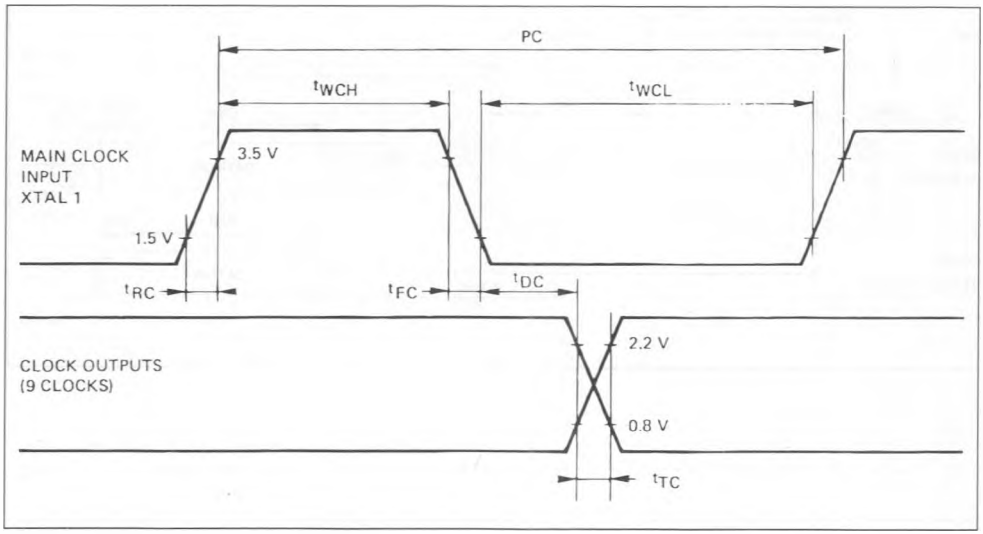
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level Voltage				1.5	V
V_{IH}	Input High Level Voltage		3.5			V
I_{IL}	Input Low Level Current	$DGND \leq V_I \leq V_{IL\ max}$	–15			µA
I_{IH}	Input High Level Current	$V_{IH\ min} \leq V_I \leq V^+$			15	µA

CLOCK WAVE FORMS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
PC	Main Clock Period	XTAL1 Input	150	173.6		ns
t_{WCL}	Main Clock Low Level Width	XTAL1 Input	50			ns
t_{WCH}	Main Clock High Level Width	XTAL1 Input	50			ns
t_{RC}	Main Clock Rise Time	XTAL1 Input			50	ns
t_{FC}	Main Clock Fall Time	XTAL1 Input			50	ns
t_{DC}	Clock Output Delay Time	All Clock Outputs CL=50 pF			500	ns
t_{TC}	Clock Output Transition Time	All Clock Outputs CL=50 pF			100	ns

Unless otherwise noted, electrical characteristics are specified over the operating range. Typical values are given for $V^+ = 5.0$ V and $t_{amb} = 25$ C.

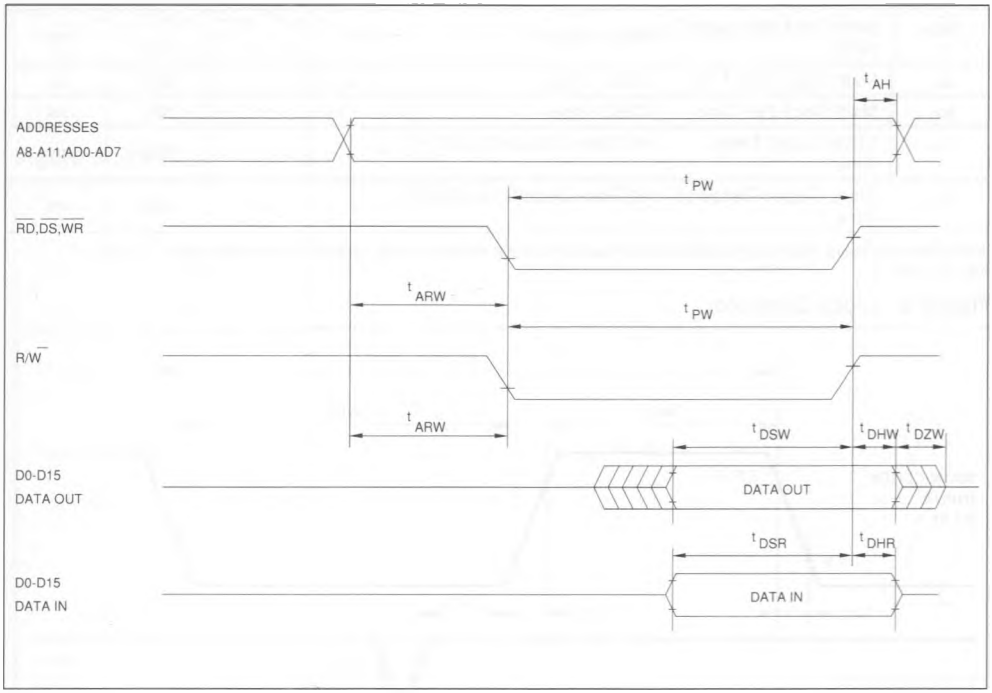
Figure 6 : Clock Generator.



4.3.3.LOCAL BUS TIMING
(V_{CC} = 5.0 V ± 5 %, T_A = 0° to + 70°C, see figure 7)

Symbol	Parameter	Min.	Max.	Unit
t_{PW}	$\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Pulse Width	1/2 tc – 15	1/2 tc	ns
t_{AH}	Address Hold Time	10		ns
t_{DSW}	Data Set-up Time, Write Cycle	25		ns
t_{DHW}	Data Hold Time, Write Cycle	10		ns
t_{DZW}	$\overline{DS}$ High to Data High Impedance, Write Cycle		40	ns
t_{DSR}	Data Set-up Time, Read Cycle	20		ns
t_{DHR}	Data Hold Time, Read Cycle	5		ns
t_{ARW}	Address Valid to $\overline{WR}$, $\overline{DS}$, $\overline{RD}$ Low	1/2 tc – 40		ns

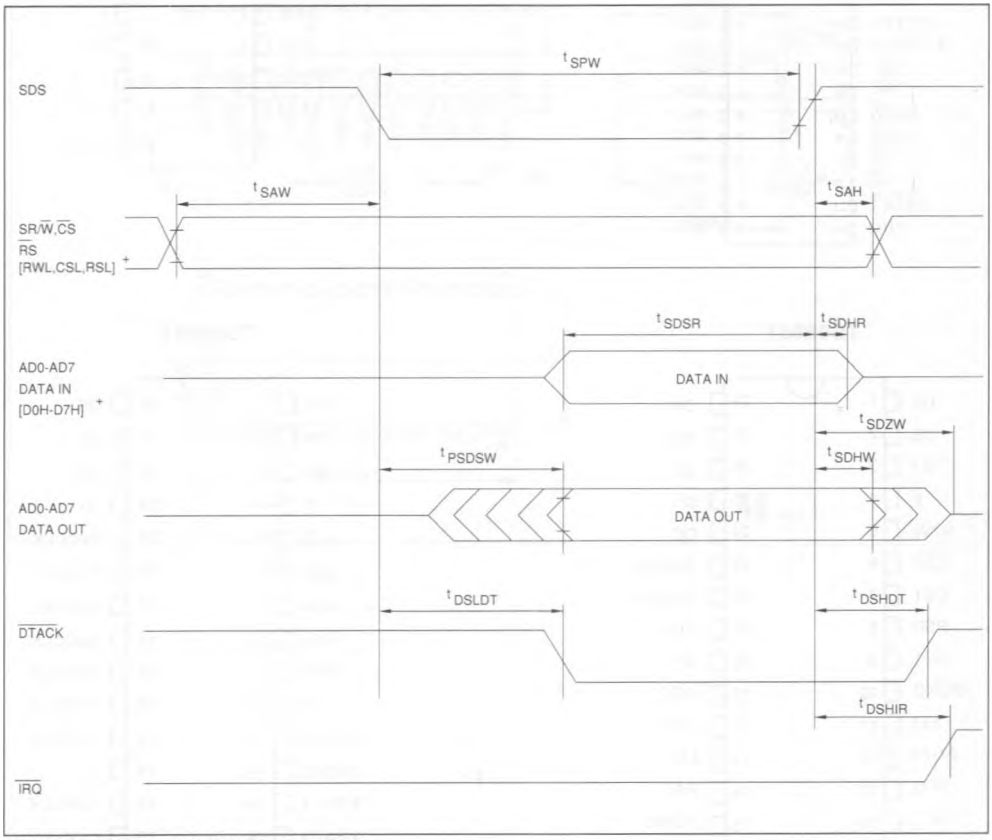
Figure 7 : Local Bus Timing Diagram.



4.3.4. SYSTEM BUS TIMING
(V_{CC} = 5.0 V ± 5 %, T_A = 0° to + 70°C, see figure 8)

Symbol	Parameter	Min.	Max.	Unit
t_{SPW}	$\overline{SDS}$ Pulse Width	60		ns
t_{SAW}	SR / $\overline{W}$, $\overline{CS}$, $\overline{RS}$ Set-up Time	20		ns
t_{SAH}	SR / $\overline{W}$, $\overline{CS}$, $\overline{RS}$ Hold After $\overline{SDS}$ High	5		ns
t_{SDSR}	Data Set-up Time, Read Cycle	20		ns
t_{SDHR}	Data Hold Time, Read Cycle	5		ns
t_{SDSW}	Data Set-up Time, Write Cycle		35	ns
t_{SDHW}	Data Hold Time, Write Cycle	10	50	ns
t_{DSHIR}	$\overline{SDS}$ High to $\overline{IRQ}$ High		800	ns
t_{SDZW}	$\overline{SDS}$ High to Data High Impedance, Write Cycle		40	ns

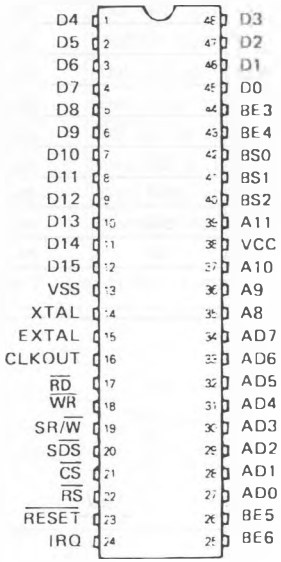
Figure 8 : System Bus Timing Diagram.



+ Note : Signal names on Host Processor Interface.

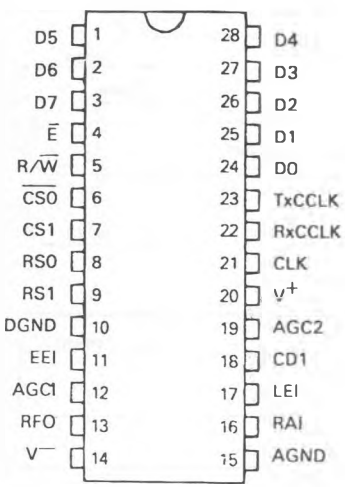
5. PIN CONNECTIONS

TS75320 - TS75321 - TS75322

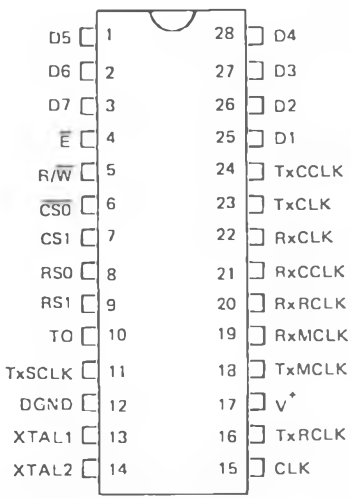


TS68950

TS68951



TS68952



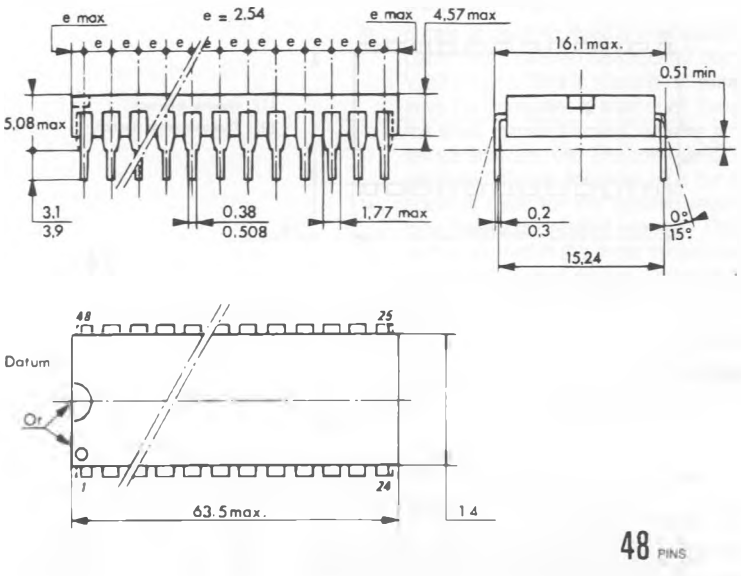
6. ORDERING INFORMATION

Part Number	Temperature Range	Package
TS75320CP	0 °C to + 70 °C	DIP48
TS75321CP	0 °C to + 70 °C	DIP48
TS75322CP	0 °C to + 70 °C	DIP48
TS68950CP	0 °C to + 70 °C	DIP24
TS68951CP	0 °C to + 70 °C	DIP28
TS68952CP	0 °C to + 70 °C	DIP28

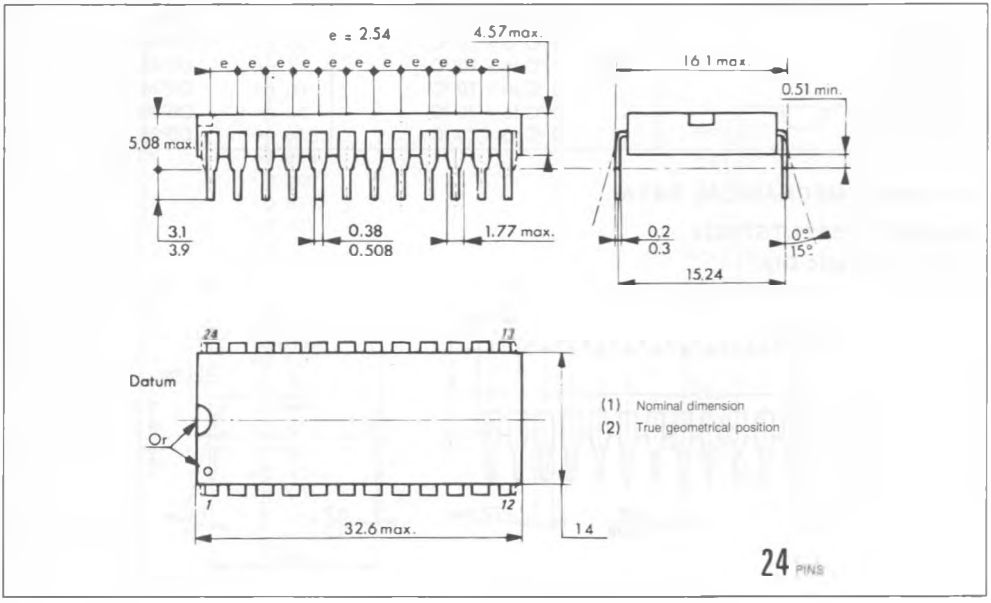
7.PACKAGE MECHANICAL DATA

TS75320/TS75321/TS75322

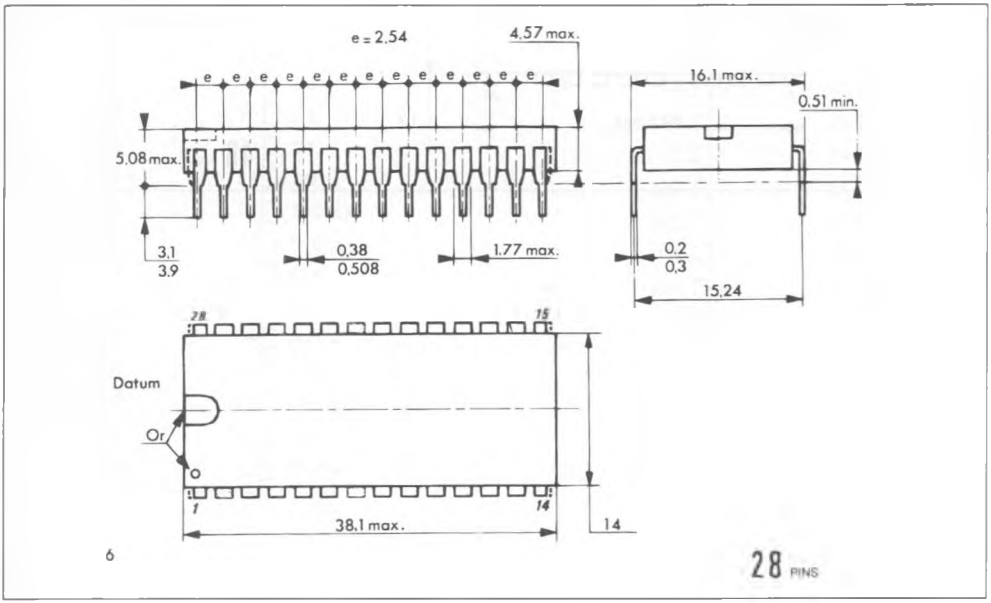
48 Pins - Plastic Dip.



TS68950
24 Pins - Plastic Dip.



TS68951/TS68952
28 Pins - Plastic Dip.



APPENDIX A
COMMAND SET DESCRIPTION

cmafe† - configure the TS68950/1/2 components of the V.32 Engine

INSTRUCTION TYPE
MAFE manipulation command

OPCODE
07

SYNOPSIS
cmafe address register code data

DESCRIPTION
cmafe is used to directly manipulate the operating parameters of the TS68950/1/2 components of the V.32 Engine. This is a low level command which allows the controller to alter such things as the transmit level, transmit timing, receive timing, and receiver parameters, etc. The command consists of a single byte OPcode followed by a byte containing the address code for the desired register and a data byte for the addressed register. The data bytes will be transferred in the order received and interpreted by the addressed device. Refer to the data sheets of the TS68950, TS68951, and TS68952 for programming specifics.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	1	1	1

BYTE 1 DEFINITION

R	R	R	0	0	0	0	0

REG CODE (Refer to TS68950 Data Sheet)

BYTE 2 DEFINITION

*	*	*	*	*	*	*	*

DATA BYTE (Refer to TS68950 Data Sheet)

APPENDIX A

cv32 - configure the V.32 Engine

INSTRUCTION TYPE
configuration control command

OPCODE
20

SYNOPSIS
cv32 speed ec orig atn al dl fc

DESCRIPTION
cv32 is used to alter the operating parameters of the V.32 Engine. The passed parameters provide a two bit speed code which selects the desired baud rate. Another parameter explicitly turns on or off the echo canceller. If the V.32 Engine is to operate in the originate mode, the orig parameter must be set. When this parameter is not set, the V.32 Engine is configured as an answer mode device. The al and dl parameters allow the user to select between the analog and digital loopback test conditions, respectively. The transmit attenuation level is selected by the atn parameter. etc.

BYTE 0 DEFINITION (OP CODE)

0	0	1	0	0	0	0	0

BYTE 1 DEFINITION

RSV	RSV	FC	EC	AL	SP1	SP0	ORIG

SPEED CODE
SP1-0
00 : 9600 bps
01 : 4800 bps
11 : 2400 bps

FLAG	BIT	DEFINITION
FC	0/1	Do not/Do force cleardown
EC†	0/1	Echo Canceller off/on
ORIG	0/1	Answer mode / Originate mode
AL†	0/1	Analog Loopback test disabled / enabled
RSV	-	Reserved

BYTE 2 DEFINITION

ATN3	ATN2	ATN1	ATN0	DL	RSV	RSV	RSV

FLAG	BIT	DEFINITION
DL†	0/1	Digital Loopback test disabled/ enabled
ATN3-0†		Transmit attenuation 0 dB to 22 dB : codes 0000 to 1011 in 2 dB steps Infinite : codes 1100 to 1111
RSV	-	Reserved

APPENDIX A

deft1† - define tone 1

INSTRUCTION TYPE
tone control command

OPCODE
0E

SYNOPSIS
deft tone descriptor

DESCRIPTION
deft1 is a command which used to program tone generator 1. The 16 bit value provided is used as the phase offset per sample for the generator. The deft1 command does not enable the tone generator. See also tgen.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	1	1	0

BYTE 1 DEFINITION

P7	P6	P5	P4	P3	P2	P1	P0

LOW BYTE OF DESCRIPTOR.

BYTE 2 DEFINITION

P15	P14	P13	P12	P11	P10	P9	P8

HI BYTE OF DESCRIPTOR.

deft2† - define tone 2

INSTRUCTION TYPE
tone control command

OPCODE
0F

SYNOPSIS
deft tone descriptor

DESCRIPTION
deft2 is a command which used to program tone generator 2. The 16 bit value provided is used as the phase offset per sample for the generator. The deft2 command does not enable the tone generator. See also tgen.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	1	1	1

BYTE 1 DEFINITION

P7	P6	P5	P4	P3	P2	P1	P0

LOW BYTE OF DESCRIPTOR.

BYTE 2 DEFINITION

P15	P14	P13	P12	P11	P10	P9	P8

HI BYTE OF DESCRIPTOR.

APPENDIX A

frzc - Freeze the echo canceller adaptation

INSTRUCTION TYPE
operational control command

OPCODE
160000

SYNOPSIS
frzec

DESCRIPTION
frzec causes the V.32 Engine to enable or disable the adaptation of the echo canceller, to the current parameter.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	0	1	1	0

BYTE 1 DEFINITION

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION

0	0	0	0	0	0	0	0

frezq - Freeze the equalizer adaptation

INSTRUCTION TYPE
operational control command

OPCODE
1B0000

SYNOPSIS
frzezq

DESCRIPTION
frzezq causes the V.32 Engine to disable the adaptation of the equalizer.

BYTE 0 (OP CODE)

0	0	0	1	0	1	1	0

BYTE 1 DEFINITION

0	0	0	0	0	0	C	0

BYTE 2 DEFINITION

0	0	0	0	0	0	0	0

APPENDIX A

hshk - begin handshake sequence

INSTRUCTION TYPE
operational control command

OPCODE
040000

SYNOPSIS
hshk

DESCRIPTION
hshk is used to command the V.32 Engine to begin the handshake sequence processing. The progress of the handshake is reported to the control processor along with the data bits. For detailed information, refer to appendix B.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	1	0	0

BYTE 1 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

APPENDIX A

init† - Initialize the V.32 Engine

INSTRUCTION TYPE
operational control command

OPCODE
0600C0

SYNOPSIS
init

DESCRIPTION
init forces the V.32 Engine to reset all parameters to their default conditions and restart operations.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	1	1	0

BYTE 1 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

1	1	0	0	0	0	0	0

jmp† - force code execution at address

INSTRUCTION TYPE
operational control command

OPCODE
06

SYNOPSIS
jmp processor code address

DESCRIPTION
jmp forces the selected processor of the V.32 Engine to begin execution at the address specified.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	1	1	0

BYTE 1 DEFINITION

A7	A6	A5	A4	A3	A2	A1	A0

ADDRESS LOW

BYTE 2 DEFINITION (OP CODE)

P1	P0	0	0	0	A10	A9	A8

PROC CODE P1-0
00 : Master
01 : Receiver
10 : Echo Cancel
11 : All

ADDRESS HI A10-A8

APPENDIX A

nop - no operation is specified

INSTRUCTION TYPE
operational control command

OPCODE
000000

SYNOPSIS
nop

DESCRIPTION
nop is used when communications with the V.32 Engine are required but no action is desired.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 1 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

rrr1† - Read MAFE register RR1

INSTRUCTION TYPE
MAFE manipulation command
OPCODE
080000
SYNOPSIS
rrr1
DESCRIPTION
rrr1 causes the V.32 Engine to read the 12 bit contents of the MAFE chipset register RR1. The data is returned in a standard three byte format. The least significant data byte is returned in byte 1, followed by the most significant data byte. Byte 0 is the standard response format (refer to appendix B) with DAV1 and DAV2 bits set to 1. Consult the data sheet of the TS68951 for the specifics of the returned data.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	0	0	0

BYTE 1 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

APPENDIX A

rrr2† - Read MAFE register RR2

INSTRUCTION TYPE
MAFE manipulation command

OPCODE
090000

SYNOPSIS
rrr2

DESCRIPTION
rrr2 causes the V.32 Engine to read the 12 bit contents of the MAFE chipset register RR2. The data is returned in a standard three byte format. The least significant data byte is returned in byte 1, followed by the most significant data byte. Byte 0 is the standard response format (refer to appendix B) with DAV1 and DAV2 bits set to 1. Consult the data sheet of the TS68951 for the specifics of the returned data.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	0	0	1

BYTE 1 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

rtra - force a retrain of the V.32 Engine

INSTRUCTION TYPE
operational control command

OPCODE
050000

SYNOPSIS
rtra

DESCRIPTION
rtra is used to force the V.32 Engine to initiate a retrain sequence on the channel.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	1	0	1

BYTE 1 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

APPENDIX A

setgn† - set global gain factor

INSTRUCTION TYPE
operational control command

OPCODE
02

SYNOPSIS
stegn gain value

DESCRIPTION
setgn is a command which used to scale the transmit samples. The 16 bit value provided is used as the multiplicative constant to be multiplied with each transmit sample.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	0	1	0

BYTE 1 DEFINITION

G7	G6	G5	G4	G3	G2	G1	G0

LOW BYTE OF GAIN VALUE.

BYTE 2 DEFINITION

G15	G14	G13	G12	G11	G10	G9	G8

HI BYTE OF GAIN VALUE.

slnt - Disable tone generators

INSTRUCTION TYPE
tone command

OPCODE
0D0000

SYNOPSIS
slnt

DESCRIPTION
slnt causes the V.32 Engine to disable the tone generators, thus stopping the tone output (i.e. send silence).

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	1	0	1

BYTE 1 DEFINITION

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

APPENDIX A

spac† - Store Parameter And Count

INSTRUCTION TYPE
memory manipulation command

OPCODE
13

SYNOPSIS
spac lo-byte hi-byte

DESCRIPTION
spac is a command which used to write an arbitrary 16 bit value into the writable memory location currently specified by the Memory Address Register. The content of the Memory Address Register is incremented by 1 at the completion of command execution. See also WARP.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	0	0	1	1

BYTE 1 DEFINITION

D7	D6	D5	D4	D3	D2	D1	D0

LOW BYTE OF DATA

BYTE 2 DEFINITION

D15	D14	D13	D12	D11	D10	D9	D8

HI BYTE OF DATA

spam† - Store Parameter in Addressed Memory

INSTRUCTION TYPE
memory manipulation command

OPCODE
12

SYNOPSIS
spam lo-byte hi-byte

DESCRIPTION
spam is a command which used to write an arbitrary 16 bit value into the writable memory location currently specified by the Memory Address Register. See also WARP.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	0	0	1	0

BYTE 1 DEFINITION

D7	D6	D5	D4	D3	D2	D1	D0

LOW BYTE OF DATA

BYTE 2 DEFINITION

D15	D14	D13	D12	D11	D10	D9	D8

HI BYTE OF DATA.

APPENDIX A

tgen - Enable and disable tone generators

INSTRUCTION TYPE
tone control command

OPCODE
0D

SYNOPSIS
tgen tg code

DESCRIPTION
tgen causes the V.32 Engine to enable or disable tone generator 1 and tone generator 2, according to the parameter provided. Either tone generator 1 or tone generator 2 can be scaled by the parameter provided in byte 2. If neither is scaled and both tone generators are enabled, tone 2 has a level 2 dB higher than tone 1. The user cannot scale both tone generators. If both generators are selected to be scaled, tone generator 1 has higher priority.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	1	0	1

BYTE 1 DEFINITION (TONE CODE)

0	0	0	0	TGN2	TGN1	0	0

TG CODE TGC2-1	TONE GEN 1	TONE GEN 2
00	disabled	disabled
01†	enabled	disabled
10†	disabled	enabled
11	enabled	enabled

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

tone - Select and transmit tone (s)

INSTRUCTION TYPE
tone select and command

OPCODE
0C

SYNOPSIS
tone tone code

DESCRIPTION
tone causes the V.32 Engine to program the tone generators for the specified tone or tones. The tones are defined by the tone code parameter passed in the second byte of the command. See also tonetab for the predefined single and double tones, and the commands deft and tgen for user definable tones and tone generator control.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	1	0	0

BYTE 1 DEFINITION (TONE CODE)

T7	T6	T5	T4	T3	T2	T1	T0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

Tone Code	Tone Parameters
0	DTMF 0 (941 & 1336 Hz)
1	DTMF 1 (697 & 1209 Hz)
2	DTMF 2 (697 & 1336 Hz)
3	DTMF 3 (697 & 1477 Hz)
4	DTMF 4 (770 & 1209 Hz)
5	DTMF 5 (770 & 1336 Hz)
6	DTMF 6 (770 & 1477 Hz)
7	DTMF 7 (852 & 1209 Hz)
8	DTMF 8 (852 & 1336 Hz)
9	DTMF 9 (852 & 1477 Hz)
A	(697 & 1633 Hz)
B	(770 & 1633 Hz)
C	(852 & 1633 Hz)
D	(941 & 1633 Hz)
E	DTMF * (941 & 1209 Hz)
F	DTMF # (941 & 1477 Hz)
10	Answer tone (2100 Hz)

APPENDIX A

ufzec - Unfreeze the echo canceller adaptation

INSTRUCTION TYPE
operational control command

OPCODE
170000

SYPNOSIS
ufzec

DESCRIPTION
Ufzec causes the V.32 Engine to enable the adaptation of the echo canceller.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	0	1	1	1

BYTE 1 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

ufzeq - Unfreeze the equalizer adaptation

INSTRUCTION TYPE
operational control command

OPCODE
1C0000

SYPNOSIS
ufzeq

DESCRIPTION
Ufzeq causes the V.32 Engine to enable the adaptation of the equalizer.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	1	1	0	0

BYTE 2 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 3 DEFINITION

0	0	0	0	0	0	0	0

APPENDIX A

warp† - Write Address & Return Parameter

INSTRUCTION TYPE
memory manipulation command

OPCODE
10

SYNOPSIS
warp address

DESCRIPTION
warp is a command which is used to write the Memory Address Register of the V.32 Engine. The V.32 Engine responds with the contents of the addressed location. The data is returned in a standard three byte transfer. The least significant data byte is returned in the byte 1, followed by the most significant data byte. Byte 0 is the standard response format (refer to appendix B) with DAV1 and DAV2 bits set to 1.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	0	0	0	0

BYTE 1 DEFINITION

A7	A6	A5	A4	A3	A2	A1	A0

LOW BYTE OF DATA

BYTE 2 DEFINITION

P1	P0	M1	M0	A11	A10	A9	A8

PROC CODE P1-0	MEM CODE M1-0	ADDRESS HI A11-A8
00 : Master	00 : XRAM	
10 : Receiver	01 : YRAM	
01 : Echo Canceller	10 : EMEM	
	11 : CROM	

warpx† - Write Address & Return Parameter Complex

INSTRUCTION TYPE
memory manipulation command

OPCODE
11

SYNOPSIS
warpx address

DESCRIPTION
warpx is a command which is used to write the Memory Address Register of the V.32 Engine. The V.32 Engine responds with the contents of the most significant bytes of the addressed location and the addressed location + 1. The data is returned in a standard three byte transfer. Byte 0 is the standard response format (refer to appendix B) with DAV1 and DAV2 bits set to 1. Byte 1 is used to return the 8 most significant bits contained in the addressed location. The 8 most significant bits of the addressed location + 1 are returned in byte 2.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	0	0	0	1

BYTE 1 DEFINITION

A7	A6	A5	A4	A3	A2	A1	A0

LOW BYTE OF DATA

BYTE 2 DEFINITION

P1	P0	M1	M0	A11	A10	A9	A8

APPENDIX A

wtr1† - Write MAFE register TR1

INSTRUCTION TYPE
MAFE manipulation command

OPCODE
0A

SYNOPSIS
wtr1

DESCRIPTION
wtr1 causes the V.32 Engine to take the two supplied data bytes and write them in sequence to the MAFE chipset register TR1.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	0	1	0

BYTE 1 DEFINITION (DATA)

D3	D2	D1	D0	0	0	0	0

BYTE 2 DEFINITION (DATA)

D11	D10	D9	D8	D7	D6	D5	D4

wtr2† - Write MAFE register TR2

INSTRUCTION TYPE
MAFE manipulation command

OPCODE
0B

SYNOPSIS
wtr2

DESCRIPTION
wtr2 causes the V.32 Engine to take the two supplied data bytes and write them in sequence to the MAFE chipset register TR2.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	0	1	1

BYTE 1 DEFINITION (DATA)

D3	D2	D1	D0	0	0	0	0

BYTE 2 DEFINITION (DATA)

D11	D10	D9	D8	D7	D6	D5	D4

APPENDIX A

xmit - transmit data to other modem

INSTRUCTION TYPE
data communications command

OPCODE
01

SYNOPSIS
xmit data

DESCRIPTION
xmit is used to command the V.32 Engine to send data. The OP code for the xmit command is a single byte. The data bits to be transmitted are stored in the second byte, where D0 is the first bit to be transmitted.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	0	0	1

BYTE 1 DEFINITION

D7	D6	D5	D4	D3	D2	D1	D0

D0-D7 DATA BITS

BYTE 2 DEFINITION

0	0	0	0	0	0	0	0

xmiti† - transmit data to other modem and initiate additional cycle

INSTRUCTION TYPE
data communications command

OPCODE
03

SYNOPSIS
xmit data

DESCRIPTION
xmit is used to command the V.32 Engine to send data. The OP code for the xmit command is a single byte. The data bits to be transmitted are stored in the second byte, where D0 is the first bit to be transmitted.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	0	1	1

BYTE 1 DEFINITION

D7	D6	D5	D4	D3	D2	D1	D0

D0-D7 DATA BITS

BYTE 2 DEFINITION

0	0	0	0	0	0	0	0

APPENDIX B
STATUS REPORTING DESCRIPTION

BYTE 0 DEFINITION

F11	F10	F01	F00	DAV2	DAV1	H	107

FLAG CODE F01-00	CALL ESTAB	HANDSHAKE OPERATIONS	DATA XFER OPERATIONS
00	no tones	line quality is good	line quality is good
01	Band 1 detected	line terrible (local retrain req.)	line quality is poor
10	Band 2 detected	time out	line terrible (local retrain req.)
11	Both bands detected	line cleardown	remote retrain sequence detected
F11-10			
00	reserved	9600 bps no trellis	reserved
01	Answer tone	4800 bps	reserved
10	AC detected	9600 bps trellis	reserved
11	reserved	2400 bps	reserved

DAV1	DAV2	DEFINITION
0	0	Data is in byte 1 and 2.
0	1	Data is in byte 1 and status word in byte 2.
1	0	No data bits and status word is in byte 2.
1	1	Answer to the last command is in bytes 1 and 2.

FLAG	BIT	DEFINITION
H	0/1	Handshake is not/is in progress
107	0/1	Set circuit 107 off/on

BYTE 1 DEFINITION

RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

BYTE 1 DEFINITION†

ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0

Bit	Call Modem	Answer Modem
ST7	AC detected	AA detected
ST6	AC-CA detected	AA-CC detected
ST5	CA-AC detected	Silence detected
ST4	S detected	S detected
ST3	S-S/detected	S-S / detected
ST2	R1 detected	R2 detected
ST1	R3 detected	N/A
ST0	E detected	E detected

APPENDIX C

This appendix describes the interconnection between the different chips.

SYSTEM INTERFACE

Signal Name	Chip/Pin	Description
DOH..D7H	TS75321/27..34	System Data Bus : connect to host processor.
CSL	TS75321/21	Chip Select : connect to host processor.
RSL	TS75321/22	Register Select : connect to host processor.
DSL	TS75321/20	Data Strobe : connect to host.
RWL	TS75321/19	Read/Write : connect to host.
INTL	TS75321/24	Interrupt Request : connect to host processor
RSTL1 RSTL2 RSTL0	TS75321/23 TS75322/23 TS75320/23	Reset : connect to host processor. Reset Reset

CLOCK SIGNAL

Signal Name	Chip/Pin	Description
TxRCLK	TS68952/16 TS75321/26	Transmit baud clock.
TxCCLK	TS68952/24 TS75321/44 TS68950/19 TS68951/23	Transmit conversion clock.
RxRCLK	TS68952/20 TS75321/43 TS75322/44	Receive baud clock.
RxCCLK	TS68952/21 TS75321/25 TS75322/43 TS68951/22	Receive conversion clock.
TxSCLK	TS68952/11	If not used must be grounded.
XTL1	TS68952/13	External crystal input : must be connected via a 5.76 MHz crystal to XTL2.
XTL2	TS68952/14	External Crystal Input
CLK	TS68952/15 TS68950/18 TS68951/21	Main analog clock : this output, in accordance with the XTL1/2 crystal, must be 1.4 MHz (+ - 7Hz).
25 MHz	TS75320/15 TS75321/15 TS75322/15	Main digital clock : connect to a 25 MHz oscillator.
TxCCLK RxCCLK	TS68952/23 TS68952/22	Transmit bit clock. Receive bit clock.

APPENDIX C

ANALOG SIGNALS

Signal Name	Chip/pin	Description
ATO	TS68950/15	Analog Transmit Output : connect to DAA.
EEO[T]	TS68950/16 TS68951/11	Analog echo cancelling estimation.
LEI	TS68951/17	Local Echo Input : connect to DAA.
RAI	TS68951/16	Receive Analog Input : connect to DAA.
RFO	TS68951/13	This pin must be connected throught a 1 µF nonpolarised capacitor to AGC1 input.
AGC1	TS68951/12	
AGC2	TS68951/19	Connect to the analog loop back signal (see schematic).
CD1	TS68951/18	Connect to the analog ground through a 1 µF nonpolarised capacitor

Caution : T The connection between EEO (TS68950/16) and EEI (TS68951/11) must be as close as possible to avoid parasitics on echo estimate signal.

INTER DSP AND EXTERNAL MEMORY CONNECTION

Signal Name	Chip/Pin	Description
0D0..0D15	TS75320/45..48,1..12 RAM0/IO0..IO15	Data Bus
1D8..1D15	TS75321/5..12 TS75320/27..34 RAM0/AD0..AD7 TS68950/20..24, 1..3	Data and Address Buses
1D0..1D7	TS75321/45..48, 1..4 TS75322/27..34 RAM2/AD0..AD7	Data and Address Buses
2D9..2D15	TS75322/6..12 TS68951/25..28, 1..3 TS68952/25..28, 1..3 RAM2/IO9..IO15	Data Bus
2D8	TS75322/5 TS68951/24 RAM2/IO8	Data Pin
2D0..2D7	TS75322/45..48, 1..4 RAM2/IO0..IO7	Data Bus
1A11	TS75321/39 TS75320/21 TS75322/21 TS68950/7	Address Line
1A10	TS75321/37 TS68950/6	Adress Line
1A9	TS75321/36 TS68950/9 TS75320/22	Address Line

Note : RAM0 Refer to DSP0 4Kx16 External memory.
RAM2 Refer to DSP2 2Kx16 External memory.

Where : IO is bidirectional data bus
AD is address line
WEL is Write Enable (active low)
CEL is Chip Select (active low)

APPENDIX C

INTER DSP AND EXTERNAL MEMORY CONNECTION (continued)

Signal Name	Chip/Pin	Description
1A8	TS75321/35 TS68950/8 TS75322/22	Address Line
1RWL	TS75321/18 TS75320/19 TS75322/19 TS68950/5	Control Line
1DSL	TS75321/17 TS75320/20 TS75322/20 TS68950/4	Control Line
0A8..0A11	TS75320/35..37,39 RAM0/AD8..AD11	Address Line
0DSL	TS75320/17 RAM0/CEL	Control Line
0RWL	TS75320/18 RAM0/WEL	Control Line
2A8..2A11	TS75322/35..37,39 TS68951/8,9,6,7 TS68952/8,9,6,7 RAM2/A8..A10,CEL	Address Line
2DSL	TS75322/17 TS68951/4 TS68952/4 RAM2/OEL	Control Line
2RWL	TS75322/18 TS68951/5 TS68952/5 RAM2/WEL	Control Line
0IRQL	TS75320/24 TS75321/42	Synchro Line
2IRQL	TS75322/24 TS75321/41	Synchro Line

Note : RAM0 Refer to DSP0 4Kx16 External memory.
RAM2 Refer to DSP2 2Kx16 External memory.

Where : IO is bidirectional data bus
AD is address line
WEL is Write Enable (active low)
CEL is Chip Select (active low)
OEL is Output Enable (active low)

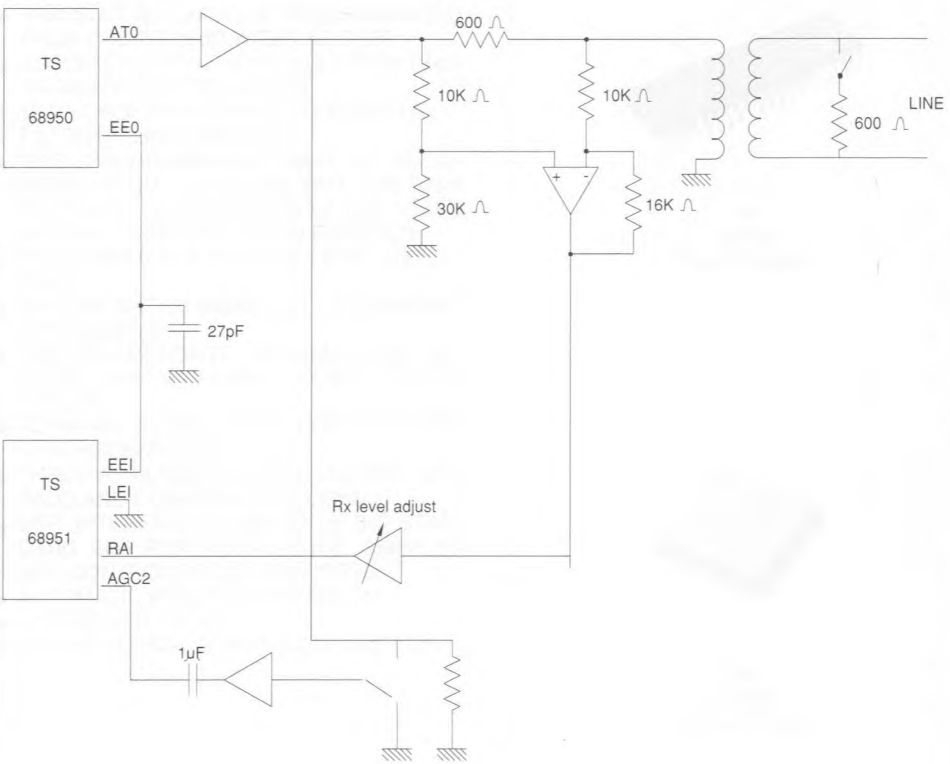
APPENDIX C

POWER SUPPLY AND MISCELLANEOUS

Signal Name	Chip/Pin	Description
+ 5VA	TS68951/20 TS68950/17	Positive Analog Power Supply
- 5VA	TS68951/14 TS68950/12	Negative Analog Power Supply
AGND	TS68950/13 TS68951/15	Analog Ground
VCC	TS75320/38 TS75321/38 TS75322/38 TS68952/17	Main Digital Power Supply
DGND	TS75320/13 TS75321/13 TS75322/13 TS68950/10 TS68951/10 TS68952/12	Digital Ground Power Supply
xtal	TS75320/14 TS75321/14 TS75322/14	Not Connected (must be left open)
Clkout	TS75320/16 TS75321/16 TS75322/16	Not Connected (25 MHz/4)
TO	TS68952/10	Not Connected (must be left open)
AGND	TS68950/14	Auxiliary Input
DGND	TS75321/40 TS75320/40..44 TS75320/25..26 TS75322/40..42 TS75322/25..26 TS68950/11	Not Used

APPENDIX C

Figure 9 : Analog Path.



APPENDIX D
REFERENCES

[1] CCITT recommendation V.32.
[2] CCITT recommendation V.54.
[3] Data sheet of the TS75320 , V.32 modem echo canceller, SGS - THOMSON Microelectronics.
[4] Data sheet of the TS68930, TS68931 programmable signal processor, SGS - THOMSON Microelectronics.
[5] Data sheet of the TS68950 transmitter interface chip, SGS - THOMSON Microelectronics.
[6] Data sheet of the TS68951 receiver interface chip, SGS - THOMSON Microelectronics.
[7] Data sheet of the TS68952 clock generation chip, SGS - THOMSON Microelectronics.
[8] Application guide : Using the TS75320 Echo canceller in V.32 modems, SGS - THOMSON Microelectronics.