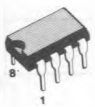
SGS-THOMSON MICROELECTRONICS

TS59C11

1K BIT SERIAL CMOS EEPROM

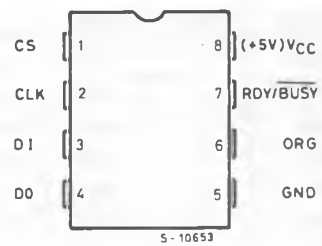
- HIGHLY RELIABLE CMOS FLOATING GATE TECHNOLOGY.
- SINGLE 5-VOLT SUPPLY
- EIGHT PIN PACKAGE.
- 64 x 16 OR 128 x 8 USER SELECTABLE SERIAL MEMORY
- COMPATIBLE WITH GENERAL INSTRUMENT GI 5911
- SELF TIMED PROGRAMMING CYCLE
- WORD AND CHIP ERASABLE
- 10,000 ERASE/WRITE CYCLES.
- TEN YEARS DATA RETENTION
- POWER-ON DATA PROTECTION



P
DIP-8
(Plastic Package)

(Ordering Information at the end of the datasheet)

PIN CONNECTIONS



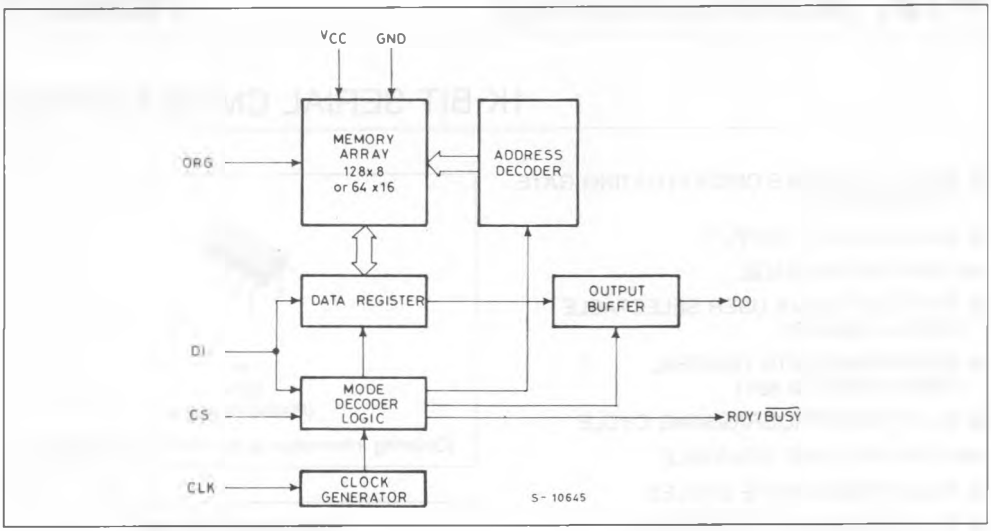
PIN NAMES

CS	CHIP SELECT
CLK	CLOCK INPUT
DI	SERIAL DATA INPUT
DO	SERIAL DATA OUTPUT
ORG	ORGANIZATION INPUT
R/$\overline{B}$	READY/$\overline{BUSY}$ OUTPUT
V_{CC}	+5V POWER SUPPLY
GND	GROUND

PIN DESCRIPTION

Name	No	Description
CS	1	Chip Select
CLK	2	Clock Input
DI	3	Serial Data Input
DO	4	Serial Data Output
GND	5	Ground
ORG	6	Memory Array Organization Selection Input. When the ORG pin is connected to +5, the 64 x 16 organization is selected. When it is connected to ground, the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pull up device will select the 64 x 16 organization.
RDY/$\overline{BUSY}$	7	Status Output
V_{CC}	8	+5V Power Supply

BLOCK DIAGRAM



INSTRUCTION SET

Instruction	Start bit	Opcode	Address		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1000	A_6-A_0	A_5-A_0			Read Address A_N-A_O
PROGRAM	1	x 100	A_6-A_0	A_5-A_0	D_7-D_0	D_{15}-D_0	Program Address A_N-A_0
PEN	1	0011	0000000	000000			Program Enable
PDS	1	0000	0000000	000000			Program Disable
ERAL	1	0010	0000000	000000			Erase All Addresses
WRAL	1	0001	0000000	000000	D_7-D_0	D15-D_0	Program All Addresses

DI/DO: It is possible to connect the Data In and Data Out pins together. However, with this configuration it si possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A_0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A_0. The higher the current sourcing capability of A_0, the higher the voltage at the Data Out pin.

POWER-ON DATA PROTECTION CIRCUITRY: During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	+7	V
	Voltage on any input pin	GND −0.3 to +7	V
	Voltage or any output pin	V_{CC} +0.3 GND −0.3	V
T_{STG}	Storage temperature range	−65 to +150	°C
	Lead temperature (Soldering: 10 seconds)	+300	°C

READ OPERATION

DC CHARACTERISTICS

T_{amb} = 0°C to 70°C for CP, T_{amb} = − 40 to + 85°C for VP, V_{CC} = 5V ± 10% (Unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
V_{CC}	Operating voltage		4.5		5.5	V
I_{CC1}	Operating current	V_{CC} = 5.5V, CS = V_{IH} CP range VP range			 4 4	mA
I_{CC2}	Standby current	V_{CC} = 5.5V, CS = DI = SK = GND + 0.1V)			100	µA
V_{IL}	Input low voltage		− 0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC} + 1	V
V_{OL}	Output low voltage	I_{OL} = 2.1mA			0.4	V
V_{OH}	Output high voltage	I_{OH} = − 400µA	2.4			V
I_{LI}	Input leakage current	V_{in} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{out} = 5.5V, CS = 0			10	µA

AC CHARACTERISTICS

(T_{amb} = 0° to 70°C for CP, T_{amb} = − 40 to + 85°C for VP, V_{CC} = 5V ± 10% (Unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
	SK max (Maximum frequency)				250	KHz
	SK duty cycle		25	50	75	%
T_{CSS}	CS setup time		0.2			µs
T_{CSH}	CS hold time		0			µs
T_{DIS}	DI Setup time		0.4			µs
T_{DIH}	Data input hold time		0.4			µs
T_{CPW}	CLK pulse width		2.0			µs
T_{PD1} T_{PD0}	Data output delay	CL = 100pF, V_{OL} = 0.8V, V_{OH} = 2.0V and V_{IH} = 2.4V, V_{IL} = 0.45V			2.0 2.0	µs
t_{PR}	Status low time (programming time)				10	ms

FIG. 1 - SYNCHRONOUS DATA TIMINGS

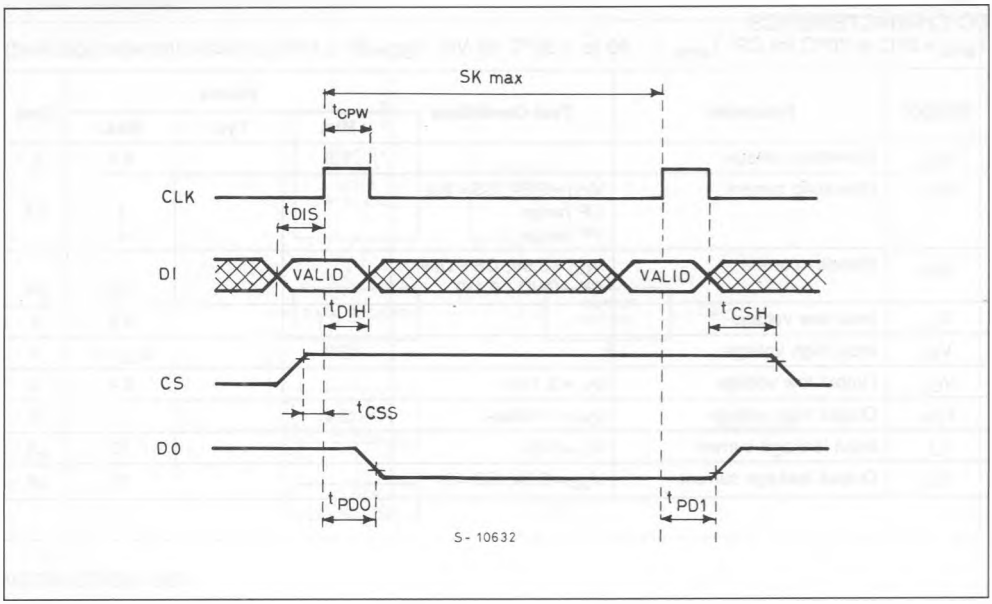
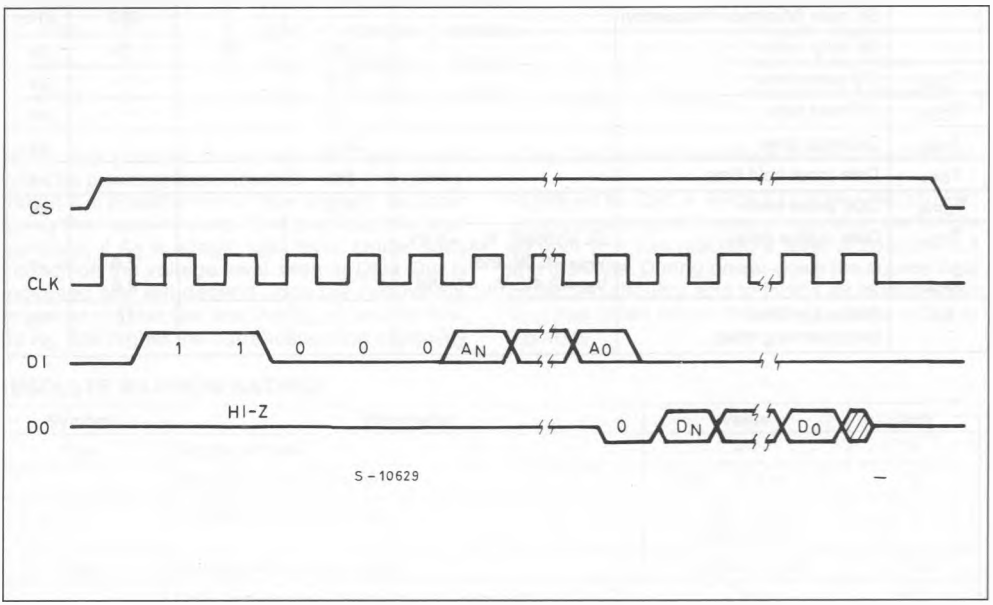


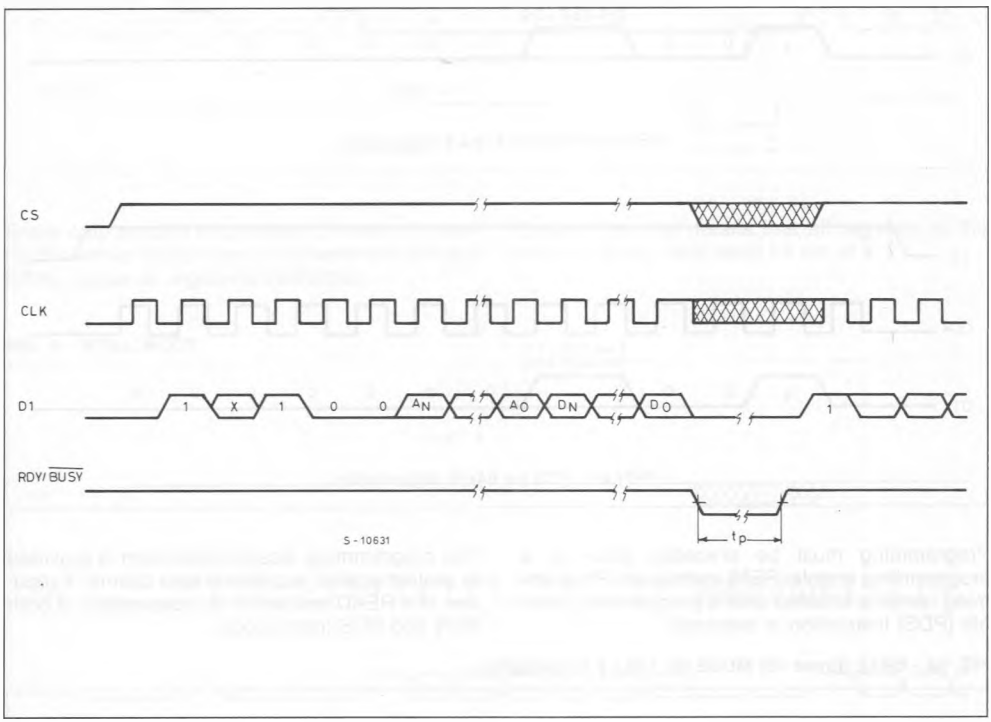
FIG. 2 - READ MODE



The READ instruction is the only instruction which outputs serial data on the DO pin. After a READ isntruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a serial-out shift register. A dummy bit (logical "0") precedes the data output string. The output data changes during the high states of the system clock.

Organization	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

FIG. 3 - PROGRAM MODE



The PROGRAM instruction is followed by either eight or sixteen bits of data, which are to be written into the specified address.

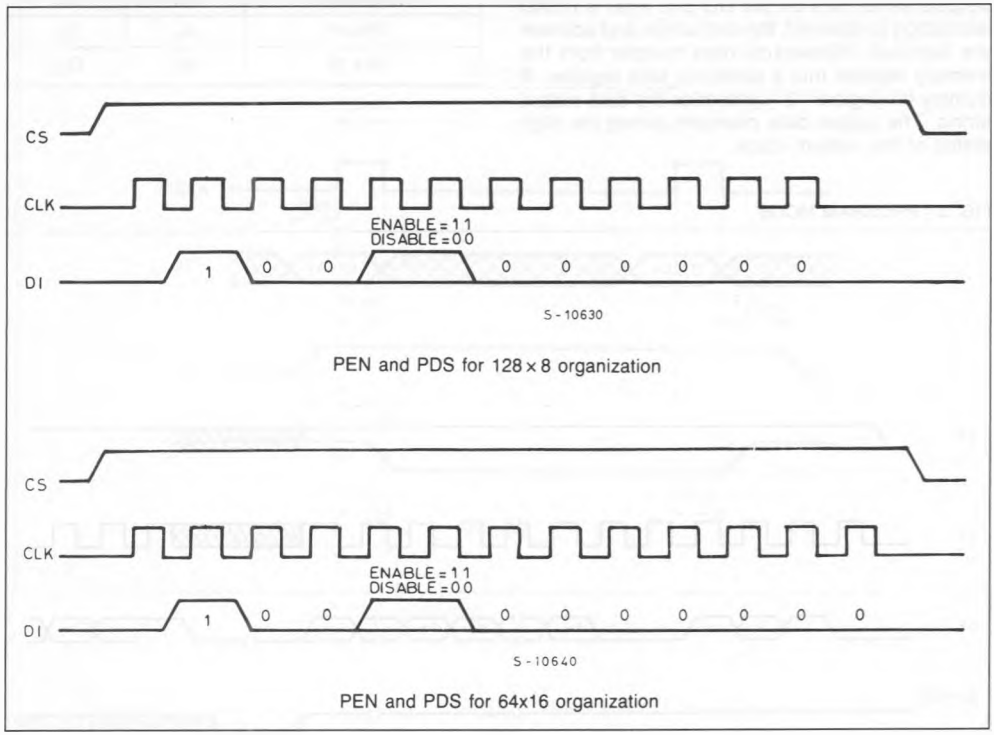
After the last data bit (DO) has been shifted into the data register the contents of the specified address will be erased and the new data written to the same address.

During the automatic erase/write sequence the RDY/BUSY output will go low for the duration of the automatic programming cycle as indicated by tp.

During a program cycle the internal erase and write operations occur automatically and are self-timed on the device. A single memory location may also be erased by programming that address with all "1's".

Organization	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

FIG. 4 - PEN (Program enable) AND PDS (Program Disable)



Programming must be preceded once by a programming enable (PEN) instruction. Programming remains enabled until a programming disable (PDS) instruction is executed.

The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both PEN and PDS instructions.

FIG. 5a - ERAL (Erase all) MODE for 128 x 8 Organization

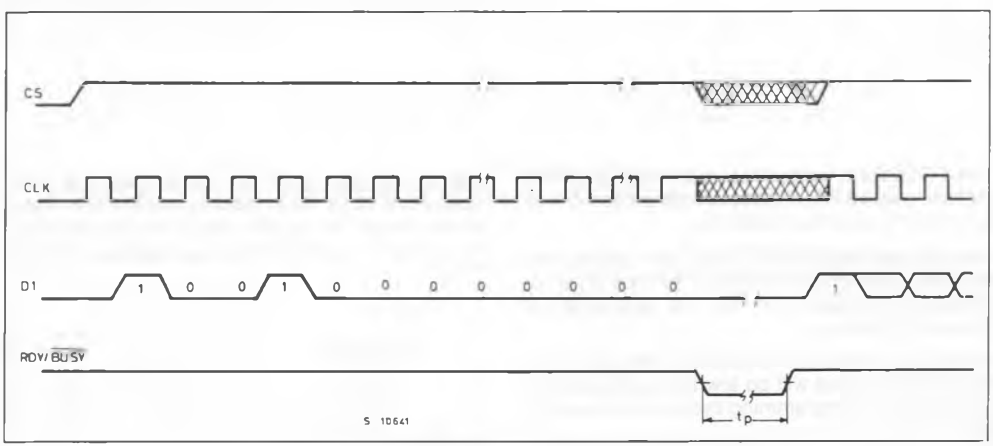
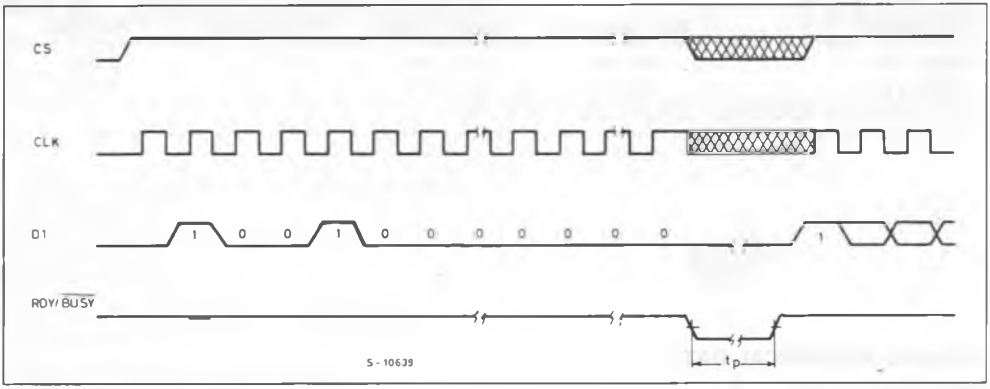


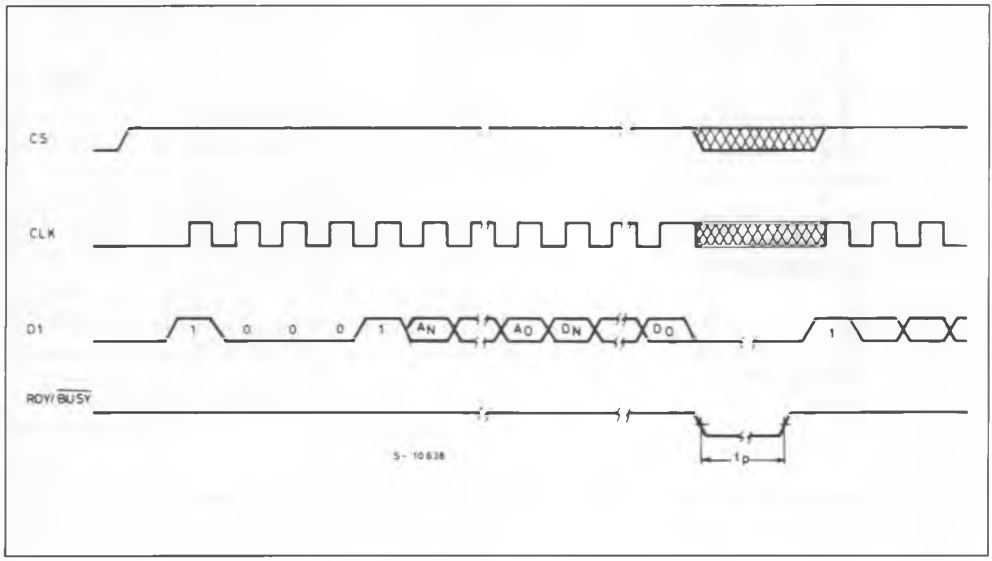
FIG. 5b - ERAL (Erase all) MODE for 64 x 16 Organization



Entire chip erasing is provided for ease of clearing the whole memory and is implemented with the ERAL (erase all registers) instruction.

Erasing the chip means that all registers in the memory array have each bit set to a 1.

FIG. 6 - WRAL MODE



The WRAL instruction is followed by either eight or sixteen bits of data. After the last data bit (D_0) has been shifted into the data register the contents of all adresses will be erased an the new data written to all adresses. The pre-erasing and writing of new data occur automatically and are self-timed on-chip.

During the automatic erase/write sequence the RDY/$\overline{\text{DUSY}}$ output will low for the duration of the automatic programming cycle as indicated by tp.

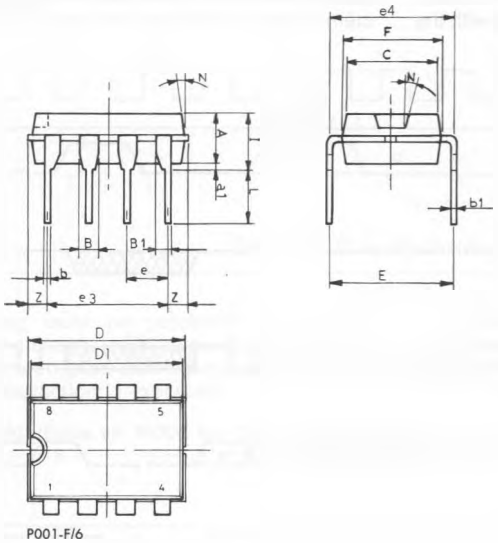
Organization	A_N-A_0	D_N
128 x 8	0000000	D_7
64 x 16	000000	D_{15}

ORDERING INFORMATION

Part Number	Max Frequency	Supply Voltage	Temp. Range	Package
TS59C11CP	250 KHz	5V ± 10%	0 to +70°C	DIP-8
TS59C11VP	250 KHz	5V ± 10%	−40 to +85°C	DIP-8

PACKAGE MECHANICAL DATA

8-PIN PLASTIC DIP



P001-F/6

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1	0.70			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.50			0.02	
b1	0.38		0.50	0.015		0.020
C						
D			9.80			0.386
D1						
E		8.90			0.350	
e		2.54			0.100	
e3		7.62			0.300	
e4						
F			7.10			0.280
I			4.80			0.189
L		3.30			0.130	
N						
Z	0.44		1.60	0.017		0.063