

3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH ± 15 -kV IEC ESD PROTECTION

Check for Samples: [TRS3243E](#)

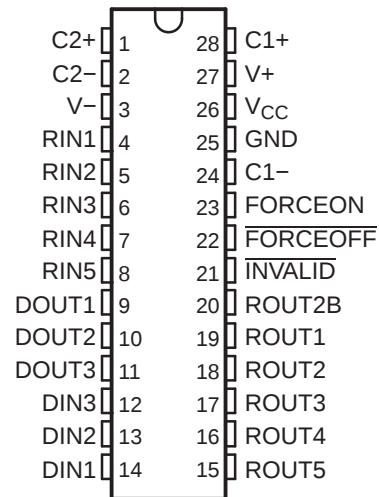
FEATURES

- Single-Chip and Single-Supply Interface for IBM™ PC/AT™ Serial Port
- ESD Protection for RS-232 Bus Pins
 - ± 15 -kV Human-Body Model (HBM)
 - ± 8 -kV IEC61000-4-2, Contact Discharge
 - ± 15 -kV IEC61000-4-2, Air-Gap Discharge
- Meets or Exceeds Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V V_{CC} Supply
- Always-Active Noninverting Receiver Output (ROUT2B)
- Designed to Transmit at a Data Rate up to 500 kbit/s
- Low Standby Current . . . 1 μ A Typ
- External Capacitors . . . $4 \times 0.1 \mu$ F
- Accepts 5-V Logic Input With 3.3-V Supply
- Designed to Be Interchangeable With Industry Standard '3243E Devices
- Serial-Mouse Driveability
- Auto-Powerdown Feature to Disable Driver Outputs When No Valid RS-232 Signal Is Sensed
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

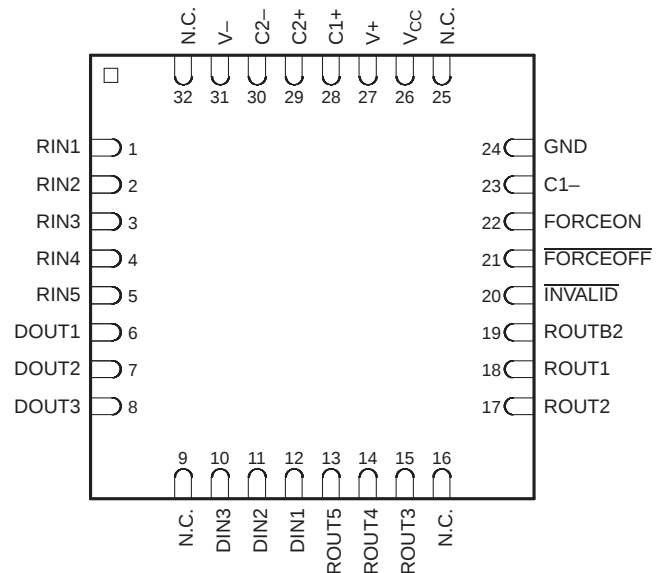
APPLICATIONS

- Battery-Powered Systems
- PDAs
- Notebooks
- Laptops
- Palmtop PCs
- Hand-Held Equipment

DB, DW, OR PW PACKAGE
(TOP VIEW)



QFN PACKAGE
(TOP VIEW)



N.C. – Not internally connected



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

IBM, PC/AT are trademarks of International Business Machines Corporation.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2007–2011, Texas Instruments Incorporated

DESCRIPTION/ORDERING INFORMATION

The TRS3243E device consists of three line drivers, five line receivers, and a dual charge-pump circuit with ± 15 -kV ESD (HBM and IEC61000-4-2, Air-Gap Discharge) and ± 8 -kV ESD (IEC61000-4-2, Contact Discharge) protection on serial-port connection pins. The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. This combination of drivers and receivers matches that needed for the typical serial port used in an IBM PC/AT, or compatible. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. In addition, the device includes an always-active noninverting output (ROUT2B), which allows applications using the ring indicator to transmit data while the device is powered down. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/ μ s driver output slew rate.

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If FORCEOFF is set low, both drivers and receivers (except ROUT2B) are shut off, and the supply current is reduced to 1 μ A. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur.

Auto-powerdown can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high, and should be done when driving a serial mouse. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The INVALID output is used to notify the user if an RS-232 signal is present at any receiver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V or less than -2.7 V or has been between -0.3 V and 0.3 V for less than 30 μ s. INVALID is low (invalid data) if all receiver input voltages are between -0.3 V and 0.3 V for more than 30 μ s. Refer to Figure 5 for receiver input levels.

The TRS3243EC is characterized for operation from 0°C to 70°C. The TRS3243EI is characterized for operation from -40°C to 85°C.

Table 1. ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SSOP – DB	Reel of 2000	TRS3243ECDBR	TRS3243EC
	SOP – DW	Reel of 2000	TRS3243ECDWR	TRS3243EC
	TSSOP – PW	Reel of 2000	TRS3243ECPWR	RS43EC
	QFN – RHB	Reel of 2000	TRS3243ECRHBR	RS43EC
-40°C to 85°C	SSOP – DB	Reel of 2000	TRS3243EIDBR	TRS3243ECI
	SOP – DW	Reel of 2000	TRS3243EIDWR	TRS3243ECI
	TSSOP – PW	Reel of 2000	TRS3243EIPWR	RS43EI
	QFN – RHB	Reel of 2000	TRS3243EIRHBR	RS43EI

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLES

Each Driver⁽¹⁾

INPUTS				OUTPUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
X	L	H	No	Z	Powered off by auto-powerdown feature

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Each Receiver⁽¹⁾

INPUTS			OUTPUT	RECEIVER STATUS
RIN	FORCEON	$\overline{\text{FORCEOFF}}$	ROUT	
X	X	L	Z	Powered off
L	X	H	H	Normal operation with auto-powerdown disabled/enabled
H	X	H	L	
Open	X	H	H	

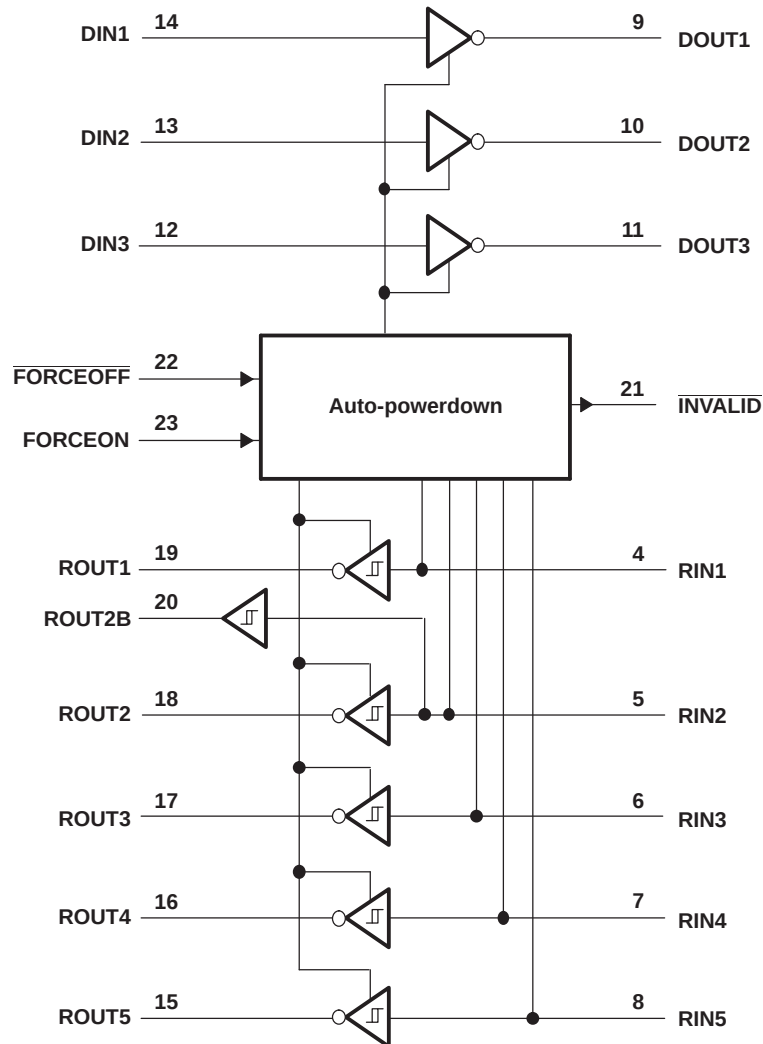
(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

ROUT2B and Outputs $\overline{\text{INVALID}}$ ⁽¹⁾

INPUTS				OUTPUTS		OUTPUT STATUS
VALID RIN RS-232 LEVEL	RIN2	FORCEON	$\overline{\text{FORCEOFF}}$	$\overline{\text{INVALID}}$	ROUT2B	
Yes	L	X	X	H	L	Always active
Yes	H	X	X	H	H	
Yes	Open	X	X	H	L	
No	Open	X	X	L	L	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾		−0.3	6	V
V+	Positive output supply voltage range ⁽²⁾		−0.3	7	V
V−	Negative output supply voltage range ⁽²⁾		0.3	−7	V
V+ − V−	Output supply voltage difference ⁽²⁾			13	V
V _I	Input voltage range	Driver ($\overline{\text{FORCEOFF}}$, FORCEON)	−0.3	6	V
		Receiver	−25	25	
V _O	Output voltage range	Driver	−13.2	13.2	V
		Receiver ($\overline{\text{INVALID}}$)	−0.3	V _{CC} + 0.3	
θ _{JA}	Package thermal impedance ⁽³⁾ (4)	DB package		62	°C/W
		DW package		46	
		PW package		62	
Lead temperature 1,6 mm (1/16 in) from case for 10 s				260	°C
T _{stg}	Storage temperature range		−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.
- (3) Maximum power dissipation is a function of T_J(max), θ_{JA} , and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_J(max) – T_A)/ θ_{JA} . Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

See [Figure 6](#)

		MIN	NOM	MAX	UNIT
Supply voltage	V _{CC} = 3.3 V	3	3.3	3.6	V
	V _{CC} = 5 V	4.5	5	5.5	
V _{IH} Driver and control high-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	V _{CC} = 3.3 V	2		V
		V _{CC} = 5 V	2.4		
V _{IL} Driver and control low-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON			0.8	V
V _I Driver and control input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	0		5.5	V
V _I Receiver input voltage		–25		25	V
T _A Operating free-air temperature	TRS3243EC	0		70	°C
	TRS3243EI	–40		85	

- (1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
I _I Input leakage current	$\overline{\text{FORCEOFF}}$, FORCEON		±0.01	±1	µA
I _{CC} Supply current (T _A = 25°C)	Auto-powerdown disabled	No load, $\overline{\text{FORCEOFF}}$ and FORCEON at V _{CC}	0.3	1	mA
	Powered off	No load, $\overline{\text{FORCEOFF}}$ at GND	1	10	
	Auto-powerdown enabled	No load, $\overline{\text{FORCEOFF}}$ at V _{CC} , FORCEON at GND, All RIN are open or grounded, All DIN are grounded	1	10	µA

- (1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
- (2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

DRIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH} High-level output voltage	All DOUT at R _L = 3 kΩ to GND	5	5.4		V
V _{OL} Low-level output voltage	All DOUT at R _L = 3 kΩ to GND	–5	–5.4		V
V _O Output voltage (mouse driveability)	DIN1 = DIN2 = GND, DIN3 = V _{CC} , 3-kΩ to GND at DOUT3, DOUT1 = DOUT2 = 2.5 mA	±5			V
I _{IH} High-level input current	V _I = V _{CC}		±0.01	±1	μA
I _{IL} Low-level input current	V _I at GND		±0.01	±1	μA
V _{hys} Input hysteresis				±1	V
I _{OS} Short-circuit output current ⁽³⁾	V _{CC} = 3.6 V, V _O = 0 V				mA
	V _{CC} = 5.5 V, V _O = 0 V				
r _O Output resistance	V _{CC} , V+, and V– = 0 V, V _O = ±2 V	300	10M		Ω
I _{off} Output leakage current	FORCEOFF = GND, V _O = ±12 V, V _{CC} = 0 to 5.5 V			±25	μA

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

Switching Characteristics⁽¹⁾

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
Maximum data rate	C _L = 1000 pF, R _L = 3 kΩ One DOUT switching, See Figure 1	250	500		kbit/s
t _{sk(p)} Pulse skew ⁽³⁾	C _L = 150 pF to 2500 pF, R _L = 3 kΩ to 7 kΩ, See Figure 2		100		ns
SR(tr) Slew rate, transition region (see Figure 1)	V _{CC} = 3.3 V, R _L = 3 kΩ to 7 kΩ, PRR = 250 kbit/s				V/μs
	C _L = 150 pF to 1000 pF	6		30	
	C _L = 150 pF to 2500 pF	4		30	

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

ESD Protection

PARAMETER	TEST CONDITIONS	TYP	UNIT
Driver outputs (pins 9–11)	HBM	±15	kV
	IEC61000-4-2, Air-Gap Discharge	±15	
	IEC61000-4-2, Contact Discharge	±8	

RECEIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = –1 mA	V _{CC} – 0.6	V _{CC} – 0.1		V
V _{OL}	Low-level output voltage	I _{OH} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.6	2.4	V
		V _{CC} = 5 V		1.9	2.4	
V _{IT–}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.1		V
		V _{CC} = 5 V	0.8	1.4		
V _{hys}	Input hysteresis (V _{IT+} – V _{IT–})			0.5		V
I _{off}	Output leakage current (except ROUT2B)	FORCEOFF = 0 V		±0.05	±10	µA
r _i	Input resistance	V _I = ±3 V or ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

Switching Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP ⁽²⁾	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF, See Figure 3	150	ns
t _{PHL}	Propagation delay time, high- to low-level output		150	ns
t _{en}	Output enable time	C _L = 150 pF, R _L = 3 kΩ, See Figure 4	200	ns
t _{dis}	Output disable time		200	ns
t _{sk(p)}	Pulse skew ⁽³⁾	See Figure 3	50	ns

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

ESD Protection

PARAMETER	TEST CONDITIONS	TYP	UNIT
Driver outputs (pins 4–8)	HBM	±15	kV
	IEC61000-4-2, Air-Gap Discharge	±15	
	IEC61000-4-2, Contact Discharge	±8	

AUTO-POWERDOWN SECTION

Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{IT+(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, FORCEOFF = V_{CC}		2.7	V
$V_{IT-(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, FORCEOFF = V_{CC}	-2.7		V
$V_{T(invalid)}$	Receiver input threshold for $\overline{INVALID}$ low-level output voltage	FORCEON = GND, FORCEOFF = V_{CC}	-0.3	0.3	V
V_{OH}	$\overline{INVALID}$ high-level output voltage	$I_{OH} = -1\text{ mA}$, FORCEON = GND, FORCEOFF = V_{CC}	$V_{CC} - 0.6$		V
V_{OL}	$\overline{INVALID}$ low-level output voltage	$I_{OL} = 1.6\text{ mA}$, FORCEON = GND, FORCEOFF = V_{CC}		0.4	V

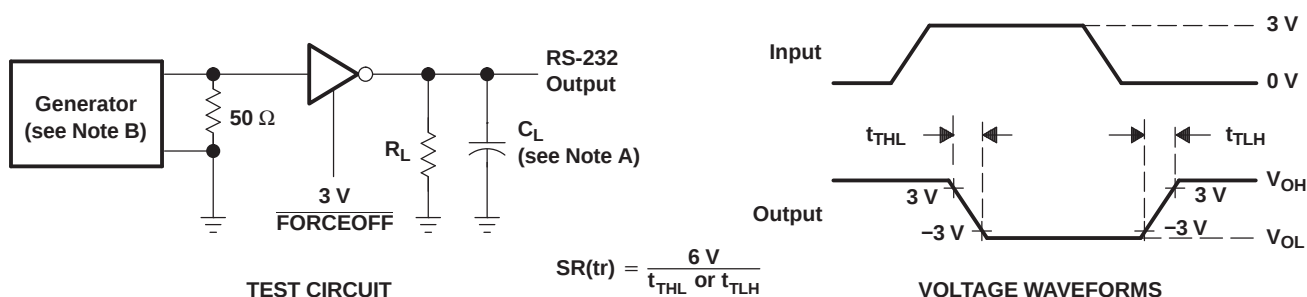
Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	TYP ⁽¹⁾	UNIT
t_{valid}	Propagation delay time, low- to high-level output	$V_{CC} = 5\text{ V}$	1	μs
$t_{invalid}$	Propagation delay time, high- to low-level output	$V_{CC} = 5\text{ V}$	30	μs
t_{en}	Supply enable time	$V_{CC} = 5\text{ V}$	100	μs

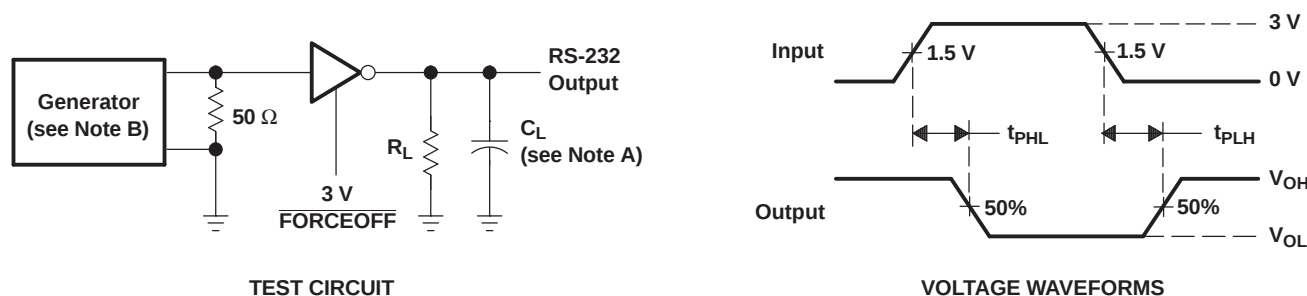
(1) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION



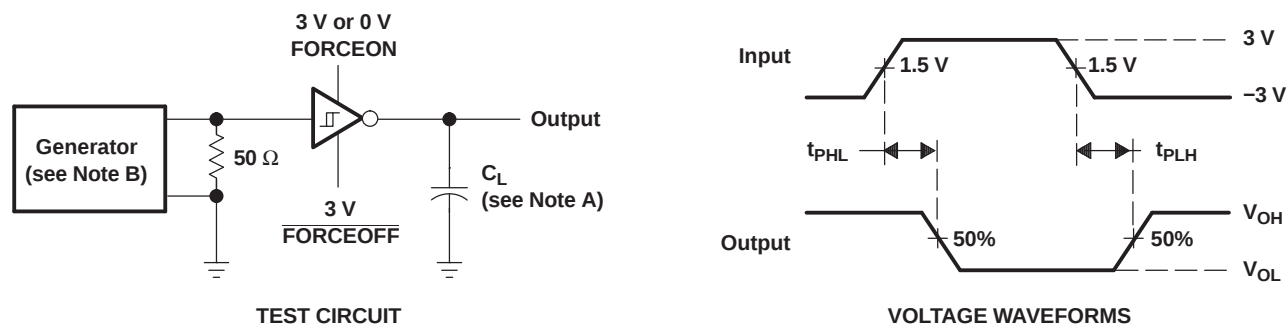
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 1. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

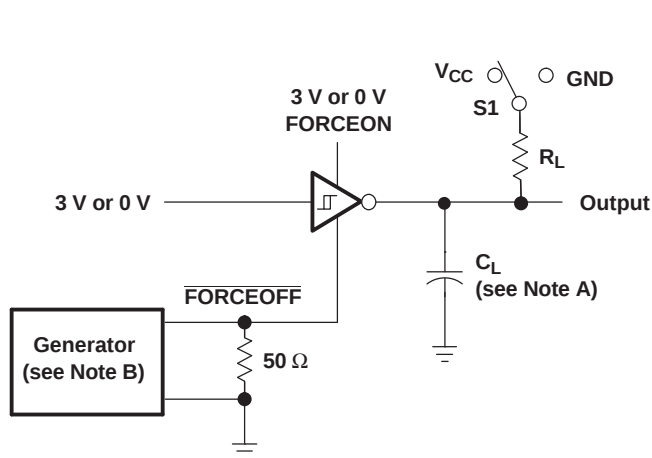
Figure 2. Driver Pulse Skew



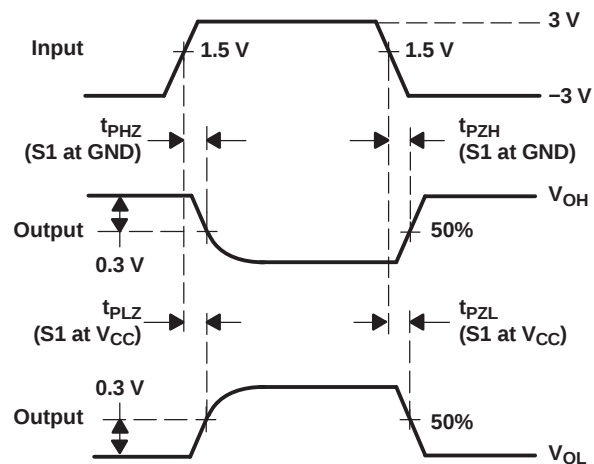
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 3. Receiver Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

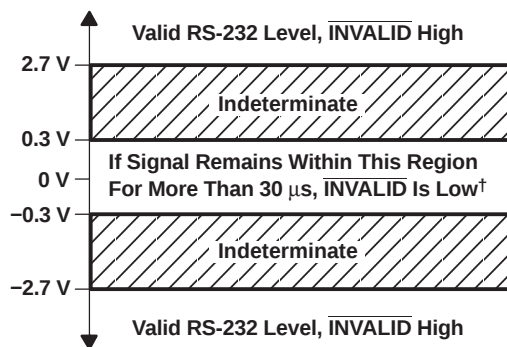
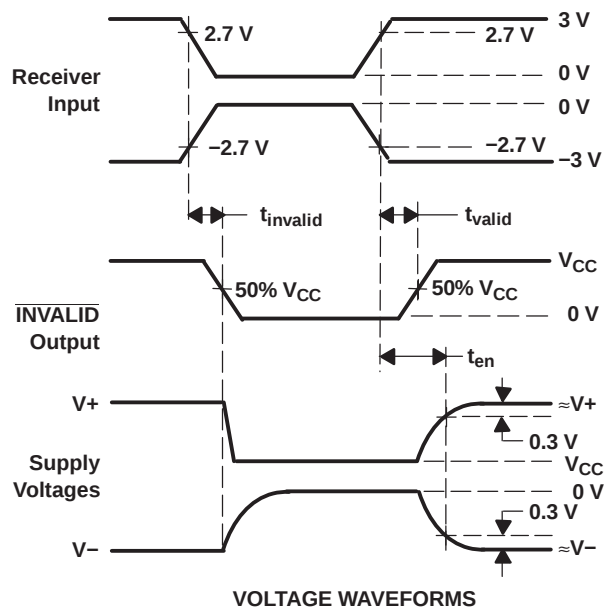
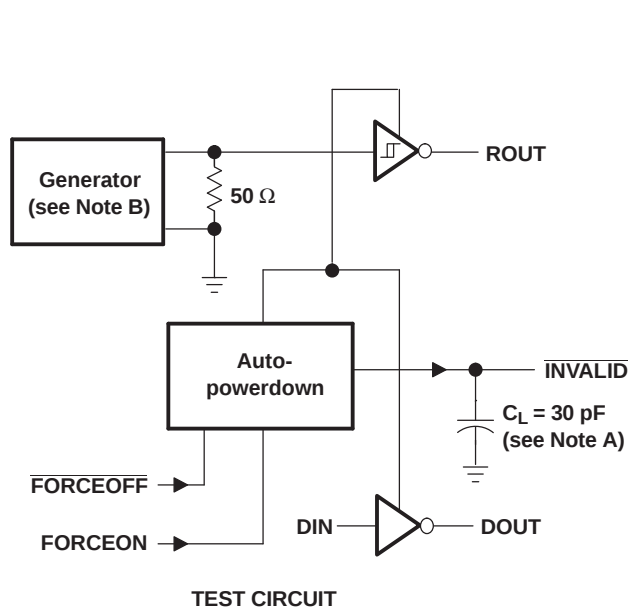


VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.
 C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 D. t_{PZL} and t_{PZH} are the same as t_{en} .

Figure 4. Receiver Enable and Disable Times

PARAMETER MEASUREMENT INFORMATION



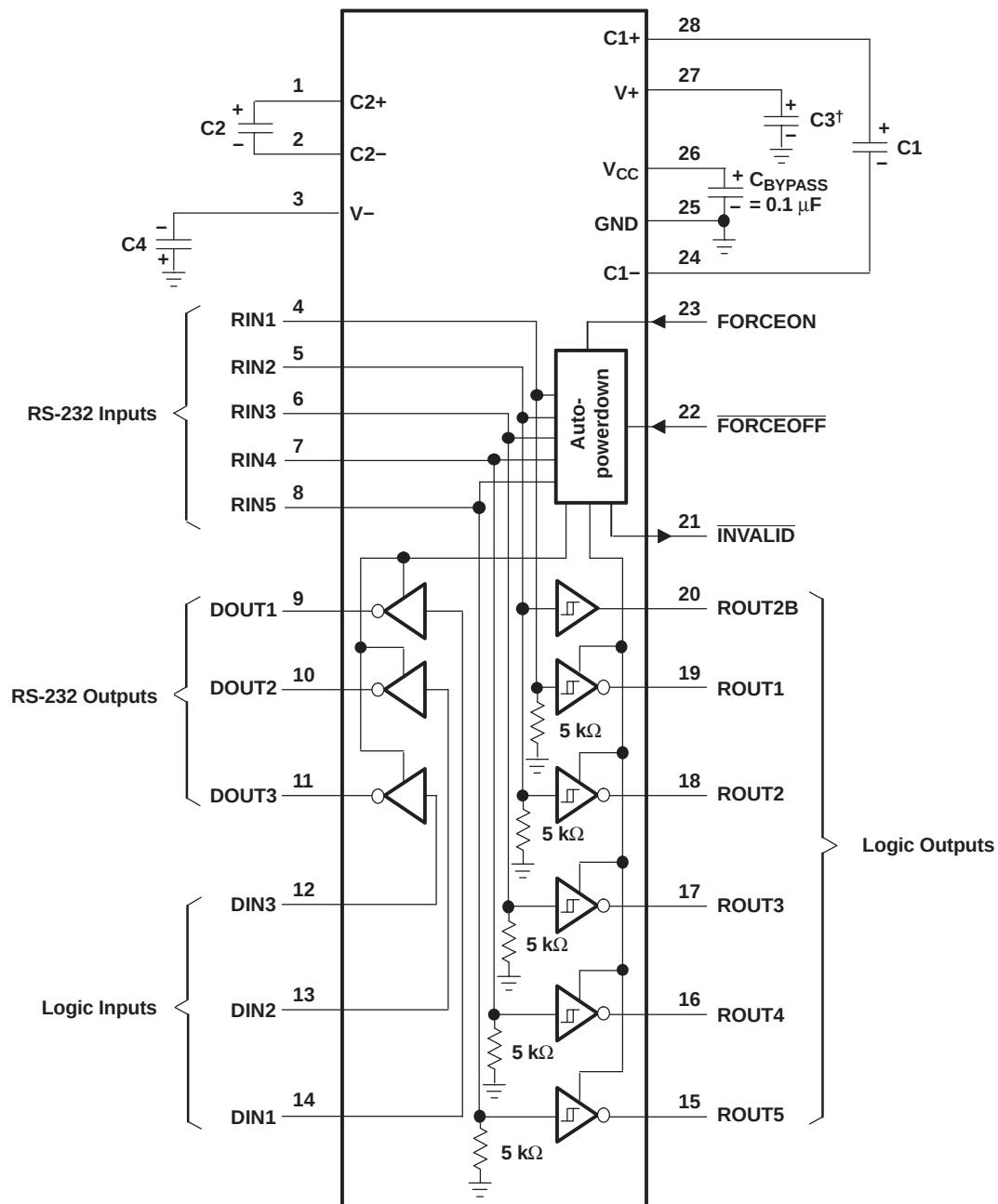
[†] Auto-powerdown disables drivers and reduces supply current to 1 μA .

NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 5 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

Figure 5. $\overline{\text{INVALID}}$ Propagation Delay Times and Supply Enabling Time

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V $\pm$ 0.3 V	0.1 μ F	0.1 μ F
5 V $\pm$ 0.5 V	0.047 μ F	0.33 μ F
3 V to 5.5 V	0.1 μ F	0.47 μ F

Figure 6. Typical Operating Circuit and Capacitor Values

APPLICATION INFORMATION

ESD Protection

TI TRS3243E devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ± 15 -kV in all states: normal operation, shutdown, and powered down. The TRS3243E devices are designed to continue functioning properly after an ESD occurrence without any latchup.

The TRS3243E devices have three specified ESD limits on the driver outputs and receiver inputs, with respect to GND:

- ± 15 -kV Human-Body Model (HBM)
- ± 15 -kV IEC61000-4-2, Air-Gap Discharge (formerly IEC1000-4-2)
- ± 8 -kV IEC61000-4-2, Contact Discharge

ESD Test Conditions

ESD testing is stringently performed by TI, based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

Human-Body Model (HBM)

The HBM of ESD testing is shown in Figure 7, while Figure 8 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the DUT through a 1.5-k Ω resistor.

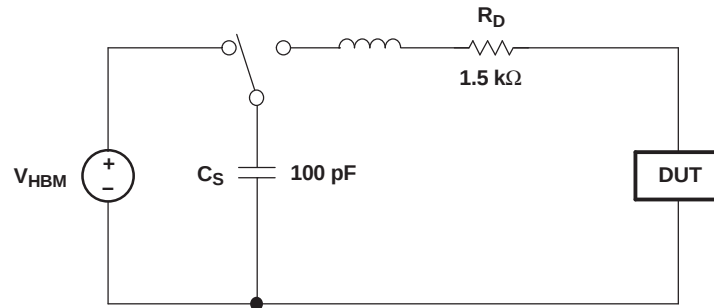


Figure 7. HBM ESD Test Circuit

APPLICATION INFORMATION

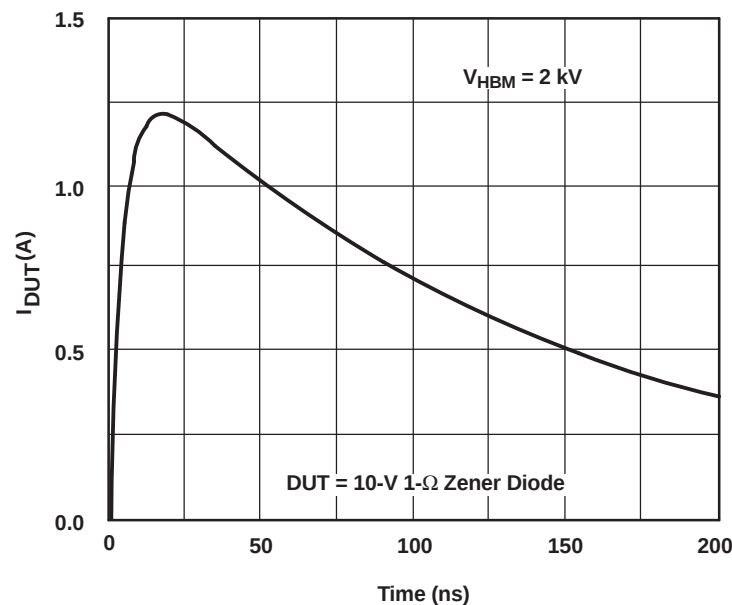


Figure 8. Typical HBM Current Waveform

IEC61000-4-2 (Formerly Known as IEC1000-4-2)

Unlike the HBM, MM, and CDM ESD tests that apply to component level integrated circuits, the IEC61000-4-2 is a system-level ESD testing and performance standard that pertains to the end equipment. The TRS3243E is designed to enable the manufacturer in meeting the highest level (Level 4) of IEC61000-4-2 ESD protection with no further need of external ESD protection circuitry. The more stringent IEC test standard has a higher peak current than the HBM, due to the lower series resistance in the IEC model.

Figure 9 shows the IEC61000-4-2 model, and Figure 10 shows the current waveform for the corresponding ± 8 -kV contact-discharge (Level 4) test. This waveform is applied to a probe that has been connected to the DUT. On the other hand, the corresponding ± 15 -kV (Level 4) air-gap discharge test involves approaching the DUT with an already energized probe.

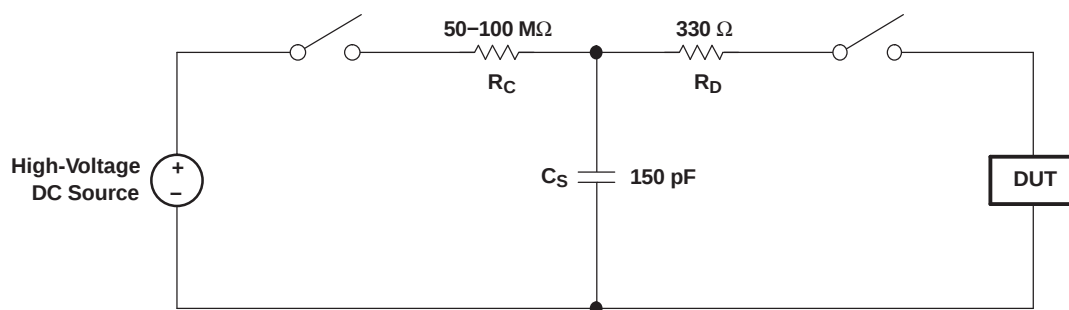


Figure 9. Simplified IEC61000-4-2 ESD Test Circuit

APPLICATION INFORMATION

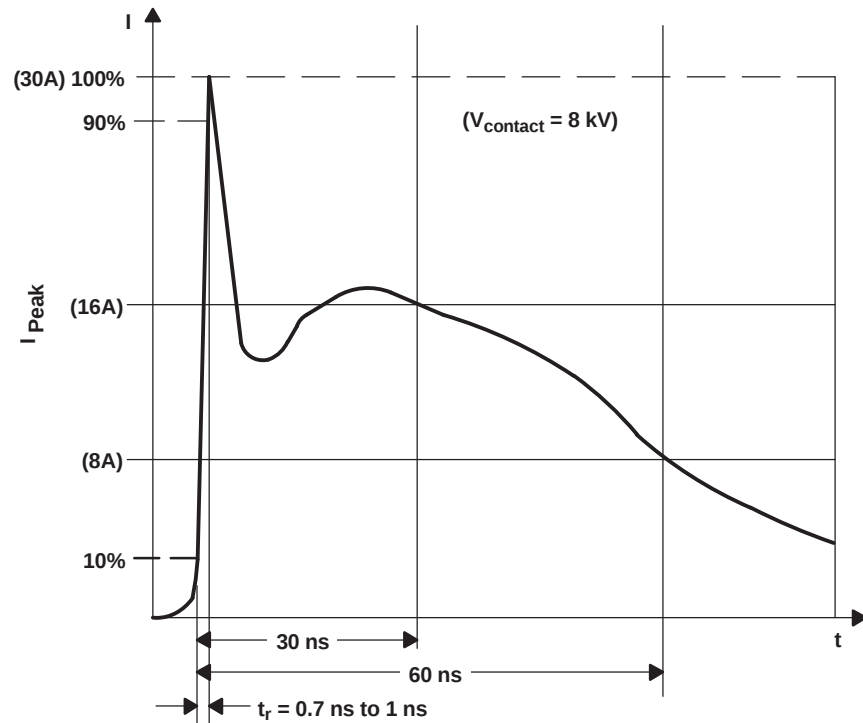


Figure 10. Typical Current Waveform of IEC61000-4-2 ESD Generator

Machine Model (MM)

The MM ESD test applies to all pins using a 200-pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test is no longer as pertinent to the RS-232 pins.

REVISION HISTORY

Changes from Revision B (July 2009) to Revision C	Page
• Deleted "VALID RIN RS-232 LEVEL" from INPUTS.	3
• Deleted "ROUT2B is active" RECEIVER STATUS and combined ROUT outputs.	3
• Added New Table "ROUT2B and <u>INVALID</u> Outputs" defining truth table for ROUT2B and INVALID outputs.	3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TRS3243ECDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243EC	Samples
TRS3243ECDBG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243EC	Samples
TRS3243ECDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243EC	Samples
TRS3243ECDBG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243EC	Samples
TRS3243ECDW	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243EC	Samples
TRS3243ECDWG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243EC	Samples
TRS3243ECDWR	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243EC	Samples
TRS3243ECDWRG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243EC	Samples
TRS3243ECPW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RS43EC	Samples
TRS3243ECPWG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RS43EC	Samples
TRS3243ECPWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RS43EC	Samples
TRS3243ECPWRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RS43EC	Samples
TRS3243ECRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	RS43EC	Samples
TRS3243ECRHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	RS43EC	Samples
TRS3243EIDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI	Samples
TRS3243EIDBG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI	Samples
TRS3243EIDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TRS3243EIDBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI	Samples
TRS3243EIDW	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI	Samples
TRS3243EIDWG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI	Samples
TRS3243EIDWR	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI	Samples
TRS3243EIDWRG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI	Samples
TRS3243EIPW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS43EI	Samples
TRS3243EIPWG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS43EI	Samples
TRS3243EIPWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS43EI	Samples
TRS3243EIPWRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS43EI	Samples
TRS3243EIRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	RS43EI	Samples
TRS3243EIRHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	RS43EI	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3243ECDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TRS3243ECDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
TRS3243ECRHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TRS3243EIDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TRS3243EIDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
TRS3243EIRHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

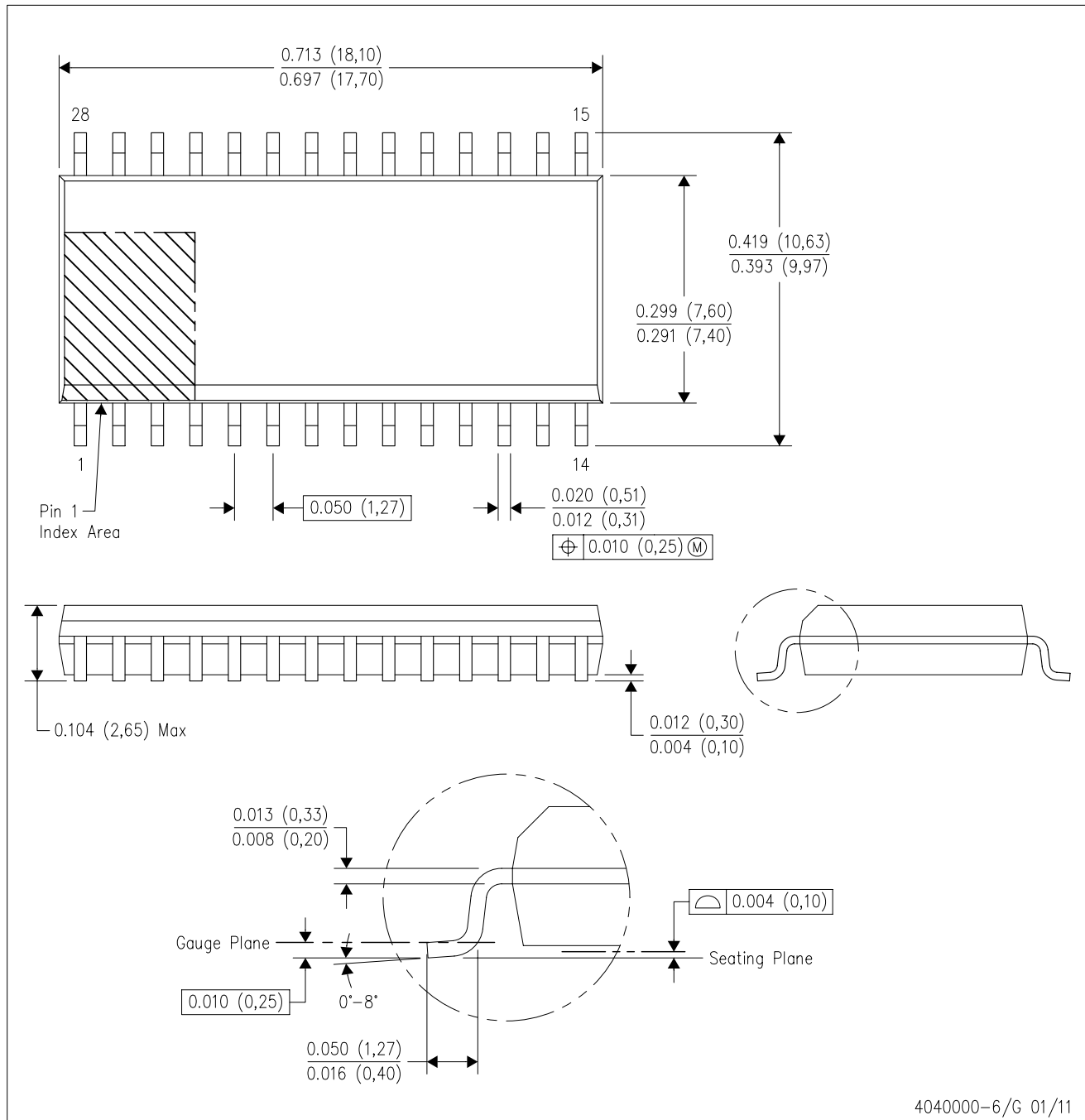


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3243ECDBR	SSOP	DB	28	2000	367.0	367.0	38.0
TRS3243ECDWR	SOIC	DW	28	1000	367.0	367.0	55.0
TRS3243ECRHBR	QFN	RHB	32	3000	367.0	367.0	35.0
TRS3243EIDBR	SSOP	DB	28	2000	367.0	367.0	38.0
TRS3243EIDWR	SOIC	DW	28	1000	367.0	367.0	55.0
TRS3243EIRHBR	QFN	RHB	32	3000	367.0	367.0	35.0

DW (R-PDSO-G28)

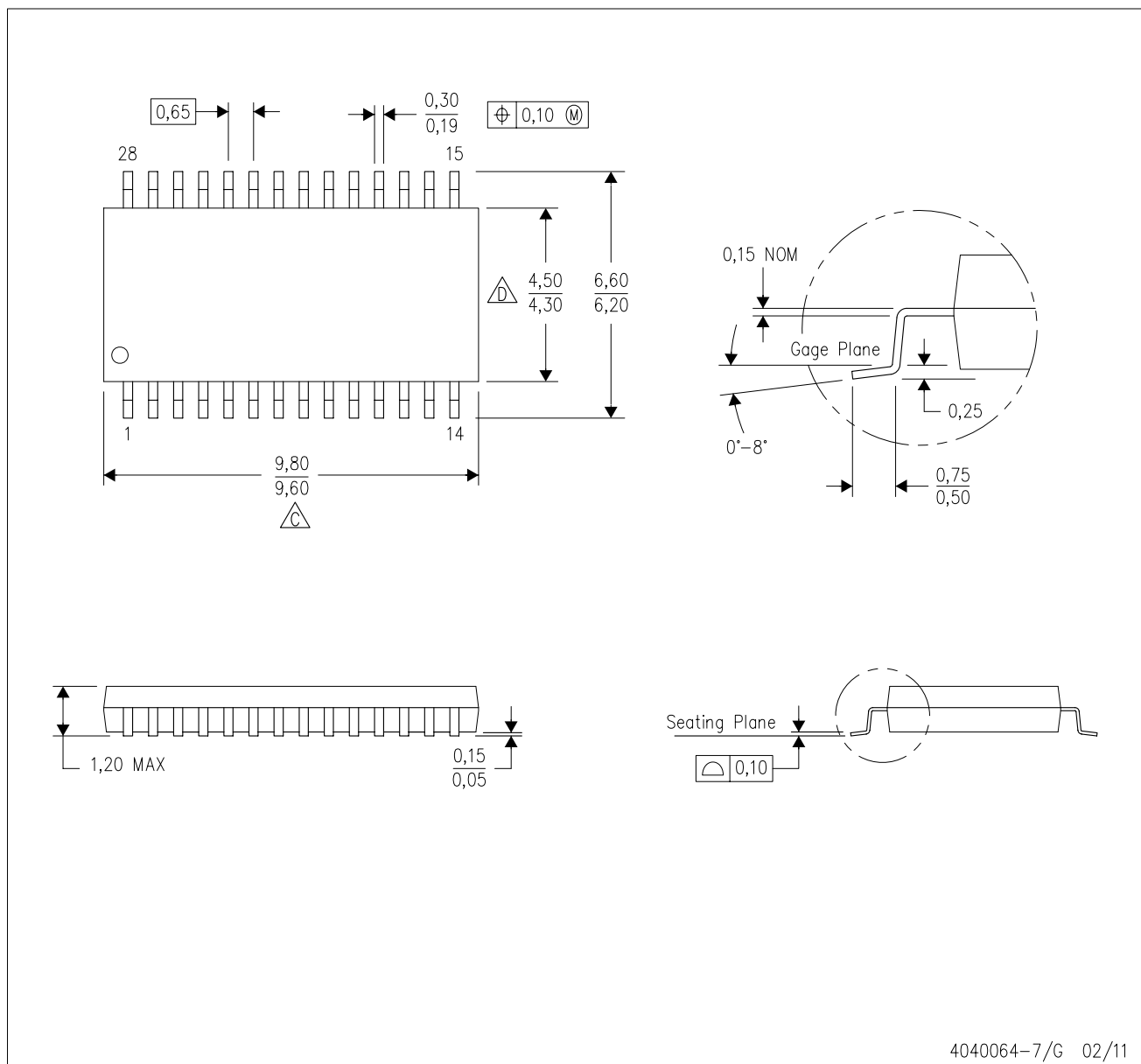
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AE.

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

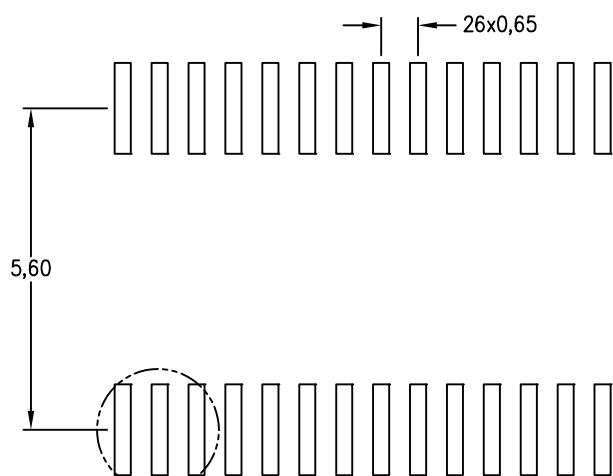


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

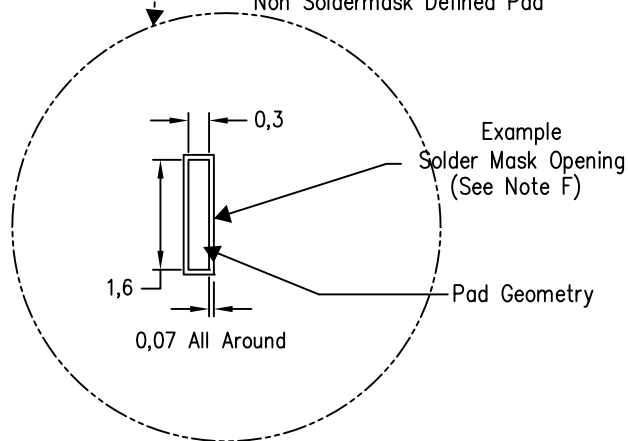
PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

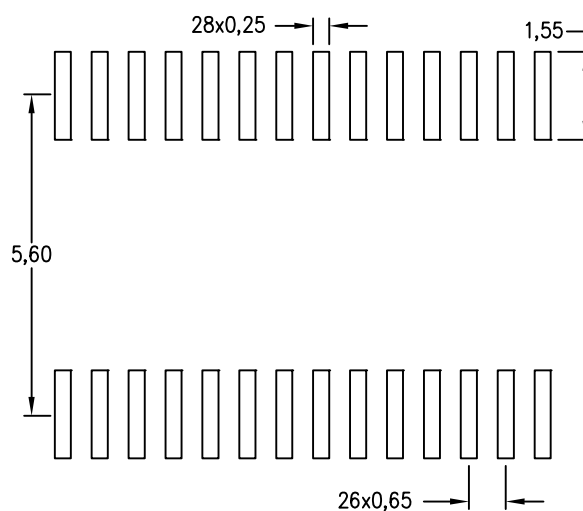
Example Board Layout



Example
Non Soldermask Defined Pad



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



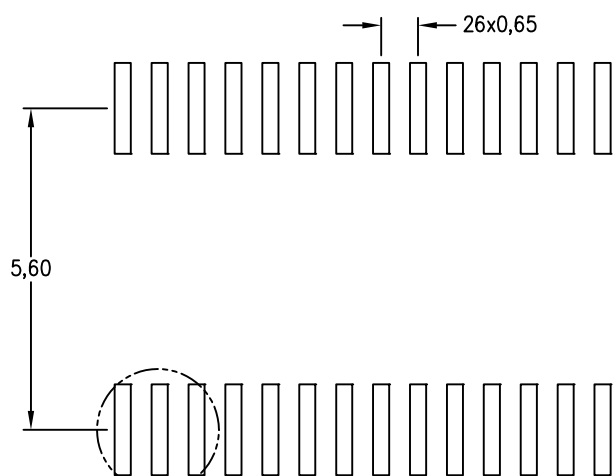
4211284-6/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

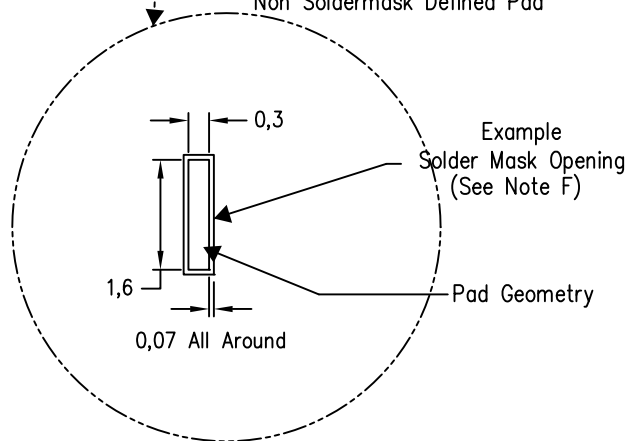
PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

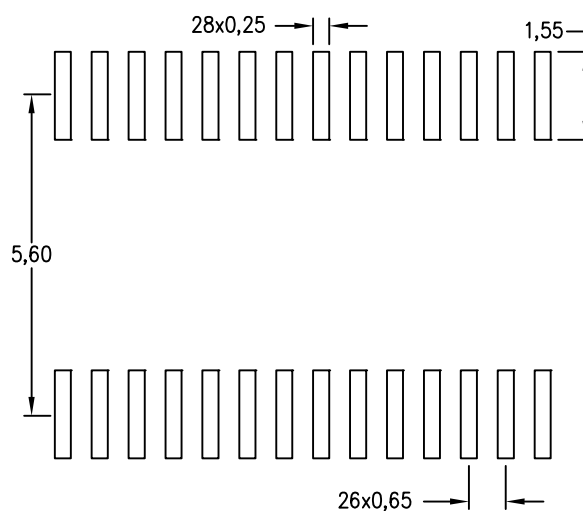
Example Board Layout



Example
Non Soldermask Defined Pad



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

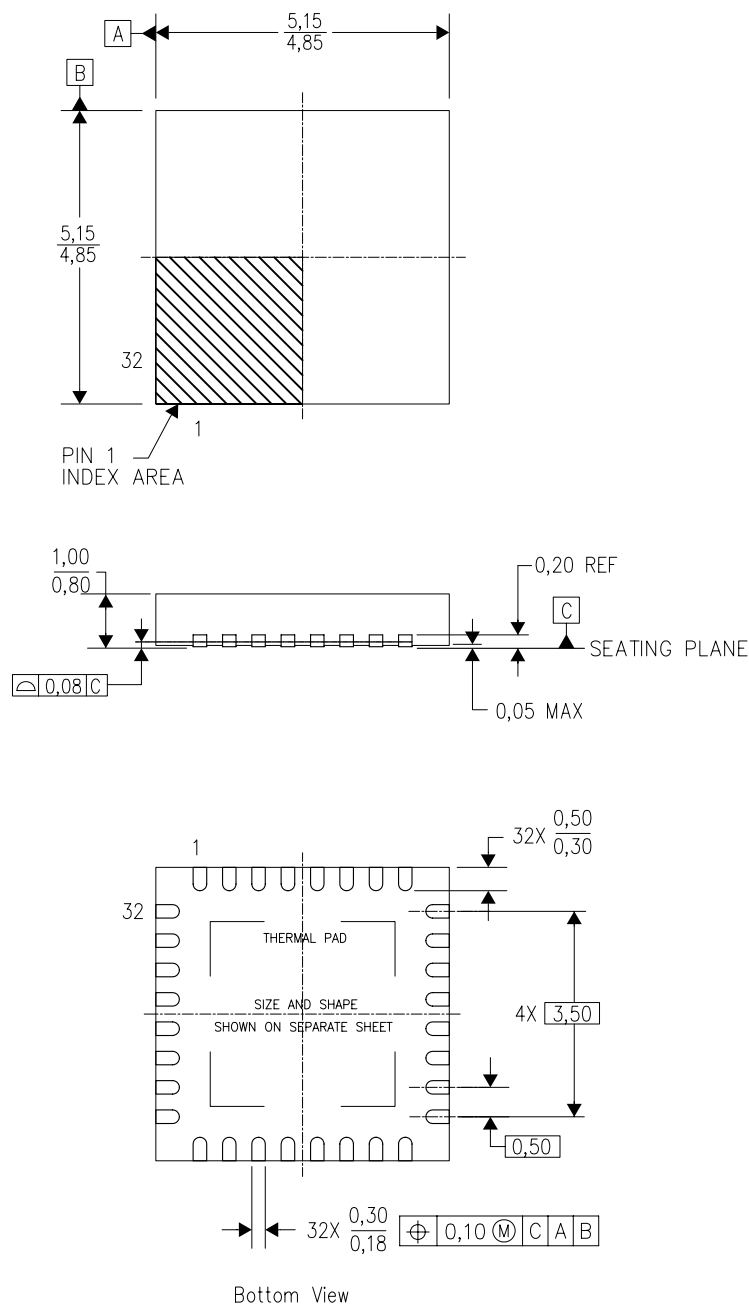


4211284-6/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



4204326/D 06/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) Package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

RHB (S-PVQFN-N32)

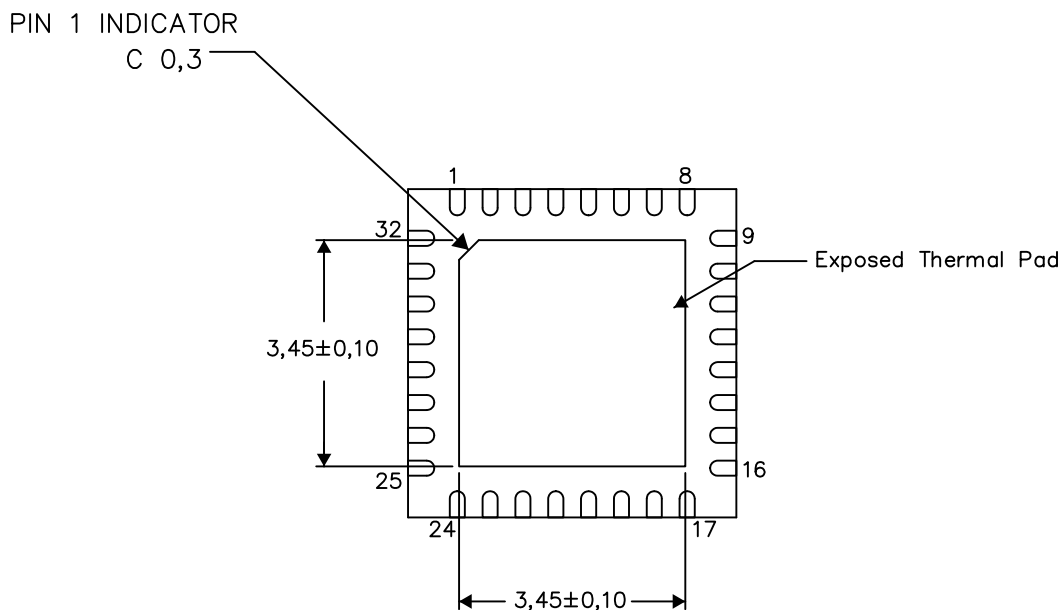
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

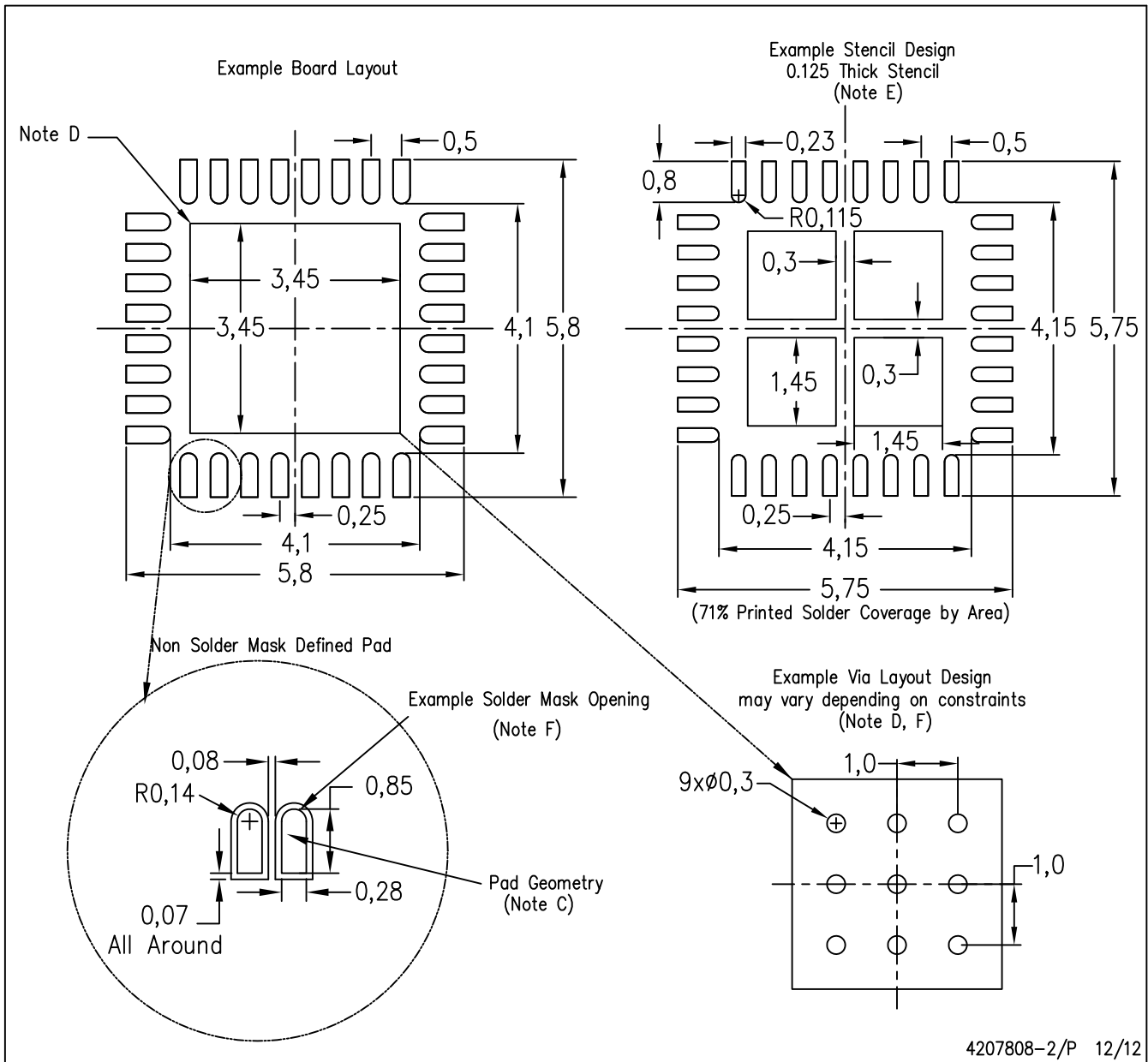
Exposed Thermal Pad Dimensions

4206356-2/X 12/12

NOTE: A. All linear dimensions are in millimeters

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



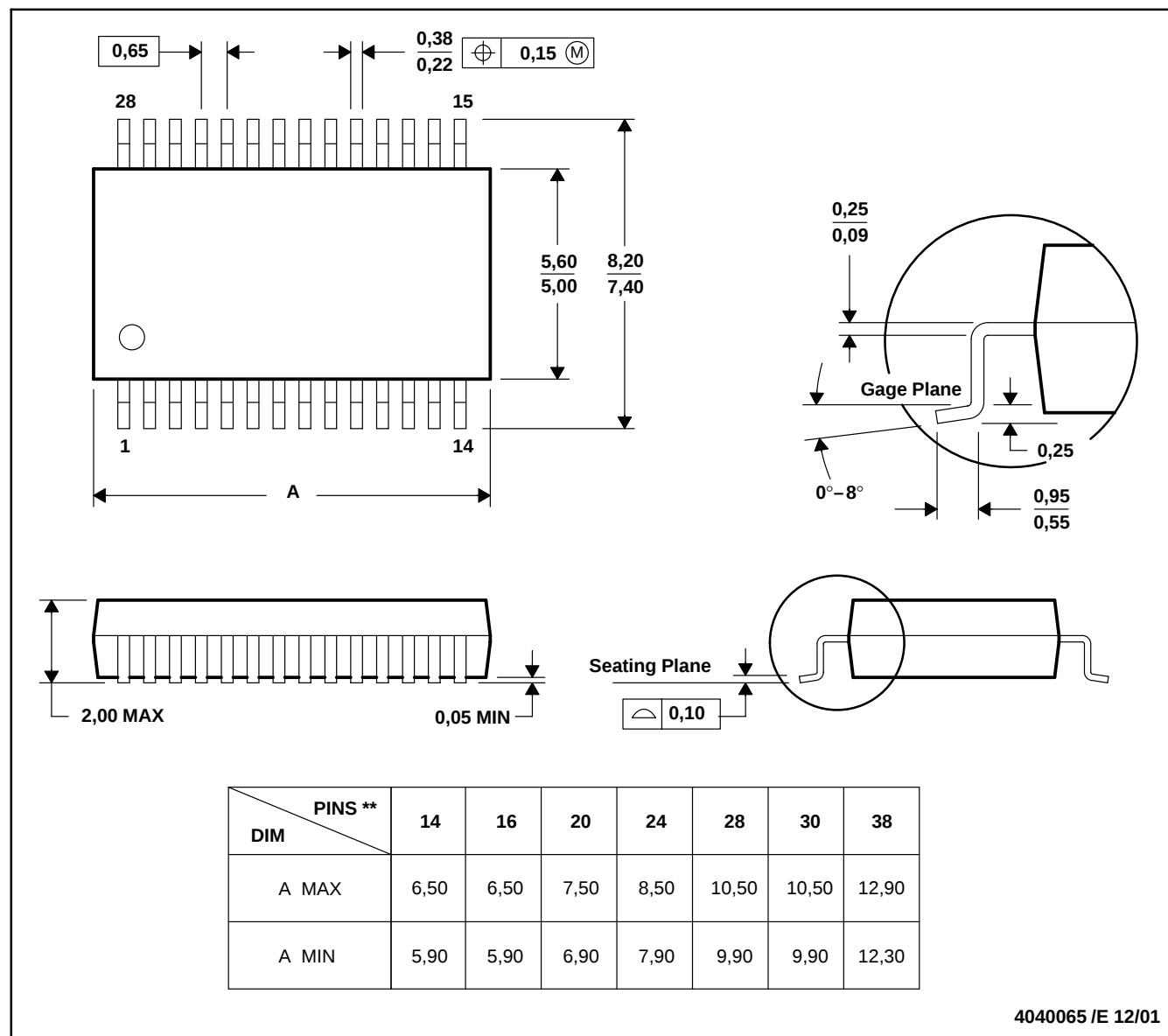
4207808-2/P 12/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com