PMIC FOR E Ink® Vizplex™ ENABLED ELECTRONIC PAPER DISPLAY

Check for Samples: TPS65182, TPS65182B

FEATURES

- **Single Chip Power Management Solution for E Ink® Vizplex™ Electronic Paper Displays**
- **Generates Positive and Negative Gate and Source Driver Voltages and Back-Plane Bias from a Single, Low-Voltage Input Supply**
- **3-V to 6-V Input Voltage Range**
- **Boost Converter for Positive Rail Base**
- **Inverting Buck-Boost Converter for Negative Rail Base**
- **Two Adjustable LDOs for Source Driver Supply**
  - **LDO1: 15 V, 120 mA (VPOS)**
  - **LDO2: –15 V, 120 mA (VNEG)**
- **Accurate Output Voltage Tracking**
  - **VPOS - VNEG = ±50 mV**
- **Two Charge Pumps for Gate Driver Supply**
  - **CP1: 22 V, 10 mA (VDDH)**
  - **CP2: –20 V, 12 mA, (VEE)**
- **Adjustable VCOM Driver for Accurate Panel-Backplane Biasing**
  - **–0.3 V to –2.5 V**
  - **Adjustable Through External Potentiometer**
  - **15-mA Max Integrated Switch**
- **Thermistor Monitoring**
  - **–10°C to 85°C Temperature Range**
  - **±1°C Accuracy from 0°C to 50°C**
- **I²C Serial Interface**
  - **Slave Address 0x48h (1001000)**
- **Flexible Power-Up Sequencing**
- **Sleep Mode Support**
- **Thermally Enhanced Package for Efficient Heat Management (48-Pin 7 mm x 7 mm x 0.9 mm QFN)**

APPLICATIONS

- **Power Supply for Active Matrix E Ink® Vizplex™ Panels**
- **E-Book Readers**
- **EPSON® S1D13522 (ISIS) Timing Controller**
- **EPSON® S1D13521 (Broadsheet) Timing Controller**
- **Application Processors With Integrated or Software Timing Controller (OMAP™)**

DESCRIPTION

The TPS65182/TPS65182B device is a single-chip power supplies designed to for E Ink® Vizplex™ displays used in portable e-reader applications and support panel sizes up to 9.7 inches. Two high efficiency DC/DC boost converters generate ±17-V rails which are boosted to 22 V and –20 V by two change pumps to provide the gate driver supply for the Vizplex™ panel. Two tracking LDOs create the ±15-V source driver supplies which support up to 120-mA of output current. All rails are adjustable through the I²C interface to accommodate specific panel requirements.

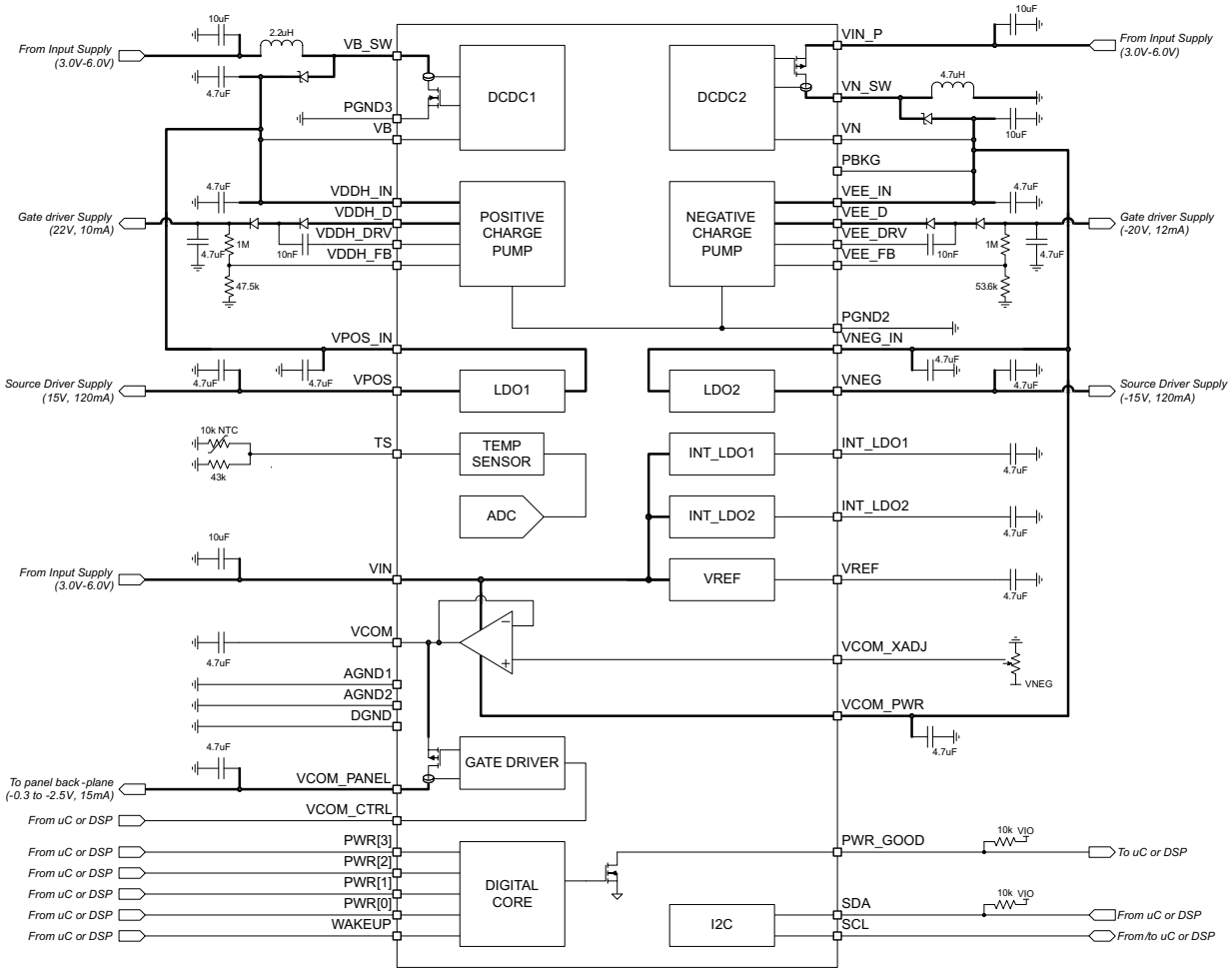
Accurate back-plane biasing is provided by a linear amplifier and can be adjusted either by an external resistor or the I²C interface. The VCOM driver can source or sink current depending on panel condition.

The TPS65182/TPS65182B provides precise temperature measurement function to monitor the panel temperature during operation. The temperature reading is updated every 60 s and can be accessed through the I²C interface.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-10°C to 85°C	RGZ	TPS65182RGZR	TPS65182
		TPS65182BRGZR	TPS65182B

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

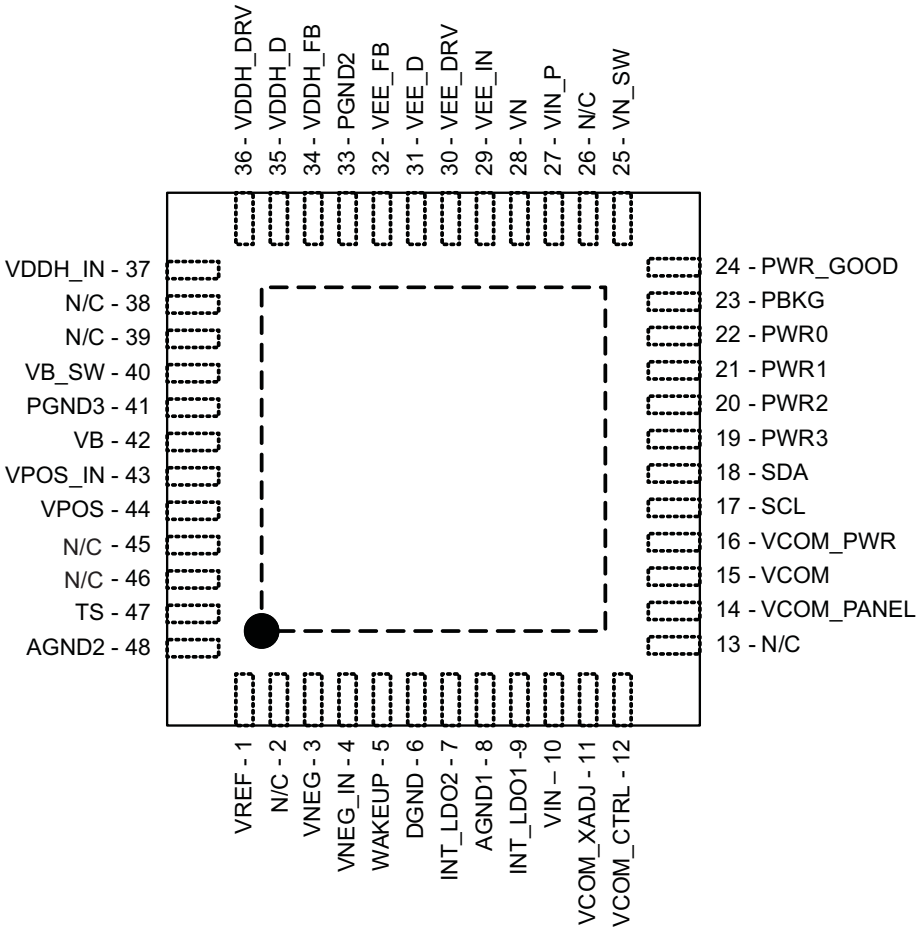
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

SELECTION GUIDE

DEVICE	PART NUMBER	STATUS
TPS6518	TPS65182RGZR	Not recommended for new designs
TPS6518B	TPS65182BRGZR	Active

DEVICE INFORMATION

RGZ PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS[1]

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VREF	1	O	Filter pin for 2.25-V internal reference to ADC
N/C	2		Not connected
VNEG	3	O	Negative supply output pin for panel source drivers
VNEG_IN	4	I	Input pin for LDO2 (VNEG)
WAKEUP	5	I	Wake up pin (active high). Pull this pin high to wake up from sleep mode.
DGND	6		Digital ground
INT_LDO2	7	O	Internal supply (digital circuitry) filter pin
AGND1	8		Analog ground for general analog circuitry
INT_LDO1	9	O	Internal supply (analog circuitry) filter pin
VIN	10	I	Input power supply to general circuitry
VCOM_XADJ	11	I	Analog input for conventional VCOM setup method. Tie this pin to ground if VCOM is set through I^2C interface.
VCOM_CTRL	12	I	VCOM_PANEL gate driver enable (active high)
N/C	13		Not connected

(1) There will be 0-ns, 93.75-µs, 62.52-µs of deglitch for PWRx, WAKEUP, and VCOM_CTRL, respectively.

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VCOM_PANEL	14	O	Panel common-voltage output pin
VCOM	15	O	Filter pin for panel common-voltage driver
VCOM_PWR	16	I	Internal supply input pin to VCOM buffer. Connect to the output of DCDC2.
SCL	17	I	Serial interface (I^2C) clock input
SDA	18	I/O	Serial interface (I^2C) data input/output
PWR3	19	I	Enable pin for CP1 (VDDH) (active high)
PWR2	20	I	Enable pin for LDO1 (VPOS) (active high)
PWR1	21	I	Enable pin for CP2 (VEE) (active high)
PWR0	22	I	Enable pin for LDO2 (VNEG) and VCOM (active high)
PWR_GOOD	24	O	Open drain power good output pin (active low)
VN_SW	25	O	Inverting buck-boost converter switch out (DCDC2)
N/C	26		Not connected
VIN_P	27	I	Input power supply to inverting buck-boost converter (DCDC2)
VN	28	I	Feedback pin for inverting buck-boost converter (DCDC2)
VEE_IN	29	I	Input supply pin for CP1 (VEE)
VEE_DRV	30	O	Driver output pin for negative charge pump (CP2)
VEE_D	31	O	Base voltage output pin for negative charge pump (CP2)
VEE_FB	32	I	Feedback pin for negative charge pump (CP2)
PGND2	33		Power ground for CP1 (VDDH) and CP2 (VEE) charge pumps
VDDH_FB	34	I	Feedback pin for positive charge pump (CP1)
VDDH_D	35	O	Base voltage output pin for positive charge pump (CP1)
VDDH_DRV	36	O	Driver output pin for positive charge pump (CP1)
VDDH_IN	37	I	Input supply pin for positive charge pump (CP1)
N/C	38		Not connected
N/C	39		Not connected
VB_SW	40	O	Boost converter switch out (DCDC1)
PGND3	41		Power ground for DCDC1
VB	42	I	Feedback pin for boost converter (DCDC1)
VPOS_IN	43	I	Input pin for LDO1 (VPOS)
VPOS	44	O	Positive supply output pin for panel source drivers
N/C	45		Not connected
N/C	46		Not connected
TS	47	I	Thermistor input pin. Connect a 10k NTC thermistor and a 43k linearization resistor between this pin and AGND2.
AGND2	48		Reference point to external thermistor and linearization resistor
PowerPad (PBKG)	23		Die substrate/thermal pad. Connect to VN with short, wide trace. Wide copper trace will improve heat dissipation. PowerPad must not be connected to ground.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)(2)

			VALUE	UNIT
	Input voltage range at VIN, VINP		–0.3 to 7	V
	Ground pins to system ground		–0.3 to 0.3	V
	Voltage range at SDA, SCL, WAKEUP, PWR3, PWR2, PWR1, PWR0, VCOM_CTRL, VDDH_FB, VEE_FB, PWR_GOOD		–0.3 to 3.6	V
	VCOM_XADJ		–3.6 to 0.3	V
	Voltage on VB, VB_SW, VPOS_IN, VDDH_IN		–0.3 to 20	V
	Voltage on VN, VNEG_IN, VEE_IN, VCOM_PWR		–20 to 0.3	V
	Voltage from VINP to VN_SW		–0.3 to 30	V
	Peak output current		Internally limited	mA
	Continuous total power dissipation		2	W
θ_{JA}	Junction-to-ambient thermal resistance(3)		23	°C/W
T_J	Operating junction temperature		-10 to 125	°C
T_A	Operating ambient temperature(4)		-10 to 85	°C
T_{stg}	Storage temperature		-65 to 150	°C
	ESD rating	(HBM) Human body model	±2000	V
		(CDM) Charged device model	±500	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Estimated when mounted on high K JEDEC board per JESD 51-7 with thickness of 1.6 mm, 4 layers, size of 76.2 mm X 114.3 mm, and 2 oz. copper for top and bottom plane. Actual thermal impedance will depend on PCB used in the application.
(4) It is recommended that copper plane in proper size on board be in contact with die thermal pad to dissipate heat efficiently. Thermal pad is electrically connected to PBKG, which is supposed to be tied to the output of buck-boost converter. Thus wide copper trace in the buck-boost output will help heat dissipated efficiently.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Input voltage range at VIN, VINP	3	3.7	6	V
	Voltage range at SDA, SCL, WAKEUP, PWR3, PWR2, PWR1, PWR0, VCOM_CTRL, VDDH_FB, VEE_FB, VCOM_XADJ, PWR_GOOD	0		3.6	V
T_A	Operating ambient temperature range	–10		85	°C
T_J	Operating junction temperature range	–10		125	°C

RECOMMENDED EXTERNAL COMPONENTS

PART NUMBER	VALUE	SIZE	MANUFACTURER
INDUCTORS			
LQH44PN4R7MP0	4.7 µH	4 mm x 4 mm x 1.65 mm	Murata
VLS252012T-2R2M1R3	2.2 µH	2 mm x 2.5 mm x 1.2 mm	TDK
CAPACITORS			
GRM21BC81E475KA12L	4.7 µF, 25 V, X6S	805	Murata
GRM32ER71H475KA88L	4.7 µF, 50 V, X7R	1210	Murata
All other caps	X5R or better		
DIODES			
BAS3010		SOD-323	Infineon
MBR130T1		SOD-123	ON-Semi
THERMISTOR			
NCP18XH103F03RB	10 KΩ	603	Murata

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.7 V, T_A = –10°C to 85ºC, Typical values are at T_A = 25ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE						
V_{IN}	Input voltage range		3	3.7	6	V
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling		2.9		V
V_{HYS}	Undervoltage lockout hysteresis	V_{IN} rising		400		mV
INPUT CURRENT						
I_Q	Operating quiescent current into VIN	Device switching, no load		5.5		mA
I_{STD}	Operating quiescent current into VIN	Device in standby mode		130		µA
I_{SLEEP}	Shutdown current	Device in sleep mode		2.8	10	µA
INTERNAL SUPPLIES						
VI_{NT_LDO1}	Internal supply			2.7		V
V_{INT_LDO2}	Internal supply			2.7		V
V_{REF}	Internal supply			2.25		V
DCDC1 (POSITIVE BOOST REGULATOR)						
V_{IN}	Input voltage range		3	3.7	6	V
V_{OUT}	Output voltage range			17		V
	DC set tolerance		-5		5	%
I_{OUT}	Output current				160	mA
$R_{DS(ON)}$	MOSFET on resistance	V_{IN} = 3.7 V		350		mΩ
I_{LIMIT}	Switch current limit			1.5		A
	Switch current accuracy		-30		30	%
f_{SW}	Switching frequency			1		MHz
L	Inductor			2.2		µH
C	Capacitor			2x4.7		µF
ESR	Capacitor ESR			20		mΩ
DCDC2 (INVERTING BUCK-BOOST REGULATOR)						
V_{IN}	Input voltage range		3	3.7	6	V
V_{OUT}	Output voltage range			-17		V
	DC set tolerance		-5		5	%
I_{OUT}	Output current				160	mA
$R_{DS(ON)}$	MOSFET on resistance	V_{IN} = 3.7 V		350		mΩ
I_{LIMIT}	Switch current limit			1.5		A
	Switch current accuracy		-30		30	%
L	Inductor			4.7		µH
C	Capacitor			2x4.7		µF
ESR	Capacitor ESR			20		mΩ
LDO1 (VPOS)						
V_{POS_IN}	Input voltage range		16.15	17	17.85	V
V_{SET}	Output voltage set value	V_{IN} = 17 V	14.25	15	15.75	V
$V_{INTERVAL}$	Output voltage set resolution	V_{IN} = 17 V		250		mV
V_{POS_OUT}	Output voltage range	V_{SET} = 15 V, I_{LOAD} = 20 mA	14.85	15	15.15	V
V_{OUTTOL}	Output tolerance	V_{SET} = 15 V, I_{LOAD} = 20 mA	-1		1	%
$V_{DROPOUT}$	Dropout voltage	I_{LOAD} = 120 mA			250	mV
$V_{LOADREG}$	Load regulation – DC	I_{LOAD} = 10% to 90%			1	%
I_{LOAD}	Load current range			120		mA
I_{LIMIT}	Output current limit		200			mA
T_{SS}	Soft start time			1		ms

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 3.7 V, T_A = –10°C to 85ºC, Typical values are at T_A = 25ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C	Recommended output capacitor			4.7		µF
LDO2 (VNEG)						
V_{NEG_IN}	Input voltage range		-17.85	-17	-16.15	V
V_{SET}	Output voltage set value	V_{IN} = –17 V	-15.75	-15	-14.25	V
$V_{INTERVAL}$	Output voltage set resolution	V_{IN} = –17 V		250		mV
V_{NEG_OUT}	Output voltage range	V_{SET} = –15 V, I_{LOAD} = –20 mA	-15.15	-15	-14.85	V
V_{OUTTOL}	Output tolerance	V_{SET} = –15 V, I_{LOAD} = –20 mA	-1		1	%
$V_{DROPOUT}$	Dropout voltage	I_{LOAD} = 120 mA			250	mV
$V_{LOADREG}$	Load regulation – DC	I_{LOAD} = 10% to 90%			1	%
I_{LOAD}	Load current range			120		mA
I_{LIMIT}	Output current limit		200			mA
T_{SS}	Soft start time			1		ms
C	Recommended output capacitor			4.7		µF
LD01 (POS) AND LDO2 (VNEG) TRACKING						
V_{DIFF}	Difference between VPOS and VNEG	V_{SET} = ±15 V, I_{LOAD} = ±20 mA, 0°C to 60°C	-50		50	mV
VCOM DRIVER						
V_{COM}	Output voltage range		-2.5		-0.3	V
G	V_{COM} gain (V_{COM_XADJ}/V_{COM})	V_{COM_ADJ} = 0 V		1		V/V
VCOM SWITCH						
T_{ON}	Switch ON time	V_{COM} = –1.25 V, V_{COM_PANEL} = 0 V C_{VCOM} = 4.7 µF, C_{VCOM_PANEL} = 4.7 µF			1	ms
$R_{DS(ON)}$	MOSFET ON resistance	V_{COM} = –1.25 V, I_{COM} = 30 mA		20	35	Ω
I_{LIMIT}	MOSFET current limit	Not tested in production		200		mA
I_{SWLEAK}	Switch leakage current	V_{COM} = 0 V, V_{COM_PANEL} = –2.5 V			8.3	nA
CP1 (VDDH) CHARGE PUMP						
V_{DDH_IN}	Input voltage range		16.15	17	17.85	V
V_{FB}	Feedback voltage			1		V
	Accuracy		-3		3	%
V_{DDH_OUT}	Output voltage range	V_{SET} = 22 V, I_{LOAD} = 2 mA	21	22	23	V
I_{LOAD}	Load current range				10	mA
f_{SW}	Switching frequency			560		KHz
C_D	Recommended driver capacitor			10		nF
C_O	Recommended output capacitor			4.7		µF
CP2 (VEE) NEGATIVE CHARGE PUMP						
V_{EE_IN}	Input voltage range		-17.75	-17	-16.15	V
V_{FB}	Feedback voltage			-1		V
	Accuracy		-3		3	%
V_{EE_OUT}	Output voltage range	V_{SET} = –20 V, I_{LOAD} = 3 mA	-21	-20	-19	V
I_{LOAD}	Load current range				12	mA
f_{SW}	Switching frequency			560		KHz
C_D	Recommended driver capacitor			10		nF
C_O	Recommended output capacitor			4.7		µF

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 3.7 V, T_A = –10°C to 85ºC, Typical values are at T_A = 25ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMISTOR MONITOR(1)						
A_{TMS}	Temperature to voltage ratio	Not tested in production		-0.0158		V/°C
$Offset_{TMS}$	Offset	Temperature = 0°C		1.575		V
V_{TMS_HOT}	Temp hot trip voltage (T = 50°C)	TEMP_HOT_SET = 0x8C		0.768		V
V_{TMS_COOL}	Temp hot escape voltage (T = 45°C)	TEMP_COOL_SET = 0x82		0.845		V
V_{TMS_MAX}	Maximum input level			2.25		V
R_{NTC_PU}	Internal pull up resistor			7.307		KΩ
R_{LINEAR}	External linearization resistor			43		KΩ
ADC_{RES}	ADC resolution	Not tested in production, 1 bit		16.1		mV
ADC_{DEL}	ADC conversion time	Not tested in production		19		µs
$TMST_{TOL}$	Accuracy	Not tested in production	-1		1	LSB
LOGIC LEVELS AND TIMING CHARTERISTICS (SCL, SDA, PWR_GOOD, PWRx, WAKEUP)						
V_{OL}	Output low threshold level	I_O = 3 mA, sink current (SDA, PWR_GOOD)			0.4	V
V_{IL}	Input low threshold level				0.4	V
V_{IH}	Input high threshold level		1.2			V
$I_{(bias)}$	Input bias current	V_{IO} = 1.8 V			1	µA
$t_{low,WAKEUP}$	WAKEUP low time	minimum low time for WAKEUP pin	150			ms
f_{SCL}	SCL clock frequency				400	KHz
OSCILLATOR						
f_{OSC}	Oscillator frequency			9		MHz
	Frequency accuracy	T_A = –40°C to 85°C	-10		10	%
THERMAL SHUTDOWN						
T_{SHTDWN}	Thermal trip point			150		°C
	Thermal hysteresis			20		°C

(1) 10-KΩ Murata NCP18XH103F03RB thermistor (1%) in parallel with a linearization resistor (43 KΩ, 1%) are used at TS pin for panel temperature measurement.

MODES OF OPERATION

The TPS65182/TPS65182B has three modes of operation, SLEEP, STANDBY, and ACTIVE. SLEEP mode is the lowest-power mode in which all internal circuitry is turned off. In STANDBY, all power rails are shut down but the device is ready to accept commands through PWR[3:0] pins and/or I^2C interface. In ACTIVE mode one or more power rails are enabled.

SLEEP

This is the lowest power mode of operation. All internal circuitry is turned off and the device does not respond to I^2C communications. TPS65182/TPS65182B enters SLEEP mode whenever WAKEUP pin is pulled low.

STANDBY

In STANDBY all internal support circuitry is powered up and the device is ready to accept commands either through GPIO or I^2C control but none of the power rails are enabled. To enter STANDBY mode the WAKEUP pin must be pulled high and all PWRx pins must be pulled low. The device also enters STANDBY mode if input under voltage lock out (UVLO), positive boost under voltage (VB_UV), or inverting buck-boost under voltage (VN_UV) is detected, or thermal shutdown occurs.

ACTIVE

The device is in ACTIVE mode when any of the output rails are enabled and no fault condition is present. This is the normal mode of operation while the device is powered up. In ACTIVE mode, a falling edge on any PWRx pin shuts down and a rising edge powers up the corresponding rail.

MODE TRANSISITONS

SLEEP → ACTIVE

WAKEUP pin is pulled high (rising edge) with any PWRx pin high. Rails come up in a pre-defined power-up sequence.

SLEEP → STANDBY

WAKEUP pin is pulled high (rising edge) with all PWRx pins low. Rails will remain down until one or more PWRx pin is pulled high.

ACTIVE → SLEEP

WAKEUP pin is pulled low (falling edge). Rails are shut down following the pre-defined power-down sequence.

ACTIVE → STANDBY

WAKEUP pin is high. All PWRx pins are pulled low (falling edge). Rails shut down in the order in which PWRx pins are pulled low. In the event of thermal shut down (TSD), under voltage lock out (UVLO), positive boost or inverting buck-boost under voltage (UV), the device shuts down all rails in a pre-defined power-down sequence.

STANDBY → ACTIVE

WAKEUP pin is high and any PWRx pin is pulled high (rising edge). Rails come up in the same order as PWRx pins are pulled high.

STANDBY → SLEEP

WAKEUP pin is pulled low (falling edge) while none of the output rails are enabled.

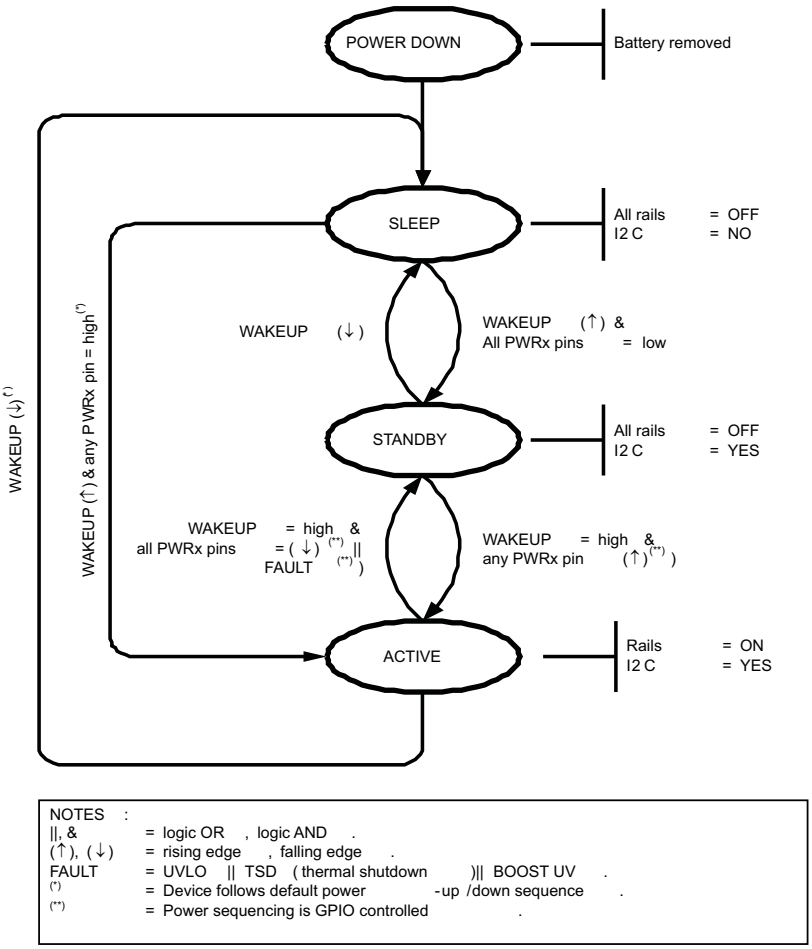


Figure 1. Global State Diagram

WAKE-UP AND POWER UP SEQUENCING

The TPS65182/TPS65182B supports a default power-up sequence supporting E Ink® Vizplex™ displays. It also offers full user control of the power-up sequence through GPIO control using the PWR3, 2, 1, 0 pins. Using GPIO control, the output rails are enabled/disabled in the order in which the PWRx pins are asserted/de-asserted, respectively, and the power-up timing is controlled by the host only. Rails are in regulation 2 ms after their respective PWRx pin has been asserted with the exception of the first rail, which takes 6 ms to power up. The additional time is needed to power up the positive and inverting buck-boost regulator which need to be turned on before any other rail can be enabled. Once all rails are enabled and in regulation the PWR_GOOD pin is released (pin status = HiZ and power good line is pulled high by external pull-up resistor). The PWRx pins are assigned to the rails as follows:

- PWR0: LDO2 (VNEG) and VCOM
- PWR1: CP2 (VEE)
- PWR3: LDO2 (VPOS)
- PWR4: CP1 (VDDH)

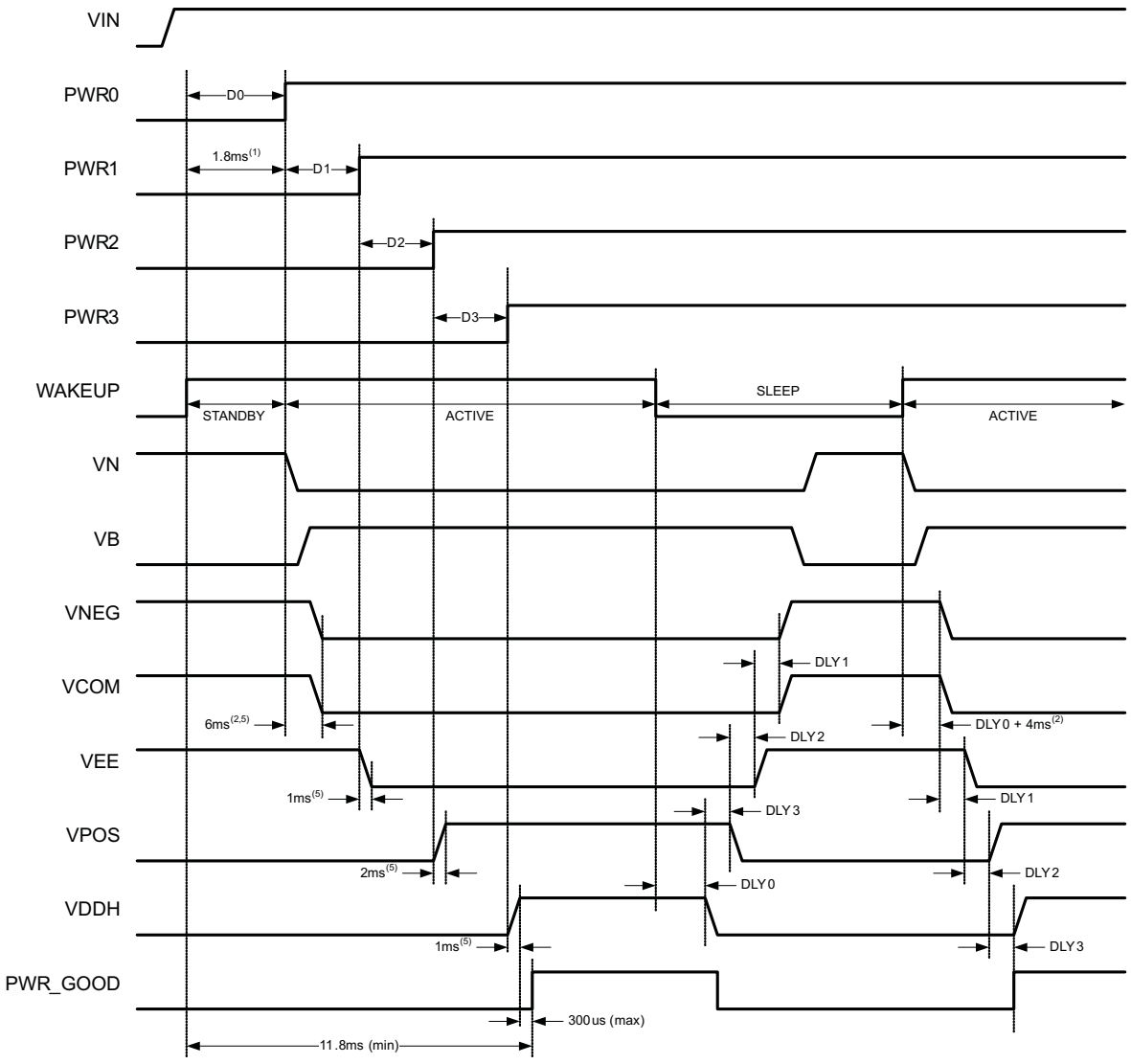
Rails are powered down whenever the host de-asserts the respective PWRx pin, and once all rails are disabled the device enters STANDBY mode. The next step is then to de-assert the WAKEUP pin to enter SLEEP mode which is the lowest-power mode of operation.

It is possible for the host to force the TPS65182/TPS65182B directly into SLEEP mode from ACTIVE mode by de-asserting the WAKEUP pin in which case the device follows the pre-defined power-down sequence before entering SLEEP mode.

DEPENDENCIES BETWEEN RAILS

Charge pumps, LDOs, and VCOM driver are dependent on the positive and inverting buck-boost converters and several dependencies exist that affect the power-up sequencing. These dependencies are listed below.

1. Inverting buck-boost (DCDC2) must be in regulation before positive boost (DCDC1) can be enabled. Internally, DCDC1 enable is gated by DCDC2 power good.
2. Positive boost (DCDC1) must be in regulation before LDO2 (VNEG) can be enabled. Internally LDO2 enable is gated DCDC1 power-good.
3. Positive boost (DCDC1) must be in regulation before VCOM can be enabled; Internally VCOM enable is gated by DCDC1 power good.
4. Positive boost (DCDC1) must be in regulation before negative charge pump (CP2) can be enabled. Internally CP2 enable is gated by DCDC1 power good.
5. Positive boost (DCDC1) must be in regulation before positive charge pump (CP1) can be enabled. Internally CP1 enable is gated by DCDC1 power good.
6. LDO2 must be in regulation before LDO1 can be enabled. Internally LDO1 enable is gated by LDO2 power good.
7. The minimum delay time between any two PWRx pins must be > 62.5 µs in order to follow the power up sequence defined by GPIO control. If any two PWRx pins are pulled up together (< 62.5 µs apart) rails will be staggered in a manner that a subsequent rail's enable is gated by PG of a preceding rail. In this case, the default order of power-up is LDO2 (VNEG), CP2 (VEE), LDO1 (VPOS), and CP1(VDDH). If any two PWRx pins are pulled low then all rails will go down at the same time.



(1) Minimum delay time between WAKEUP rising edge and IC rady to accept I 2C transaction.
(2) It takes 2ms minimum for each internal boost regulator to start up before VNEG can be enabled .
(5) It takes up to 2ms for LDOs (VPOS,VNEG) and 1ms for charge pumps (VDDH,VEE), to reach their steady state after being enabled.
DLY0-DLY3 are power up/down delays are factory-set to 2ms.

Figure 2. Power-Up and Power-Down Timing Diagram

SOFTSTART

Softstart for DCDC1, DCDC2, LDO1, and LDO2 is accomplished by lowering the current limits during start-up. If DCDC1 or DCDC2 are unable to reach power-good status within 10 ms, the device enters STANDBY mode.

VCOM ADJUSTMENT

VCOM can be adjusted by an external potentiometer by connecting a potentiometer to the VCOM_XADJ pin. The potentiometer must be connected between ground and a negative supply. The gain from VCOM_XADJ to VCOM is 1 and therefore the voltage applied to VCOM_XADJ pin should range from -0.3 to -2.5V.

VPOS / VNEG SUPPLY TRACKING

LDO1 (VPOS) and LDO2 (VNEG) track each other in a way that they are of opposite sign but same magnitude. The sum of VLDO1 and VLOD2 is guaranteed to be < 50 mV.

FAULT HANDLING AND RECOVERY

The TPS65182/TPS65182B monitors input and output voltages and die temperature and will take action if operating conditions are outside normal limits. Whenever the TPS65182/TPS65182B encounters:

- Thermal Shutdown (TSD)
- Positive Boost Under Voltage (VB_UV)
- Inverting Buck-Boost Under Voltage (VN_UV)
- Input Under Voltage Lock Out (UVLO)

it will shut down all power rails and enter STANDBY mode. Shut down follows the pre-defined power-down sequence and once a fault is detected, the PWR_GOOD pin is pulled low.

Whenver the TPS65182/TPS65182B encounters under voltage on VNEG (VNEG_UV), VPOS (VPOS_UV), VEE (VEE_UV) or VDDH (VDDH_UV) it will shut down the corresponding rail (plus any dependent rail) only and remain in ACTIVE mode, allowing the DCDC converters to remain up. Again, the PWR_GOOD pin will be pulled low.

As the PWRx inputs are edge sensitive, the host must toggle the PWRx pins to re-enable the rails through GPIO control, i.e. it must bring the PWRx pins low before asserting them again.

POWER GOOD PIN

The power good pin (PWR_GOOD) is an open drain output that is pulled high when all four power rails (CP1, CP2, LDO1, LDO2) are in regulation and is pulled low if any of the rails encounters a fault. PWR_GOOD remains low if one of the rails is not enabled by the host and only after all rails are in regulation PWR_GOOD is released to HiZ state (pulled up by external resistor).

PANEL TEMPERATURE MONITORING

The TPS65182/TPS65182B provides circuitry to bias and measure an external negative temperature coefficient resistor (NTC) to monitor device temperature in a range from –10°C to 85°C with and accuracy of ±1°C from 0°C to 50°C. Temperature reading is automatically updated every 60 s.

NTC BIAS CIRCUIT

Figure 3 below shows the block diagram of the NTC bias and measurement circuit. The NTC is biased from an internally generated 2.25-V reference voltage through an integrated 7.307-KΩ bias resistor. A 43-KΩ resistor is connected parallel to the NTC to linearize the temperature response curve. The circuit is designed to work with a nominal 10-KΩ NTC and achieves accuracy of ±1°C from 0°C to 50°C. The voltage drop across the NTC is digitized by a 10-bit SAR ADC and translated into an 8-bit two's complement by digital per Table 1.

Table 1. ADC Output Value vs Termperature

TEMPERATURE	TMST_VALUE[7:0]
< -10°C	1111 0110
-10°C	1111 0110
-9°C	1111 0111
...	...
-2°C	1111 1110
-1°C	1111 1111
0°C	0000 0000
1°C	0000 0001
2°C	0000 0010
...	...
25°C	0001 1001
...	
85°C	0101 0101
> 85°C	0101 0101

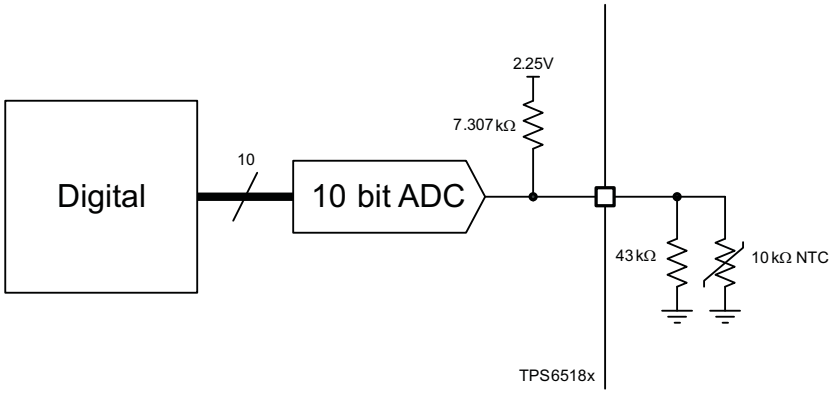


Figure 3. NTC Bias and Measurement Circuit

I²C BUS OPERATION

The TPS65182/TPS65182B supports a special I²C mode making it compatible with the EPSON® Broadsheet S1D13521 timing controller. Standard I²C protocol requires the following steps to read data from a register:

1. Send device slave address, R/nW bit set low (write command)
2. Send register address
3. Send device slave address, R/nW set high (read command)
4. The slave will respond with data from the specified register address.end device slave address, R/nW set high (read command).

The EPSON® Broadsheet S1D13521 controller does not support I²C writes nor I²C reads from addressed registers, therefore the TPS65182/TPS65182B I²C interface has been modified and the reading the temperature data is reduced to two steps:

1. Send device address, R/nW set high (read command)
2. Read the data from the slave. The slave will respond with data from TMST_VALUE register address.

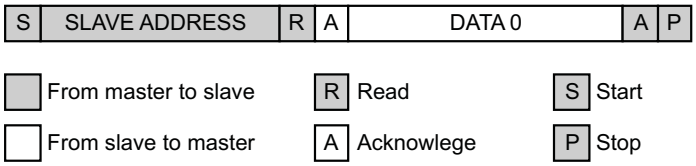


Figure 4. Subaddress in I²C Transmission

The I²C Bus is a communications link between a controller and a series of slave terminals. The link is established using a two-wired bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases where the serial data line is bi-directional for data communication between the controller and the slave terminals. Each device has an open Drain output to transmit data on the serial data line. An external pull-up resistor must be placed on the serial data line to pull the drain output high during data transmission.

Data transmission is initiated with a start bit from the controller as shown in Figure 5. The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the device will receive serial data on the SDA input and check for valid address and control information. If the appropriate group and address bits are set for the device, then the device will issue an acknowledge pulse and prepare the receive subaddress data. Subaddress data is decoded and responded to as per the Register Map section of this document. Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low to high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line must occur during the low portion of the SCL signal. An acknowledge is issued after the reception of valid address, sub-address and data words. Reference Figure 5.

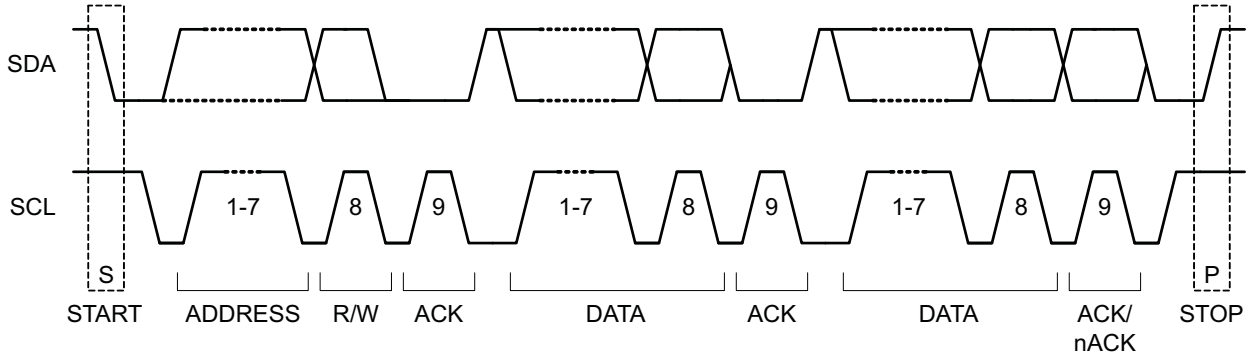


Figure 5. I²C Start/Stop/Acknowledge Protocol

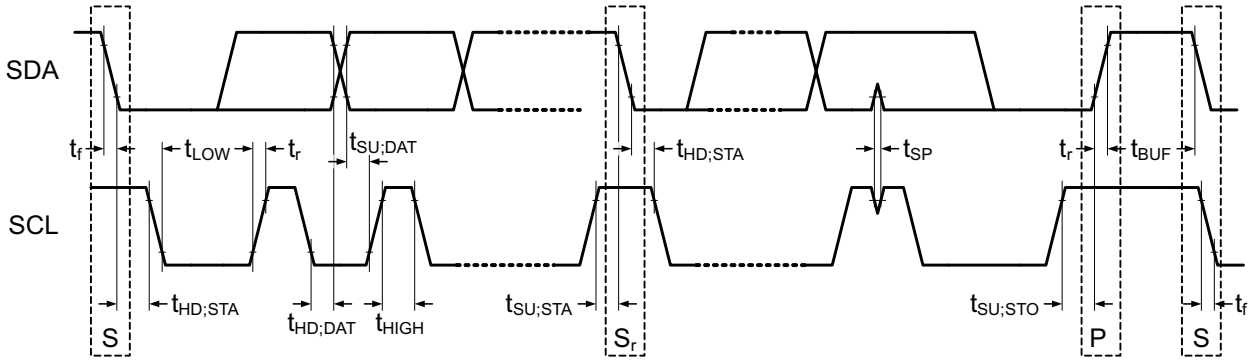


Figure 6. I²C Data Transmission Timing

DATA TRANSMISSION TIMING

V_{BAT} = 3.6 V ±5%, T_A = 25ºC, C_L = 100 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(SCL)}$	Serial clock frequency		100		400	KHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	SCL = 100 KHz	4			µs
		SCL = 400 KHz	600			ns
t_{LOW}	LOW period of the SCL clock	SCL = 100 KHz	4.7			µs
		SCL = 400 KHz	1.3			
t_{HIGH}	HIGH period of the SCL clock	SCL = 100 KHz	4			µs
		SCL = 400 KHz	600			ns
$t_{SU;STA}$	Set-up time for a repeated START condition	SCL = 100 KHz	4.7			µs
		SCL = 400 KHz	600			ns
$t_{HD;DAT}$	Data hold time	SCL = 100 KHz	0		3.45	µs
		SCL = 400 KHz	0		900	ns
$t_{SU;DAT}$	Data set-up time	SCL = 100 KHz	250			ns
		SCL = 400 KHz	100			
t_r	Rise time of both SDA and SCL signals	SCL = 100 KHz			1000	ns
		SCL = 400 KHz			300	
t_f	Fall time of both SDA and SCL signals	SCL = 100 KHz			300	ns
		SCL = 400 KHz			300	
$t_{SU;STO}$	Set-up time for STOP condition	SCL = 100 KHz	4			µs
		SCL = 400 KHz	600			ns
t_{BUF}	Bus Free Time Between Stop and Start Condition	SCL = 100 KHz	4.7			µs
		SCL = 400 KHz	1.3			
t_{SP}	Pulse width of spikes which mst be suppressed by the input filter	SCL = 100 KHz	n/a		n/a	ns
		SCL = 400 KHz	0		50	
C_b	Capacitive load for each bus line	SCL = 100 KHz			400	pF
		SCL = 400 KHz			400	

REGISTER ADDRESS MAP

REGISTER	ADDRESS (HEX)	NAME	DEFAULT VALUE	DESCRIPTION
0	0x00	TMST_VALUE	N/A	Thermistor value read by ADC

THERMISTOR READOUT (TMST_VALUE)

Address – 0x00h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	TMST_VALUE[7:0]							
READ/WRITE	R	R	R	R	R	R	R	R
RESET VALUE	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

FIELD NAME	BIT DEFINITION
TMST_VALUE[7:0]	Temperature read-out 1111 0110 – < -10°C 1111 0110 – -10°C 1111 0111 – -9°C ... 1111 1110 – -2°C 1111 1111 – -1 °C 0000 0000 – 0 °C 0000 0001 – 1°C 0000 0010 – 2°C ... 0001 1001 – 25°C ... 0101 0101 – 85°C 0101 0101 – > 85°C

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS65182BRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS65182BRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS65182RGZR	NRND	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS65182RGZT	NRND	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

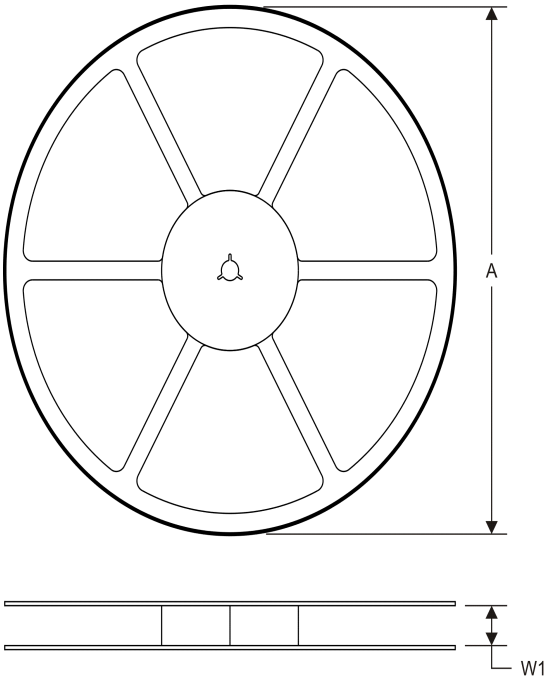
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

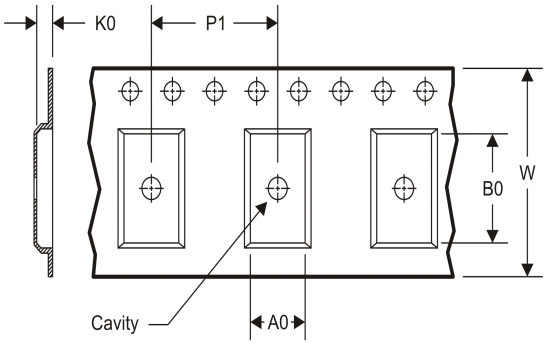
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



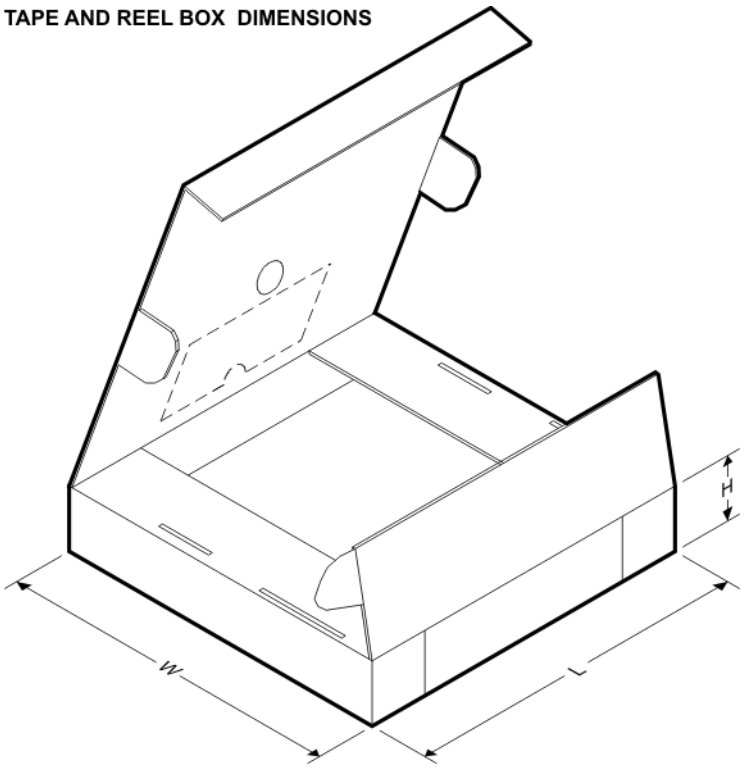
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65182BRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
TPS65182BRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
TPS65182RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
TPS65182RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

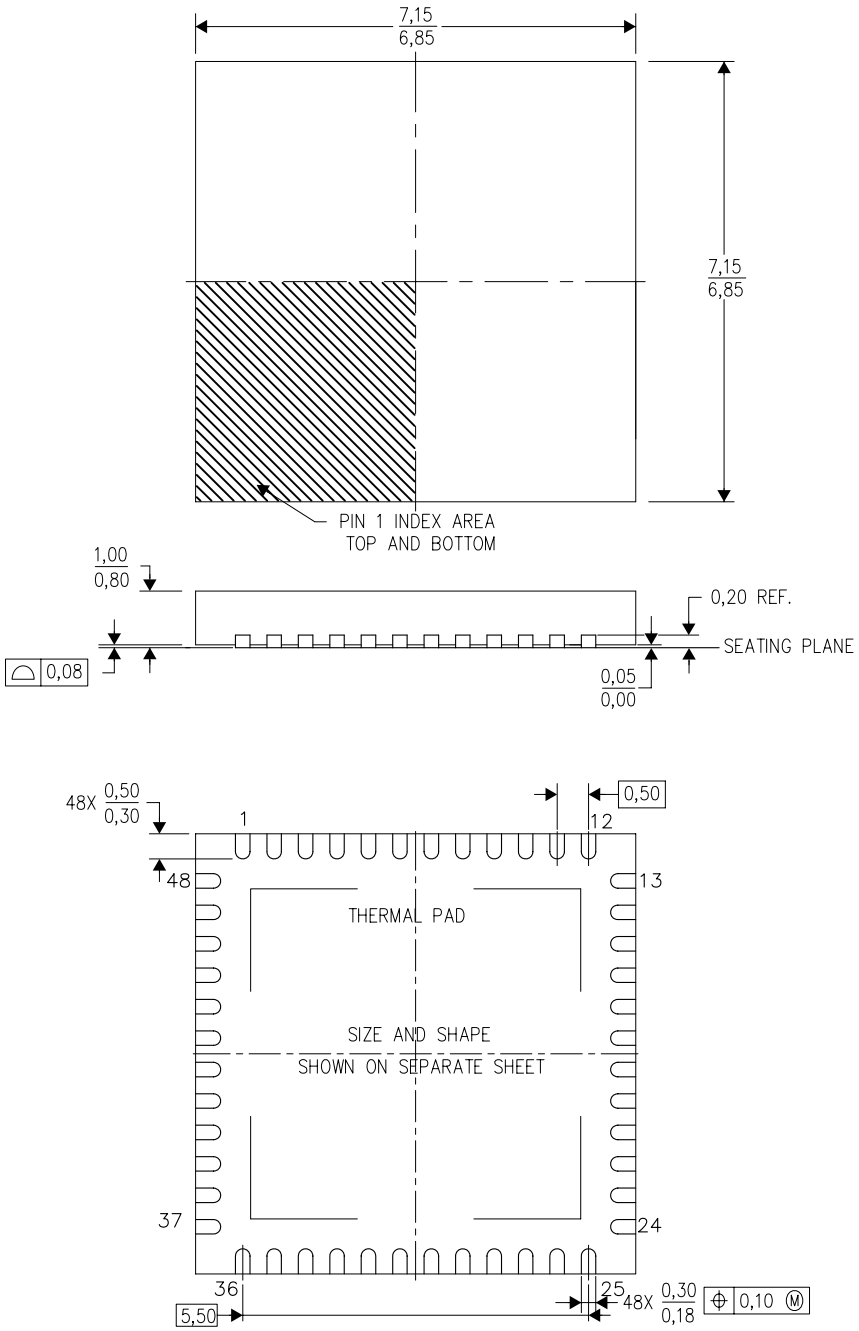
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65182BRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
TPS65182BRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
TPS65182RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
TPS65182RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

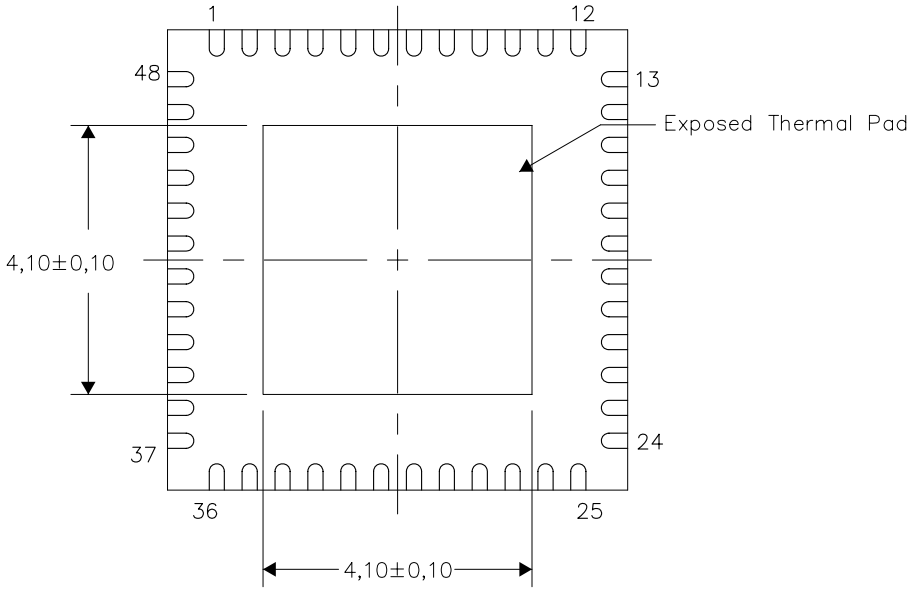
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



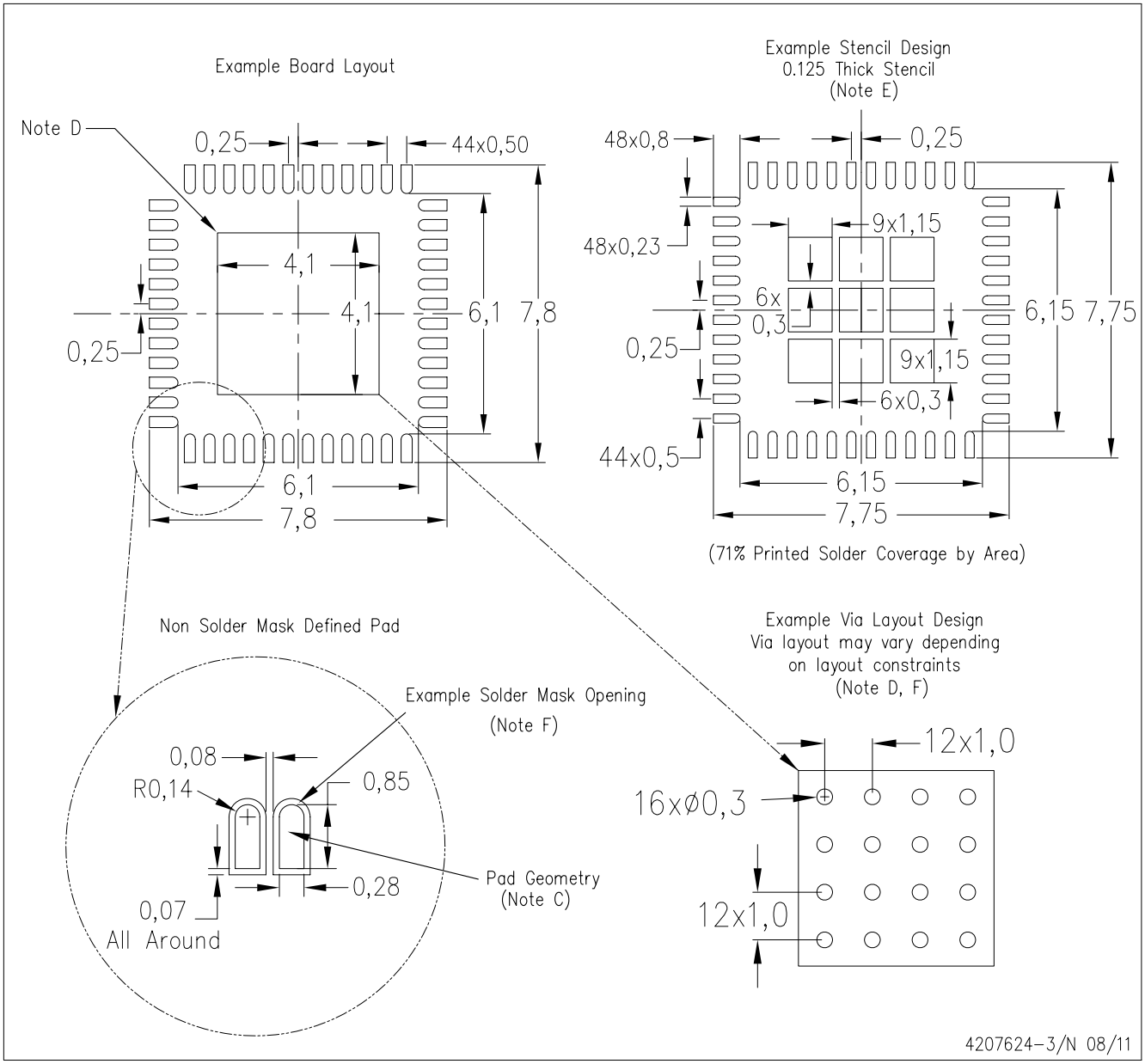
Bottom View

Exposed Thermal Pad Dimensions

4206354–3/R 08/11

NOTE: All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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