

## 650 kHz/1.2 MHz, 18.5 V STEP-UP DC-DC CONVERTER WITH 3.2 A SWITCH

Check for Samples: [TPS61087](#)

### FEATURES

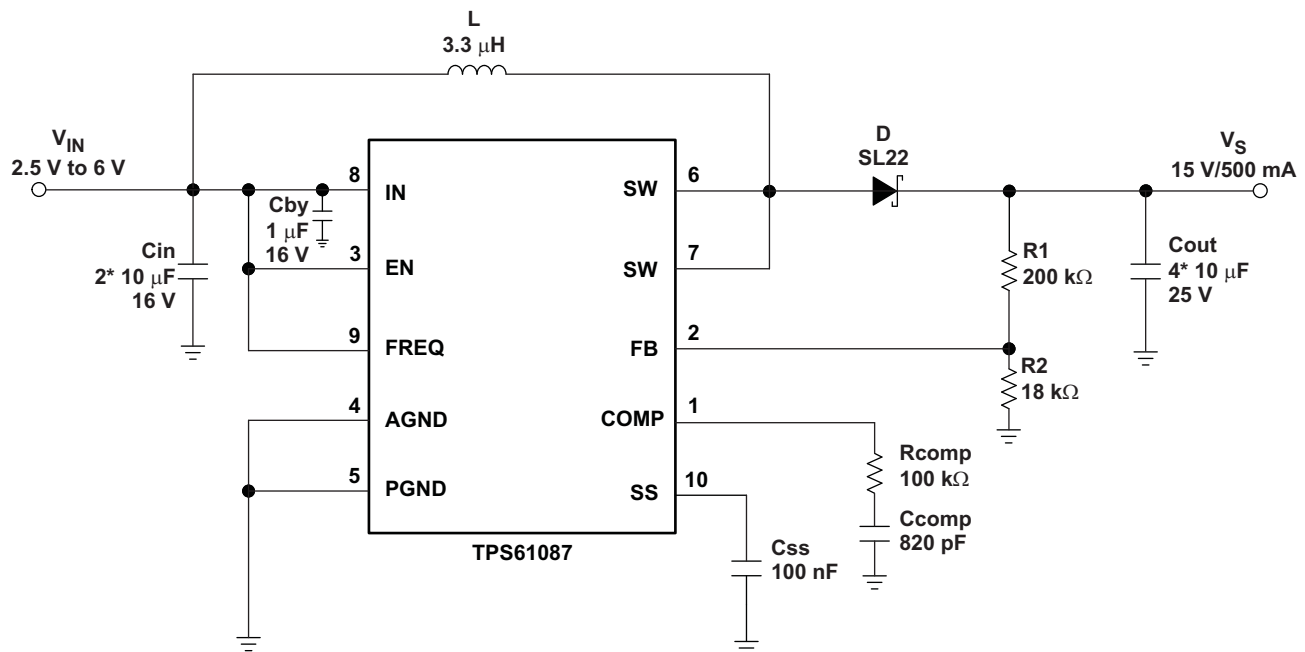
- 2.5 V to 6 V Input Voltage Range
- 18.5 V Boost Converter With 3.2 A Switch Current
- 650 kHz/1.2 MHz Selectable Switching Frequency
- Adjustable Soft-Start
- Thermal Shutdown
- Undervoltage Lockout
- 10-Pin QFN and thin QFN Packages

### APPLICATIONS

- Handheld Devices
- GPS Receiver
- Digital Still Camera
- Portable Applications
- DSL Modem
- PCMCIA Card
- TFT LCD Bias Supply

### DESCRIPTION

The TPS61087 is a high frequency, high efficiency DC to DC converter with an integrated 3.2 A, 0.13  $\Omega$  power switch capable of providing an output voltage up to 18.5 V. The selectable frequency of 650 kHz or 1.2 MHz allows the use of small external inductors and capacitors and provides fast transient response. The external compensation allows optimizing the application for specific conditions. A capacitor connected to the soft-start pin minimizes inrush current at startup.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### ORDERING INFORMATION<sup>(1)</sup> (2)

| T <sub>A</sub> | ORDERING    | PACKAGE      | PACKAGE MARKING |
|----------------|-------------|--------------|-----------------|
| –40 to 85°C    | TPS61087DRC | QFN-10 (DRC) | PMOQ            |
|                | TPS61087DSC | QFN-10 (DSC) | PMWI            |

- (1) The DRC package is available taped and reeled.  
 (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                                   | VALUE                        | UNIT |
|---------------------------------------------------|------------------------------|------|
| Input voltage range I <sub>N</sub> <sup>(2)</sup> | –0.3 to 7.0                  | V    |
| Voltage range on pins EN, FB, SS, FREQ, COMP      | –0.3 to 7.0                  | V    |
| Voltage on pin SW                                 | –0.3 to 20                   | V    |
| ESD rating HBM                                    | 2                            | kV   |
| ESD rating MM                                     | 200                          | V    |
| ESD rating CDM                                    | 500                          | V    |
| Continuous power dissipation                      | See Dissipation Rating Table |      |
| Operating junction temperature range              | –40 to 150                   | °C   |
| Storage temperature range                         | –65 to 150                   | °C   |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.  
 (2) All voltage values are with respect to network ground terminal.

### DISSIPATION RATINGS<sup>(1)</sup> (2)

| PACKAGE | T <sub>A</sub> ≤ 25°C<br>POWER RATING | T <sub>A</sub> = 70°C<br>POWER RATING | T <sub>A</sub> = 85°C<br>POWER RATING |
|---------|---------------------------------------|---------------------------------------|---------------------------------------|
| QFN     | 1.74 W                                | 0.96 W                                | 0.70 W                                |

- (1)  $P_D = (T_J - T_A)/R_{\theta JA}$ .  
 (2) The exposed thermal die is soldered to the PCB using thermal vias. For more information, see the Texas Instruments Application report [SLMA002](#) regarding thermal characteristics of the PowerPAD package.

### RECOMMENDED OPERATING CONDITIONS

|                                               | MIN                   | TYP | MAX  | UNIT |
|-----------------------------------------------|-----------------------|-----|------|------|
| V <sub>IN</sub> Input voltage range           | 2.5                   |     | 6    | V    |
| V <sub>S</sub> Boost output voltage range     | V <sub>IN</sub> + 0.5 |     | 18.5 | V    |
| T <sub>A</sub> Operating free-air temperature | –40                   |     | 85   | °C   |
| T <sub>J</sub> Operating junction temperature | –40                   |     | 125  | °C   |

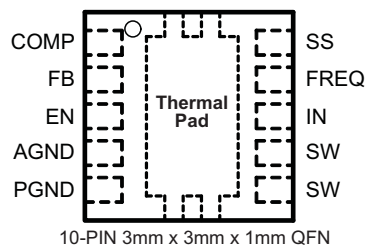
## ELECTRICAL CHARACTERISTICS

 $V_{IN} = 5\text{ V}$ ,  $EN = V_{IN}$ ,  $V_S = 15\text{ V}$ ,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , typical values are at  $T_A = 25^{\circ}\text{C}$  (unless otherwise noted)

| PARAMETER                     |                                     | TEST CONDITIONS                                                      | MIN            | TYP    | MAX   | UNIT               |
|-------------------------------|-------------------------------------|----------------------------------------------------------------------|----------------|--------|-------|--------------------|
| <b>SUPPLY</b>                 |                                     |                                                                      |                |        |       |                    |
| $V_{IN}$                      | Input voltage range                 |                                                                      | 2.5            |        | 6     | V                  |
| $I_Q$                         | Operating quiescent current into IN | Device not switching, $V_{FB} = 1.3\text{ V}$                        |                | 75     | 100   | $\mu\text{A}$      |
| $I_{SDVIN}$                   | Shutdown current into IN            | $EN = \text{GND}$                                                    |                |        | 1     | $\mu\text{A}$      |
| $V_{UVLO}$                    | Under-voltage lockout threshold     | $V_{IN}$ falling                                                     |                |        | 2.4   | V                  |
|                               |                                     | $V_{IN}$ rising                                                      |                |        | 2.5   | V                  |
| $T_{SD}$                      | Thermal shutdown                    | Temperature rising                                                   |                | 150    |       | $^{\circ}\text{C}$ |
| $T_{SDHYS}$                   | Thermal shutdown hysteresis         |                                                                      |                | 14     |       | $^{\circ}\text{C}$ |
| <b>LOGIC SIGNALS EN, FREQ</b> |                                     |                                                                      |                |        |       |                    |
| $V_{IH}$                      | High level input voltage            | $V_{IN} = 2.5\text{ V}$ to $6.0\text{ V}$                            | 2              |        |       | V                  |
| $V_{IL}$                      | Low level input voltage             | $V_{IN} = 2.5\text{ V}$ to $6.0\text{ V}$                            |                |        | 0.5   | V                  |
| $I_{INLEAK}$                  | Input leakage current               | $EN = \text{FREQ} = \text{GND}$                                      |                |        | 0.1   | $\mu\text{A}$      |
| <b>BOOST CONVERTER</b>        |                                     |                                                                      |                |        |       |                    |
| $V_S$                         | Boost output voltage                |                                                                      | $V_{IN} + 0.5$ |        | 18.5  | V                  |
| $V_{FB}$                      | Feedback regulation voltage         |                                                                      | 1.230          | 1.238  | 1.246 | V                  |
| $g_m$                         | Transconductance error amplifier    |                                                                      |                | 107    |       | $\mu\text{A/V}$    |
| $I_{FB}$                      | Feedback input bias current         | $V_{FB} = 1.238\text{ V}$                                            |                |        | 0.1   | $\mu\text{A}$      |
| $r_{DS(on)}$                  | N-channel MOSFET on-resistance      | $V_{IN} = V_{GS} = 5\text{ V}$ , $I_{SW} = \text{current limit}$     |                | 0.13   | 0.18  | $\Omega$           |
|                               |                                     | $V_{IN} = V_{GS} = 3\text{ V}$ , $I_{SW} = \text{current limit}$     |                | 0.16   | 0.23  |                    |
| $I_{SWLEAK}$                  | SW leakage current                  | $EN = \text{GND}$ , $V_{SW} = V_{IN} = 6.0\text{ V}$                 |                |        | 2     | $\mu\text{A}$      |
| $I_{LIM}$                     | N-Channel MOSFET current limit      |                                                                      | 3.2            | 4.0    | 4.8   | A                  |
| $I_{SS}$                      | Soft-start current                  | $V_{SS} = 1.238\text{ V}$                                            | 7              | 10     | 13    | $\mu\text{A}$      |
| $f_S$                         | Oscillator frequency                | $\text{FREQ} = V_{IN}$                                               | 0.9            | 1.2    | 1.5   | MHz                |
|                               |                                     | $\text{FREQ} = \text{GND}$                                           | 480            | 650    | 820   | kHz                |
|                               | Line regulation                     | $V_{IN} = 2.5\text{ V}$ to $6.0\text{ V}$ , $I_{OUT} = 10\text{ mA}$ |                | 0.0002 |       | %/V                |
|                               | Load regulation                     | $V_{IN} = 5.0\text{ V}$ , $I_{OUT} = 1\text{ mA}$ to $1\text{ A}$    |                | 0.11   |       | %/A                |

## PIN ASSIGNMENT

DRC, DSC PACKAGE  
(TOP VIEW)



## PIN FUNCTIONS

| PIN  |                      | I/O | DESCRIPTION                                                                                                                      |
|------|----------------------|-----|----------------------------------------------------------------------------------------------------------------------------------|
| NAME | NO.                  |     |                                                                                                                                  |
| COMP | 1                    | I/O | Compensation pin                                                                                                                 |
| FB   | 2                    | I   | Feedback pin                                                                                                                     |
| EN   | 3                    | I   | Shutdown control input. Connect this pin to logic high level to enable the device                                                |
| AGND | 4,<br>Thermal<br>Pad |     | Analog ground                                                                                                                    |
| PGND | 5                    |     | Power ground                                                                                                                     |
| SW   | 6, 7                 |     | Switch pin                                                                                                                       |
| IN   | 8                    |     | Input supply pin                                                                                                                 |
| FREQ | 9                    | I   | Frequency select pin. The power switch operates at 650 kHz if FREQ is connected to GND and at 1.2 MHz if FREQ is connected to IN |
| SS   | 10                   |     | Soft-start control pin. Connect a capacitor to this pin if soft-start needed. Open = no soft-start                               |

## TYPICAL CHARACTERISTICS

### TABLE OF GRAPHS

|                |                                          |                                                                | FIGURE    |
|----------------|------------------------------------------|----------------------------------------------------------------|-----------|
| $I_{OUT(max)}$ | Maximum load current                     | vs. Input voltage at High frequency (1.2 MHz)                  | Figure 1  |
| $I_{OUT(max)}$ | Maximum load current                     | vs. Input voltage at Low frequency (650 kHz)                   | Figure 2  |
| $\eta$         | Efficiency                               | vs. Load current, $V_S = 15\text{ V}$ , $V_{IN} = 5\text{ V}$  | Figure 3  |
| $\eta$         | Efficiency                               | vs. Load current, $V_S = 9\text{ V}$ , $V_{IN} = 3.3\text{ V}$ | Figure 4  |
|                | PWM switching - discontinuous conduction |                                                                | Figure 5  |
|                | PWM switching - continuous conduction    |                                                                | Figure 6  |
|                | Load transient response                  | at High frequency (1.2 MHz)                                    | Figure 7  |
|                | Load transient response                  | at Low frequency (650 kHz)                                     | Figure 8  |
|                | Soft-start                               |                                                                | Figure 9  |
|                | Supply current                           | vs. Supply voltage                                             | Figure 10 |
|                | Oscillator frequency                     | vs. Load current                                               | Figure 11 |
|                | Oscillator frequency                     | vs. Supply voltage                                             | Figure 12 |

The typical characteristics are measured with the inductors 7447789003 3.3  $\mu\text{H}$  (high frequency) or 74454068 6.8  $\mu\text{H}$  (low frequency) from Wurth and the rectifier diode SL22.

# TYPICAL CHARACTERISTICS (continued)

MAXIMUM LOAD CURRENT  
VS  
INPUT VOLTAGE

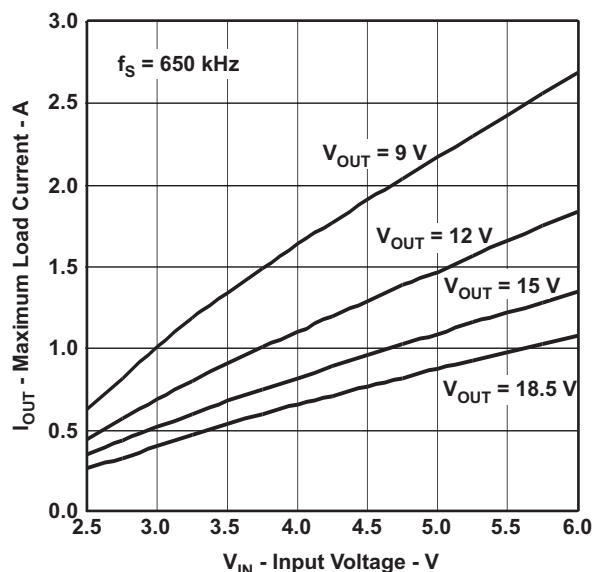


Figure 1.

MAXIMUM LOAD CURRENT  
VS  
INPUT VOLTAGE

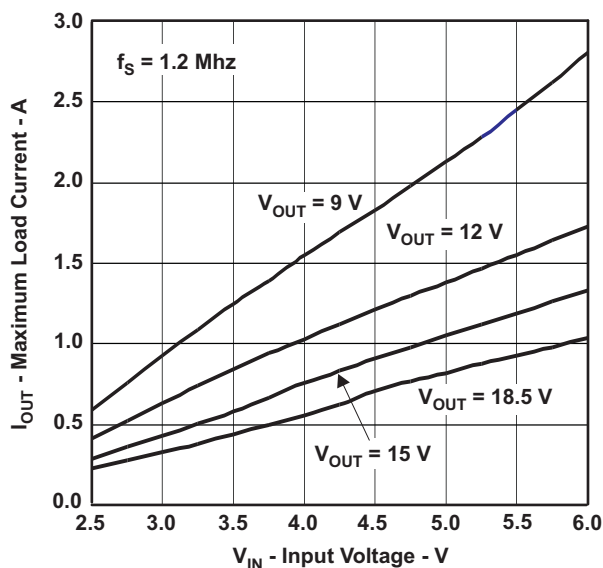


Figure 2.

EFFICIENCY  
VS  
LOAD CURRENT

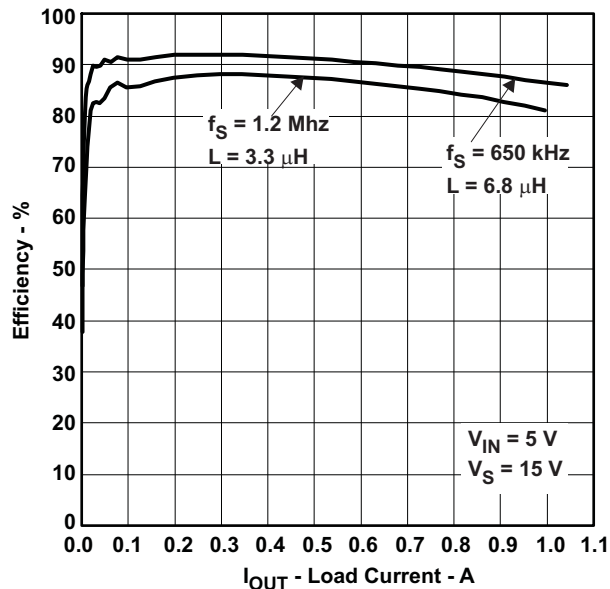


Figure 3.

EFFICIENCY  
VS  
LOAD CURRENT

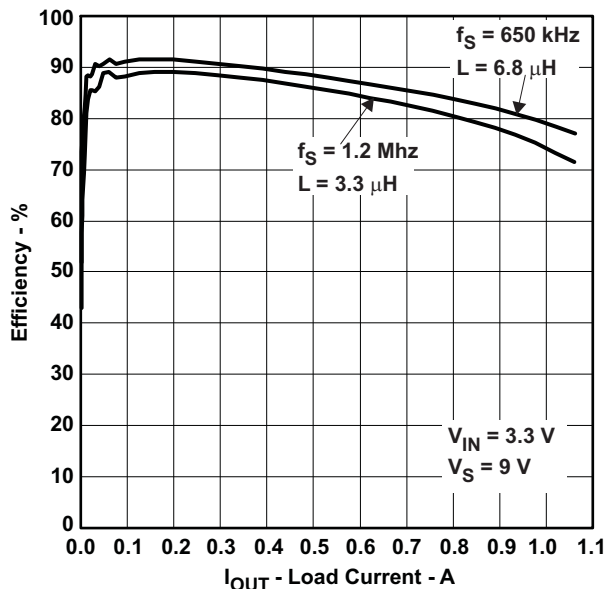


Figure 4.

## TYPICAL CHARACTERISTICS (continued)

PWM SWITCHING  
DISCONTINUOUS CONDUCTION MODE

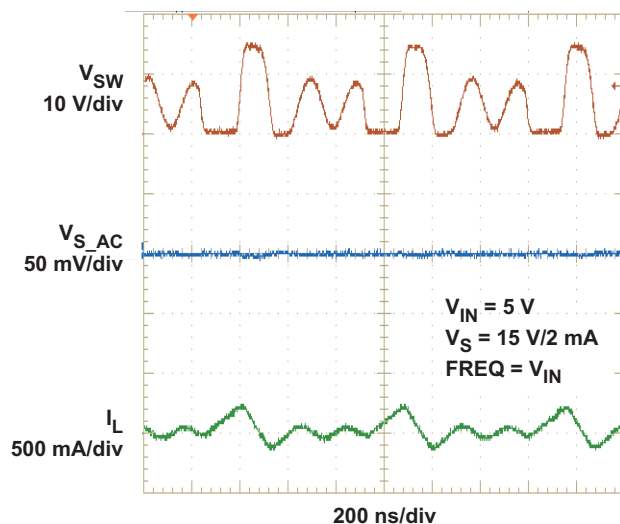


Figure 5.

PWM SWITCHING  
CONTINUOUS CONDUCTION MODE

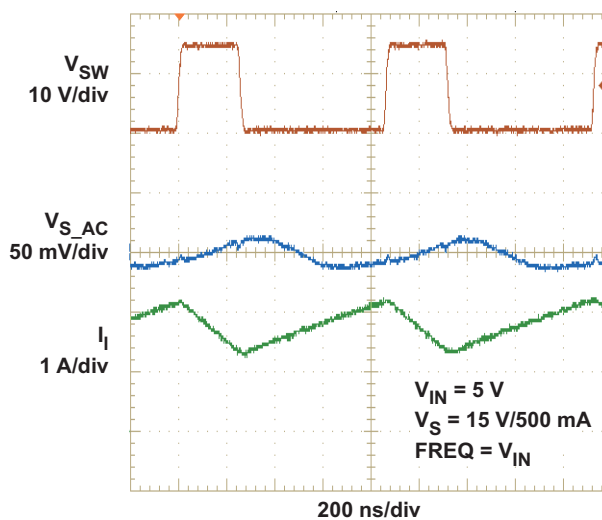


Figure 6.

LOAD TRANSIENT RESPONSE  
HIGH FREQUENCY (1.2 MHz)

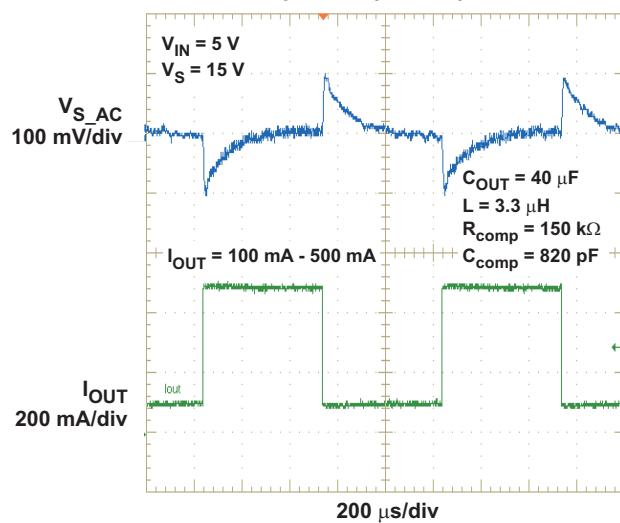


Figure 7.

LOAD TRANSIENT RESPONSE  
LOW FREQUENCY (650 kHz)

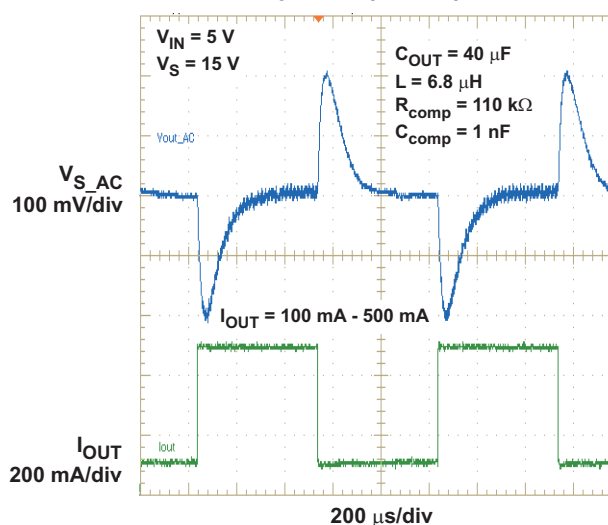


Figure 8.

## TYPICAL CHARACTERISTICS (continued)

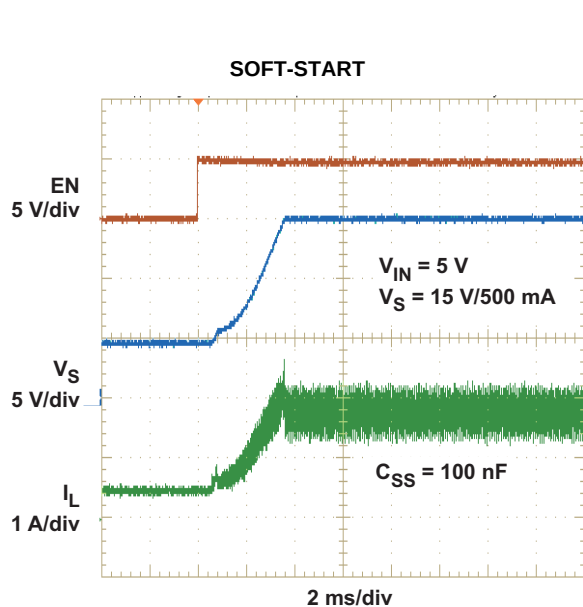


Figure 9.

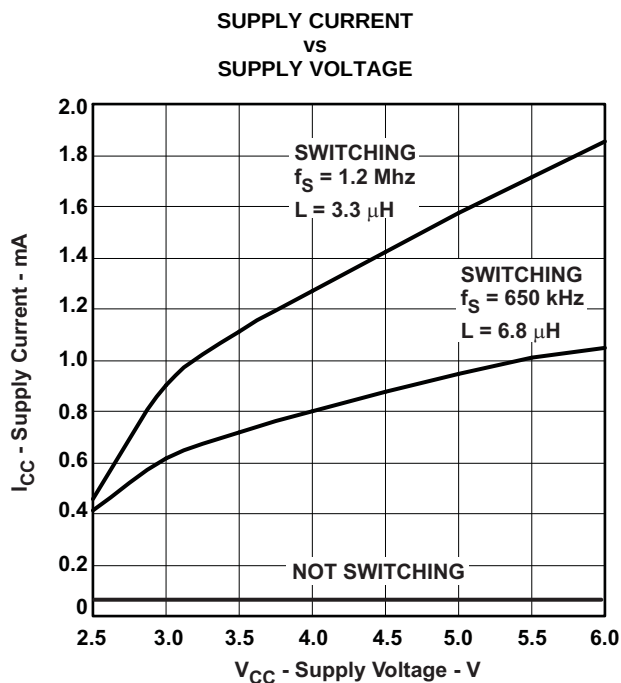


Figure 10.

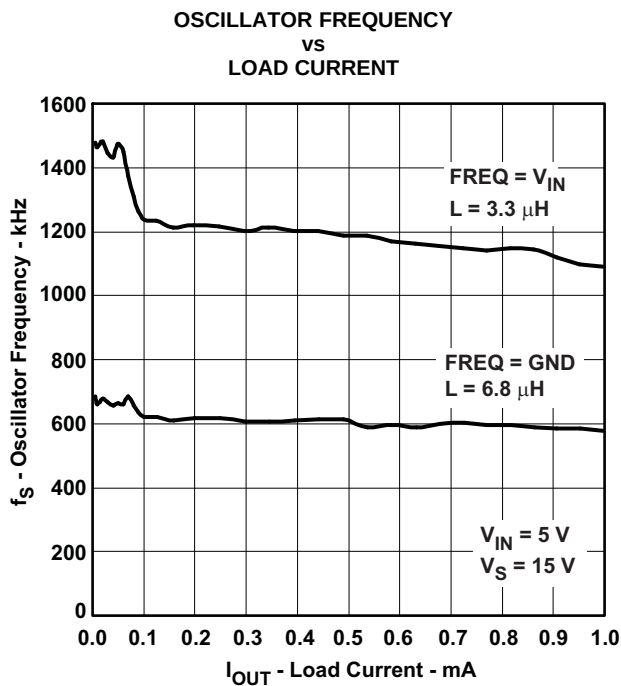


Figure 11.

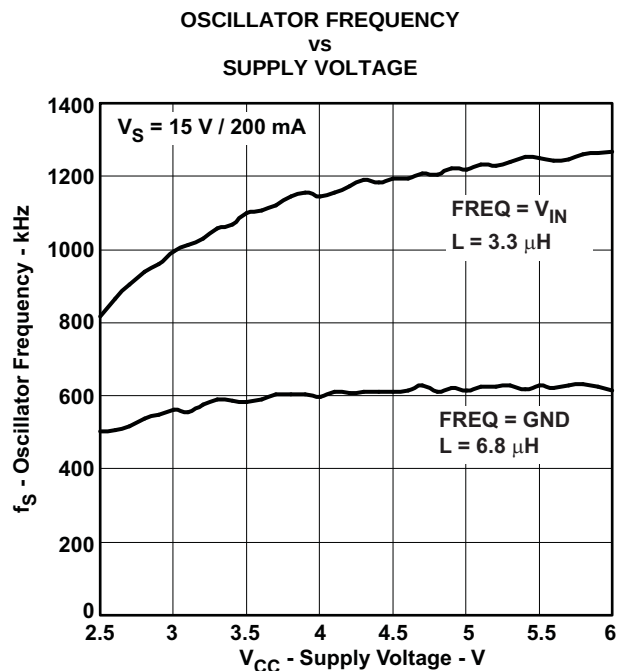
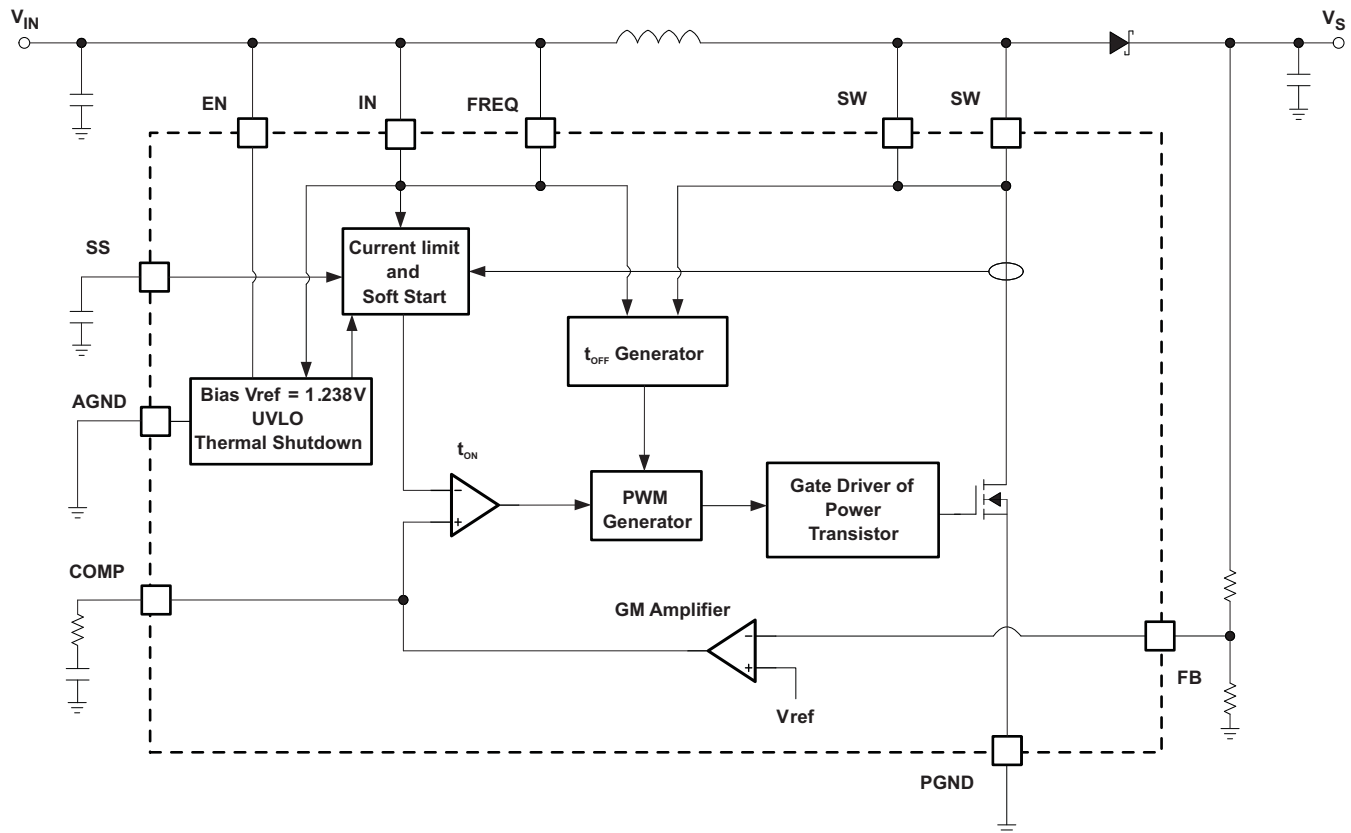


Figure 12.

**DETAILED DESCRIPTION****Figure 13. Block Diagram**

The boost converter is designed for output voltages up to 18.5 V with a switch peak current limit of 3.2 A minimum. The device, which operates in a current mode scheme with quasi-constant frequency, is externally compensated for maximum flexibility and stability. The switching frequency is selectable between 650 kHz and 1.2 MHz and the minimum input voltage is 2.5 V. To limit the inrush current at start-up a soft-start pin is available.

TPS61087 boost converter's novel topology using adaptive off-time provides superior load and line transient responses and operates also over a wider range of applications than conventional converters.

The selectable switching frequency offers the possibility to optimize the design either for the use of small sized components (1.2 MHz) or for higher system efficiency (650 kHz). However, the frequency changes slightly because the voltage drop across the  $r_{DS(on)}$  has some influence on the current and voltage measurement and thus on the on-time (the off-time remains constant).

The converter operates in continuous conduction mode (CCM) as soon as the input current increases above half the ripple current in the inductor, for lower load currents it switches into discontinuous conduction mode (DCM). If the load is further reduced, the part starts to skip pulses to maintain the output voltage.

## Design Procedure

The first step in the design procedure is to verify that the maximum possible output current of the boost converter supports the specific application requirements. A simple approach is to estimate the converter efficiency, by taking the efficiency numbers from the provided efficiency curves or to use a worst case assumption for the expected efficiency, e.g. 90%.

1. Duty cycle,  $D$ :

$$D = 1 - \frac{V_{IN} \cdot \eta}{V_S} \quad (1)$$

2. Maximum output current,  $I_{out(max)}$  :

$$I_{out(max)} = \left( I_{LIM(min)} - \frac{\Delta I_L}{2} \right) \cdot (1 - D) \quad (2)$$

3. Peak switch current in application,  $I_{swpeak}$  :

$$I_{swpeak} = \frac{\Delta I_L}{2} + \frac{I_{out}}{1 - D} \quad (3)$$

with the inductor peak-to-peak ripple current,  $\Delta I_L$

$$\Delta I_L = \frac{V_{IN} \cdot D}{f_S \cdot L} \quad (4)$$

and

|                |                                                                                                          |
|----------------|----------------------------------------------------------------------------------------------------------|
| $V_{IN}$       | Minimum input voltage                                                                                    |
| $V_S$          | Output voltage                                                                                           |
| $I_{LIM(min)}$ | Converter switch current limit (minimum switch current limit = 3.2 A)                                    |
| $f_S$          | Converter switching frequency (typically 1.2 MHz or 650 kHz)                                             |
| $L$            | Selected inductor value                                                                                  |
| $\eta$         | Estimated converter efficiency (please use the number from the efficiency plots or 90% as an estimation) |

The peak switch current is the steady state peak switch current that the integrated switch, inductor and external Schottky diode has to be able to handle. The calculation must be done for the minimum input voltage where the peak switch current is the highest.

## Soft-start

The boost converter has an adjustable soft-start to prevent high inrush current during start-up. To minimize the inrush current during start-up an external capacitor, connected to the soft-start pin SS and charged with a constant current, is used to slowly ramp up the internal current limit of the boost converter. When the EN pin is pulled high, the soft-start capacitor  $C_{SS}$  is immediately charged to 0.3 V. The capacitor is then charged at a constant current of 10  $\mu$ A typically until the output of the boost converter  $V_S$  has reached its Power Good threshold (roughly 98% of  $V_S$  nominal value). During this time, the SS voltage directly controls the peak inductor current, starting with 0 A at  $V_{SS} = 0.3$  V up to the full current limit at  $V_{SS} = 800$  mV. The maximum load current is available after the soft-start is completed. The larger the capacitor the slower the ramp of the current limit and the longer the soft-start time. A 100 nF capacitor is usually sufficient for most of the applications. When the EN pin is pulled low, the soft-start capacitor is discharged to ground.

## Inductor Selection

The TPS61087 is designed to work with a wide range of inductors. The main parameter for the inductor selection is the saturation current of the inductor which should be higher than the peak switch current as calculated in the *Design Procedure* section with additional margin to cover for heavy load transients. An alternative, more conservative, is to choose an inductor with a saturation current at least as high as the maximum switch current limit of 4.8 A. The other important parameter is the inductor DC resistance. Usually the lower the DC resistance the higher the efficiency. It is important to note that the inductor DC resistance is not the only parameter determining the efficiency. Especially for a boost converter where the inductor is the energy storage element, the type and core material of the inductor influences the efficiency as well. At high switching frequencies of 1.2 MHz inductor core losses, proximity effects and skin effects become more important. Usually an inductor with a larger form factor gives higher efficiency. The efficiency difference between different inductors can vary between 2% to 10%. For the TPS61087, inductor values between 3  $\mu\text{H}$  and 6  $\mu\text{H}$  are a good choice with a switching frequency of 1.2 MHz, typically 3.3  $\mu\text{H}$ . At 650 kHz we recommend inductors between 6  $\mu\text{H}$  and 13  $\mu\text{H}$ , typically 6.8  $\mu\text{H}$ . Possible inductors are shown in [Table 1](#).

Typically, it is recommended that the inductor current ripple is below 35% of the average inductor current. Therefore, the following equation can be used to calculate the inductor value,  $L$ :

$$L = \left( \frac{V_{IN}}{V_S} \right)^2 \cdot \left( \frac{V_S - V_{IN}}{I_{out} \cdot f_S} \right) \cdot \left( \frac{\eta}{0.35} \right) \quad (5)$$

with

|           |                                                                                                          |
|-----------|----------------------------------------------------------------------------------------------------------|
| $V_{IN}$  | Minimum input voltage                                                                                    |
| $V_S$     | Output voltage                                                                                           |
| $I_{out}$ | Maximum output current in the application                                                                |
| $f_S$     | Converter switching frequency (typically 1.2 MHz or 650 kHz)                                             |
| $\eta$    | Estimated converter efficiency (please use the number from the efficiency plots or 90% as an estimation) |

**Table 1. Inductor Selection**

| L<br>( $\mu\text{H}$ ) | SUPPLIER         | COMPONENT<br>CODE | SIZE<br>(L×W×H mm)     | DCR TYP<br>(m $\Omega$ ) | I <sub>sat</sub> (A) |
|------------------------|------------------|-------------------|------------------------|--------------------------|----------------------|
| <b>1.2 MHz</b>         |                  |                   |                        |                          |                      |
| 4.2                    | Sumida           | CDRH5D28          | 5.7 × 5.7 × 3          | 23                       | 2.2                  |
| 4.7                    | Würth Elektronik | 7447785004        | 5.9 × 6.2 × 3.3        | 60                       | 2.5                  |
| 5                      | Coilcraft        | MSS7341           | 7.3 × 7.3 × 4.1        | 24                       | 2.9                  |
| 5                      | Sumida           | CDRH6D28          | 7 × 7 × 3              | 23                       | 2.4                  |
| 4.6                    | Sumida           | CDR7D28           | 7.6 × 7.6 × 3          | 38                       | 3.15                 |
| 4.7                    | Würth Elektronik | 7447789004        | 7.3 × 7.3 × 3.2        | 33                       | 3.9                  |
| 3.3                    | Würth Elektronik | 7447789003        | 7.3 × 7.3 × 3.2        | 30                       | 4.2                  |
| <b>650 kHz</b>         |                  |                   |                        |                          |                      |
| 10                     | Würth Elektronik | 744778910         | 7.3 × 7.3 × 3.2        | 51                       | 2.2                  |
| 10                     | Sumida           | CDRH8D28          | 8.3 × 8.3 × 3          | 36                       | 2.7                  |
| 6.8                    | Sumida           | CDRH6D26HPNP      | 7 × 7 × 2.8            | 52                       | 2.9                  |
| 6.2                    | Sumida           | CDRH8D58          | 8.3 × 8.3 × 6          | 25                       | 3.3                  |
| 10                     | Coilcraft        | DS3316P           | 12.95 × 9.40 ×<br>5.08 | 80                       | 3.5                  |
| 10                     | Sumida           | CDRH8D43          | 8.3 × 8.3 × 4.5        | 29                       | 4                    |
| 6.8                    | Würth Elektronik | 74454068          | 12.7 × 10 × 4.9        | 55                       | 4.1                  |

## Rectifier Diode Selection

To achieve high efficiency a Schottky type should be used for the rectifier diode. The reverse voltage rating should be higher than the maximum output voltage of the converter. The averaged rectified forward current  $I_{avg}$ , the Schottky diode needs to be rated for, is equal to the output current  $I_{out}$ :

$$I_{avg} = I_{out} \quad (6)$$

Usually a Schottky diode with 2 A maximum average rectified forward current rating is sufficient for most applications. The Schottky rectifier can be selected with lower forward current capability depending on the output current  $I_{out}$  but has to be able to dissipate the power. The dissipated power,  $P_D$ , is the average rectified forward current times the diode forward voltage,  $V_{forward}$ .

$$P_D = I_{avg} \cdot V_{forward} \quad (7)$$

Typically the diode should be able to dissipate around 500mW depending on the load current and forward voltage.

**Table 2. Rectifier Diode Selection**

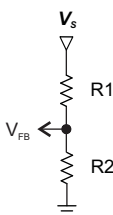
| CURRENT RATING $I_{avg}$ | $V_r$ | $V_{forward}/I_{avg}$ | SUPPLIER                | COMPONENT CODE |
|--------------------------|-------|-----------------------|-------------------------|----------------|
| 2 A                      | 20 V  | 0.44 V / 2 A          | Vishay Semiconductor    | SL22           |
| 2 A                      | 20 V  | 0.5 V / 2 A           | Fairchild Semiconductor | SS22           |

## Setting the Output Voltage

The output voltage is set by an external resistor divider. Typically, a minimum current of 50  $\mu$ A flowing through the feedback divider gives good accuracy and noise covering. A standard low side resistor of 18 k $\Omega$  is typically selected. The resistors are then calculated as:

$$R2 = \frac{V_{FB}}{70\mu A} \approx 18k\Omega \quad R1 = R2 \cdot \left( \frac{V_s}{V_{FB}} - 1 \right)$$

$$V_{FB} = 1.238V$$



(8)

## Compensation (COMP)

The regulator loop can be compensated by adjusting the external components connected to the COMP pin. The COMP pin is the output of the internal transconductance error amplifier.

Standard values of  $R_{COMP} = 16$  k $\Omega$  and  $C_{COMP} = 2.7$  nF will work for the majority of the applications.

See [Table 3](#) for dedicated compensation networks giving an improved load transient response. The following equations can be used to calculate  $R_{COMP}$  and  $C_{COMP}$ :

$$R_{COMP} = \frac{110 \cdot V_{IN} \cdot V_s \cdot C_{out}}{L \cdot I_{out}} \quad C_{COMP} = \frac{V_s \cdot C_{out}}{7.5 \cdot I_{out} \cdot R_{COMP}} \quad (9)$$

with

|           |                                                 |
|-----------|-------------------------------------------------|
| $V_{IN}$  | Minimum input voltage                           |
| $V_s$     | Output voltage                                  |
| $C_{out}$ | Output capacitance                              |
| $L$       | Inductor value, e.g. 3.3 $\mu$ H or 6.8 $\mu$ H |
| $I_{out}$ | Maximum output current in the application       |

Make sure that  $R_{COMP} < 120$  k $\Omega$  and  $C_{COMP} > 820$  pF, independent of the results of the above formulas.

**Table 3. Recommended Compensation Network Values at High/Low Frequency**

| FREQUENCY      | L      | V <sub>S</sub> | V <sub>IN</sub> ± 20% | R <sub>COMP</sub> | C <sub>COMP</sub> |
|----------------|--------|----------------|-----------------------|-------------------|-------------------|
| High (1.2 MHz) | 3.3 µH | 15 V           | 5 V                   | 100 kΩ            | 820 pF            |
|                |        |                | 3.3 V                 | 91 kΩ             | 1.2 nF            |
|                |        | 12 V           | 5 V                   | 68 kΩ             | 820 pF            |
|                |        |                | 3.3 V                 | 68 kΩ             | 1.2 nF            |
|                |        | 9 V            | 5 V                   | 39 kΩ             | 820 pF            |
|                |        |                | 3.3 V                 | 39 kΩ             | 1.2 nF            |
| Low (650 kHz)  | 6.8 µH | 15 V           | 5 V                   | 51 kΩ             | 1.5 nF            |
|                |        |                | 3.3 V                 | 47 kΩ             | 2.7 nF            |
|                |        | 12 V           | 5 V                   | 33 kΩ             | 1.5 nF            |
|                |        |                | 3.3 V                 | 33 kΩ             | 2.7 nF            |
|                |        | 9 V            | 5 V                   | 18 kΩ             | 1.5 nF            |
|                |        |                | 3.3 V                 | 18 kΩ             | 2.7 nF            |

Table 3 gives conservative  $R_{COMP}$  and  $C_{COMP}$  values for certain inductors, input and output voltages providing a very stable system. For a faster response time, a higher  $R_{COMP}$  value can be used to enlarge the bandwidth, as well as a slightly lower value of  $C_{COMP}$  to keep enough phase margin. These adjustments should be performed in parallel with the load transient response monitoring of TPS61087.

### Input Capacitor Selection

For good input voltage filtering low ESR ceramic capacitors are recommended. TPS61087 has an analog input IN. Therefore, a 1 µF bypass is highly recommended as close as possible to the IC from IN to GND.

Two 10 µF (or one 22 µF) ceramic input capacitors are sufficient for most of the applications. For better input voltage filtering this value can be increased. See Table 4 and typical applications for input capacitor recommendation.

### Output Capacitor Selection

For best output voltage filtering a low ESR output capacitor like ceramic capacitor is recommended. Four 10 µF ceramic output capacitors (or two 22 µF) work for most of the applications. Higher capacitor values can be used to improve the load transient response. See Table 4 for the selection of the output capacitor.

**Table 4. Rectifier Input and Output Capacitor Selection**

|                  | CAPACITOR/SIZE | VOLTAGE RATING | SUPPLIER    | COMPONENT CODE  |
|------------------|----------------|----------------|-------------|-----------------|
| C <sub>IN</sub>  | 22 µF/1206     | 16 V           | Taiyo Yuden | EMK316 BJ 226ML |
| IN bypass        | 1 µF/0603      | 16 V           | Taiyo Yuden | EMK107 BJ 105KA |
| C <sub>OUT</sub> | 10 µF/1206     | 25 V           | Taiyo Yuden | TMK316 BJ 106KL |

To calculate the output voltage ripple, the following equation can be used:

$$\Delta V_C = \frac{V_S - V_{IN}}{V_S \cdot f_S} \cdot \frac{I_{out}}{C_{out}} \quad \Delta V_{C\_ESR} = I_{L(peak)} \cdot R_{C\_ESR} \quad (10)$$

with

|                     |                                                                                               |
|---------------------|-----------------------------------------------------------------------------------------------|
| $\Delta V_C$        | Output voltage ripple dependent on output capacitance, output current and switching frequency |
| $V_S$               | Output voltage                                                                                |
| $V_{IN}$            | Minimum input voltage of boost converter                                                      |
| $f_S$               | Converter switching frequency (typically 1.2 MHz or 650 kHz)                                  |
| $I_{out}$           | Output current                                                                                |
| $\Delta V_{C\_ESR}$ | Output voltage ripple due to output capacitors ESR (equivalent series resistance)             |
| $I_{SWPEAK}$        | Inductor peak switch current in the application                                               |

$R_{C\_ESR}$  Output capacitors equivalent series resistance (ESR)

$\Delta V_{C\_ESR}$  can be neglected in many cases since ceramic capacitors provide low ESR.

### Frequency Select Pin (FREQ)

The frequency select pin FREQ allows to set the switching frequency of the device to 650 kHz (FREQ = low) or 1.2 MHz (FREQ = high). Higher switching frequency improves load transient response but reduces slightly the efficiency. The other benefits of higher switching frequency are a lower output ripple voltage. The use of a 1.2 MHz switching frequency is recommended unless light load efficiency is a major concern.

### Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages an undervoltage lockout is included that disables the device, if the input voltage falls below 2.4 V.

### Thermal Shutdown

A thermal shutdown is implemented to prevent damages due to excessive heat and power dissipation. Typically the thermal shutdown happens at a junction temperature of 150°C. When the thermal shutdown is triggered the device stops switching until the junction temperature falls below typically 136°C. Then the device starts switching again.

### Overvoltage Prevention

If overvoltage is detected on the FB pin (typically 3 % above the nominal value of 1.238 V) the part stops switching immediately until the voltage on this pin drops to its nominal value. This prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

## APPLICATION INFORMATION

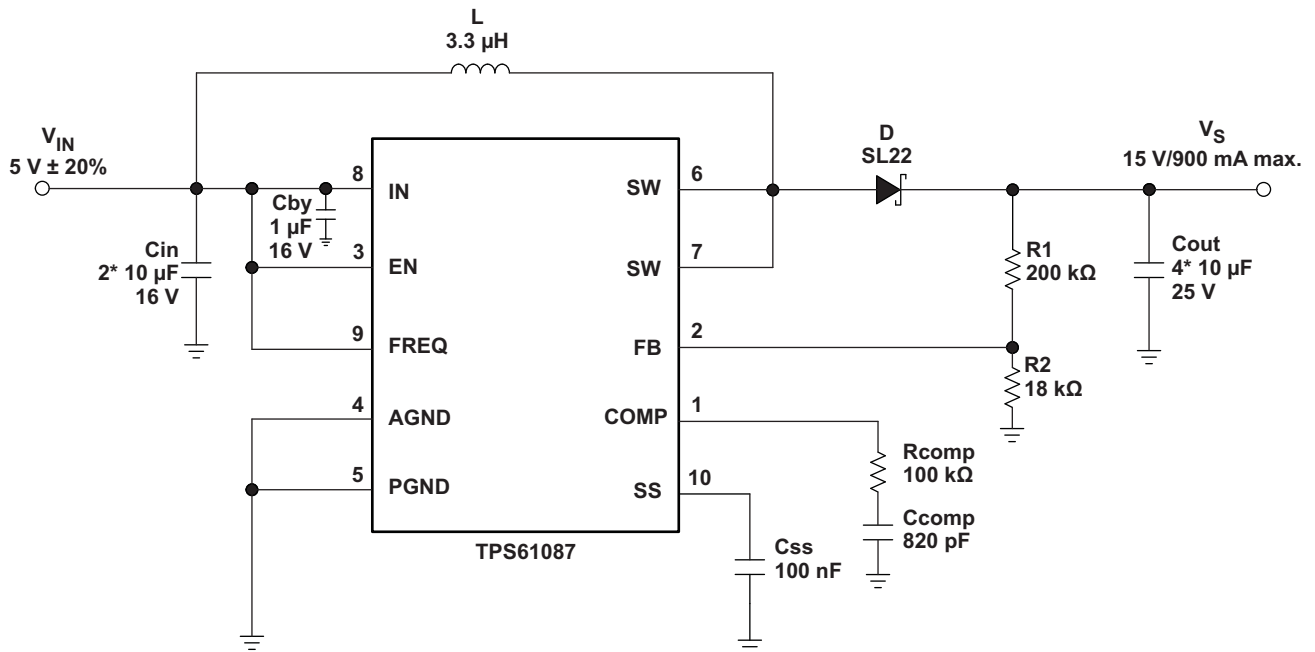


Figure 14. Typical Application, 5 V to 15 V ( $f_s = 1.2$  MHz)

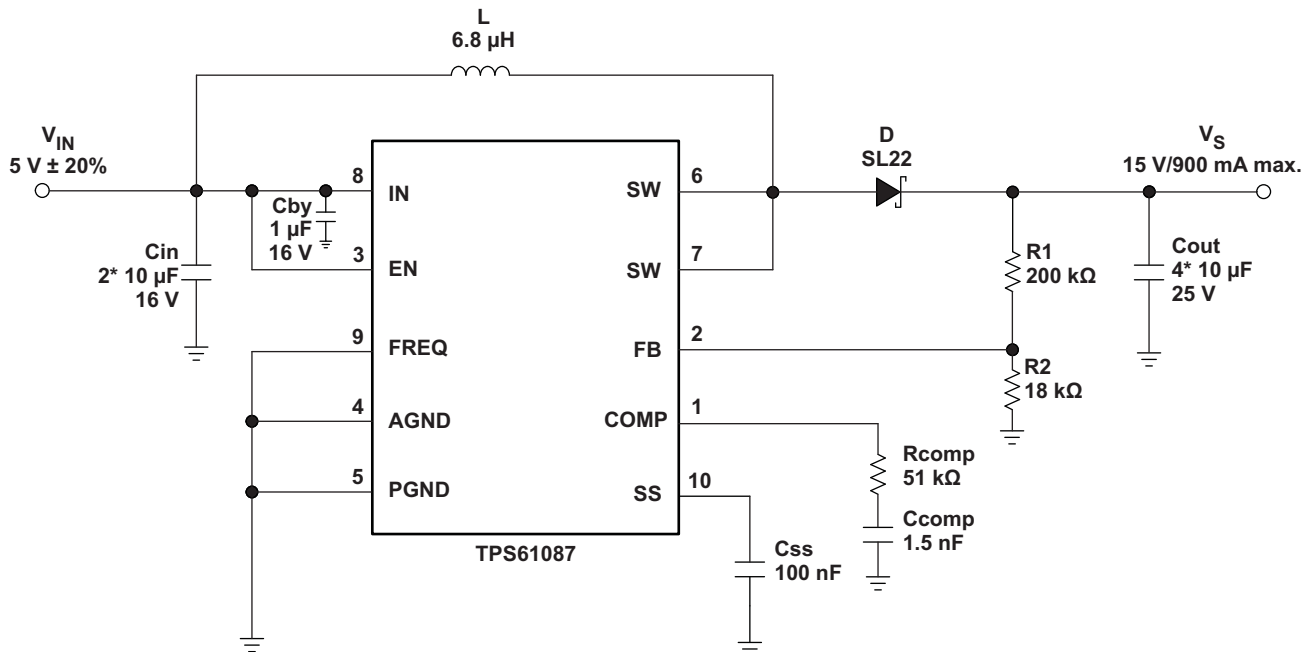


Figure 15. Typical Application, 5 V to 15 V ( $f_s = 650$  kHz)

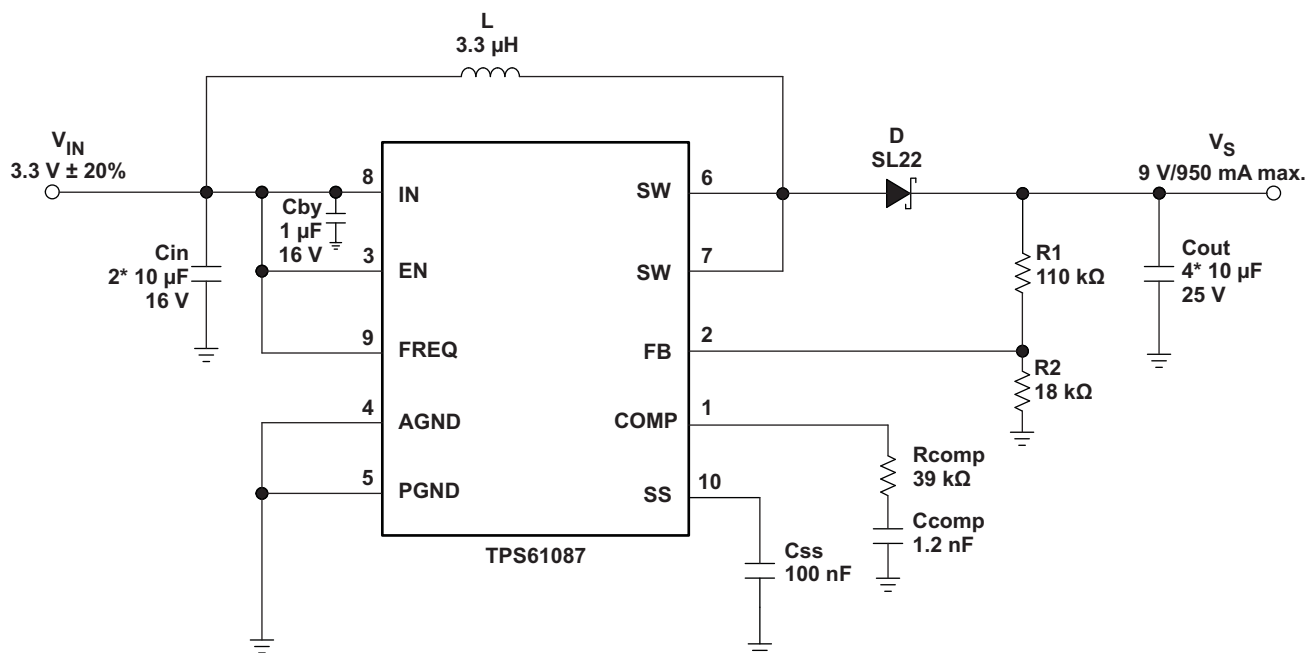


Figure 16. Typical Application, 3.3 V to 9 V ( $f_s = 1.2$  MHz)

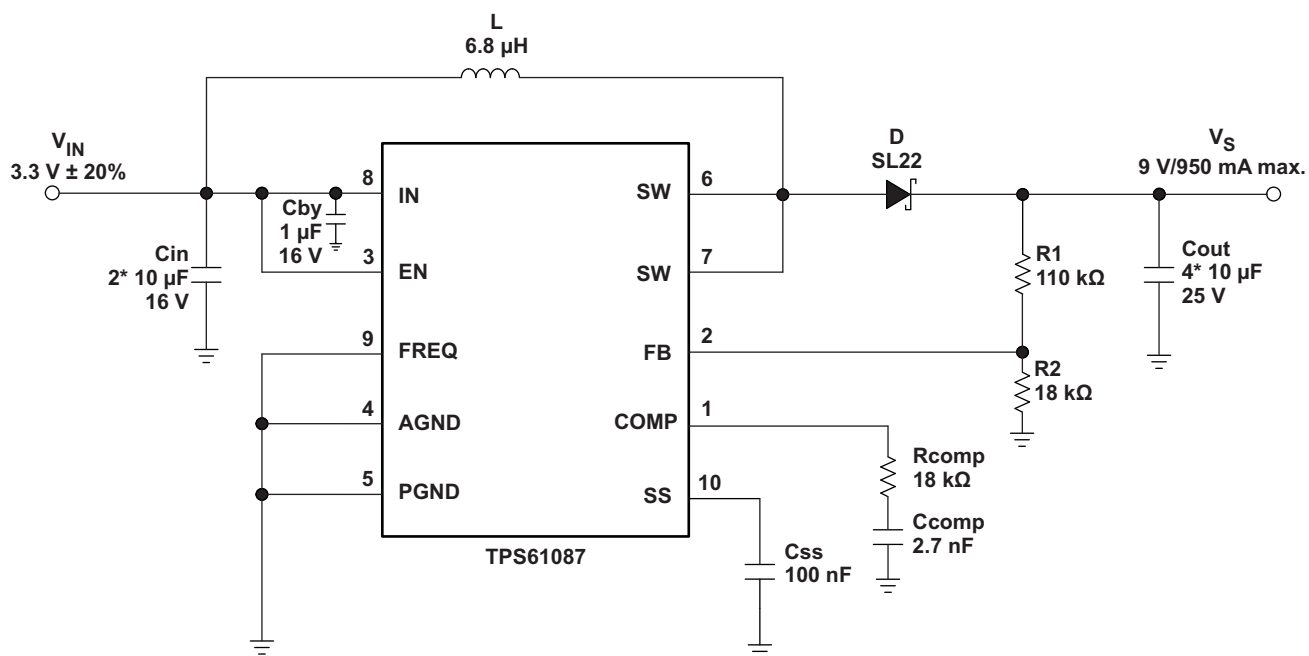


Figure 17. Typical Application, 3.3 V to 9 V ( $f_s = 650$  kHz)

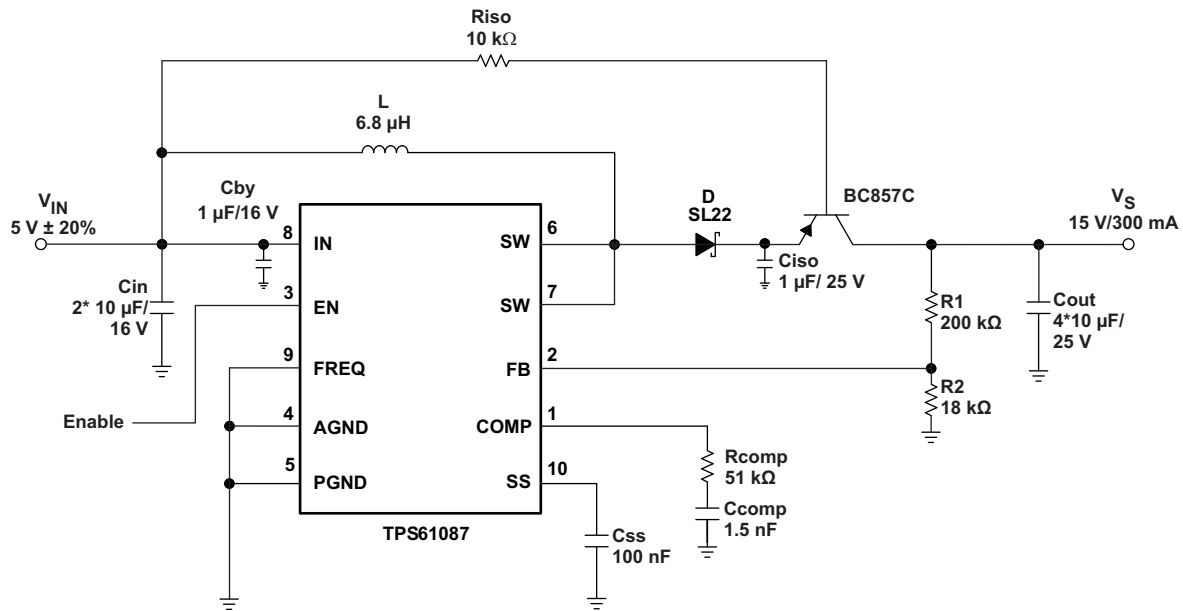


Figure 18. Typical Application with External Load Disconnect Switch

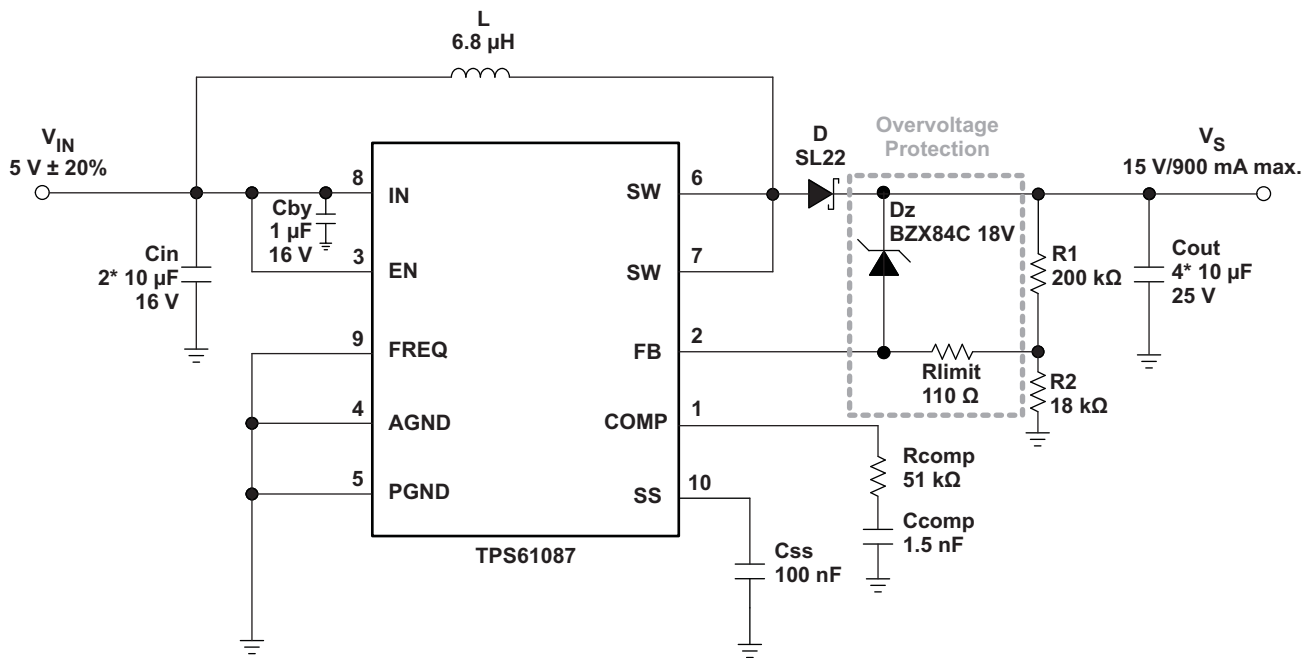


Figure 19. Typical Application, 5 V to 15 V ( $f_s = 1.2\text{ MHz}$ ) with Overvoltage Protection

## TFT LCD APPLICATION

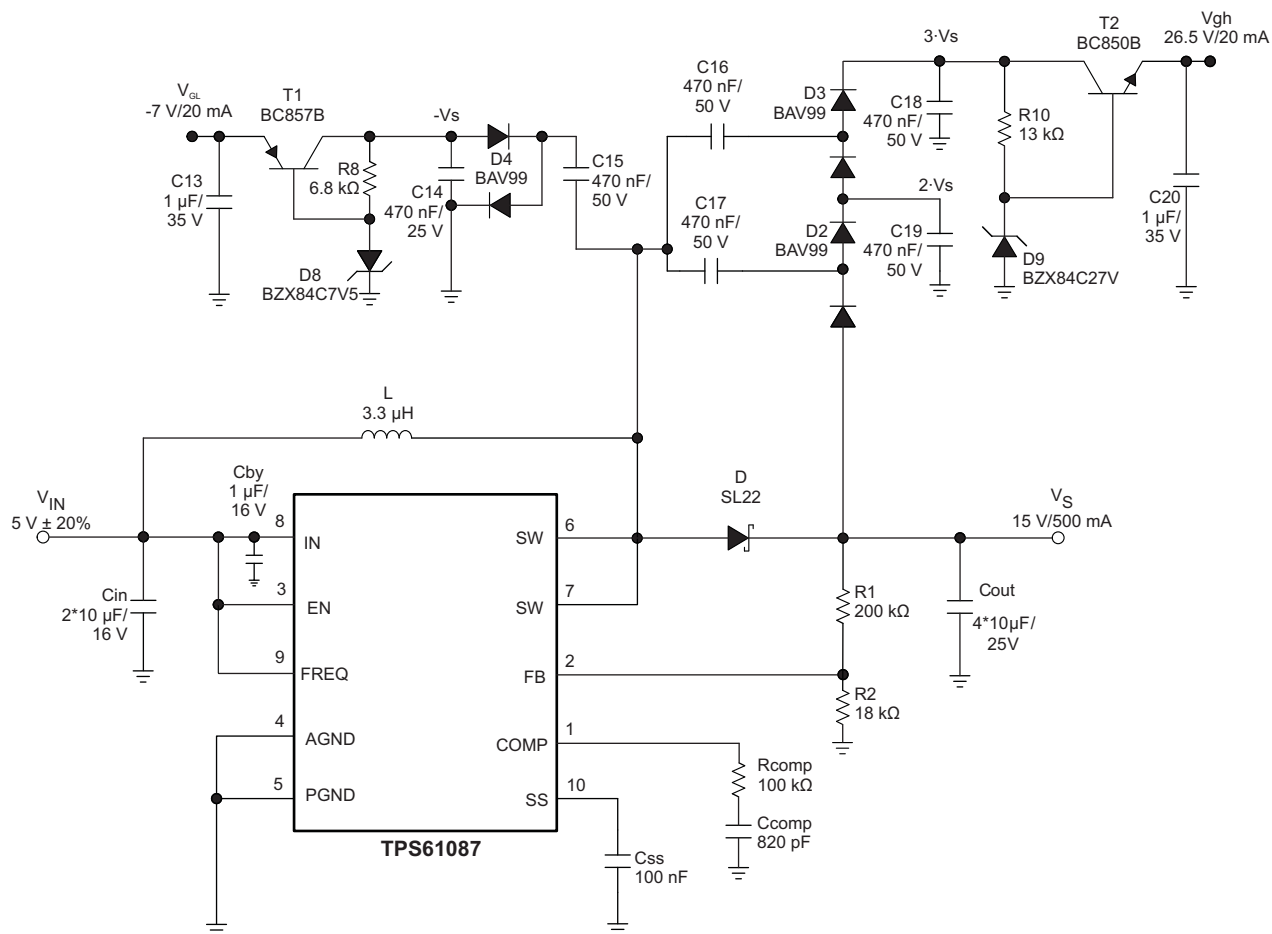


Figure 20. Typical Application 5 V to 15 V ( $f_s = 1.2\text{ MHz}$ ) for TFT LCD with External Charge Pumps (VGH, VGL)

## WHITE LED APPLICATIONS

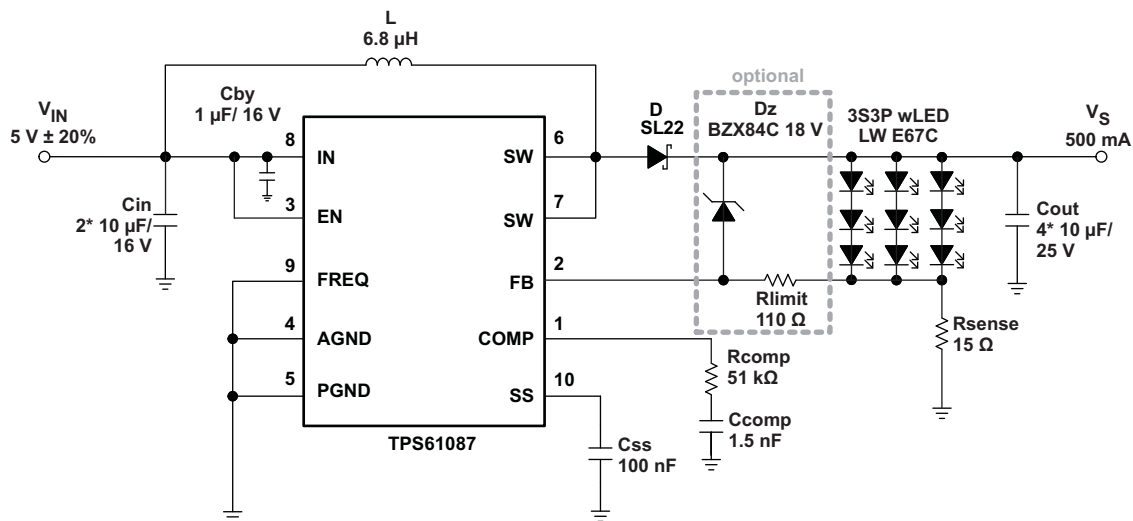


Figure 21. Simple Application (5 V input voltage) ( $f_s = 650$  kHz) for wLED Supply (3S3P) (with optional clamping Zener diode)

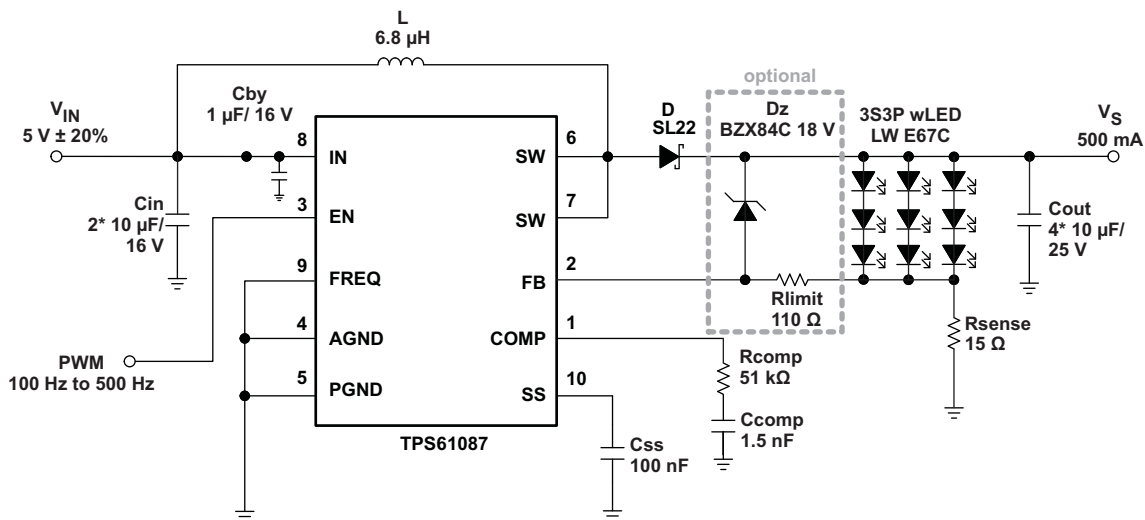
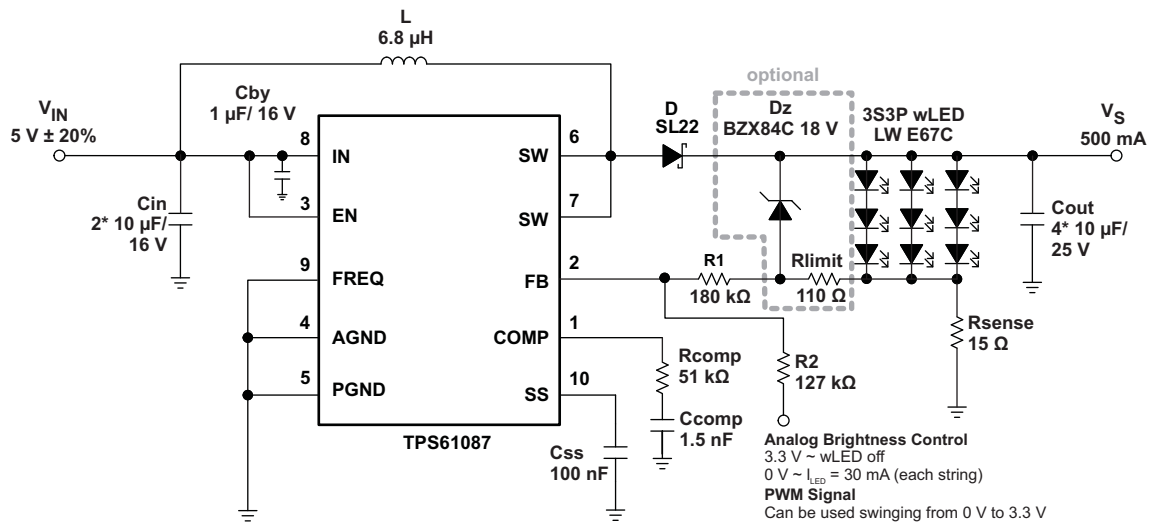


Figure 22. Simple Application (5 V input voltage) ( $f_s = 650$  kHz) for wLED Supply (3S3P) with Adjustable Brightness Control using a PWM Signal on the Enable Pin (with optional clamping Zener diode)



**Figure 23. Simple Application (5 V input voltage) ( $f_s = 650$  kHz) for wLED Supply (3S3P) with Adjustable Brightness Control using an Analog Signal on the Feedback Pin (with optional clamping Zener diode)**

## REVISION HISTORY

| Changes from Original (May 2008) to Revision A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Page                                                                                                       |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|
| <ul style="list-style-type: none"> <li>Added three paragraphs of text to the Detailed Description - following the Block Diagram .....</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 8                                                                                                          |
| Changes from Revision A (June 2008) to Revision B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | Page                                                                                                       |
| <ul style="list-style-type: none"> <li>Added DSC device to top of front page .....</li> <li>Changed the Description to read From: The selectable frequency of 650 kHz and 1.2 MHz... To: The selectable frequency of 650 kHz or 1.2 MHz .....</li> <li>Added DSC package to ORDERING INFORMATION .....</li> <li>Deleted Lead temperature from Absolute Maximum Ratings .....</li> <li>Changed Voltage on pin SW from 20 V to –0.3 to 20 V in Absolute Maximum Ratings .....</li> <li>Deleted <math>R_{\theta JA}</math> from DISSIPATION RATINGS .....</li> <li>Changed <math>f_{osc}</math> to <math>f_s</math> in Electrical Characteristics Boost Converter Oscillator Frequency .....</li> <li>Changed <math>FREQ = high</math> to <math>FREQ = V_{IN}</math> in Electrical Characteristics Boost Converter Oscillator Frequency .....</li> <li>Changed <math>FREQ = low</math> to <math>FREQ = GND</math> in Electrical Characteristics Boost Converter Oscillator Frequency .....</li> <li>Added DSC package to PIN ASSIGNMENT .....</li> <li>Added Maximum load current vs. Input voltage graph .....</li> <li>Added Maximum load current vs. Input voltage graph .....</li> <li>Changed <math>f</math> to <math>f_s</math> and Frequency to Oscillator Frequency in <a href="#">Figure 11</a> .....</li> <li>Changed <math>f</math> to <math>f_s</math> and Frequency to Oscillator Frequency in <a href="#">Figure 12</a> .....</li> <li>Changed the text to the Detailed Description - reduced the number of paragraphs from four to two. ....</li> <li>Changed the Design Procedures step 3 details - to make formulas easier to understand .....</li> <li>Changed Inductor Selection text From: Typically, it is recommended that the inductor current ripple is below 20% To: Typically, it is recommended that the inductor current ripple is below 35% .....</li> <li>Changed the format of <a href="#">Table 3</a> .....</li> <li>Changed wording in Compensation description .....</li> <li>Added detailed information following <a href="#">Table 4</a> - to make formulas easier to understand .....</li> <li>Changed wording in Thermal Shutdown section .....</li> </ul> | 1<br>1<br>2<br>2<br>2<br>2<br>3<br>3<br>3<br>4<br>4<br>4<br>7<br>7<br>8<br>9<br>10<br>12<br>12<br>12<br>13 |

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package Qty | Eco Plan<br>(2)            | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples                 |
|------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| TPS61087DRCR     | ACTIVE        | SON          | DRC                | 10   | 3000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 85    | PMOQ                     | <a href="#">Samples</a> |
| TPS61087DRCRG4   | ACTIVE        | SON          | DRC                | 10   | 3000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 85    | PMOQ                     | <a href="#">Samples</a> |
| TPS61087DRCT     | ACTIVE        | SON          | DRC                | 10   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 85    | PMOQ                     | <a href="#">Samples</a> |
| TPS61087DRCTG4   | ACTIVE        | SON          | DRC                | 10   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 85    | PMOQ                     | <a href="#">Samples</a> |
| TPS61087DSCR     | ACTIVE        | WSON         | DSC                | 10   | 3000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 85    | PMWI                     | <a href="#">Samples</a> |
| TPS61087DSCT     | ACTIVE        | WSON         | DSC                | 10   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 85    | PMWI                     | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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**OTHER QUALIFIED VERSIONS OF TPS61087 :**

- Automotive: [TPS61087-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


|    |                                                           |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS61087DRCR | SON          | DRC             | 10   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS61087DRCR | SON          | DRC             | 10   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS61087DRCT | SON          | DRC             | 10   | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS61087DRCT | SON          | DRC             | 10   | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS61087DSCR | SON          | DSC             | 10   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS61087DSCT | SON          | DSC             | 10   | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS

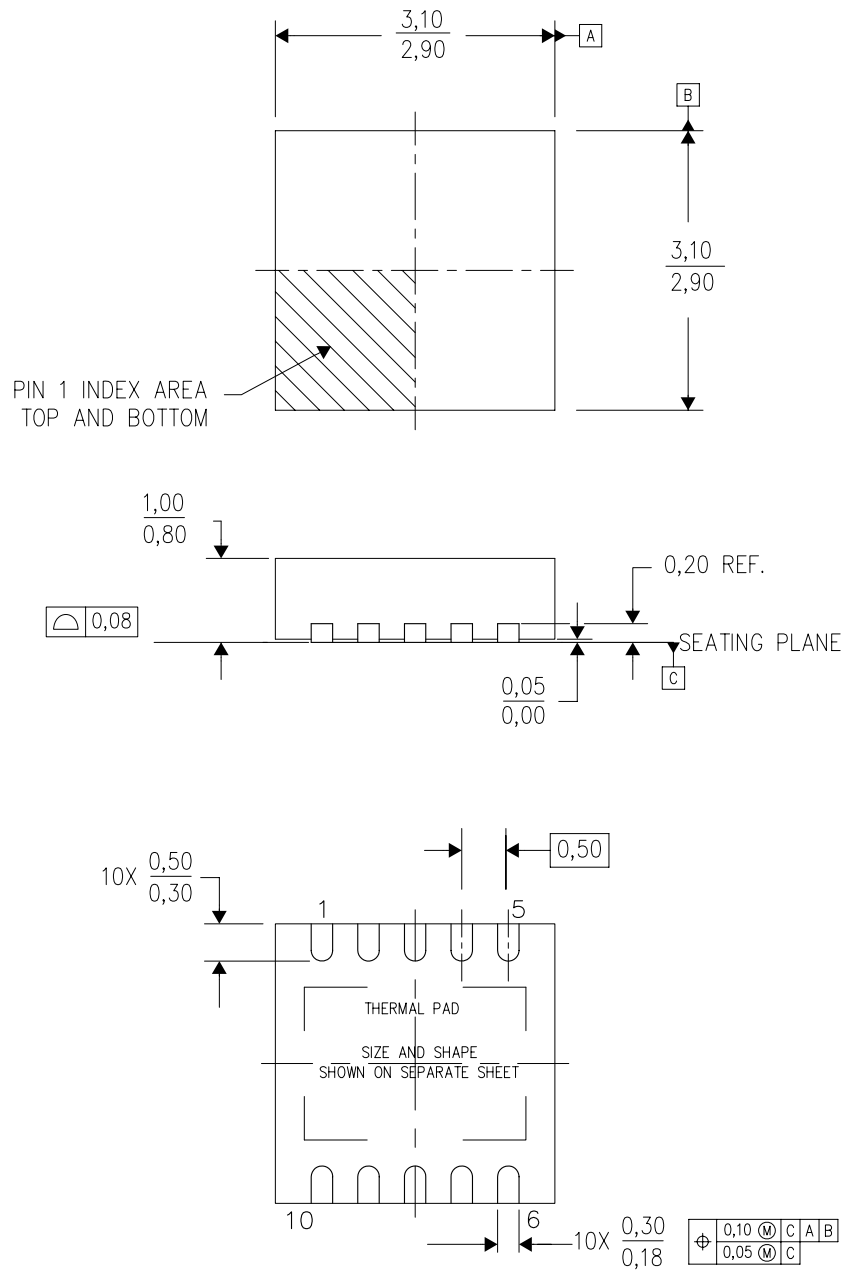


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS61087DRCR | SON          | DRC             | 10   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS61087DRCR | SON          | DRC             | 10   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS61087DRCT | SON          | DRC             | 10   | 250  | 210.0       | 185.0      | 35.0        |
| TPS61087DRCT | SON          | DRC             | 10   | 250  | 210.0       | 185.0      | 35.0        |
| TPS61087DSCR | SON          | DSC             | 10   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS61087DSCT | SON          | DSC             | 10   | 250  | 210.0       | 185.0      | 35.0        |

DRC (S-PVSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



4204102-3/L 09/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Small Outline No-Lead (SON) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

DRC (S-PVSON-N10)

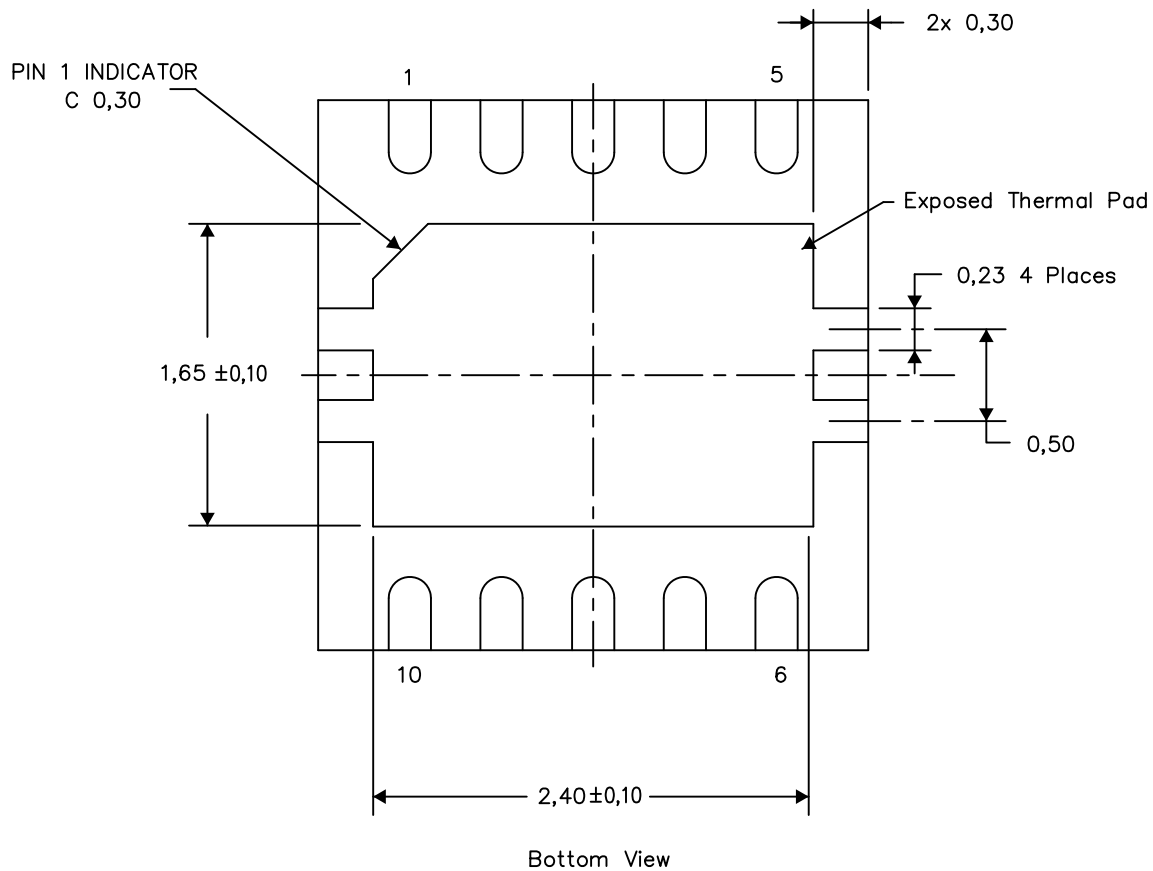
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



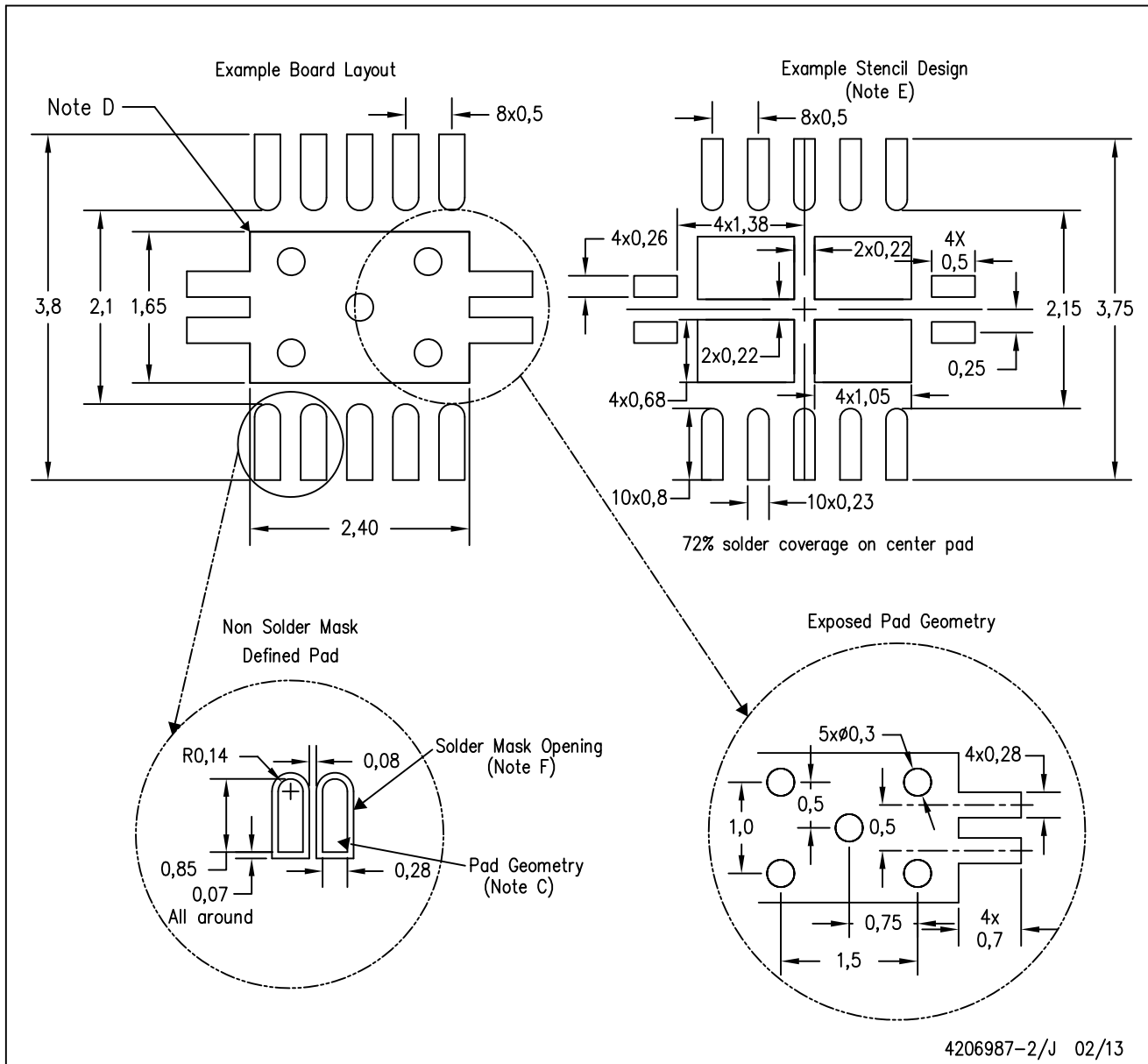
Exposed Thermal Pad Dimensions

4206565-3/Q 12/12

NOTE: A. All linear dimensions are in millimeters

DRC (S-PVSON-N10)

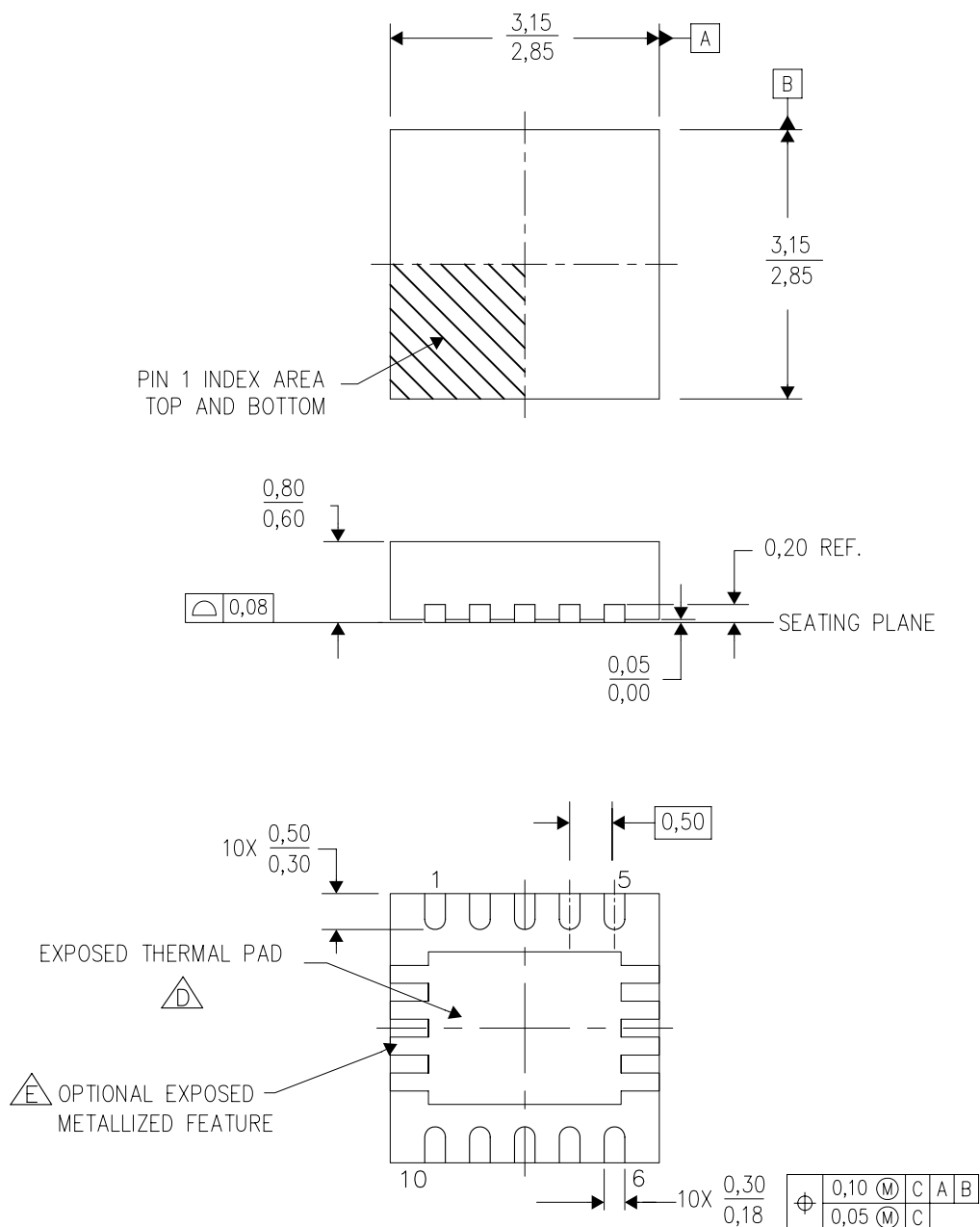
PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

DSC (S-PWSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



4207383/E 01/11

- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
 B. This drawing is subject to change without notice.  
 C. Small Outline No-Lead (SON) package configuration.  
 D. The package thermal pad must be soldered to the board for thermal and mechanical performance.  
 E. See the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

## THERMAL PAD MECHANICAL DATA

DSC (S-PWSON-N10)

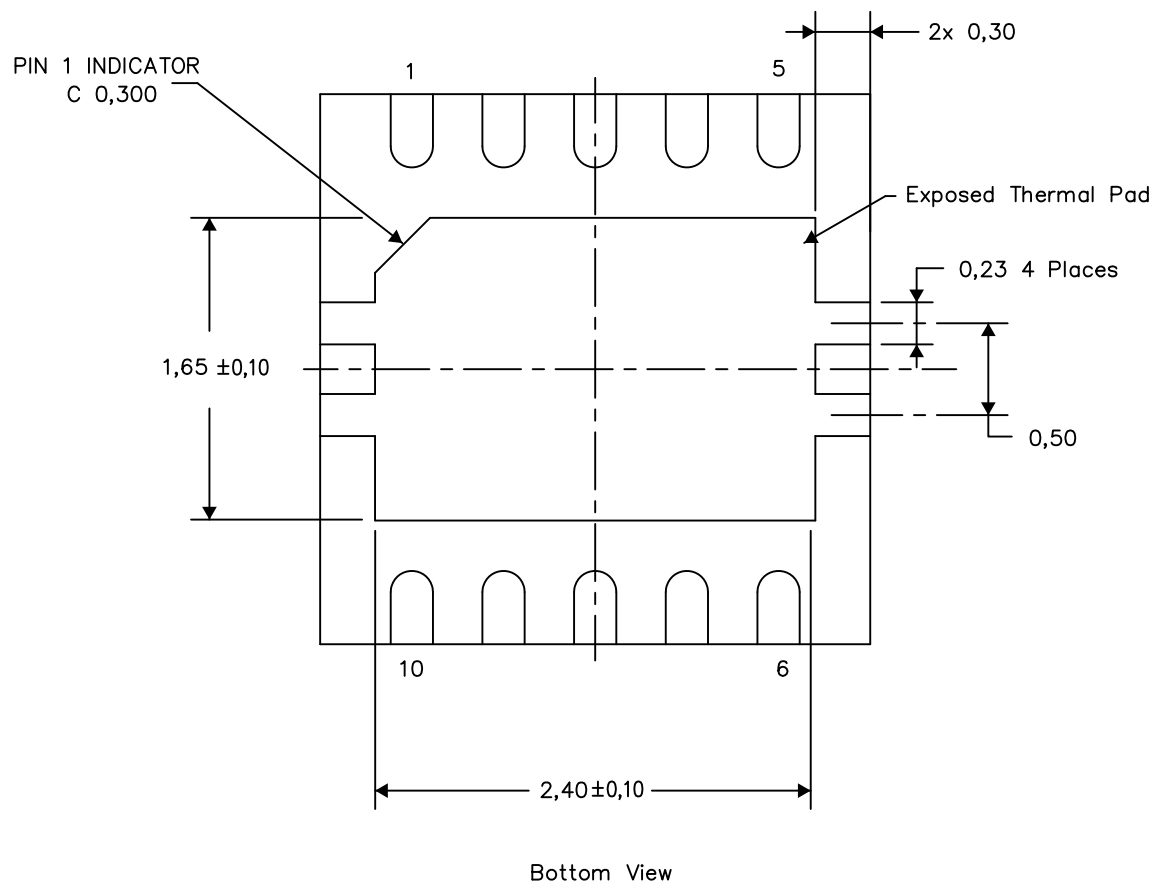
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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The exposed thermal pad dimensions for this package are shown in the following illustration.



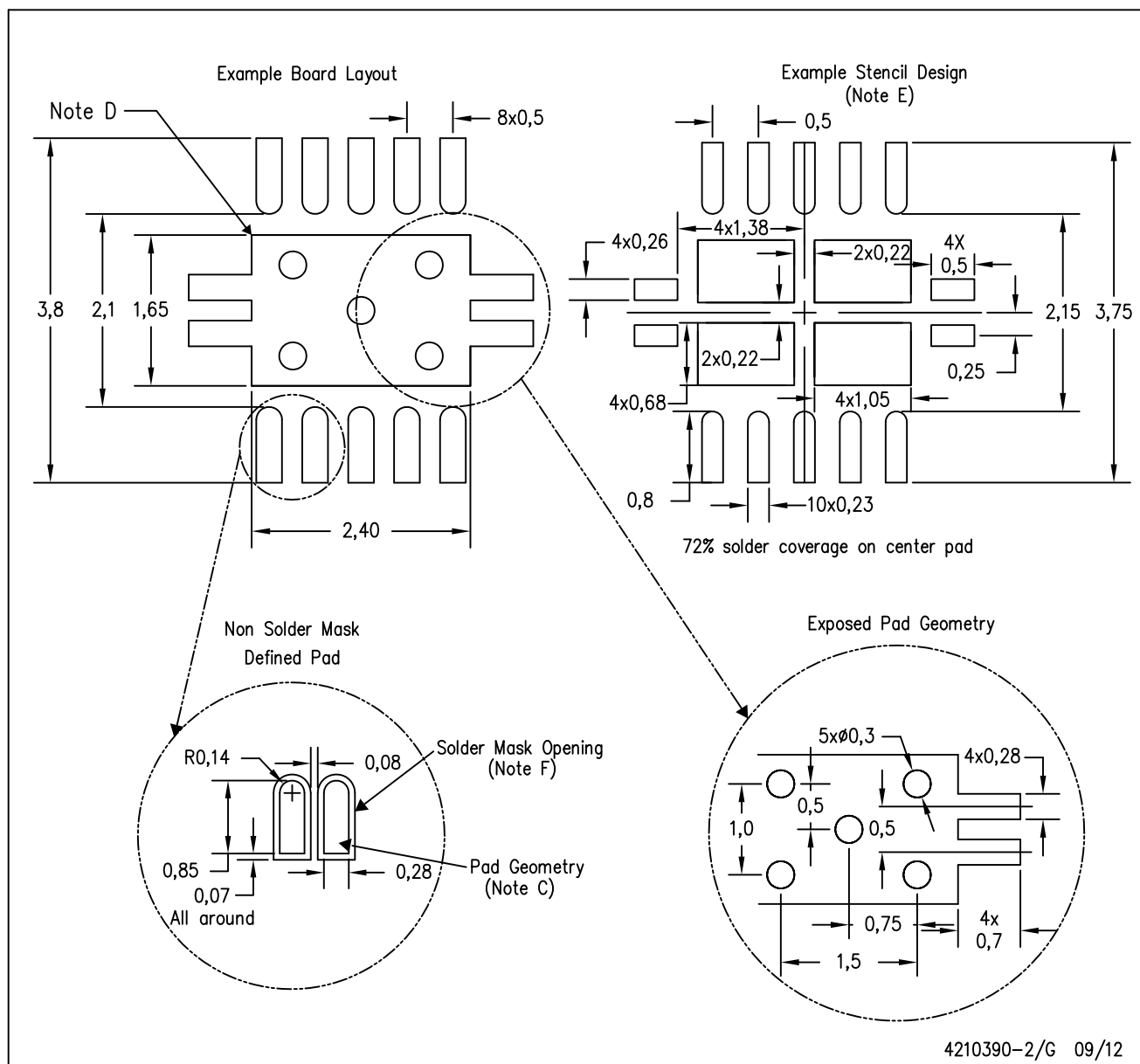
### Exposed Thermal Pad Dimensions

4210391-2/1 12/12

NOTE: A. All linear dimensions are in millimeters

DSC (S-PWSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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