# SINGLE SYNCHRONOUS STEP-DOWN CONTROLLER FOR LOW VOLTAGE POWER RAILS

**Check for Samples: TPS53114**

## FEATURES

- **D-CAP2™ Mode Control**
  - **Fast Transient Response**
  - **No External Parts Required For Loop Compensation**
  - **Compatible with Ceramic Output Capacitors**
- **High Initial Reference Accuracy (±1%)**
- **Low Output Ripple**
- **Wide Input Voltage Range: 4.5 V to 24 V**
- **Output Voltage Range: 0.76 V to 5.5 V**
- **Low-Side $R_{DS(on)}$ Loss-Less Current Sensing**
- **Adaptive Gate Drivers with Integrated Boost Diode**
- **Adjustable Soft Start**
- **Pre-Biased Soft Start**
- **Selectable Switching Frequency 350 kHz / 700 kHz**
- **Cycle-By-Cycle Over Current Limiting Control**
- **Thermally Compensated OCP by 4000 ppm/°C at $I_{TRIP}$**

## APPLICATIONS

- **Point-of-Load Regulation in Low Power Systems for Wide Range of Applications**
  - **Digital TV Power Supply**
  - **Networking Home Terminal**
  - **Digital Set Top Box (STB)**
  - **DVD Player / Recorder**
  - **Gaming Consoles**

## DESCRIPTION

The TPS53114 is a single, adaptive on-time D-CAP2™ mode synchronous buck controller. The TPS53114 enables system designers to complete the suite of various end equipment's power bus regulators with cost effective low external component count and low standby current solution. The main control loop for the TPS53114 uses the D-CAP2™ mode control which provides a very fast transient response with no external components. The TPS53114 also has a circuit that enables the device to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP and ultra-low ESR ceramic capacitors. The device provides convenient and efficient operation with input voltages from 4.5 V to 24 V and output voltage from 0.76 V to 5.5 V.

The TPS53114 is available in the 16-pin TSSOP and HTSSOP packages, and is specified from –40°C to 85°C ambient temperature range.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## TYPICAL APPLICATION CIRCUITS

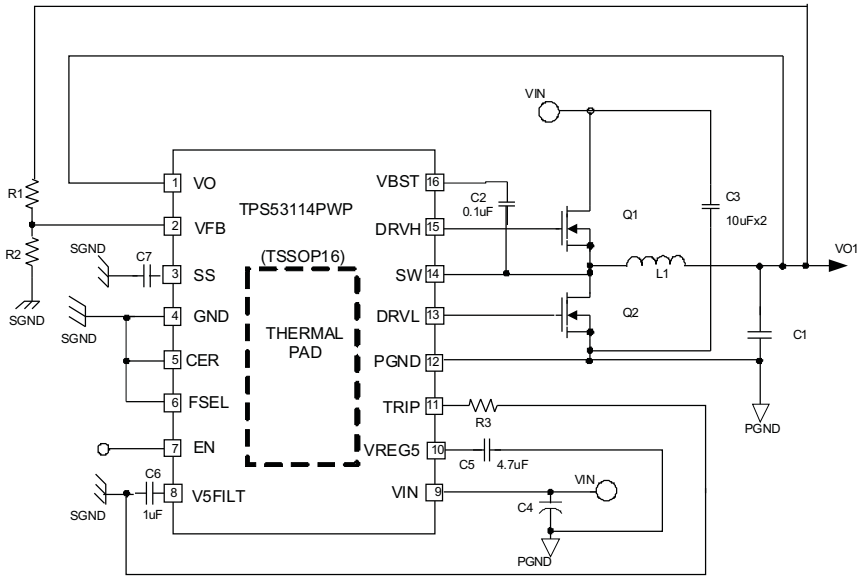



**Figure 1. HTSSOP**

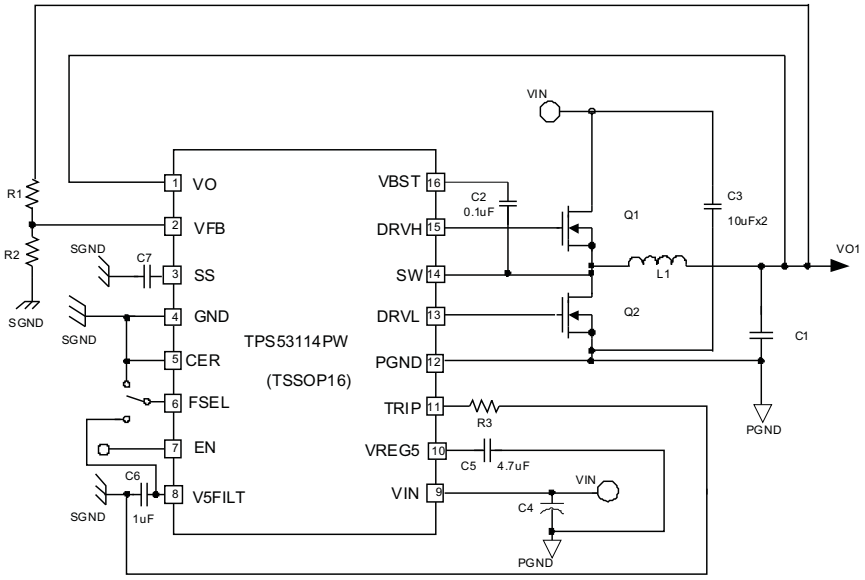



**Figure 2. TSSOP**

## ORDERING INFORMATION(1) (2)

| $T_A$ | PACKAGE(3) | ORDERING PART NUMBER | PINS | OUTPUT SUPPLY | ECO PLAN |
|---|---|---|---|---|---|
| –40°C to 85°C | HTSSOP (Thermal Pad ) | TPS53114PWPR | 16 | Tape-and-Reel | Green (RoHS & no Sb/Br) |
| | | TPS53114PWP | | Tube | |
| | TSSOP | TPS53114PWR | | Tape-and-Reel | |
| | | TPS53114PW | | Tube | |

(1) All packaging options have Cu NIPDAU lead/ball finish.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

## ABSOLUTE MAXIMUM RATINGS

Operating under free-air temperature range (unless otherwise noted) (1)

| | | VALUE | UNIT |
|---|---|---|---|
| Input voltage range | VIN, EN | –0.3 to 26 | V |
| | VBST | –0.3 to 32 | |
| | VBST - SW | –0.3 to 6 | |
| | V5FILT, VFB, TRIP, VO, FSEL, CER | –0.3 to 6 | |
| Output voltage range | DRVH | –1 to 32 | V |
| | DRVH - SW | –0.3 to 6 | |
| | SW | –2 to 26 | |
| | DRVL, VREG5, SS | –0.3 to 6 | |
| | PGND | –0.3 to 0.3 | |
| $T_A$ | Operating ambient temperature range | –40 to 85 | °C |
| $T_{STG}$ | Storage temperature range | –55 to 150 | °C |
| $T_J$ | Junction temperature range | –40 to 150 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## DISSIPATION RATING TABLE (2 oz. trace and copper pad with solder)

| PACKAGE | $T_A$ < 25°C POWER RATING | DERATING FACTOR ABOVE $T_A$ = 25°C | $T_A$ = 85°C POWER RATING |
|---|---|---|---|
| 16-pin HTSSOP (PWP) | 2.73 W | 27.3 mW/°C | 1.09 W |
| 16-pin TSSOP (PW) | 0.62 W | 6.2 mW/°C | 0.25 W |

## RECOMMENDED OPERATING CONDITIONS

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| | Supply input voltage range | VIN | 4.5 | 24 | V |
| | | V5FILT | 4.5 | 5.5 | |
| | Input voltage range | VBST | –0.1 | 30 | V |
| | | VBST - SW | –0.1 | 5.5 | |
| | | VFB, VO, FSEL, CER | –0.1 | 5.5 | |
| | | TRIP | –0.1 | 0.3 | |
| | | EN | –0.1 | 24 | |
| | Output Voltage range | DRVH | –0.1 | 30 | V |
| | | VBST - SW | –0.1 | 5.5 | |
| | | SW | 1.8 | 24 | |
| | | DRVL, VREG5, SS | –0.1 | 5.5 | |
| | | PGND | –0.1 | 0.1 | |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |
| $T_J$ | Operating junction temperature | | –40 | 125 | °C |

## ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range, VIN = 12 V (unless otherwise noted)

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| $I_{IN}$ | VIN supply current | VIN current, $T_A$ = 25°C, VREG5 tied to V5FLT, EN = 5V, VFB = 0.8V, SW = 0.5V | | 350 | 600 | µA |
| $I_{VINSDN}$ | VIN shutdown current | VIN current, $T_A$ = 25°C, No Load , EN = 0V, VREG5 = ON | | 28 | 60 | µA |
| **VFB VOLTAGE and DISCHARGE RESISTANCE** | | | | | | |
| $V_{BG}$ | Bandgap Initial regulation accuracy | $T_A$ = 25°C | –1.0 | | 1.0 | % |
| $V_{VFBTHL}$ | VFB threshold voltage | $T_A$ = 25°C , FSEL = 0 V, CER = V5FILT | 755 | 765 | 775 | mV |
| | | $T_A$ = –40°C to 85°C, FSEL = 0V, CER = V5FILT | 752 | | 778 | |
| $V_{VFBTHH}$ | VFB threshold voltage | $T_A$ = 25°C , FSEL = CER = V5FILT | 748 | 758 | 768 | mV |
| | | $T_A$ = –40°C to 85°C, FSEL = CER = V5FILT | 745 | | 771 | |
| $I_{VFB}$ | VFB Input Current | VFB = 0.8V, $T_A$ = 25°C | –100 | –10 | 100 | nA |
| $R_{Dischg}$ | Vo Discharge Resistance | EN = 0V, VO = 0.5V, $T_A$ = 25°C | | 40 | 80 | Ω |
| **VREG5 OUTPUT** | | | | | | |
| $V_{VREG5}$ | VREG5 Output Voltage | $T_A$=25°C, 5.5V < VIN < 24V, 0 < $I_{VREG5}$ < 10mA | 4.8 | 5.0 | 5.2 | V |
| $V_{LN5}$ | Line regulation | 5.5V < VIN < 24V, $I_{VREG5}$ = 10mA | | | 20 | mV |
| $V_{LD5}$ | Load regulation | 1mA < $I_{VREG5}$ < 10mA | | | 40 | mV |
| $I_{VREG5}$ | Output current | VIN = 5.5V, $V_{VREG5}$ = 4.0V, $T_A$ = 25°C | | 170 | | mA |
| **OUTPUT: N-CHANNEL MOSFET GATE DRIVERS** | | | | | | |
| $R_{DRVH}$ | DRVH resistance | Source, $I_{DRVH}$ = –100mA | | 5.5 | 11 | Ω |
| | | Sink, $I_{DRVH}$ = 100mA | | 2.5 | 5 | |
| $R_{DRVL}$ | DRVL resistance | Source, $I_{DRVL}$ = –100mA | | 4 | 8 | Ω |
| | | Sink, $I_{DRVL}$ = 100mA | | 2 | 4 | |
| $T_D$ | Dead time | DRVH-low to DRVL-on | 20 | 50 | 80 | ns |
| | | DRVL-low to DRVH-on | 20 | 40 | 80 | |
| **INTERNAL BST DIODE** | | | | | | |
| $V_{FBST}$ | Forward Voltage | $V_{VREG5-VBST}$, IF = 10mA, $T_A$ = 25°C | 0.7 | 0.8 | 0.9 | V |
| $I_{VBSTLK}$ | VBST Leakage Current | VBST = 29V, SW = 24V, $T_A$ = 25°C | | 0.1 | 1 | µA |

## ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range, VIN = 12 V (unless otherwise noted)

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ON-TIME TIMER CONTROL** | | | | | | |
| $T_{ONL}$ | On Time | SW = 12V, VO = 1.8V, FSEL = 0V | | 390 | | ns |
| $T_{ONH}$ | On Time | SW = 12V, VO = 1.8V, FSEL = V5FILT | | 139 | | ns |
| $T_{OFFL}$ | Min off time | SW = 0.7V, $T_A$ = 25°C, VFB = 0.7V, FSEL = 0V | | 285 | | ns |
| $T_{OFFH}$ | Min off time | SW = 0.7V, $T_A$ = 25°C, VFB = 0.7V, FSEL = V5FILT | | 216 | | ns |
| **SOFT START** | | | | | | |
| $I_{ssc}$ | SS charge current | VSS = 0V , SOURCE CURRENT | 1.4 | 2.0 | 2.6 | µA |
| $I_{ssd}$ | SS discharge current | VSS = 0.5V , SINK CURRRENT | 100 | 150 | | µA |
| **UVLO** | | | | | | |
| $V_{UV5VFILT}$ | V5FILT UVLO threshold | V5FILT rising | 3.7 | 4.0 | 4.3 | V |
| | | Hysteresis | 0.2 | 0.3 | 0.4 | |
| **LOGIC THRESHOLD** | | | | | | |
| $V_{ENH}$ | EN H-level threshold voltage | EN | 2.0 | | | V |
| $V_{ENL}$ | EN L-level threshold voltage | EN | | | 0.3 | V |
| **CURRENT SENSE** | | | | | | |
| $I_{TRIP}$ | TRIP source current | VTRIP = 0.1V, $T_A$ = 25°C | 8.5 | 10 | 11.5 | µA |
| $TC_{ITRIP}$ | $I_{TRIP}$ temperature coefficient | on the basis of 25°C | | 4000 | | ppm/°C |
| $V_{OCLoff}$ | OCP compensation offset | ($V_{TRIP-GND}$-$V_{PGND-SW}$) voltage, $V_{TRIP-GND}$ = 60mV, $T_A$ = 25°C | –10 | 0 | 10 | mV |
| | | ($V_{TRIP-GND}$-$V_{PGND-SW}$) voltage, VTRIP-GND = 60mV | –15 | | 15 | mV |
| $V_{Rtrip}$ | Current limit threshold setting range | $V_{TRIP-GND}$ voltage | 30 | | 200 | mV |
| **OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION** | | | | | | |
| $V_{OVP}$ | Output OVP trip threshold | OVP detect | 110 | 115 | 120 | % |
| $T_{OVPDEL}$ | Output OVP prop delay | | | 1.5 | | µs |
| $V_{UVP}$ | Output UVP trip threshold | UVP detect | 65 | 70 | 75 | % |
| | | Hysteresis (recovery <20µs) | | 10 | | % |
| $T_{UVPDEL}$ | Output UVP delay | | 17 | 30 | 40 | µs |
| $T_{UVPEN}$ | Output UVP enable delay | UVP enable delay / soft start time | X1.4 | X1.7 | X2.0 | |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SDN}$ | Thermal shutdown threshold | Shutdown temperature(1) | | 150 | | °C |
| | | Hysteresis(1) | | 20 | | |

(1) Ensured by design. Not production tested.

## PIN FUNCTIONS

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| VBST | 16 | I | Supply input for high-side NFET driver. Bypass to SW with a high-quality 0.1-μF ceramic capacitor. An external schottky diode can be added from VREG5 if forward drop is critical to drive the high-side FET. |
| EN | 7 | I | Enable. Pull High to enable SMPS. |
| SS | 3 | O | Soft start programming pin. Connect capacitor from SS pin to GND to program soft start time. |
| VO | 1 | I | Output voltage input for on-time adjustment and output discharge. Connect directory to the output voltage. |
| VFB | 2 | I | D-CAP2 feedback input. Connect to output voltage with resistor divider. |
| GND | 4 | I | Signal ground pin. Connect to PGND and system ground at a single point. |
| DRVH | 15 | O | High-side N-channel MOSFET gate driver output. SW referenced driver switches between SW(OFF) and VBST(ON). |
| SW | 14 | I/O | Switch node connections for both the high-side driver and over current comparator. |
| DRVL | 13 | O | Low-side N-Channel MOSFET gate driver output. PGND referenced driver switches between PGND(OFF) and VREG5(ON). |
| PGND | 12 | I/O | Power ground connection for both the low-side driver and over current comparator. Connect PGND and GND strongly together near the IC. |
| TRIP | 11 | I | over current threshold programming pin. Connect to GND with a resister to set threshold for low-side $R_{DS(on)}$ current limit. |
| VIN | 9 | I | Supply Input for 5-V linear regulator. Bypass to GND with a minimum high-quality 0.1-μF ceramic capacitor. |
| V5FILT | 8 | I | 5-V supply input for the control circuitry except the MOSFET drivers. Bypass to GND with a minimum high-quality 1.0-μF ceramic capacitor. V5FILT is connected to VREG5 via internal 10-Ω resistor. |
| VREG5 | 10 | O | Output of 5-V linear regulator and supply for MOSFET driver. Bypass to GND with a minimum high-quality 4.7-μF ceramic capacitor. VREG5 is connected to V5FILT via internal 10-Ω resistor. |
| CER | 5 | I | Output capacitor select pin. Connect to GND for ceramic output capacitors. Connect to V5FILT for conductive polymer electrolyte type output capacitors (SP-CAP, POS-CAP, PXE). |
| FSEL | 6 | I | Switching frequency selection pin. Connect to GND for low switching frequency or connect to V5FILT for high switching frequency. |

## PIN ASSIGNMENT (TOP VIEW)

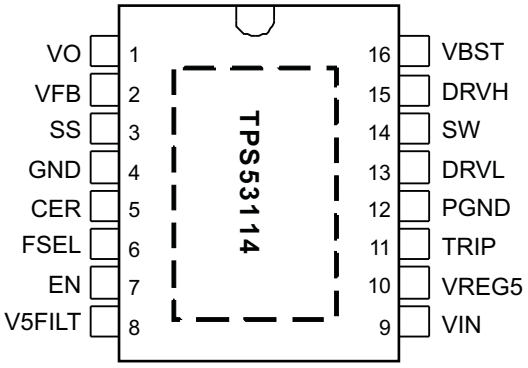



**Figure 3. HTSSOP 16-Pin PWP**

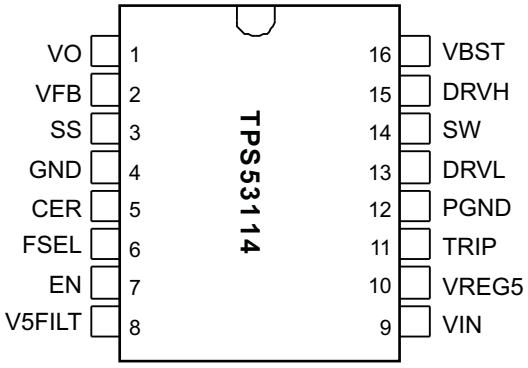
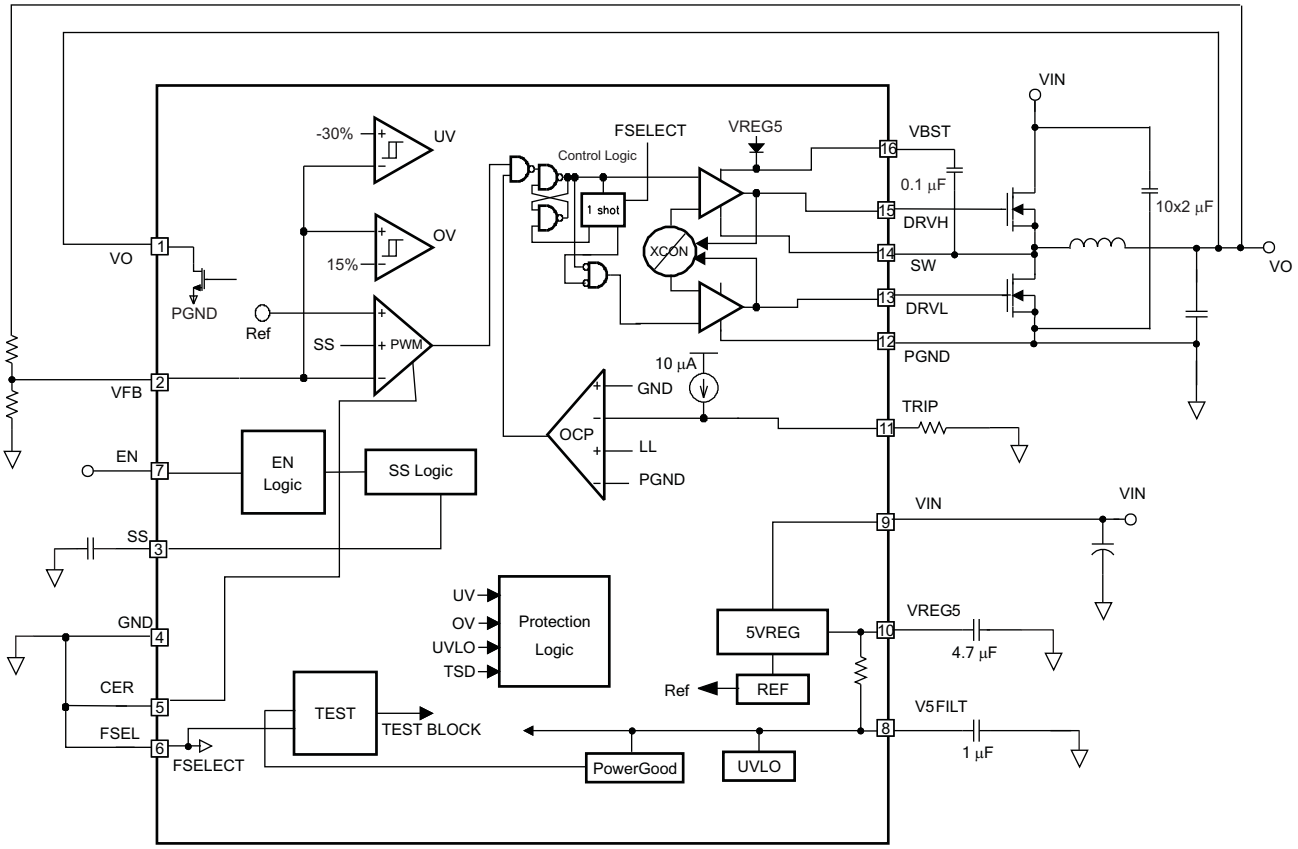



**Figure 4. TSSOP 16-Pin PW**

## FUNCTIONAL BLOCK DIAGRAM




## DETAILED DESCRIPTION

### PWM OPERATION

The main control loop of the TPS53114 is an adaptive on-time pulse width modulation (PWM) controller using a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. After an internal one-shot timer expires, this MOSFET is turned off. The one-shot timer is reset and the high-side MOSFET is turned back on when the feedback voltage falls below the reference voltage. The one shot is set by the converter input voltage VIN, and the output voltage VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. An internal ramp is added to the reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP mode control.

### DRIVERS

The TPS53114 contains two high-current resistive MOSFET gate drivers. The low-side driver is a ground referenced, VREG5 powered driver designed to drive the gate of a high-current, low $R_{DS(on)}$ N-channel MOSFET whose source is connected to PGND. The high-side driver is a floating SW referenced VBST powered driver designed to drive the gate of a high-current, low $R_{DS(on)}$ N-channel MOSFET. To maintain the VBST voltage during the high-side driver ON time, a capacitor is placed from SW to VBST. Each driver draws average current equal to gate charge ($Q_g$ at $V_{gs}$ = 5 V) times switching frequency ($f_{SW}$).

To prevent cross-conduction, there is a narrow dead-time when both high-side and low-side drivers are OFF between each driver transition. During this time the inductor current is carried by one of the MOSFET's body diodes.

## PWM FREQUENCY AND ADAPTIVE ON-TIME CONTROL

TPS53114 employs adaptive on-time control scheme and does not have a dedicated on board oscillator. TPS53114 runs with pseudo-constant frequency by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage. Therefore, when the duty ratio is VOUT/VIN, the frequency is constant.

## 5-VOLT REGULATOR

The TPS53114 has an internal 5-V low-dropout (LDO) Regulator to provide a regulated voltage for all both drivers and the IC's internal logic. A high-quality 4.7-μF or greater ceramic capacitor from VREG5 to GND is required to stabilize the internal regular. An internal 10-Ω resistor from VREG5 filters the regulator output to the IC's analog and logic input voltage, V5FILT. An additional high-quality 1.0-μF ceramic capacitor is required from V5FILT to GND to filter switching noise from VREG5.

## SOFT START

The TPS53114 has a programmable soft start . When the EN pin becomes high, 2.0-μA current begins charging the capacitor which is connected SS pin to GND. Smooth control of the output voltage is maintained during start up.

## PRE-BIAS SUPPORT

The TPS53114 supports pre-bias start-up without sinking current from the output capacitor. When enabled, the low-side driver is held off until the soft start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage (VFB)), then the TPS53114 slowly activates synchronous rectification by limiting the first DRVL pulses with a narrow on-time. This limited on-time is then incremented on a cycle-by-cycle basis until it coincides with the full 1-D off-time. This scheme prevents the initial sinking of current from the pre-bias output, and ensure that the output voltage ($V_{OUT}$) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

## SWITCHING FREQUENCY SELECTION

The TPS53114 allows the user to select from two different switching frequencies by connecting the FSEL pin to either GND or V5FILT. Connect FSEL to GND for a switching frequency ($f_{sw}$) of 350 KHz. Connect FSEL to V5FILT for a switching frequency of 700 KHz.

## OUTPUT DISCHARGE CONTROL

The TPS53114 discharges the outputs when EN is low, or the controller is turned off by the protection functions (OVP, UVP, UVLO, and thermal shutdown). The device discharges output using an internal 40-Ω MOSFET which is connected to VO and PGND. The external low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output. This discharge ensures that, on start, the regulated voltage always initializes from 0 V.

## OVER CURRENT PROTECTION

TPS53114 has a cycle-by-cycle over current limit feature. The over current limits the inductor valley current by monitoring the voltage drop across the low-side MOSFET $R_{DS(on)}$ during the low-side driver on-time. If the inductor current is larger than the over current limit (OCL), the TPS53114 delays the start of the next switching cycle until the sensed inductor current falls below the OCL current. MOSFET $R_{DS(on)}$ current sensing is used to provide an accuracy and cost effective solution without external devices. To program the OCL, the TRIP pin should be connected to GND through a trip voltage setting resistor, according to Equation 1 and Equation 2.

$$V_{TRIP} = I_{OCL} \bullet R_{DS(ON)} - \frac{(V_{IN} - V_O)}{2 \bullet L1 \bullet f_{SW}} \bullet \frac{V_O}{V_{IN}} \quad (1)$$

$$R_{TRIP}\,(k\Omega) = \frac{V_{TRIP}\,(mV)}{I_{TRIP}(\mu A)} \quad (2)$$

The trip voltage should be between 30 mV to 200 mV over all operational temperature, including the 4000 ppm/°C temperature slope compensation for the temperature dependency of the $R_{DS(on)}$. If the load current exceeds the over current limit, the voltage will begin to drop. If the over current conditions continues, the output voltage will fall below the under voltage protection threshold and the TPS53114 will shut down.

## OVER/UNDER VOLTAGE PROTECTION

TPS53114 monitors a resistor divided feedback voltage to detect over and under voltage. If the feedback voltage is higher than 115% of the reference voltage, the OVP comparator output goes high and the circuit latches the high-side MOSFET driver OFF and the low-side MOSFET driver ON. When the feedback voltage is lower than 70% of the reference voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 30 μs, TPS53114 latches OFF both top and bottom MOSFET drivers. This function is enabled approximately 1.7x $T_{SS}$ after power-on. The OVP and UVP latch off is reset when EN goes low level.

## UVLO PROTECTION

TPS53114 has V5FILT under voltage lock out protection (UVLO) that monitors the voltage of V5FILT pin. When the V5FILT voltage is lower than UVLO threshold voltage, the device is shut off. All output drivers are OFF and output discharge is ON. The UVLO is non-latch protection.

## THERMAL SHUTDOWN

The TPS53114 includes an over temperature protection shut-down feature. If the TPS53114 die temperature exceeds the OTP threshold (typically 150°C), both the high-side and low-side drivers are shut off, the output voltage discharge function is enabled and then the device is shut off until the die temperature drops. Thermal shutdown is a non-latch protection.

## TYPICAL CHARACTERISTICS

**VIN SUPPLY CURRENT vs JUNCTION TEMPERATURE**

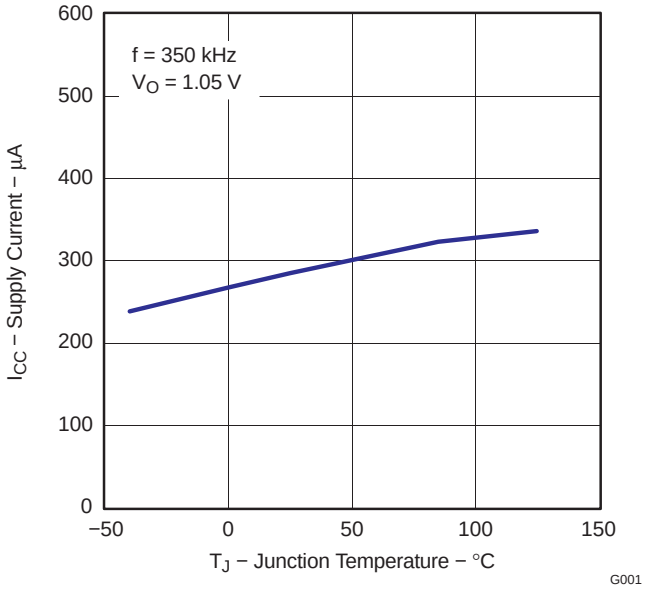



**Figure 5.**

**VIN SHUTDOWN CURRENT vs JUNCTION TEMPERATURE**

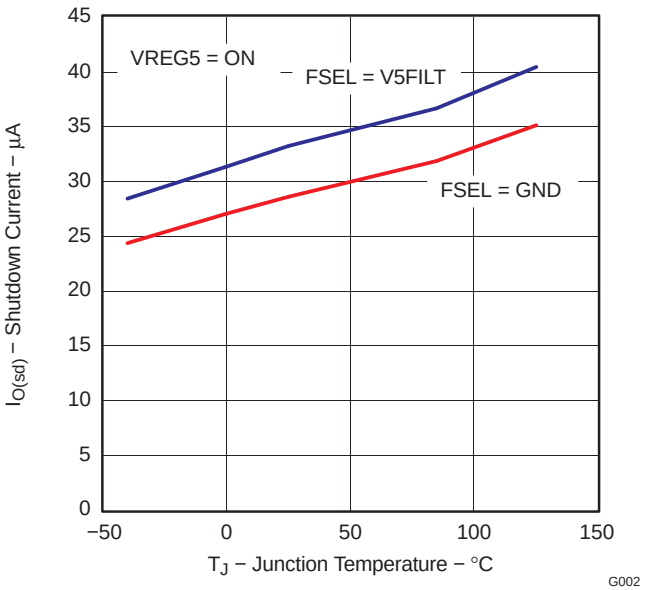



**Figure 6.**

**TRIP SOURCE CURRENT vs JUNCTION TEMPERATURE**

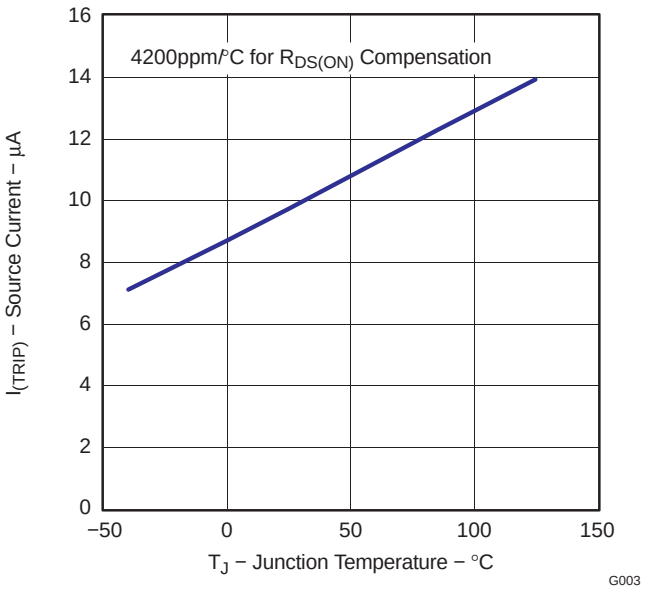



**Figure 7.**

**VREG5 VOLTAGE**

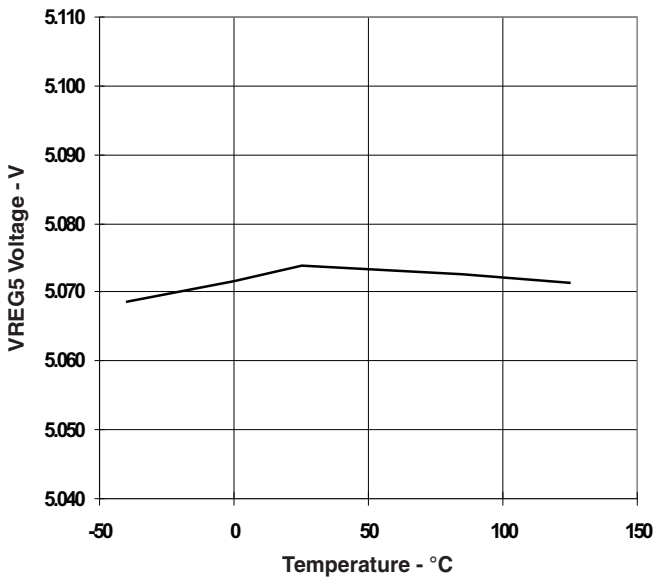



**Figure 8.**

## TYPICAL CHARACTERISTICS (continued)

**VREG5 VOLTAGE vs INPUT VOLTAGE**

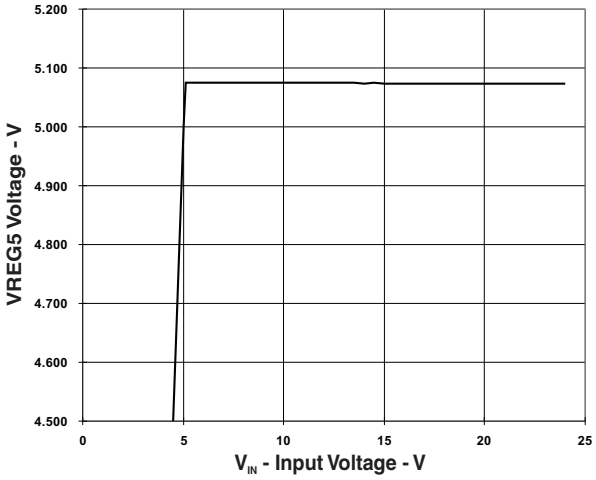



**Figure 9.**

**VFB VOLTAGE vs TEMPERATURE ($V_O$ = 1.05 V, $I_O$ = 4 A)**

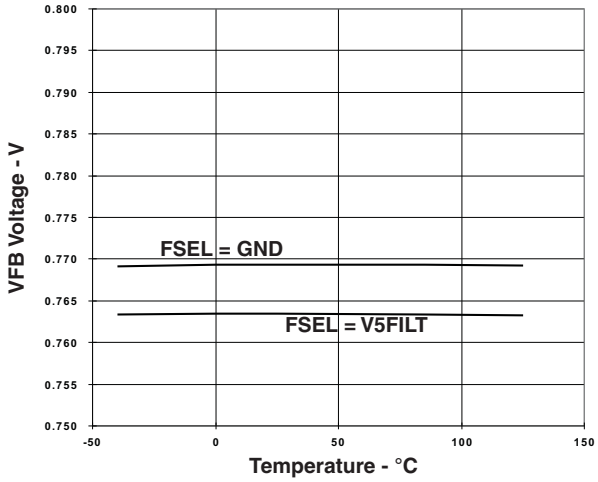



**Figure 10.**

**VFB VOLTAGE vs INPUT VOLTAGE**

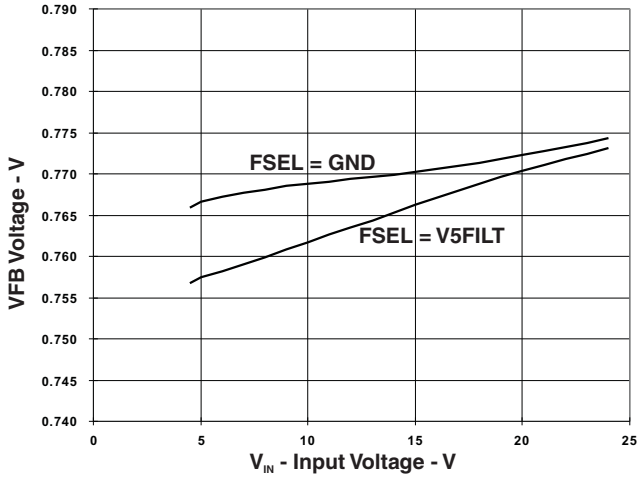



**Figure 11.**

## APPLICATION INFORMATION

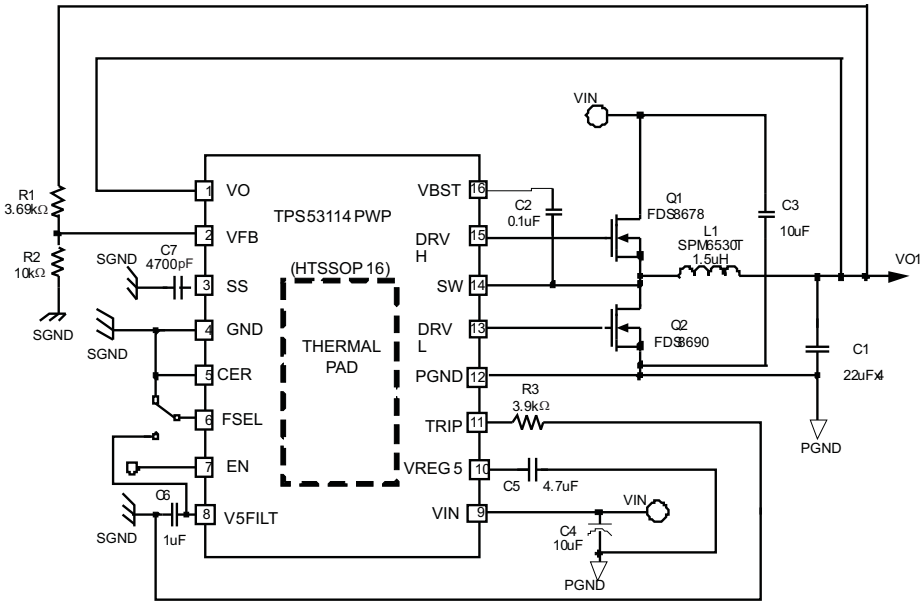



**Figure 12. Typical Application Circuit at 350-kHz Switching Frequency Selection (FSEL pin = GND)**

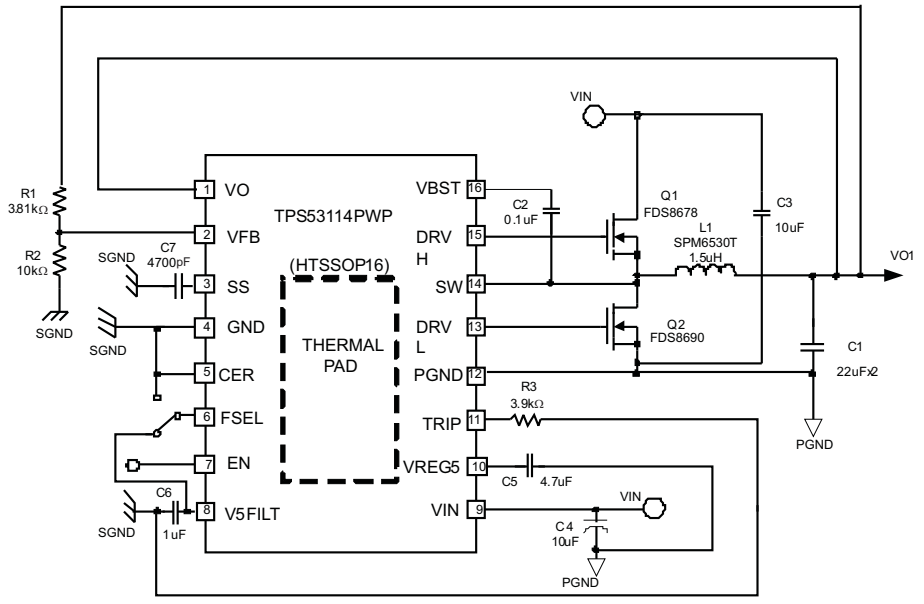



**Figure 13. Typical Application Circuit at 700-kHz Switching Frequency Selection (FSEL pin = V5FILT)**

## TYPICAL APPLICATION PERFORMANCE

Typical application performance below was taken from specific application circuits Figure 12 and Figure 13.

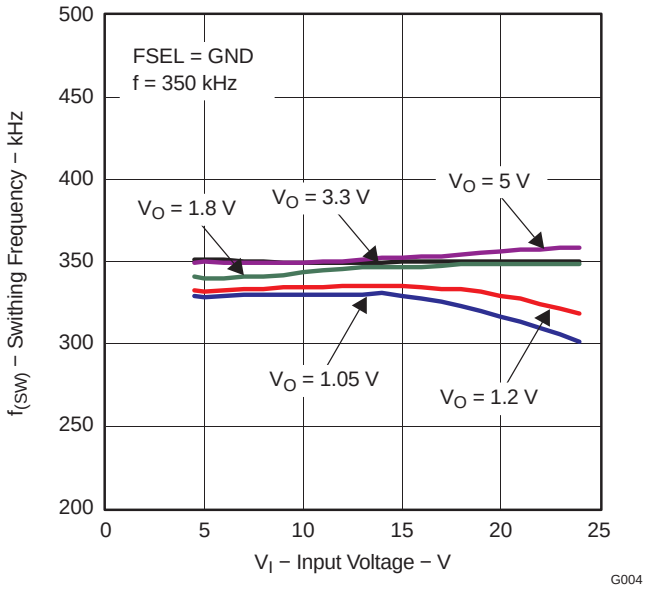



**Figure 14. SWITCHING FREQUENCY ($I_O$ = 1 A) vs. INPUT VOLTAGE**

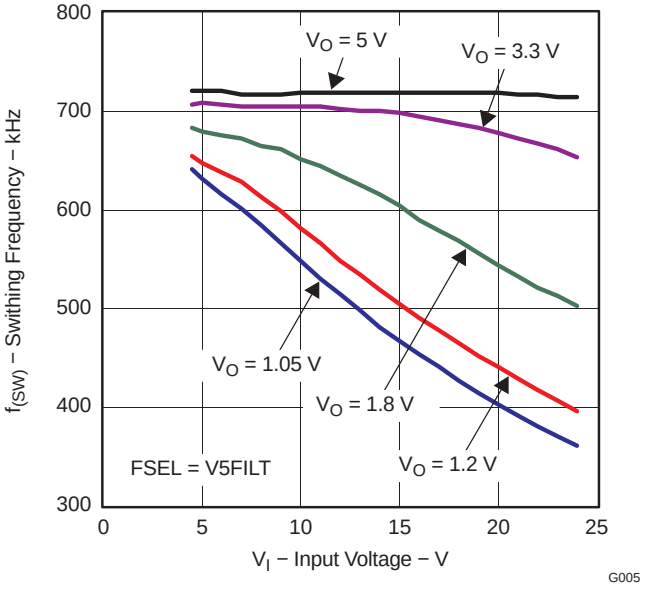



**Figure 15. SWITCHING FREQUENCY vs. INPUT VOLTAGE**

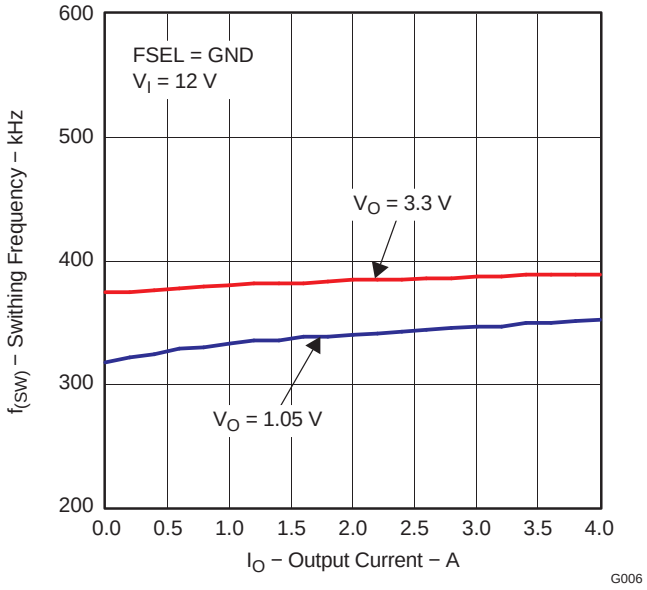



**Figure 16. SWITCHING FREQUENCY vs. OUTPUT CURRENT**

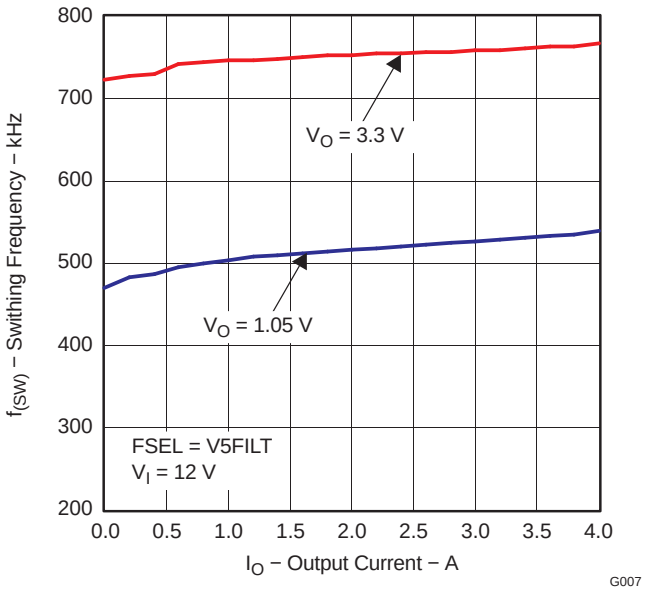



**Figure 17. SWITCHING FREQUENCY vs. OUTPUT CURRENT**

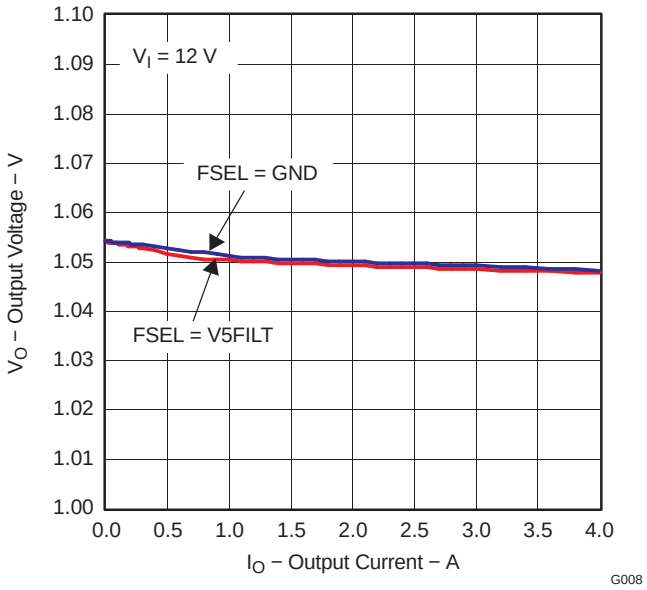



**Figure 18. 1.05-V OUTPUT VOLTAGE vs. OUTPUT CURRENT**

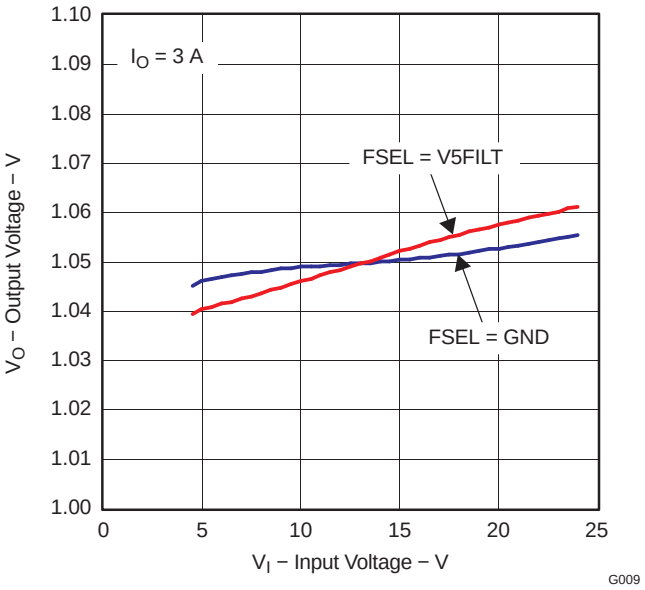



**Figure 19. 1.05-V OUTPUT VOLTAGE vs. INPUT VOLTAGE**

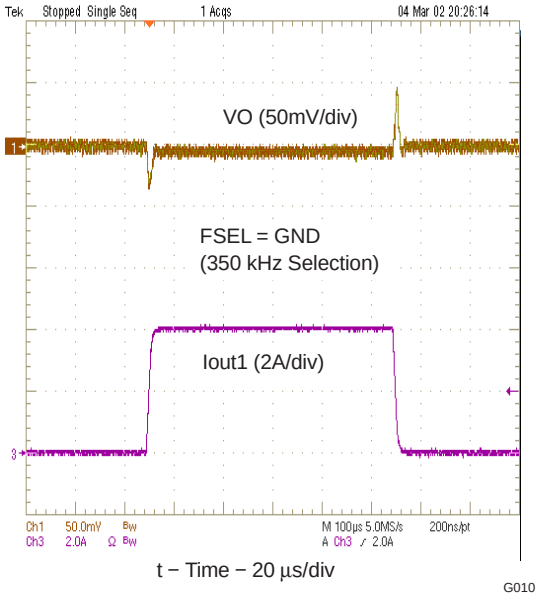



**Figure 20. 1.05-V LOAD TRANSIENT RESPONSE**

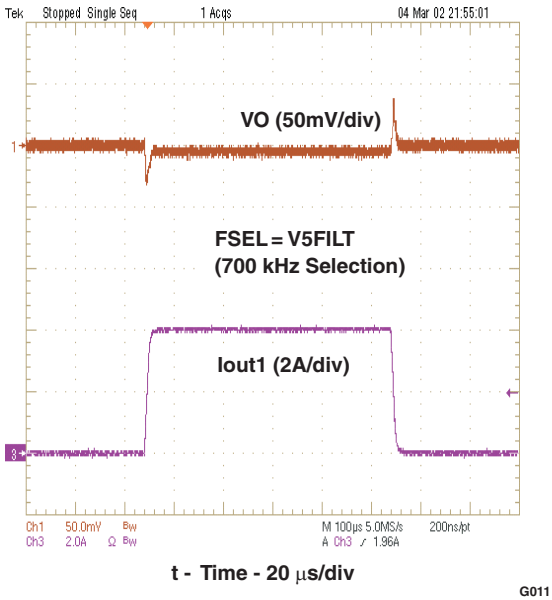



**Figure 21. 1.05-V LOAD TRANSIENT RESPONSE**

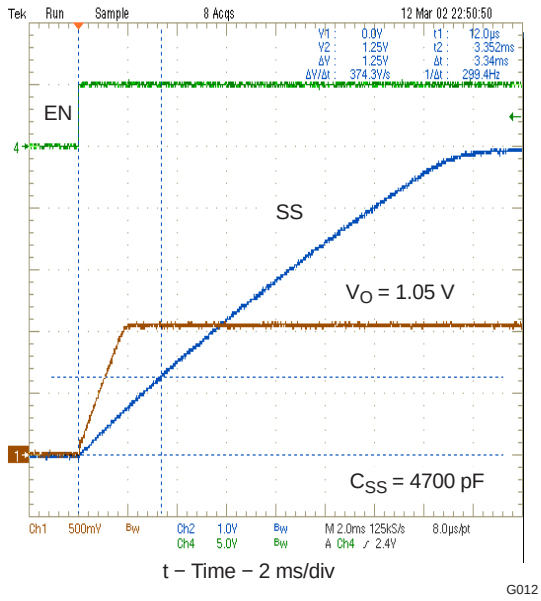



**Figure 22. STARTUP WAVEFORM**

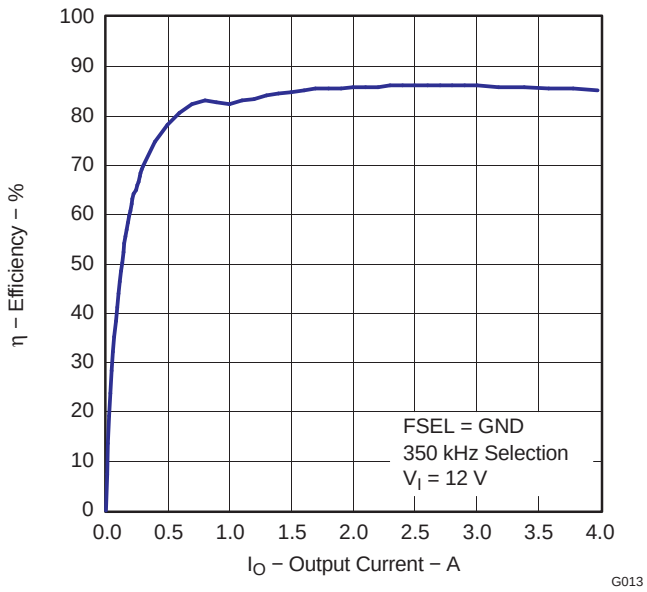



**Figure 23. 1.05-V EFFICIENCY vs. OUTPUT CURRENT**

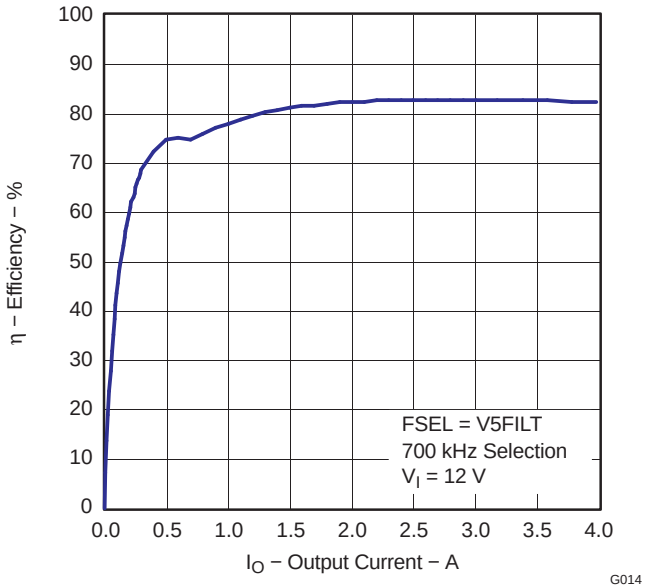



**Figure 24. 1.05-V EFFICIENCY vs. OUTPUT CURRENT**

## COMPONENT SELECTION

### CHOOSE INDUCTOR

The inductance value is selected to provide approximately 30% peak to peak ripple current at maximum load. Larger ripple current increases output ripple voltage, improve S/N ratio and contribute to stable operation. L1 can be calculated using Equation 3.

$$L1 = \frac{(V_{IN(max)} - V_O1)}{I_{L1(ripple)} \bullet f_{SW}} \bullet \frac{V_O1}{V_{IN(max)}} = \frac{3 \bullet (V_{IN(max)} - V_O1)}{I_O1 \bullet f_{SW}} \bullet \frac{V_O1}{V_{IN(max)}} \quad (3)$$

The inductors current ratings needs to support both the RMS (thermal) current and the peak (saturation) current. The RMS and peak inductor current can be estimated as follows:

$$I_{L1(ripple)} = \frac{V_{IN(max)} - V_O1}{L1 \bullet f_{SW}} \bullet \frac{V_O1}{V_{IN(max)}} \quad (4)$$

$$I_{L1(peak)} = \frac{V_{TRIP}}{R_{DS(ON)}} + I_{L1(ripple)} \quad (5)$$

$$I_{L1(RMS)} = \sqrt{I_O1^2 + \tfrac{1}{12}(I_{L1(ripple)})^2} \quad (6)$$

Note:

The calculation above shall serve as a general reference. To further improve transient response, the output inductance could be reduced further. This needs to be considered along with the selection of the output capacitor.

### CHOOSE OUTPUT CAPACITOR

The capacitor value and ESR determines the amount of output voltage ripple and load transient response. Recommend to use ceramic output capacitor.

$$C1 = \frac{\Delta I_{load}^{\ 2} \bullet L1}{2 \bullet V_O1 \bullet \Delta V_{OS}} \quad (7)$$

$$C1 = \frac{\Delta I_{load}^{\ 2} \bullet L1}{2 \bullet K \bullet \Delta V_{US}} \quad (8)$$

Where:

$$K = (V_{IN} - V_O1) \bullet \frac{T_{on}1}{T_{ON}1 + T_{min(off)}} \quad (9)$$

$$C1 = \frac{I_{L1(ripple)}}{8 \bullet V_O1_{(ripple)}} \bullet \frac{1}{f_{SW}} \quad (10)$$

Select the capacitance value greater than the largest value calculated from Equation 7, Equation 8 and Equation 10. The capacitance for C1 should be greater than 66 µF.

Where:

- $\Delta V_{OS}$ = The allowable amount of overshoot voltage in load transition
- $\Delta V_{US}$ = The allowable amount of undershoot voltage in load transition
- $T_{min(off)}$ = Minimum off time

### CHOOSE INPUT CAPACITOR

The TPS53114 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A minimum 10-µF high-quality ceramic capacitor is recommended for the input capacitor. The capacitor voltage rating needs to be greater than the maximum input voltage.

### CHOOSE BOOTSTRAP CAPACITOR

The TPS53114 requires a bootstrap capacitor from SW to VBST to provide the floating supply for the high-side drivers. A minimum 0.1-μF high-quality ceramic capacitor is recommended. The voltage rating should be greater than 10.0 V.

### CHOOSE VREG5 AND V5FILT CAPACITOR

The TPS53114 requires both the VREG5 regulator and V5FILT input are bypassed. A minimum 4.7-μF high-quality ceramic capacitor must be connected between the VREG5 and GND for proper operation. A minimum 1.0-μF high-quality ceramic capacitor must be connected between the V5FILT and GND for proper operation. Both of these capacitors' voltage ratings should be greater than 10 V.

### CHOOSE OUTPUT VOLTAGE RESISTORS

The output voltage is set with a resistor divider from output voltage node to the VFBx pin. It is recommended to use 1% tolerance or better resistors. Select R2 between 10 kΩ and 100 kΩ and use Equation 11 or Equation 12 to calculate R1.

$$R1 = \left( \frac{V_O1}{0.765 + \frac{VFB1_{(ripple)}}{2}} - 1 \right) \bullet R2 \qquad (\text{FSEL} = \text{GND}) \tag{11}$$

$$R1 = \left( \frac{V_O1}{0.758 + \frac{VFB1_{(ripple)}}{2}} - 1 \right) \bullet R2 \qquad (\text{FSEL} = \text{V5FILT}) \tag{12}$$

Where:

$VFB1_{(ripple)}$ = Ripple voltage at VFB1

### CHOOSE RESISTOR SETTING FOR OVER CURRENT LIMIT

$$V_{TRIP} = \left( I_{OCL} - \frac{(V_{IN} - V_O)}{2 \bullet L1 \bullet f_{sw}} \bullet \frac{V_O}{V_{IN}} \right) \bullet R_{DS(ON)} \tag{13}$$

$$R_{TRIP}\ (k\Omega) = \frac{V_{TRIP}\ (mV) - V_{OCLoff}}{I_{TRIP}\ (\mu A)} \tag{14}$$

Where:

- $R_{DS(ON)}$ = Low side FET on-resistance
- $I_{TRIP}$ = TRIP pin source current ( ≒ 10 μA )
- $V_{OCLoff}$ = Minimum over current limit offset voltage (-20 mV)
- $I_{OCL}$ = over current limit

### CHOOSE SOFT START CAPACITOR

Soft start timing equations are as follows:

$$T_{SS} = \frac{C_7 \bullet 0.765}{2e^{-6}}(s) \qquad (\text{FSEL} = \text{GND}) \tag{15}$$

$$T_{SS} = \frac{C_7 \bullet 0.758}{2e^{-6}}(s) \qquad (\text{FSEL} = \text{V5FILT}) \tag{16}$$

### CHOOSE PACKAGE OPTION

TPS53114 power dissipation:

$$P_d = f_{SW} \bullet (CiH + CiL) \bullet VREG5 \bullet V_{in(max)} \tag{17}$$

Where:

- $C_{iH}$ = Input capacitor of high side MOSFET
- $C_{iL}$ = Input capacitor of low side MOSFET

Choose package considering the Dissipation Rating table.

## LAYOUT SUGGESTIONS

- Keep the input switching current loop as small as possible.
- Place the input capacitor (C3, C6) close to the top switching FET. The output current loop should also be kept as small as possible.
- Keep the SW node as physically small and short as possible as to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin (VFB) of the device.
- Keep analog and non-switching components away from switching components.
- Make a single point connection from the signal ground to power ground.
- Do not allow switching current to flow under the device.

## REVISION HISTORY

| Changes from Original (April 2009) to Revision A | Page |
|---|---|
| • Updated the list of Features | 1 |

| Changes from Revision A (August 2009) to Revision B | Page |
|---|---|
| • Changed Equation 13 From: $I_{OCL}$ + To: $I_{OCL}$ - | 17 |
| • Updated Equation 14 by adding minus $V_{OCLoff}$ | 17 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| TPS53114PW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS53114PWP | ACTIVE | HTSSOP | PWP | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | Purchase Samples |
| TPS53114PWPR | ACTIVE | HTSSOP | PWP | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | Request Free Samples |
| TPS53114PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |

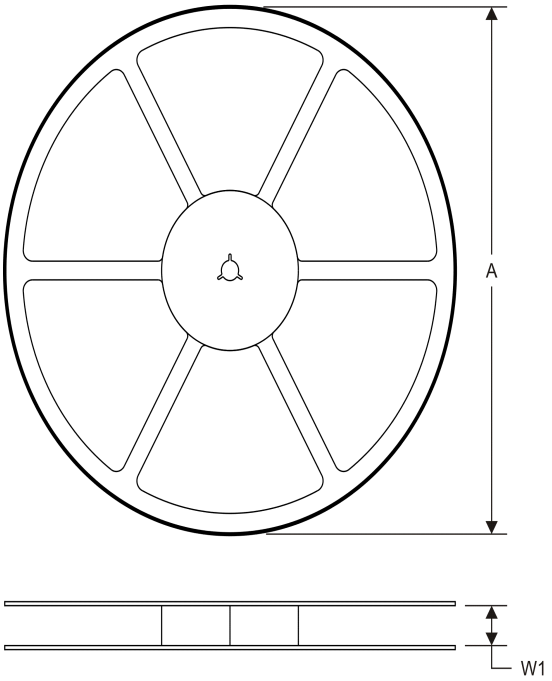
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

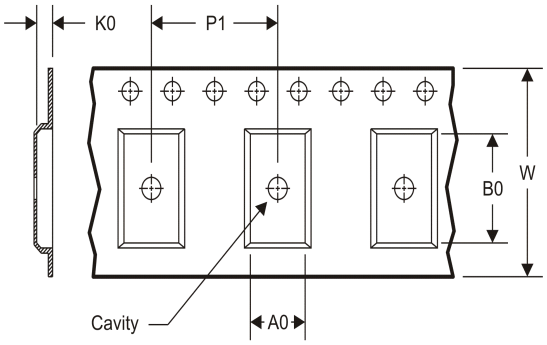
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



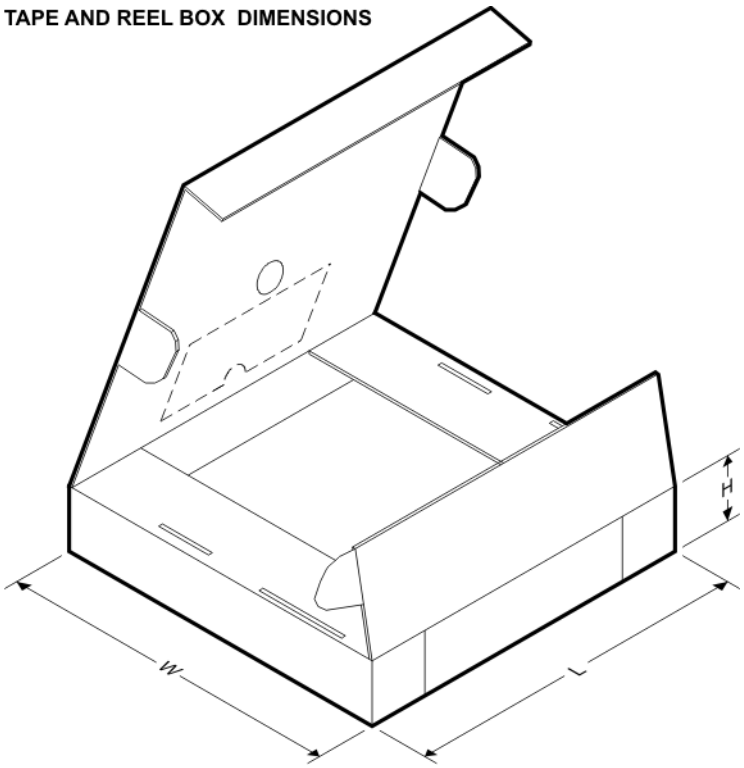

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS53114PWPR | HTSSOP | PWP | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TPS53114PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

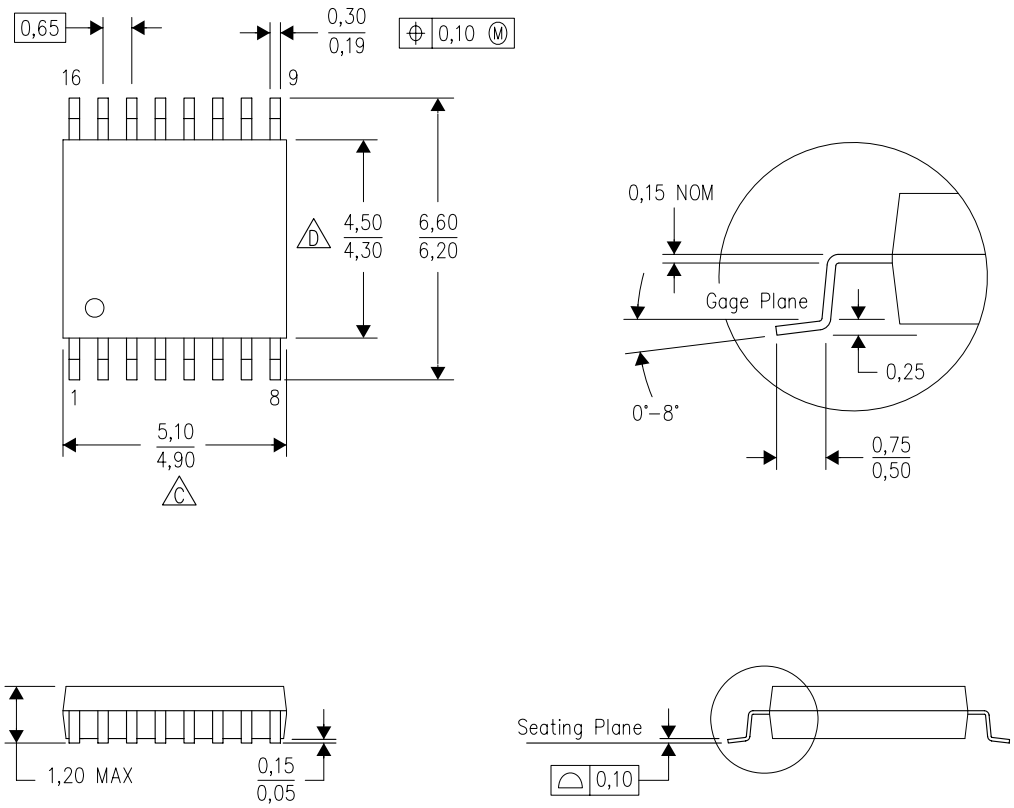
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS53114PWPR | HTSSOP | PWP | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| TPS53114PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |

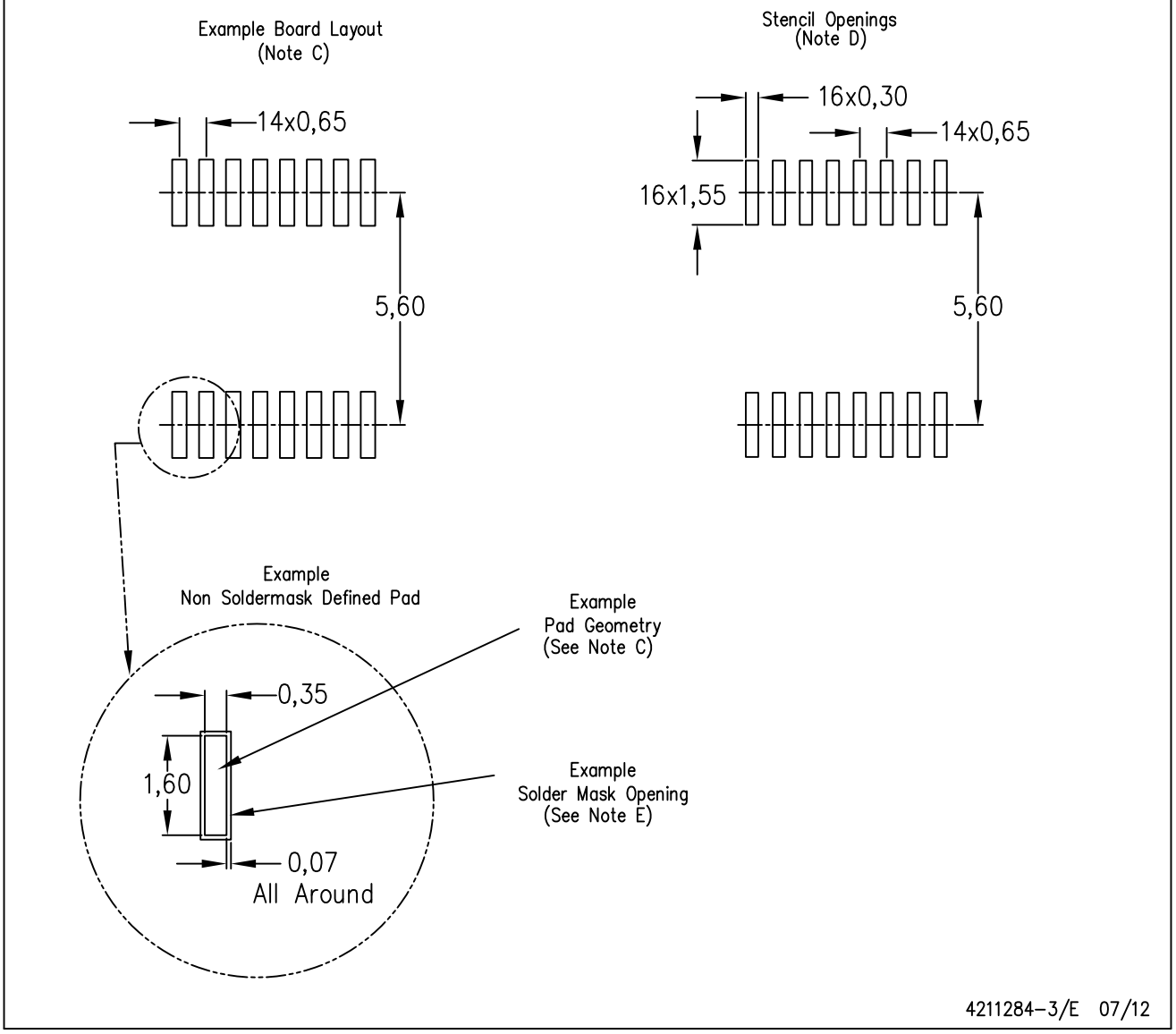
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE




4040064–4/G 02/11

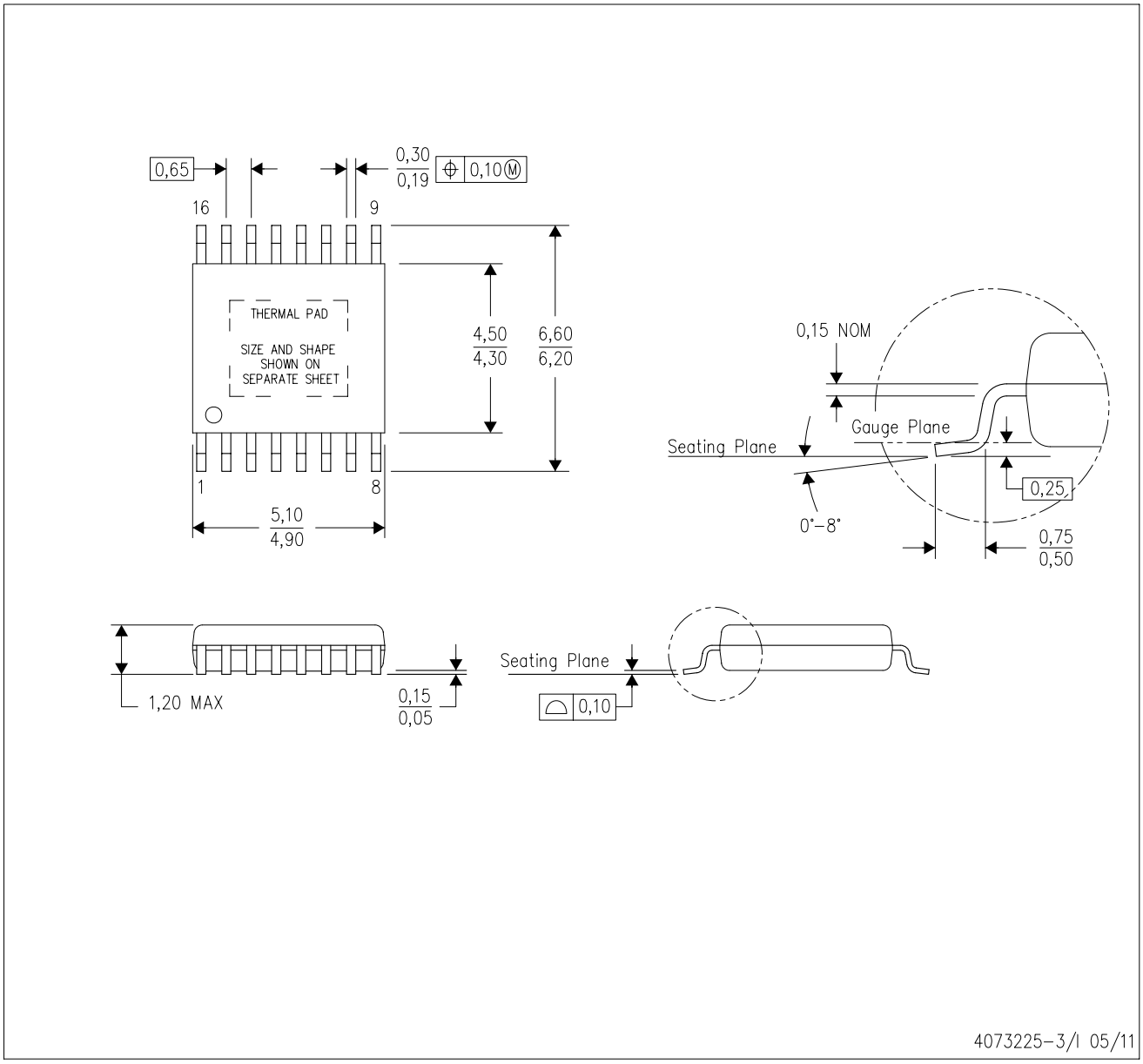
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

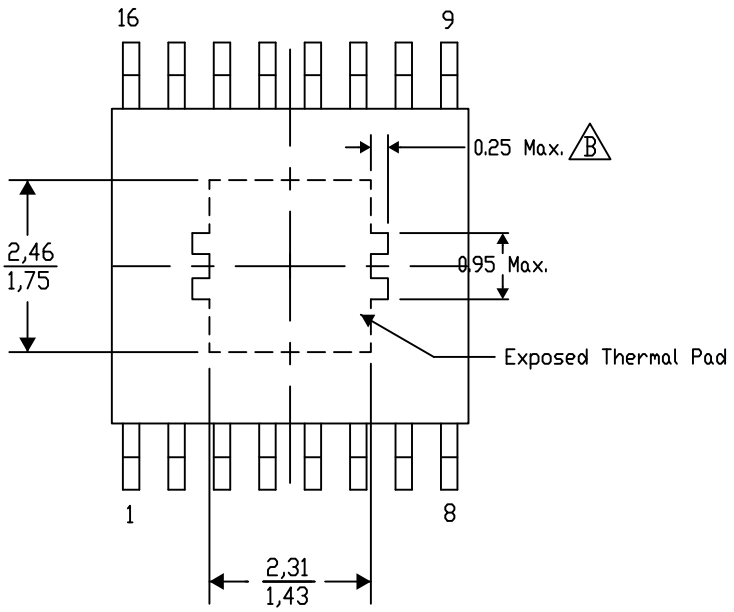
PWP (R–PDSO–G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

Exposed Thermal Pad Dimensions

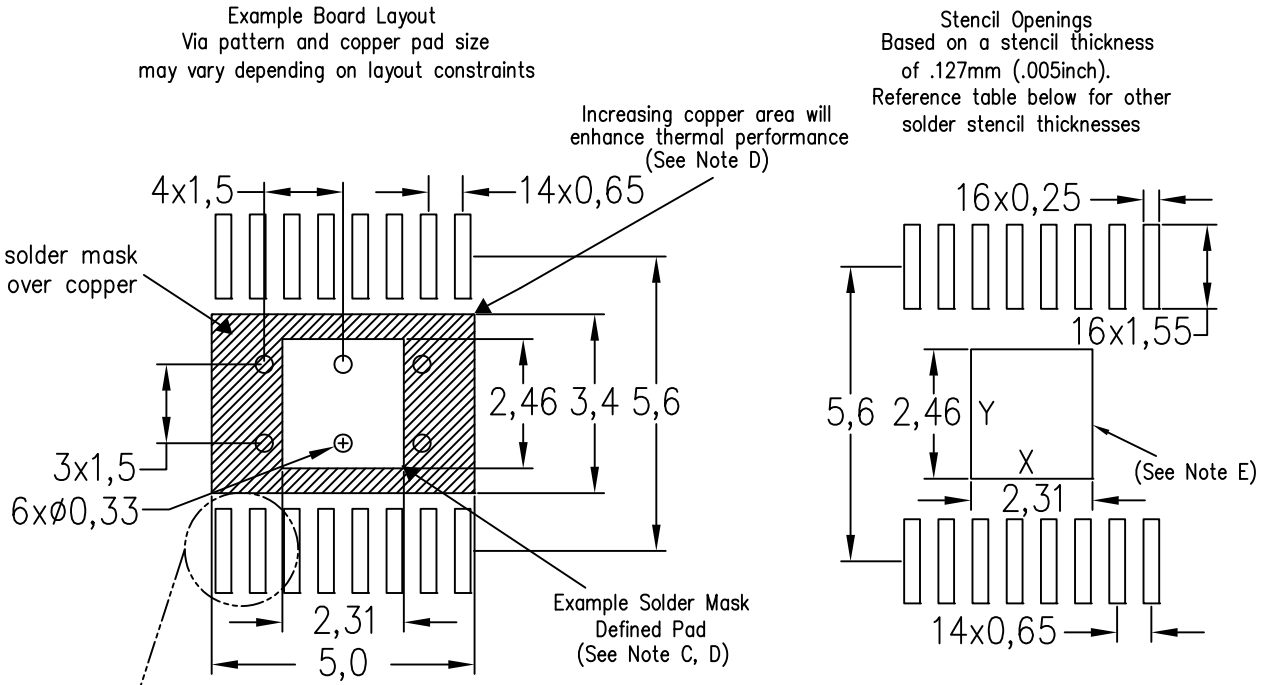
4206332–6/AC 07/12

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

## PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 2.5 | 2.65 |
| 0.127mm | 2.31 | 2.46 |
| 0.152mm | 2.15 | 2.3 |
| 0.178mm | 2.05 | 2.15 |

4207609–3/R 07/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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