

Low-Power, Dual-Voltage Detector in Small μ SON Package

Check for Samples: [TPS3779](#), [TPS3780](#)

FEATURES

- **Very Small Package:** 1.45-mm \times 1-mm SON
- **Low Quiescent Current:** 1.8 μ A (typ)
- **High Threshold and Hysteresis Accuracy:** 1.0%
- **Different Hysteresis Options:**
 - 0.5%, 1%, 5%, and 10%
- **Temperature Range:** -40°C to $+125^{\circ}\text{C}$
- **Push-Pull (TPS3779) and Open-Drain (TPS3780) Output Options**

APPLICATIONS

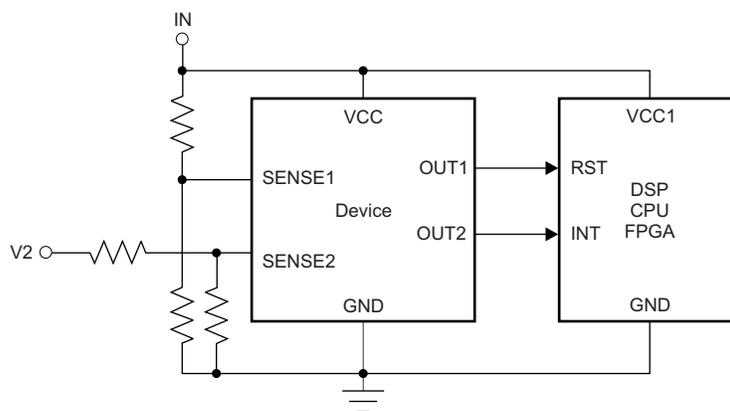
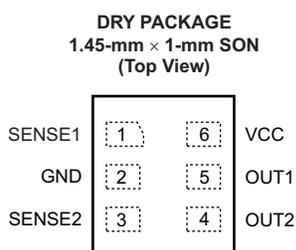
- **DSPs, Microcontrollers, or Microprocessors Applications**
- **Portable and Battery-Powered Products**
- **Cell Phones and PDAs**
- **Notebook and Desktop Computers**
- **Set-Top Boxes**

DESCRIPTION

The TPS3779 and TPS3780 are a family of two-channel voltage detectors with low-power and high-accuracy comparators, and are available in a very small μ SON package. The SENSE1 and SENSE2 monitor inputs include a built-in hysteresis for filtering to reject brief glitches, thereby ensuring stable output operation without false triggering. The family offers different factory-set hysteresis options of 0.5%, 1%, 5%, or 10%.

The TPS3779 and TPS3780 have adjustable SENSE inputs that can be configured by an external resistor divider. When the voltage at the SENSE input goes below the falling threshold, OUT is driven low. When SENSE rises above the rising threshold, OUT goes high.

The devices have a very low quiescent current of 1.8 μ A (typical) and provide a precise, space-conscious solution for voltage detection suitable for low-power, system-monitoring and portable applications.


PRODUCT PREVIEW


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PRODUCT	HYSTERESIS (%)	OUTPUT
TPS3779ADRYR	0.5	Push-pull
TPS3779ADRYT	0.5	Push-pull
TPS3779BDRYR	5	Push-pull
TPS3779BDRYT	5	Push-pull
TPS3779CDRYR	10	Push-pull
TPS3779CDRYT	10	Push-pull
TPS3779DDRYR	1	Push-pull
TPS3779DDRYT	1	Push-pull
TPS3780ADRYR	0.5	Open-drain
TPS3780ADRYT	0.5	Open-drain
TPS3780BDRYR	5	Open-drain
TPS3780BDRYT	5	Open-drain
TPS3780CDRYR	10	Open-drain
TPS3780CDRYT	10	Open-drain
TPS3780DDRYR	1	Open-drain
TPS3780DDRYT	1	Open-drain

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT ⁽²⁾
Voltage	VCC	-0.3 to +7	V
	OUT1, OUT2	-0.3 to +7	V
	SENSE1, SENSE2	-0.3 to +7	V
Current	OUT pin	±20	mA
Temperature ⁽³⁾	Operating junction, T _J	-40 to +125	°C
	Storage, T _{stg}	-65 to +150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM)	2	kV
	Charge device model (CDM)	500	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute maximum- rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to the network ground terminal.

(3) As a result of the low dissipated power in this device, it is assumed that T_J = T_A.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		TPS3779, TPS3780	UNITS
		DRY (μSON)	
		6 PINS	
θ _{JA}	Junction-to-ambient thermal resistance	TBD	°C/W
θ _{JCtop}	Junction-to-case (top) thermal resistance	TBD	
θ _{JB}	Junction-to-board thermal resistance	TBD	
ψ _{JT}	Junction-to-top characterization parameter	TBD	
ψ _{JB}	Junction-to-board characterization parameter	TBD	
θ _{JCbot}	Junction-to-case (bottom) thermal resistance	TBD	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

ELECTRICAL CHARACTERISTICS

All specifications are over the operating temperature range of $-40^{\circ}\text{C} < T_J < +125^{\circ}\text{C}$ and $1.5\text{ V} \leq V_{CC} \leq 6.5\text{ V}$, unless otherwise noted. Typical values are at $T_J = +25^{\circ}\text{C}$ and $V_{CC} = 3.3\text{ V}$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT			
V _{CC}	Input supply range	T _J = -40°C to $+125^{\circ}\text{C}$			1.5	6.5	V	
V _(POR)	Power-on reset voltage ⁽¹⁾	V _{OL} (max) = 0.2 V, I _{OL} = 15 μA				0.8	V	
I _{CC}	Supply current (into VCC pin)	V _{CC} = 3.3 V, no load, $-40^{\circ}\text{C} < T_J < +85^{\circ}\text{C}$				1.8	3.3	μA
		V _{CC} = 3.3 V, no load, $-40^{\circ}\text{C} < T_J < +125^{\circ}\text{C}$					4.5	μA
		V _{CC} = 6.5 V, no load, $-40^{\circ}\text{C} < T_J < +85^{\circ}\text{C}$				2	3.5	μA
		V _{CC} = 6.5 V, no load, $-40^{\circ}\text{C} < T_J < +125^{\circ}\text{C}$					5	μA
V _{IT+}	Positive-going input threshold voltage	V _(SENSE) rising			1.208	1.220	1.232	V
V _{IT-}	Negative-going input threshold voltage	TPS37xxA (0.5% hysteresis)			1.202	1.2139	1.226	V
		TPS37xxB (5% hysteresis)			1.147	1.159	1.170	V
		TPS37xxC (10% hysteresis)			1.087	1.098	1.109	V
		TPS37xxD (1% hysteresis)			1.196	1.208	1.220	V
I _(SENSE)	Input current ⁽²⁾	V _(SENSE) = 0 V or V _{CC}			-5		5	nA
V _{OL}	Low-level output voltage	V _{CC} ≥ 1.2 V, I _{SINK} = 0.4 mA					0.25	V
		V _{CC} ≥ 2.7 V, I _{SINK} = 2 mA					0.25	V
		V _{CC} ≥ 4.5 V, I _{SINK} = 3.2 mA					0.3	V
V _{OH}	High-level output voltage (push-pull)	V _{CC} ≥ 1.7 V, I _{SINK} = 0.4 mA			0.8 V _{CC}			V
		V _{CC} ≥ 2.7 V, I _{SINK} = 1 mA			0.8 V _{CC}			V
		V _{CC} ≥ 4.5 V, I _{SINK} = 2.5 mA			0.8 V _{CC}			V
I _{LKG(OD)}	Open-drain output leakage current	High impedance, V _(SENSE_OUT) = 6.5 V, $-40^{\circ}\text{C} < T_J < +85^{\circ}\text{C}$			-50		50	nA
		High impedance, V _(SENSE_OUT) = 6.5 V, $-40^{\circ}\text{C} < T_J < +125^{\circ}\text{C}$			-250		250	nA
t _{PD(r)}	SENSE (rising) to OUT propagation delay					10		μs
t _{PD(f)}	SENSE (falling) to OUT propagation delay	100-mV overdrive				6		μs
	Startup delay ⁽³⁾⁽²⁾					350		μs

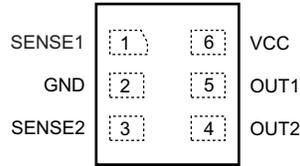
(1) The lowest supply voltage (V_{CC}) at which the output is active (t_{rise(V_{CC})} > 15 μs/V). Below V_(POR), the output cannot be determined.

(2) Specified by design.

(3) During power-up, V_{CC} must exceed 1.5 V for the start-up delay time before the output is in the correct state.

PIN CONFIGURATION

DRY PACKAGE
1.45-mm × 1-mm SON
(Top View)



PIN DESCRIPTIONS

PIN		DESCRIPTION
NAME	NO.	
GND	2	Ground
OUT2	4	OUT2 is the output for SENSE2. OUT2 is asserted (driven low) when the voltage at SENSE2 falls below V_{IT-} . OUT2 is deasserted (goes high) after SENSE2 is greater than V_{IT+} . OUT2 is a push-pull output for the TPS3779 and an open-drain output for the TPS3780. The open-drain device (TPS3780) can be pulled up to 6.5 V independent of VCC; a pull-up resistor is required for this device.
OUT1	5	OUT1 is the output for SENSE1. OUT1 is asserted (driven low) when the voltage at SENSE1 falls below V_{IT-} . OUT1 is deasserted (goes high) after SENSE1 is greater than V_{IT+} . OUT1 is a push-pull output for the TPS3779 and an open-drain output for the TPS3780. The open-drain device (TPS3780) can be pulled up to 6.5 V independent of VCC; a pull-up resistor is required for this device.
SENSE1	1	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal drops below the threshold voltage (V_{IT-}), OUT1 is asserted.
SENSE2	3	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal drops below the threshold voltage (V_{IT-}), OUT2 is asserted.
VCC	6	Supply voltage input. Connect a 1.7-V to 6.5-V supply to VCC to power the device. It is good analog design practice to place a 0.1- μ F ceramic capacitor close to this pin.

FUNCTIONAL BLOCK DIAGRAM

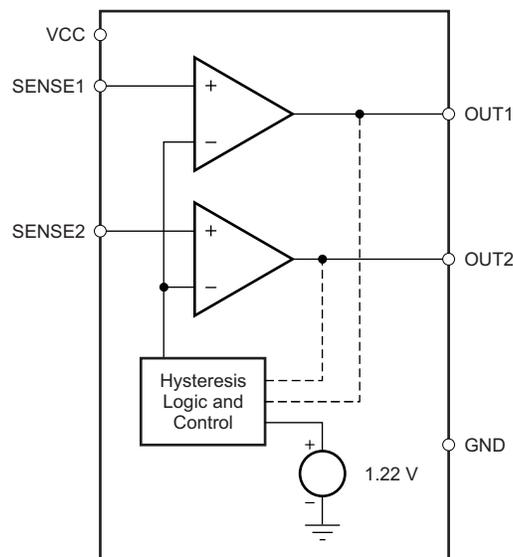


Figure 1. Block Diagram

APPLICATION INFORMATION

INPUTS (SENSE1, SENSE2)

The TPS3779 and TPS3780 have two comparators for voltage detection. Each comparator has one external input; the other input is connected to the internal reference. The comparator rising threshold is designed and trimmed to be equal to V_{IT+} and the falling threshold is trimmed to be equal to V_{IT-} . The built-in falling hysteresis options makes the devices immune to supply rail noise and ensures stable operation.

The comparator inputs can swing from ground to 6.5 V, regardless of the device supply voltage used. Although not required in most cases, it is good analog design practice to place a 1-nF to 10-nF bypass capacitor at the comparator input for extremely noisy applications in order to reduce sensitivity to transients and layout parasitic.

For each SENSE input, the corresponding output (OUT) is driven to logic low when the input voltage drops below V_{IT-} . When the voltage exceeds V_{IT+} , the output (OUT) goes to a high-impedance state; see [Figure 3](#).

OUTPUTS (OUT1, OUT2)

In a typical device application, the outputs are connected to a reset or enable input of the processor [such as a digital signal processor (DSP), central processing unit (CPU), field-programmable gate array (FPGA), or application-specific integrated circuit (ASIC)], or the outputs are connected to the enable input of a voltage regulator [such as a dc-dc or low-dropout regulator (LDO)].

The TPS3779 provides two push-pull outputs. The logic high level of the outputs is determined by the VCC pin voltage. With this configuration, pull-up resistors are not required and some board area can be saved. However, all interface logic levels should be examined. All OUT connections must be compatible with the VCC pin logic level.

The TPS3780 provides two open-drain outputs (OUT1 and OUT2); pull-up resistors must be used to hold these lines high when the output goes to a high impedance condition (not asserted). By connecting pull-up resistors to the proper voltage rails, the outputs can be connected to other devices at correct interface voltage levels. The outputs can be pulled up to 6.5 V, independent of the device supply voltage. To ensure proper voltage levels, some thought should be given while choosing the pull-up resistor values. The pull-up resistor value is determined by V_{OL} , sink current capability, and output leakage current ($I_{IKG(OD)}$). These values are specified in the [Electrical Characteristics](#) table. By using wired-AND logic, OUT1 and OUT2 can be merged into one logic signal. The [Inputs \(SENSE1, SENSE2\)](#) section describes how the outputs are asserted or de-asserted. Refer to [Figure 3](#) for a description of the relationship between threshold voltages and the respective output.

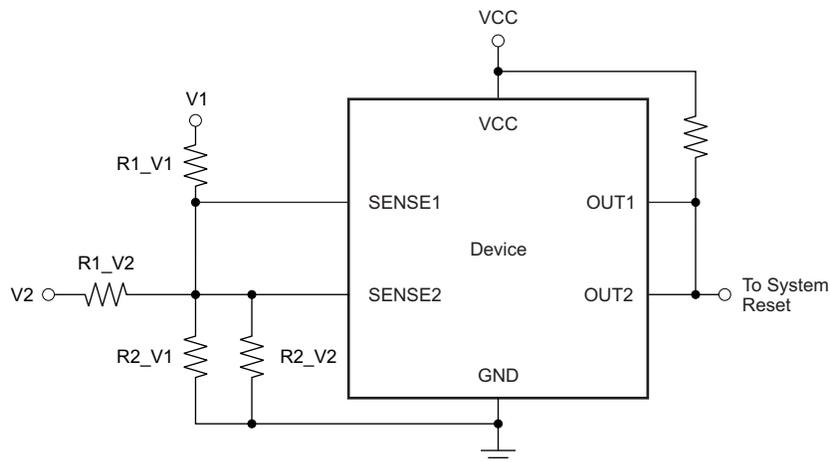


Figure 2. Application Diagram

Equation 1 and Equation 2 determine $V_{MON(noUV)}$ and $V_{MON(UV)}$, respectively.

$$V_{MON(noUV)} = \left[1 + \frac{R1}{R2} \right] \times V_{IT+} \tag{1}$$

$$V_{MON(UV)} = \left[1 + \frac{R1}{R2} \right] \times V_{IT-} \tag{2}$$

Where:

R1 and R2 are the resistor values for the resistor divider on the SENSE pins,

$V_{MON(noUV)}$ is the target voltage at which an undervoltage condition is removed when V_{MON} rises, and

$V_{MON(UV)}$ is the target voltage at which an undervoltage condition is detected.

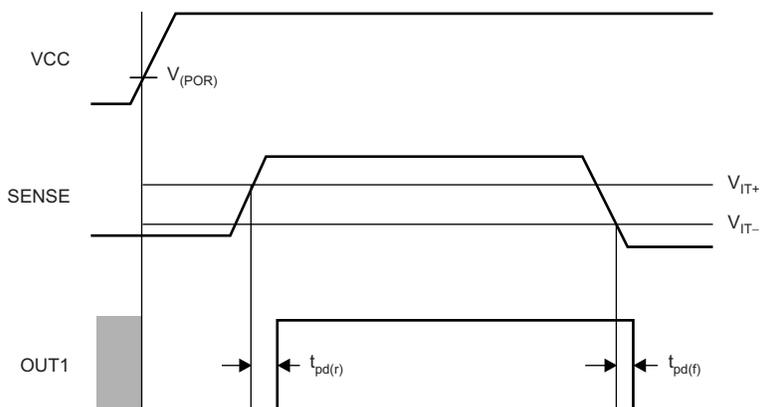


Figure 3. Timing Diagram

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS3779ADRYR	PREVIEW	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZQ	
TPS3779ADRYT	PREVIEW	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZQ	
TPS3779BDRYR	PREVIEW	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZR	
TPS3779BDRYT	PREVIEW	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZR	
TPS3779CDRYR	PREVIEW	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125		
TPS3779CDRYT	PREVIEW	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125		
TPS3779DDRYR	PREVIEW	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125		
TPS3779DDRYT	PREVIEW	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125		
TPS3780ADRYR	PREVIEW	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZU	
TPS3780ADRYT	PREVIEW	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZU	
TPS3780BDRYR	PREVIEW	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZV	
TPS3780BDRYT	PREVIEW	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZV	
TPS3780CDRYR	PREVIEW	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125		
TPS3780CDRYT	PREVIEW	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125		
TPS3780DDRYR	PREVIEW	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125		
TPS3780DDRYT	PREVIEW	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

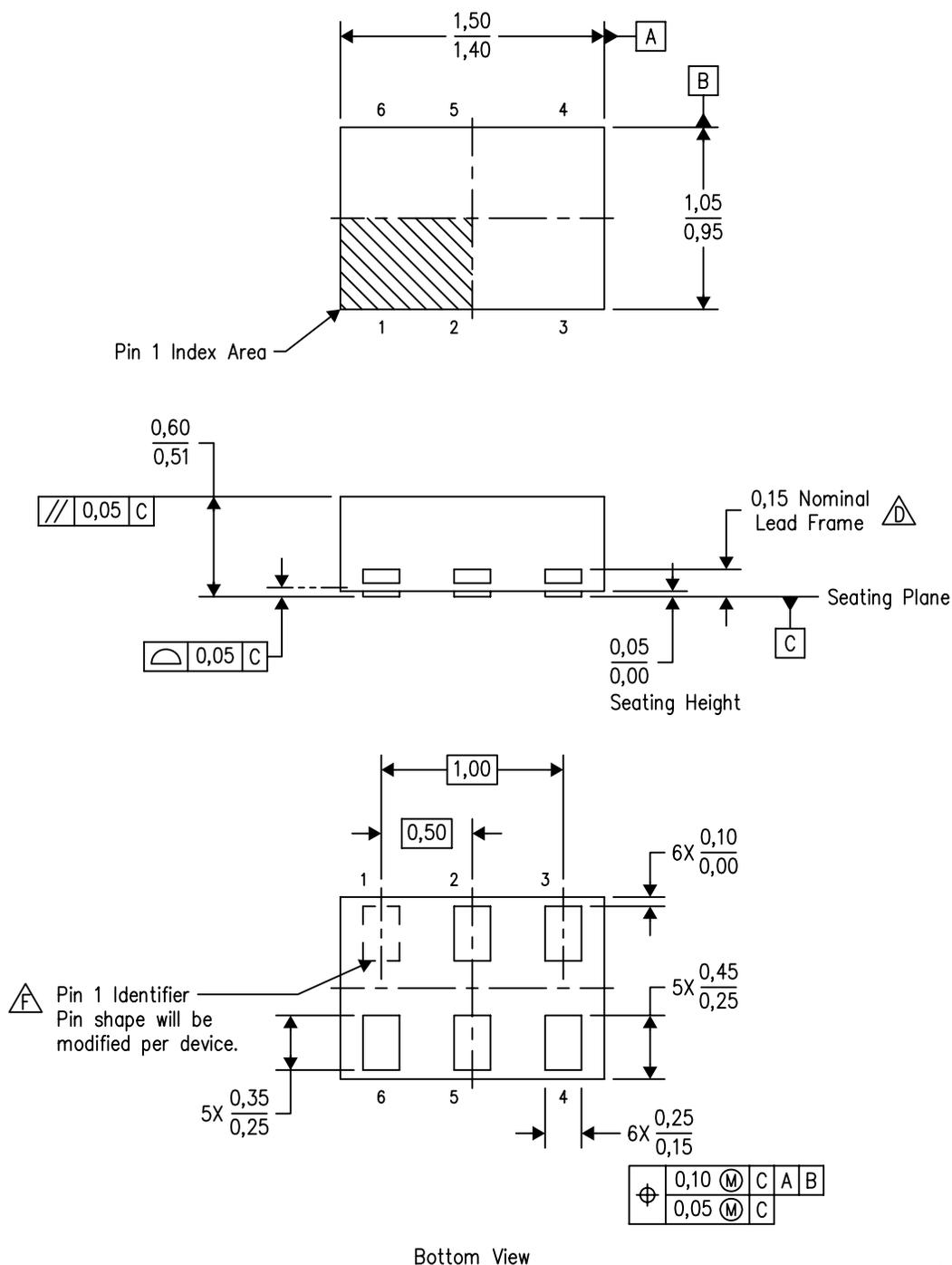
⁽⁴⁾ Only one of markings shown within the brackets will appear on the physical device.

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DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4207181/F 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 - $\triangle D$ The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
 - E. This package complies to JEDEC MO-287 variation UFAD.
 - $\triangle F$ See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

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