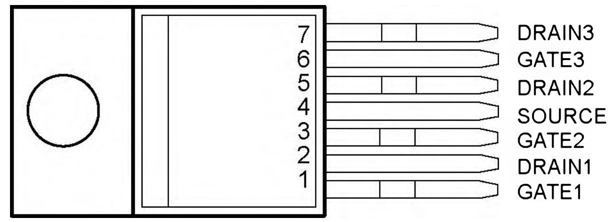
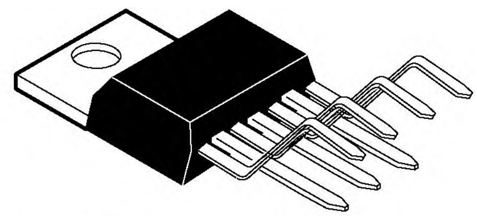
SLIS018 – SEPTEMBER 1992

- **Three 7.5-A Independent Output Channels, Continuous Current Per Channel**
- **Low $r_{DS(on)}$ . . . 0.09 Ω Typical**
- **Output Voltage . . . 60 V**
- **Pulsed Current . . . 15 A Per Channel**
- **Avalanche Energy . . . 120 mJ**

KV PACKAGE
(TOP VIEW)



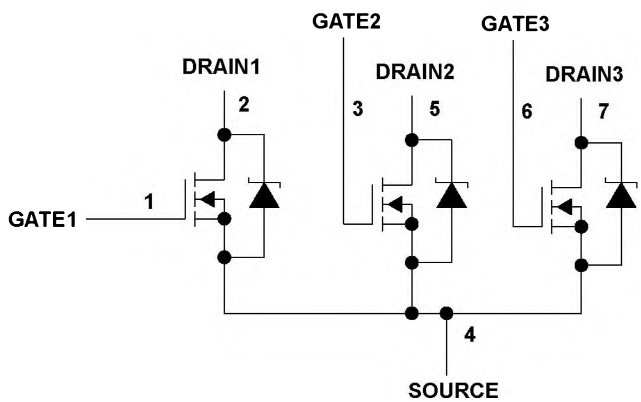


The tab is electrically connected to SOURCE.

description

The TPIC2301 is a monolithic power DMOS array that consists of three independent N-channel enhancement-mode DMOS transistors connected in a common-source configuration with open drains.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)

Drain-source voltage, V_{DS}	60 V
Gate-source voltage, V_{GS}	±20 V
Continuous source-drain diode current	7.5 A
Pulsed drain current, each output, all outputs on, I_D (see Note 1)	15 A
Continuous drain current, each output, all outputs on	7.5 A
Single-pulse avalanche energy, E_{AS} (see Figure 4)	120 mJ
Continuous power dissipation at (or below) T_A = 25°C (see Note 2)	2 W
Continuous power dissipation at (or below) T_C = 75°C, all outputs on (see Note 2)	50 W
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range, T_{stg}	–40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Pulse duration = 10 ms, duty cycle = 6%
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16 mW/°C. For operation above 75°C case temperature, and with all outputs conducting, derate linearly at the rate of 0.66 W/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TEXAS INSTRUMENTS

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electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DS}$	Drain-source breakdown voltage	I_D = 1 µA, V_{GS} = 0		60			V
V_{TGS}	Gate-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}		1.2	1.75	2.4	V
$V_{DS(on)}$	Drain-source on-state voltage	I_D = 7.5 A, V_{GS} = 15 V, See Notes 3 and 4			0.68	0.94	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.07	1	µA
			T_C = 125°C		1.3	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 20 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{GS} = –20 V, V_{DS} = 0			10	100	nA
$r_{DS(on)}$	Static drain-source on-state resistance	V_{GS} = 15 V, I_D = 7.5 A, See Notes 3 and 4 and Figures 5 and 6	T_C = 25°C		0.09	0.125	Ω
			T_C = 125°C		0.15	0.21	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 5 A, See Notes 3 and 4		3.3	4.7		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 300 kHz			490		pF
C_{oss}	Short-circuit output capacitance, common source				285		
C_{rss}	Short-circuit reverse transfer capacitance, common source				90		

NOTES: 3. Technique should limit T_J – T_C to 10°C maximum.
4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SD}	Forward on voltage	I_S = 7.5 A, V_{GS} = 0, di/dt = 100 A/µs, V_{DS} = 48 V, See Figure 1		0.8	1.3	V
t_{rr}	Reverse recovery time			200		ns
Q_{RR}	Total source-drain diode charge			1.5		µC

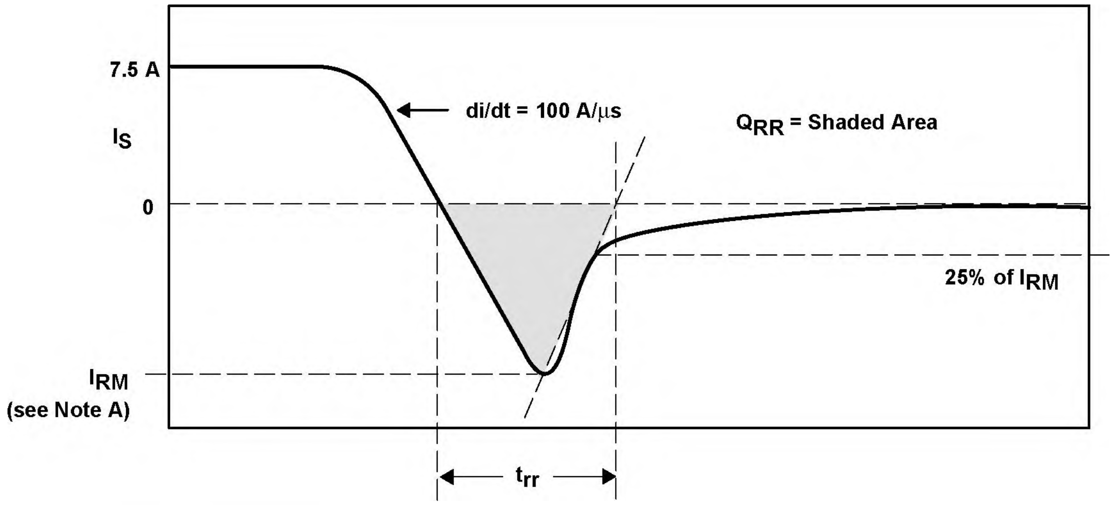
resistive-load switching characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 6.7 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		12		ns
$t_{d(off)}$	Turn-off delay time			100		
t_r	Rise time			43		
t_f	Fall time			5		
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 2.5 A, V_{GS} = 10 V, See Figure 3		13.6	18	nC
Q_{gs}	Gate-source charge			8.3	11	
Q_{gd}	Gate-drain charge			5.3	7	
L_D	Internal drain inductance			7		nH
L_S	Internal source inductance			7		

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power			62.5	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	All outputs with equal power			1.5	°C/W
		One output dissipating power			3.3	°C/W

PARAMETER MEASUREMENT INFORMATION



NOTE A: I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveforms of Source-Drain Diode

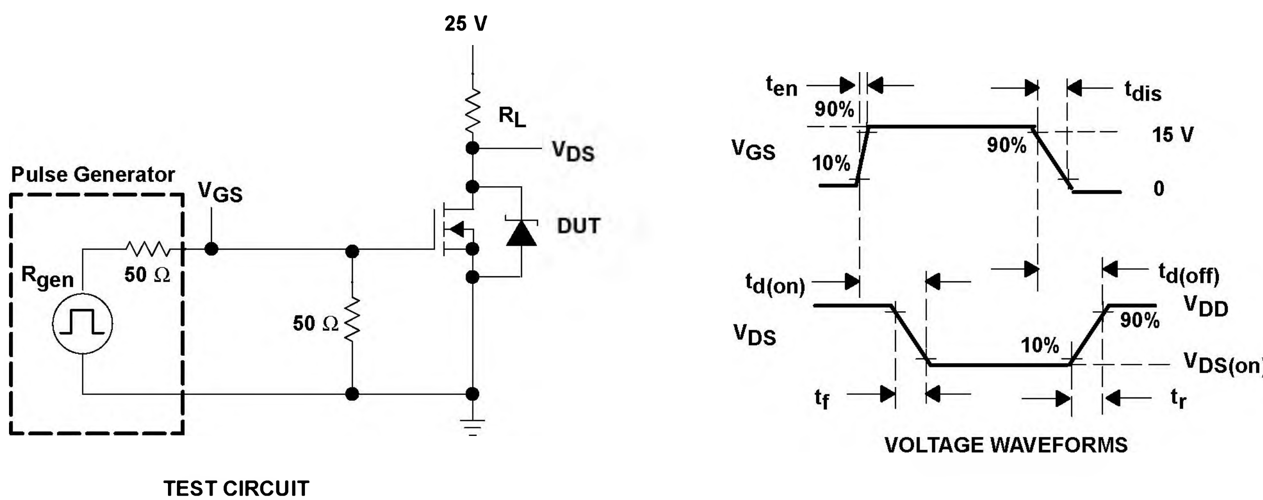


Figure 2. Resistive Switching

PARAMETER MEASUREMENT INFORMATION

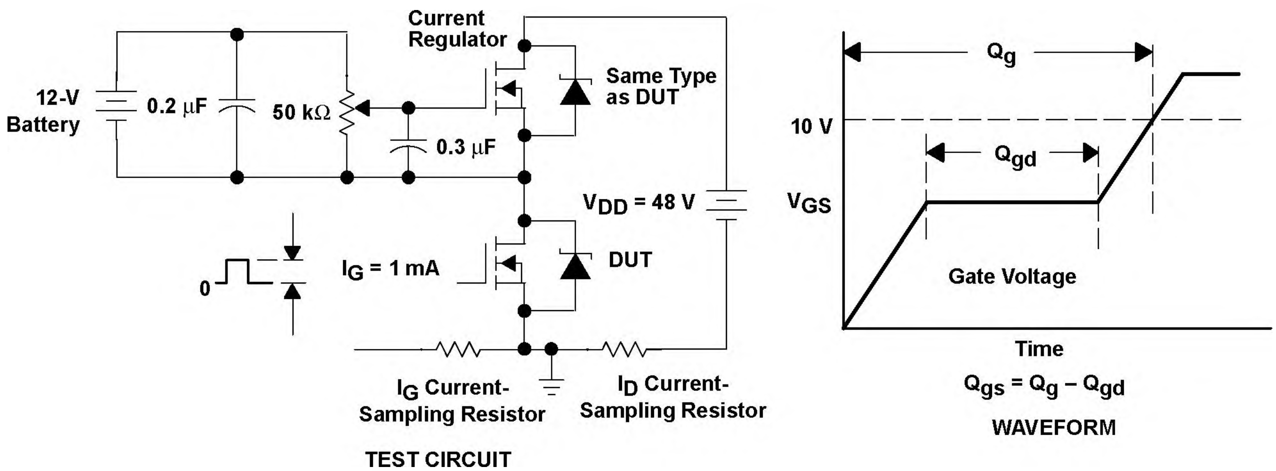
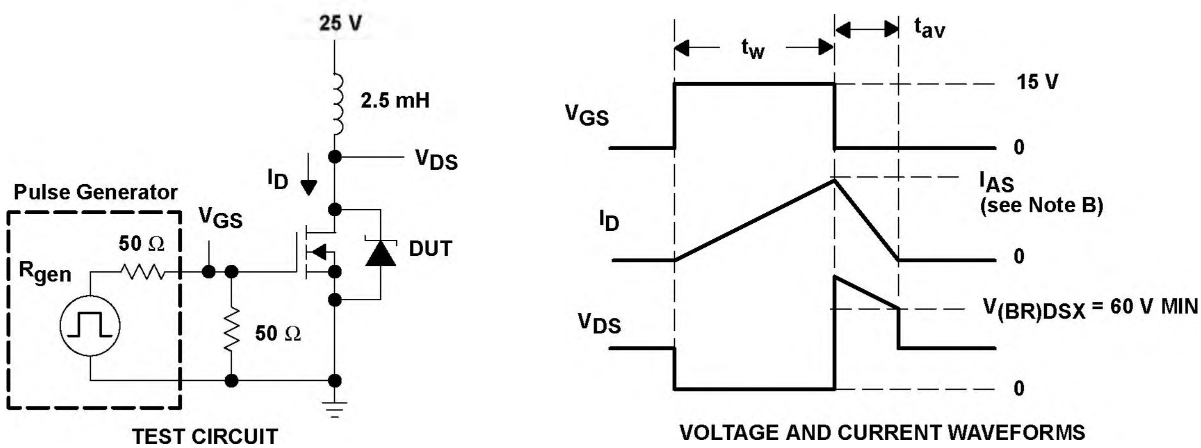


Figure 3. Gate-Charge Test Circuit and Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 7.5$ A.

Energy test level is defined as $E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 120$ mJ min.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
CASE TEMPERATURE

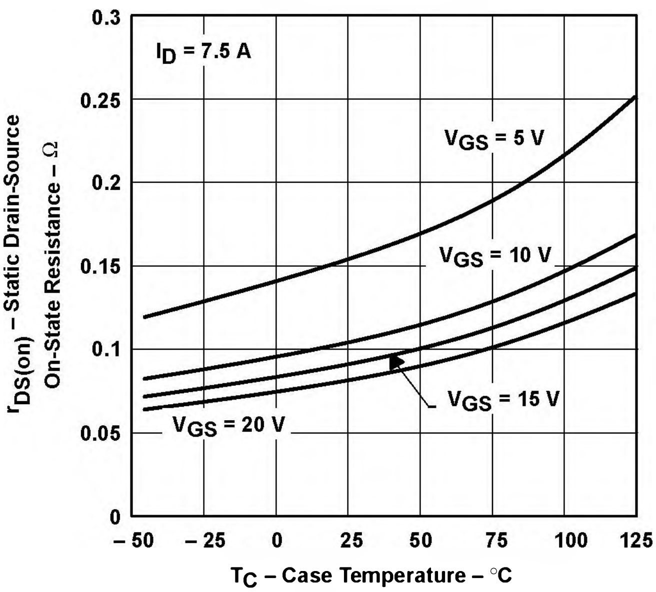


Figure 5

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

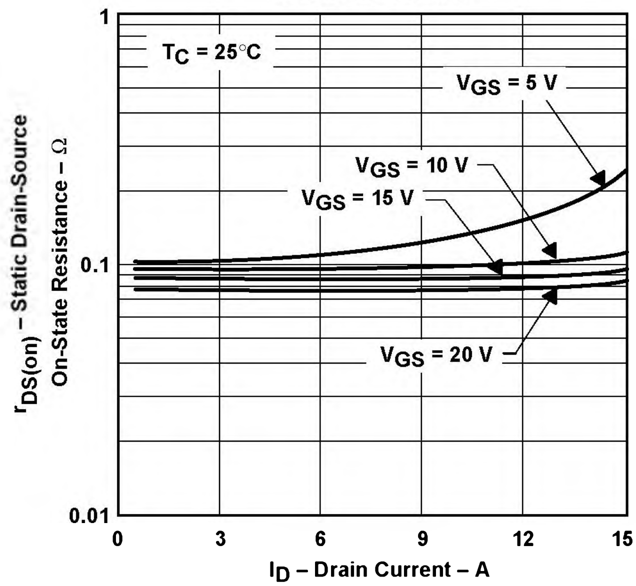


Figure 6

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

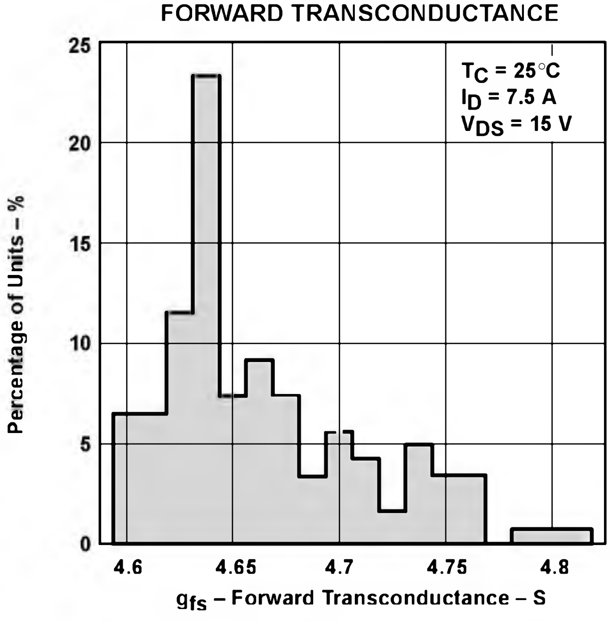


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

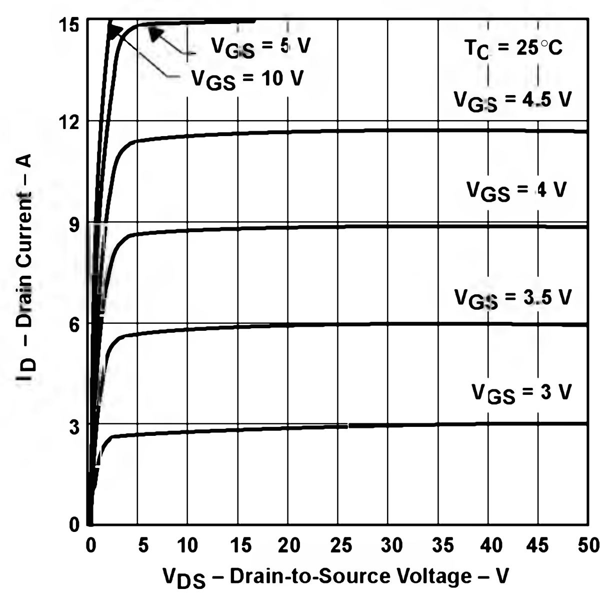


Figure 8

TYPICAL CHARACTERISTICS

GATE-SOURCE THRESHOLD VOLTAGE
vs
CASE TEMPERATURE

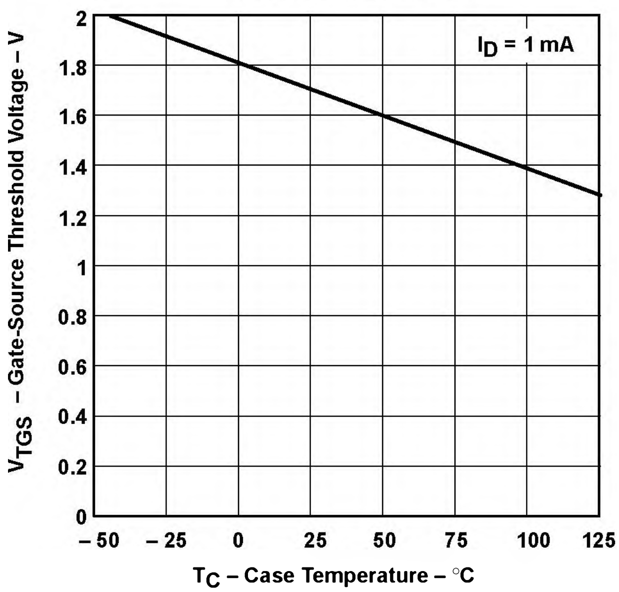


Figure 9

SOURCE-DRAIN DIODE CURRENT
vs
SOURCE-DRAIN VOLTAGE

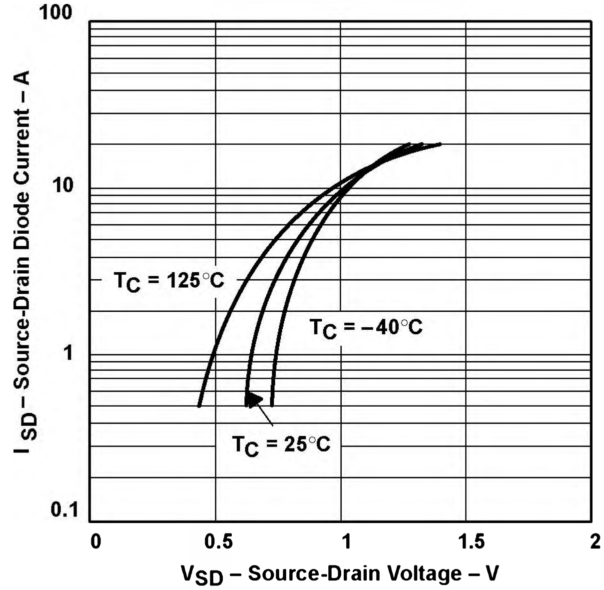


Figure 10

GATE-SOURCE VOLTAGE
vs
GATE CHARGE

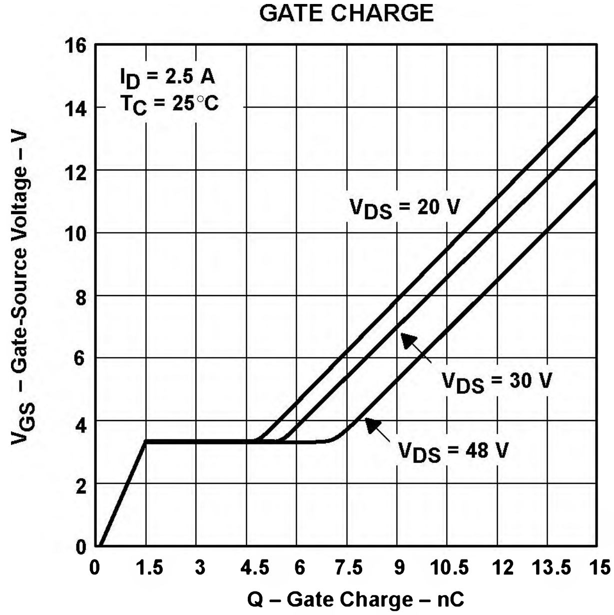


Figure 11

REVERSE RECOVERY TIME
vs
REVERSE di/dt

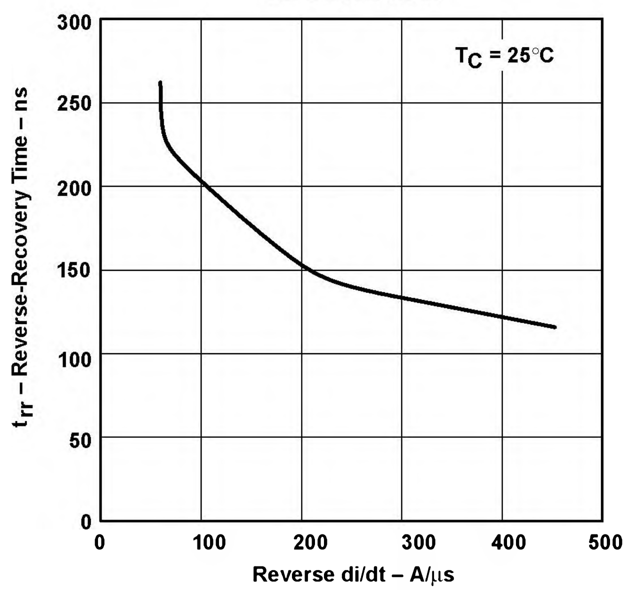


Figure 12

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TYPICAL CHARACTERISTICS

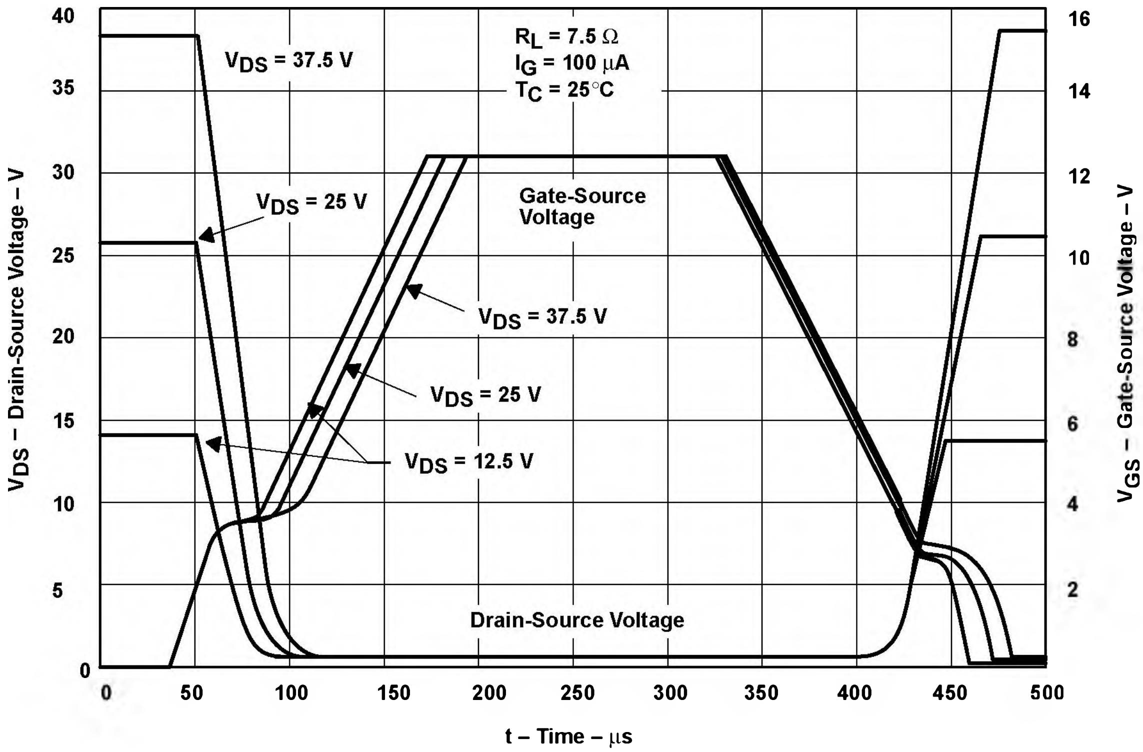


Figure 13. Resistive Switching Waveforms

THERMAL INFORMATION

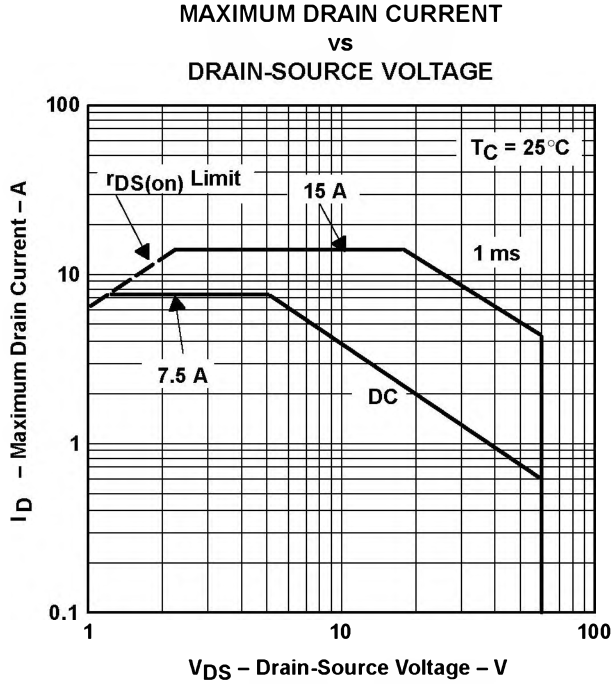


Figure 14

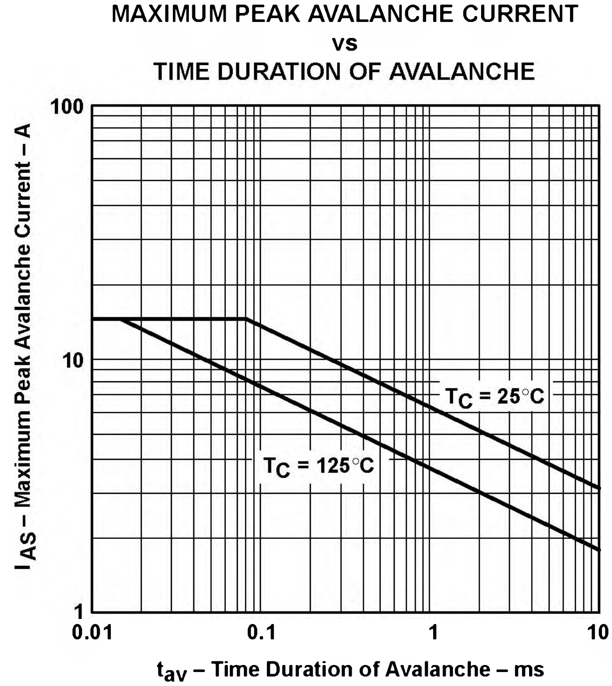
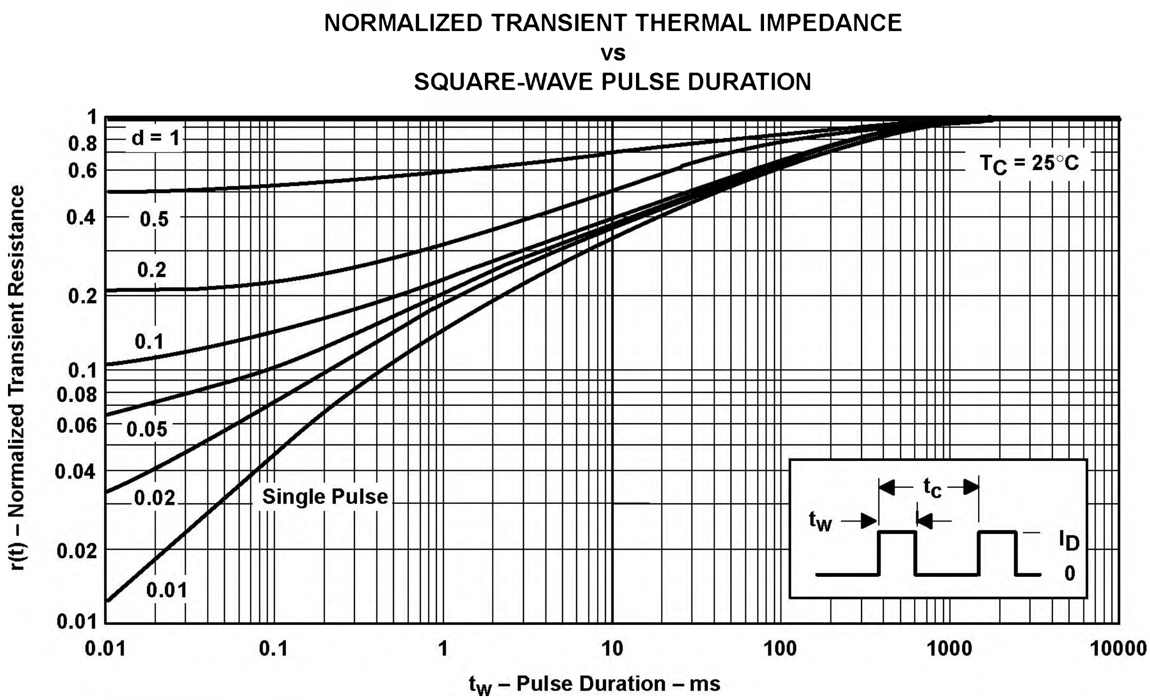


Figure 15



NOTES: $Z_{\theta JC}(t) = r(t) R_{\theta JC}$
t_w = pulse duration
t_c = period
d = duty cycle = t_w/t_c

Figure 16

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