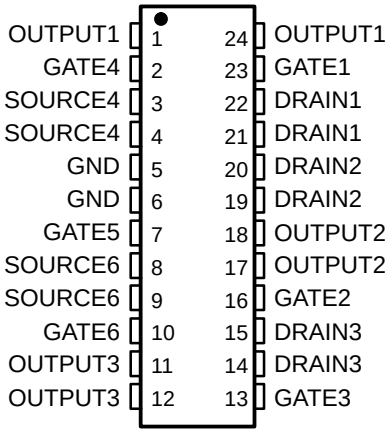
- **Low $r_{DS(on)}$ . . . 0.35 Ω Typ**
- **Voltage Output . . . 60 V**
- **Input Protection Circuitry . . . 18 V**
- **Pulsed Current . . . 4 A Per Channel**
- **Extended ESD Capability . . . 4000 V**
- **Direct Logic-Level Interface**

DW PACKAGE
(TOP VIEW)

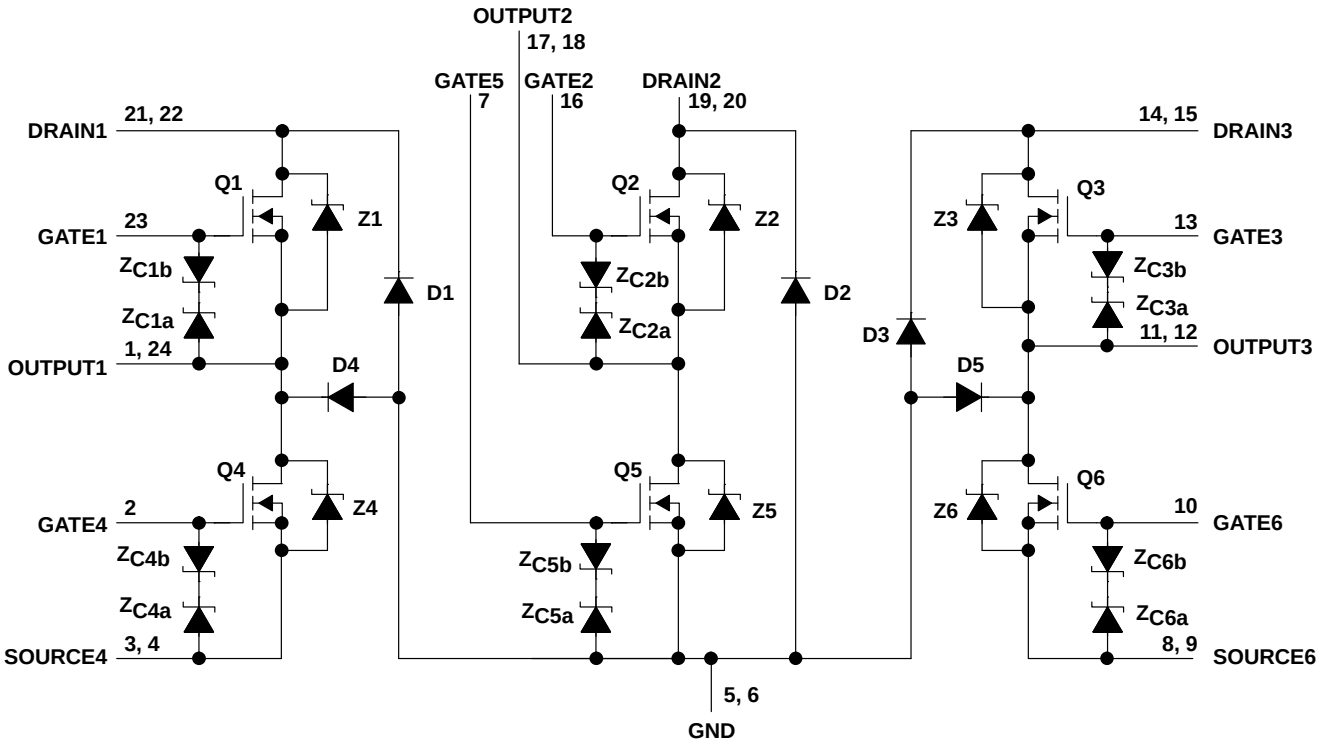


description

The TPIC1321L is a monolithic gate-protected logic-level power DMOS array that consists of six electrically isolated N-channel enhancement-mode DMOS transistors configured as 3-half H-bridges. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-kΩ resistor.

The TPIC1321L is offered in a 24-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature of –40°C to 125°C.

schematic



NOTE A: For correct operation, no terminal may be taken below GND.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Output-to-GND voltage	60 V
Drain-to-GND voltage	100 V
SOURCE4, SOURCE6-to-GND voltage	60 V
Gate-to-source voltage range, V_{GS}	–9 V to 18 V
Continuous drain current, each output, T_C = 25°C	1.25 A
Continuous source-to-drain diode current, T_C = 25°C	1.25 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	4 A
Continuous gate-to-source zener-diode current, T_C = 25°C	±50 mA
Pulsed gate-to-source zener-diode current, T_C = 25°C	±500 mA
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figures 4 and 16)	96 mJ
Continuous total dissipation, T_C = 25°C (see Figure 15)	1.39 W
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}, See Figure 5		1.5	1.75	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	I_{GS} = 250 µA		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	I_{SG} = 250 µA		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2, D3, D4, D5)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1.25 A, V_{GS} = 5 V, See Notes 2 and 3			0.44	0.5	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1.25 A, V_{GS} = 0 (Z1 – Z6), See Notes 2 and 3 and Figure 12			0.9	1.1	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 1.25 A (D1 – D5) See Notes 2 and 3			4		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	V_{GS} = 15 V, V_{DS} = 0			20	200	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	V_{SG} = 5 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 5 V, I_D = 1.25 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.35	0.4	Ω
			T_C = 125°C		0.57	0.6	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 625 mA, See Notes 2 and 3 and Figure 9		1.6	1.74		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0, See Figure 11			200	250	pF
C_{oss}	Short-circuit output capacitance, common source				175	220	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				40	75	

NOTES: 2. Technique should limit T_J – T_C to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 625 mA, V_{GS} = 0, See Figures 1 and 14	V_{DS} = 48 V, di/dt = 100 A/µs,	Z1, Z2, and Z3		45		ns
Q_{RR}	Total diode charge					50		nC

resistive-load switching characteristics, T_C = 25°C

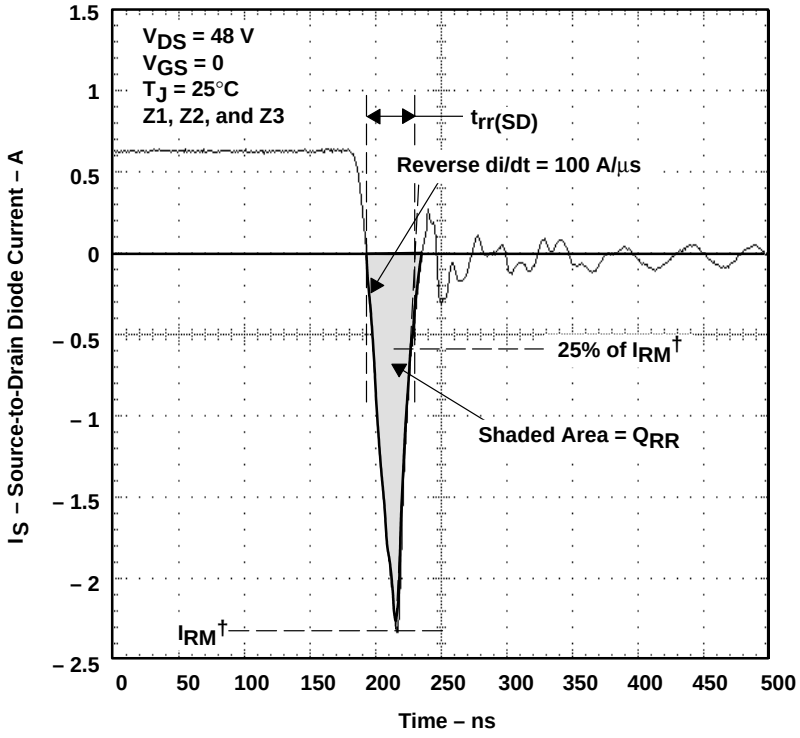
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 40 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		34	70	ns
$t_{d(off)}$	Turn-off delay time			80	150	
t_r	Rise time			28	55	
t_f	Fall time			15	30	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 625 mA, V_{GS} = 5 V, See Figure 3		4.6	5.8	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.7	0.88	
Q_{gd}	Gate-to-drain charge			2.5	3.13	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	See Notes 4 and 7		90		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	See Notes 5 and 7		44.5		
$R_{\theta JP}$	Junction-to-pin thermal resistance	See Notes 6 and 7		28		

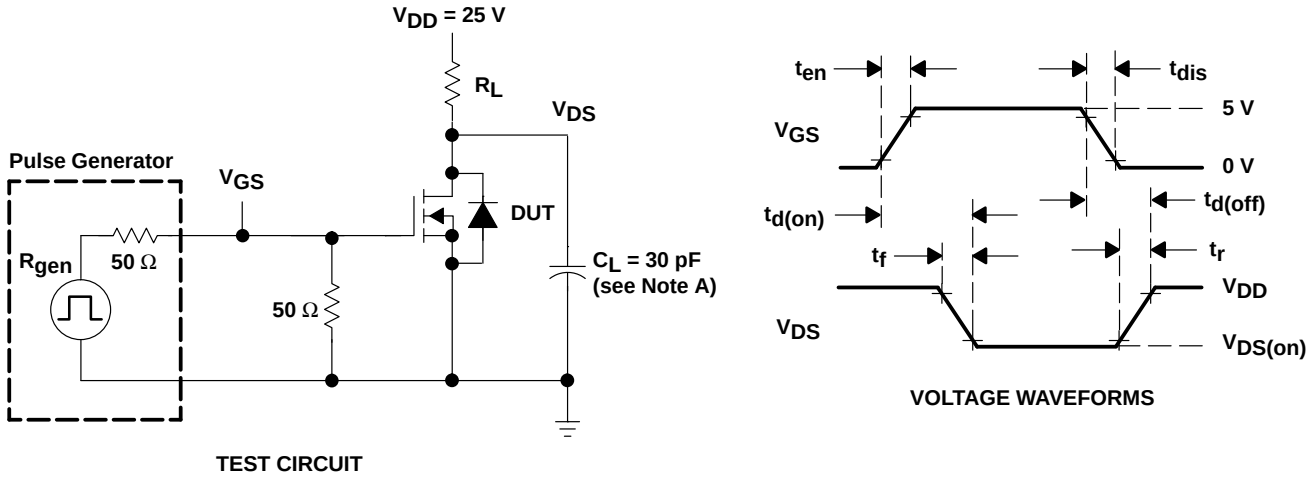
NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink.
5. Package mounted on a 24 in^2, 4-layer FR4 printed-circuit board.
6. Package mounted in intimate contact with infinite heatsink.
7. All outputs with equal power

PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

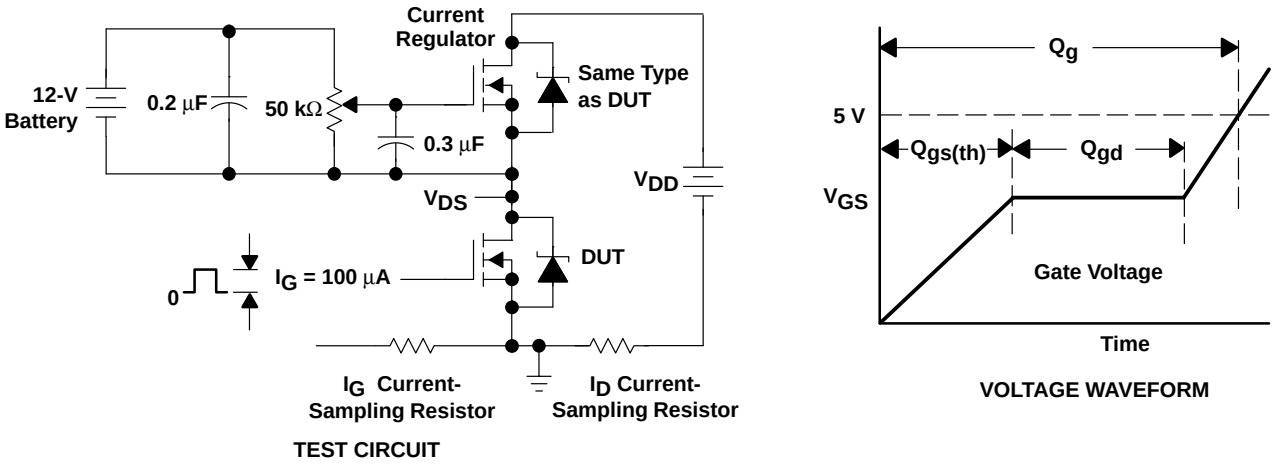
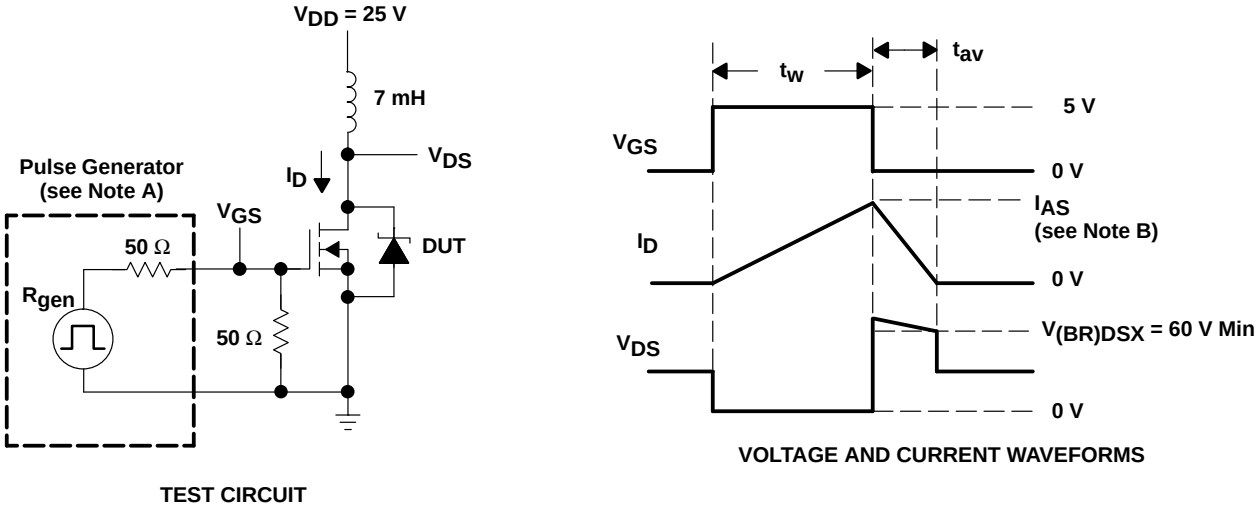


Figure 3. Gate-Charge Test Circuit and Voltage Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 4$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 96$ mJ.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

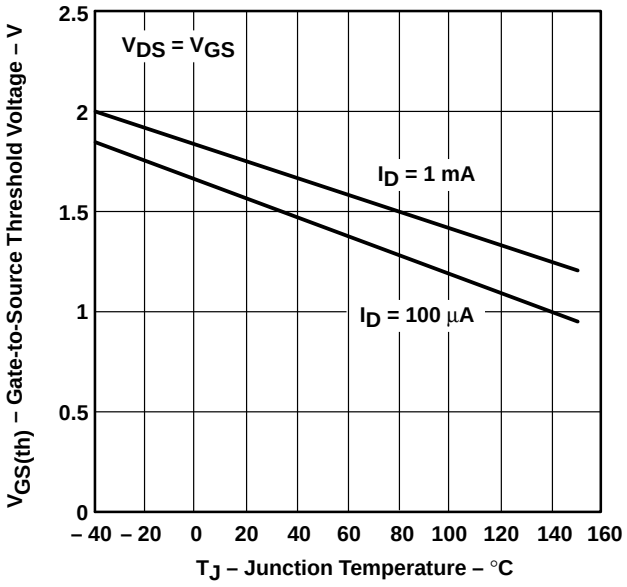


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

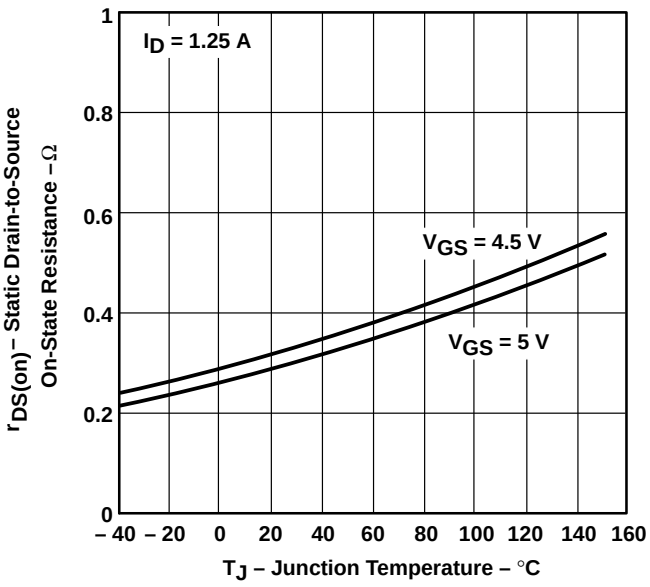


Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

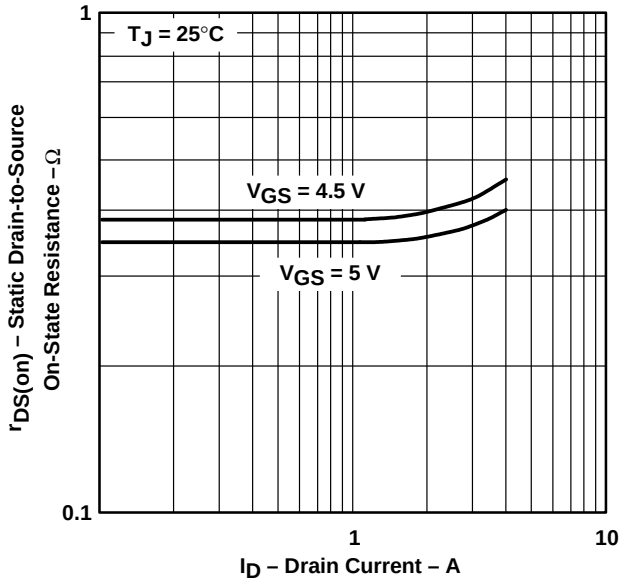


Figure 7

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

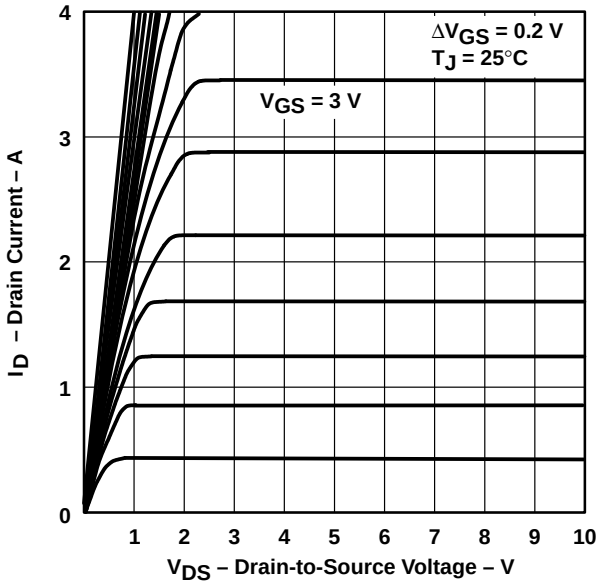


Figure 8

TYPICAL CHARACTERISTICS

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

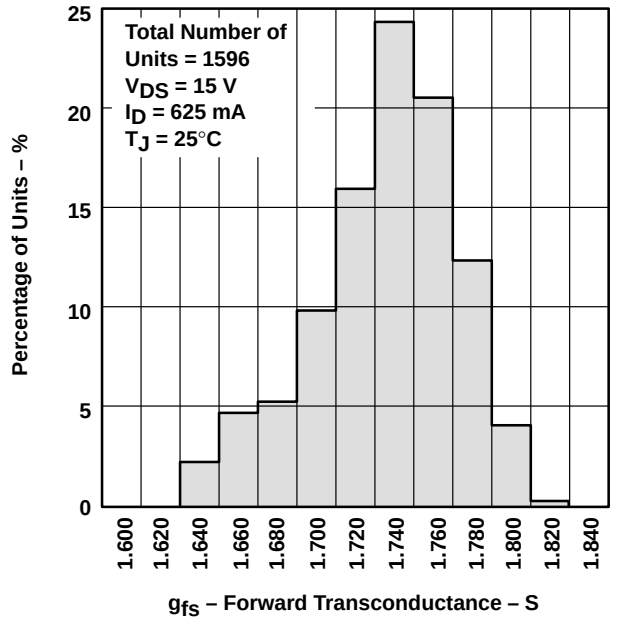


Figure 9

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

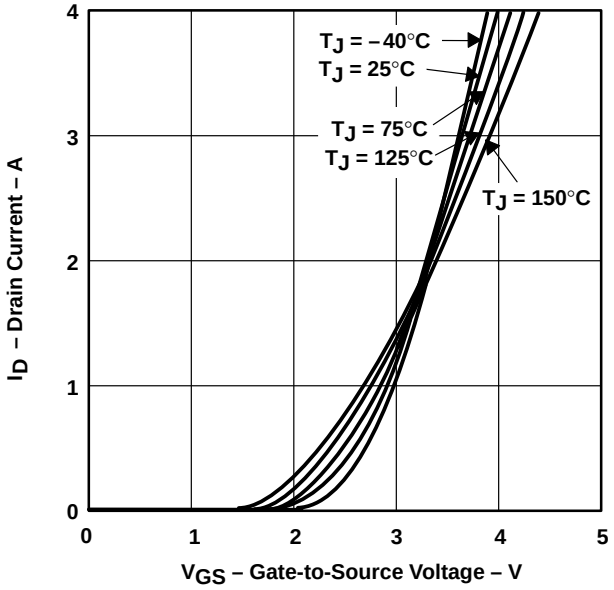


Figure 10

CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

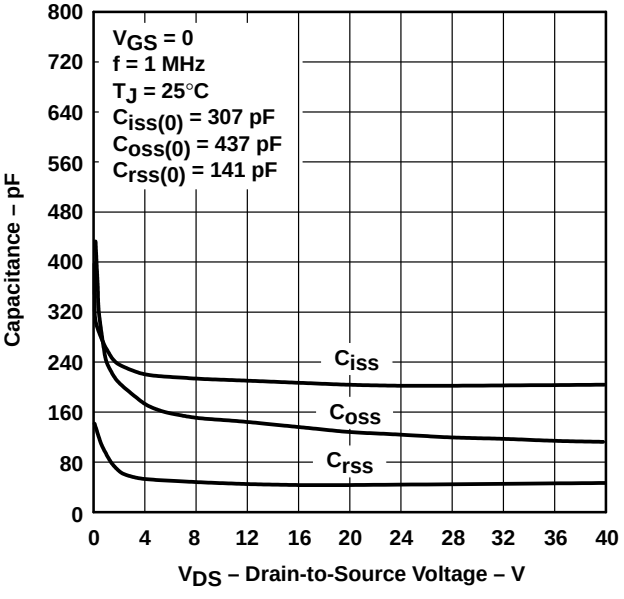


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

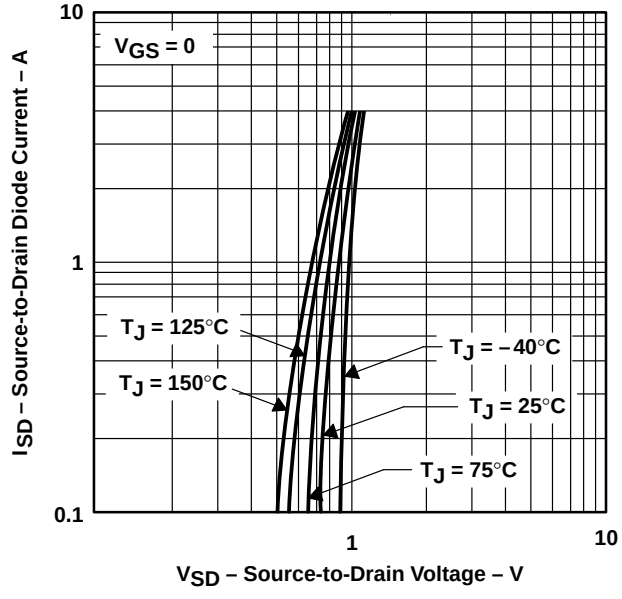


Figure 12

TYPICAL CHARACTERISTICS

**DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE**

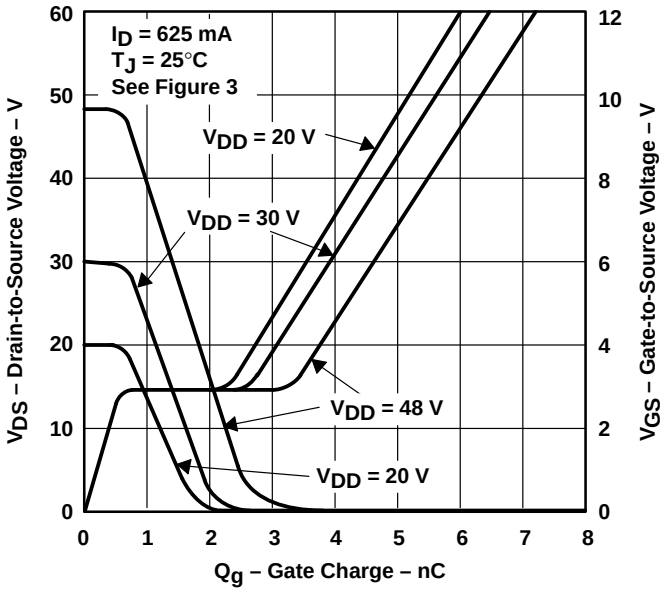


Figure 13

**REVERSE-RECOVERY TIME
vs
REVERSE di/dt**

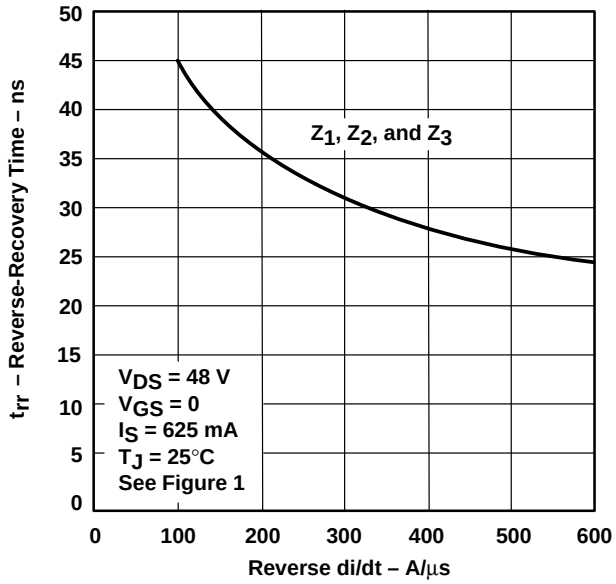
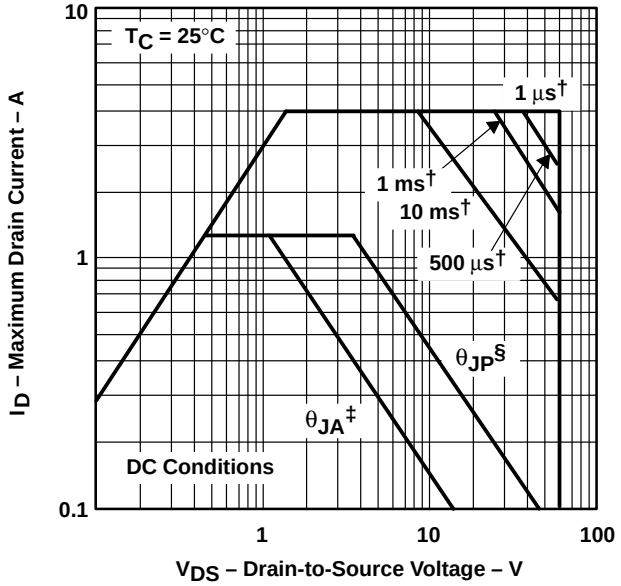


Figure 14

THERMAL INFORMATION

**MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE**



† Less than 2% duty cycle
‡ Device mounted on FR4 printed-circuit board with no heatsink.
§ Device mounted in intimate contact with infinite heatsink.

Figure 15

**MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE**

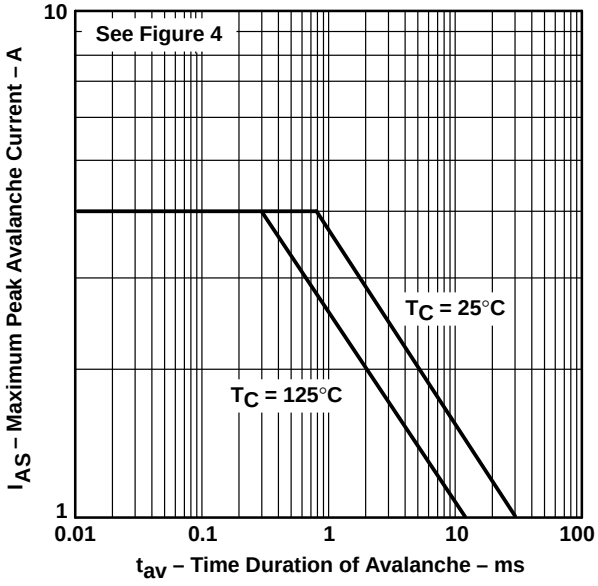
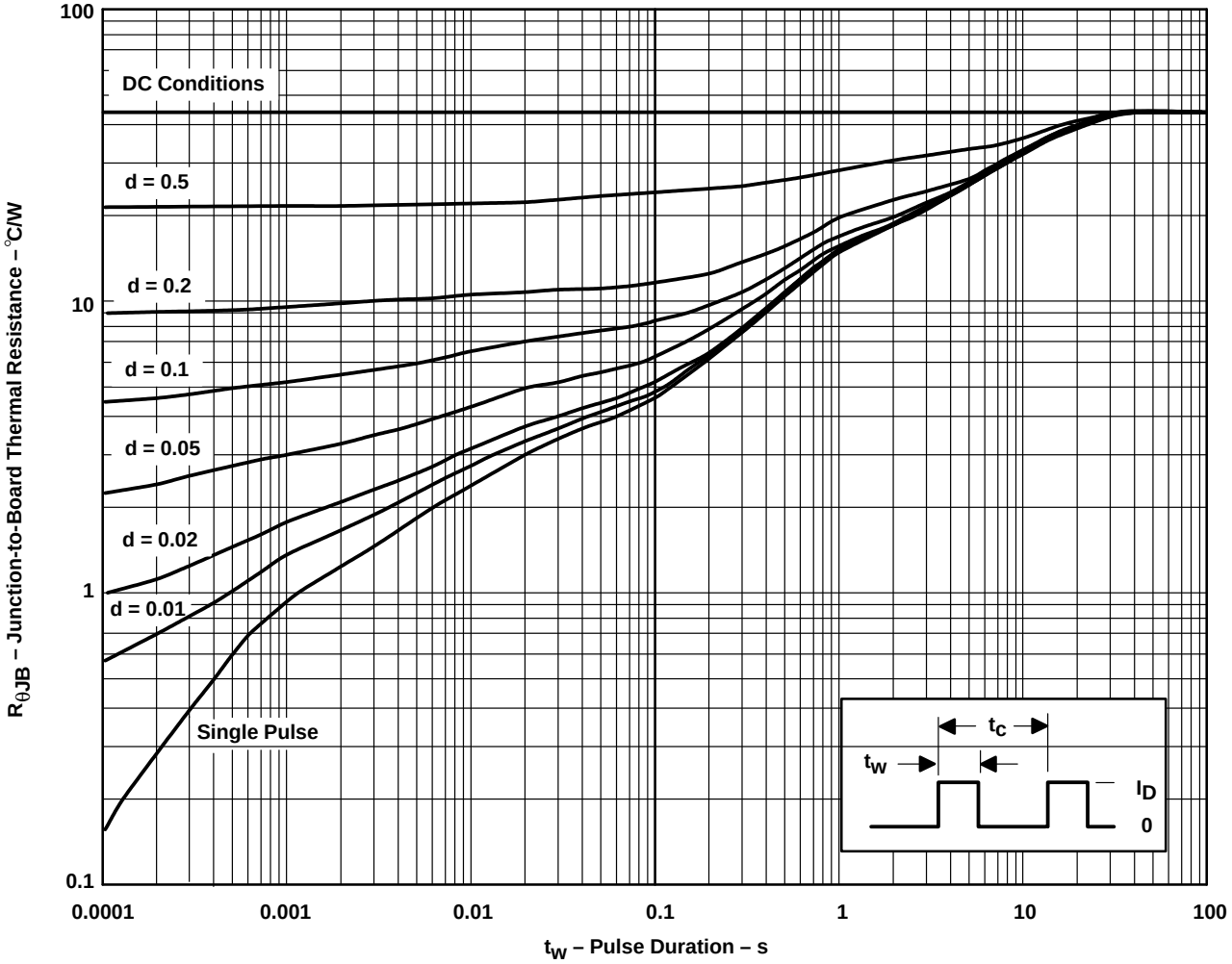


Figure 16

THERMAL INFORMATION

DW PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
vs
PULSE DURATION



† Device mounted on 24 in^2, 4-layer FR4 printed-circuit board with no heatsink.

NOTE A: $Z_{\theta B}(t) = r(t)\ R_{\theta JB}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W / t_C

Figure 17

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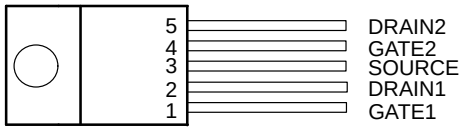
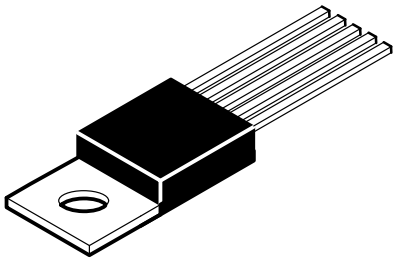
- **Two 7.5-A Independent Output Channels, Continuous Current Per Channel**
- **Low $r_{DS(on)}$ . . . 0.09 Ω Typical**
- **Output Voltage . . . 60 V**
- **Pulsed Current . . . 15 A Per Channel**
- **Avalanche Energy . . . 120 mJ**

KC PACKAGE
(TOP VIEW)



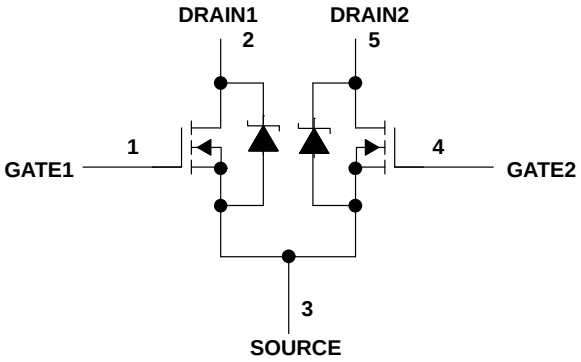
The tab is electrically connected to SOURCE.



description

The TPIC2202 is a monolithic power DMOS array that consists of two independent N-channel enhancement-mode DMOS transistors connected in a common-source configuration with open drains.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)

Drain-source voltage, V_{DS}	60 V
Gate-source voltage, V_{GS}	±20 V
Continuous source-drain diode current	7.5 A
Pulsed drain current, each output, all outputs on, I_D (see Note 1)	15 A
Continuous drain current, each output, all outputs on	7.5 A
Single-pulse avalanche energy, E_{AS} (see Figure 4)	120 mJ
Continuous power dissipation at (or below) T_A = 25°C (see Note 2)	2 W
Continuous power dissipation at (or below) T_C = 75°C, all outputs on (see Note 2)	31 W
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range, T_{stg}	–40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Pulse duration = 10 ms, duty cycle = 6%
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16 mW/°C. For operation above 75°C case temperature, and with all outputs conducting, derate linearly at the rate of 0.42 W/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded.

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)DS}$	Drain-source breakdown voltage	I_D = 1 µA,	V_{GS} = 0		60			V
V_{TGS}	Gate-source threshold voltage	I_D = 1 mA,	V_{DS} = V_{GS}		1.2	1.75	2.4	V
$V_{DS(on)}$	Drain-source on-state voltage	I_D = 7.5 A,	V_{GS} = 15 V,	See Notes 3 and 4		0.68	0.94	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V,	V_{GS} = 0	T_C = 25°C		0.07	1	µA
				T_C = 125°C		1.3	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 20 V,	V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{GS} = –20 V,	V_{DS} = 0			10	100	nA
$r_{DS(on)}$	Static drain-source on-state resistance	V_{GS} = 15 V, I_D = 7.5 A, See Notes 3 and 4 and Figures 5 and 6		T_C = 25°C		0.09	0.125	Ω
				T_C = 125°C		0.15	0.21	
g_{fs}	Forward transconductance	V_{DS} = 15 V,	I_D = 5 A,	See Notes 3 and 4	2.5	4.7		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V,	V_{GS} = 0,	f = 300 kHz		490		pF
C_{oss}	Short-circuit output capacitance, common source					285		
C_{rss}	Short-circuit reverse transfer capacitance, common source					90		

NOTES: 3. Technique should limit $T_J - T_C$ to 10°C maximum.
4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{SD}	Forward on voltage	I_S = 7.5 A, V_{DS} = 48 V,	V_{GS} = 0, See Figure 1	di/dt = 100 A/µs,		0.8	1.3	V
t_{rr}	Reverse recovery time					200		ns
Q_{RR}	Total source-drain diode charge					1.5		µC

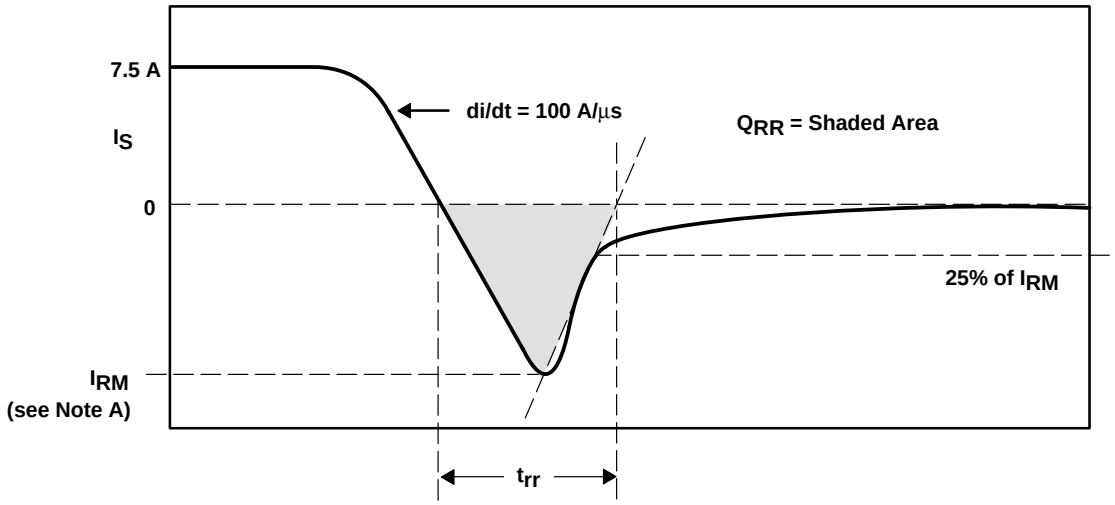
resistive-load switching characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, t_{dis} = 10 ns,	R_L = 6.7 Ω, See Figure 2	t_{en} = 10 ns,		12		ns
$t_{d(off)}$	Turn-off delay time					100		
t_r	Rise time					43		
t_f	Fall time					5		
Q_g	Total gate charge	V_{DD} = 48 V, See Figure 3	I_D = 2.5 A,	V_{GS} = 10 V,		13.6	18	nC
Q_{gs}	Gate-source charge					8.3	11	
Q_{gd}	Gate-drain charge					5.3	7	
L_D	Internal drain inductance					7		nH
L_S	Internal source inductance					7		

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power			62.5	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	All outputs with equal power			2.4	°C/W
		One output dissipating power			3.3	°C/W

PARAMETER MEASUREMENT INFORMATION



NOTE A: I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveforms of Source-Drain Diode

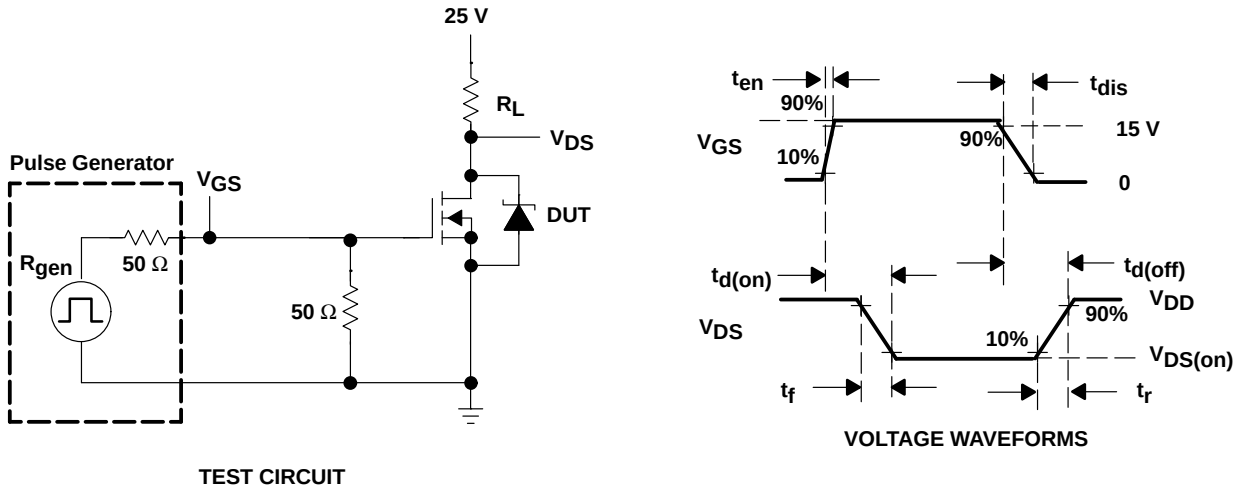


Figure 2. Test Circuit and Voltage Waveforms, Resistive Switching

PARAMETER MEASUREMENT INFORMATION

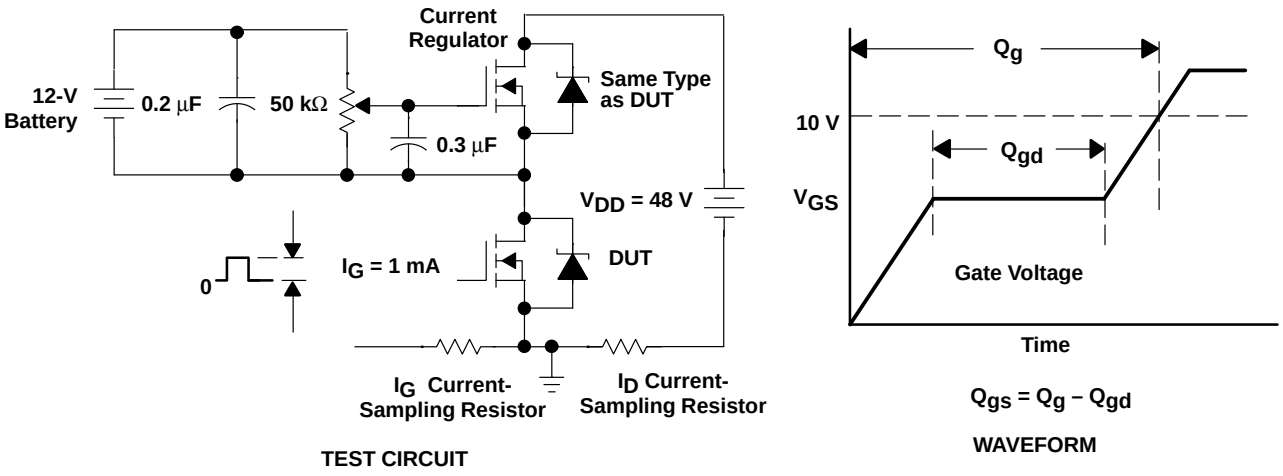
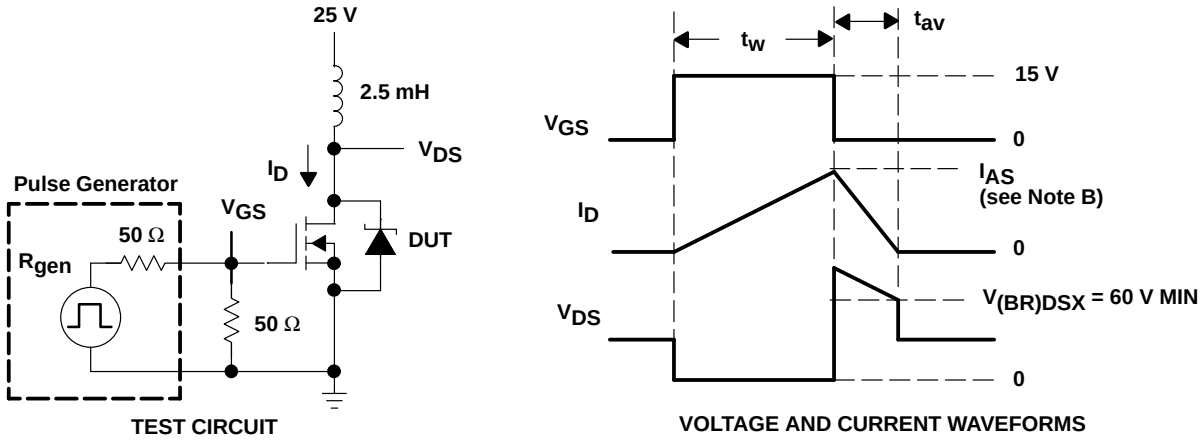


Figure 3. Gate Charge Test Circuit and Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_W) is increased until peak current $I_{AS} = 7.5$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 120$ mJ min.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs CASE TEMPERATURE

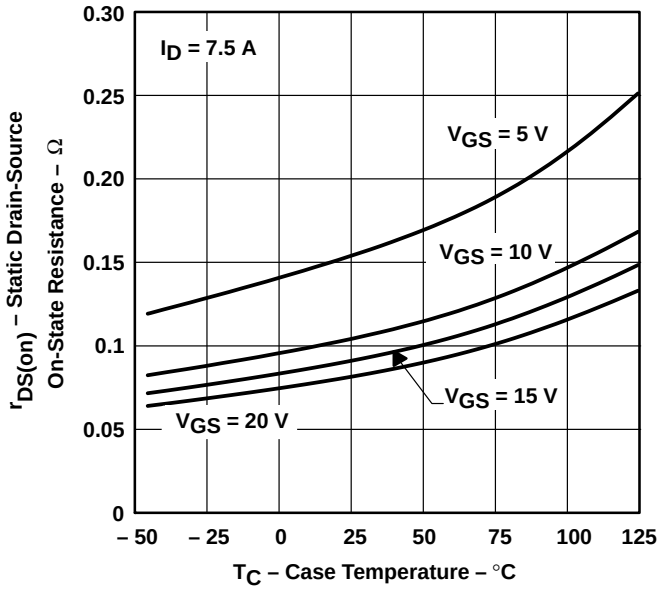


Figure 5

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

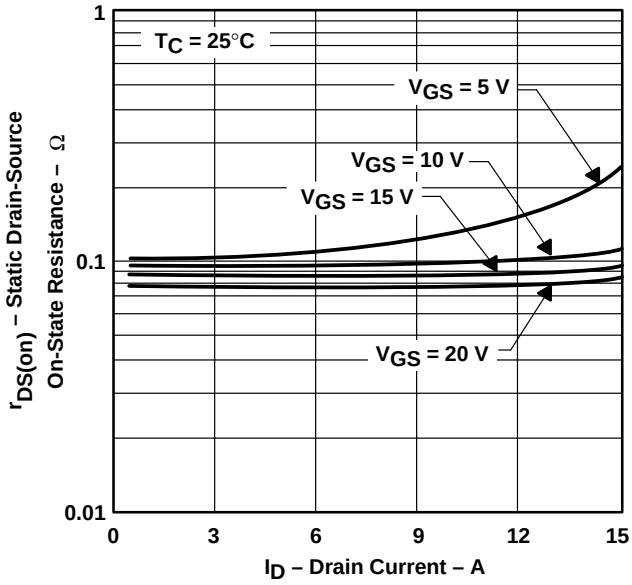


Figure 6

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

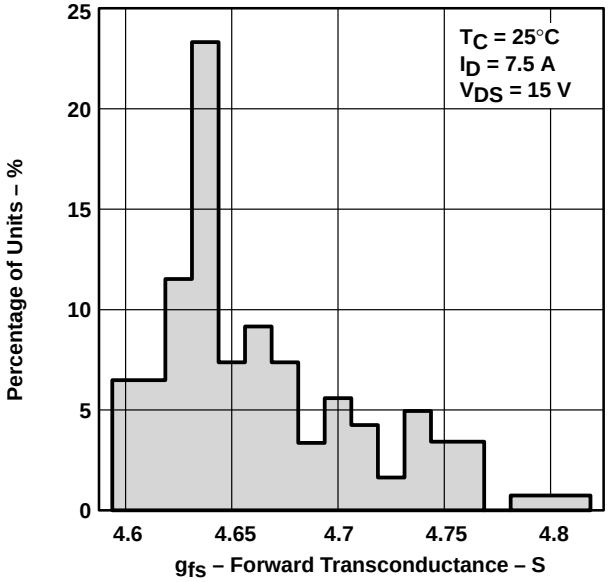


Figure 7

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

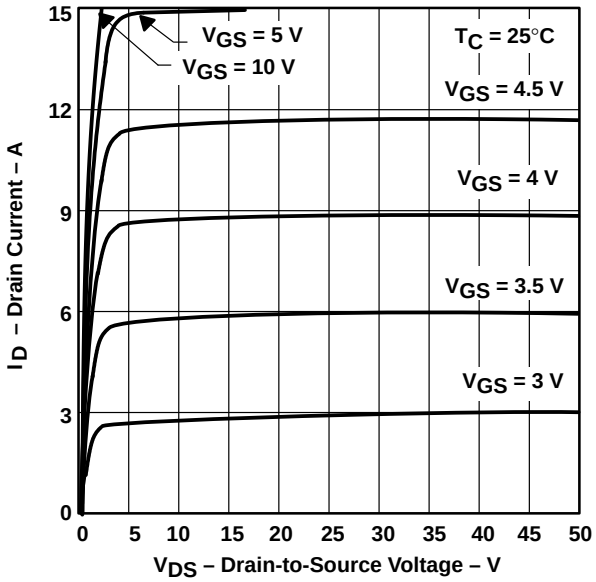


Figure 8

TYPICAL CHARACTERISTICS

GATE-SOURCE THRESHOLD VOLTAGE vs CASE TEMPERATURE

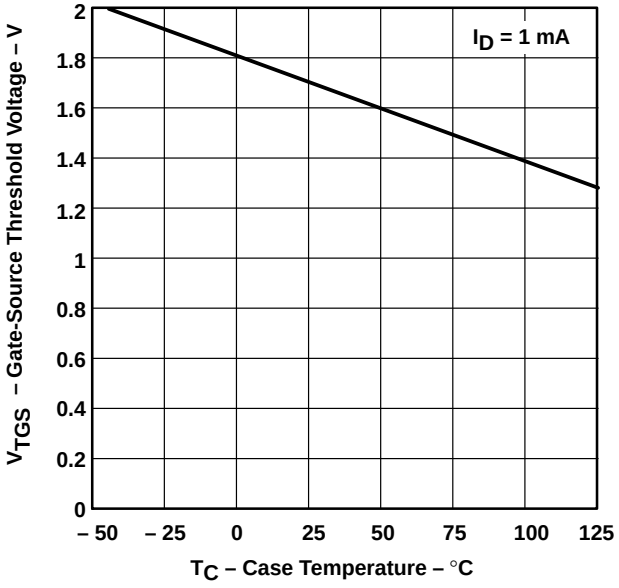


Figure 9

SOURCE-DRAIN DIODE CURRENT vs SOURCE-DRAIN VOLTAGE

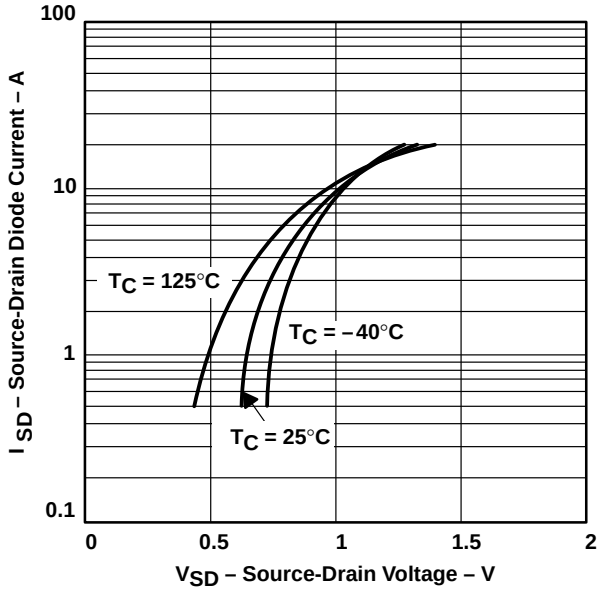


Figure 10

GATE-SOURCE VOLTAGE vs GATE CHARGE

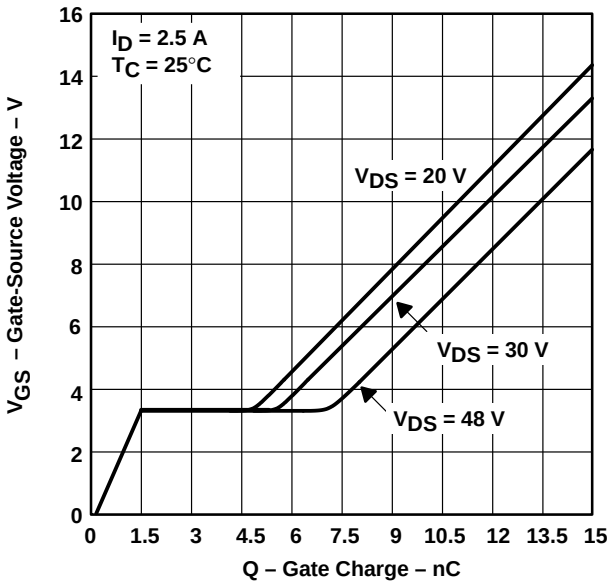


Figure 11

REVERSE RECOVERY TIME vs REVERSE di/dt

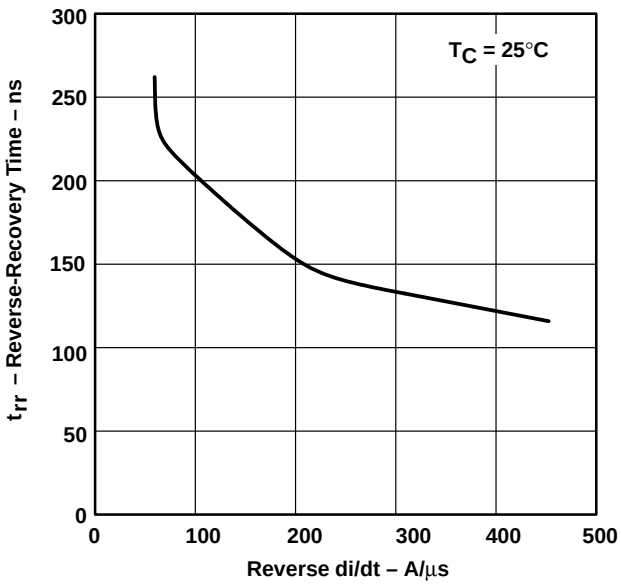


Figure 12

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TYPICAL CHARACTERISTICS

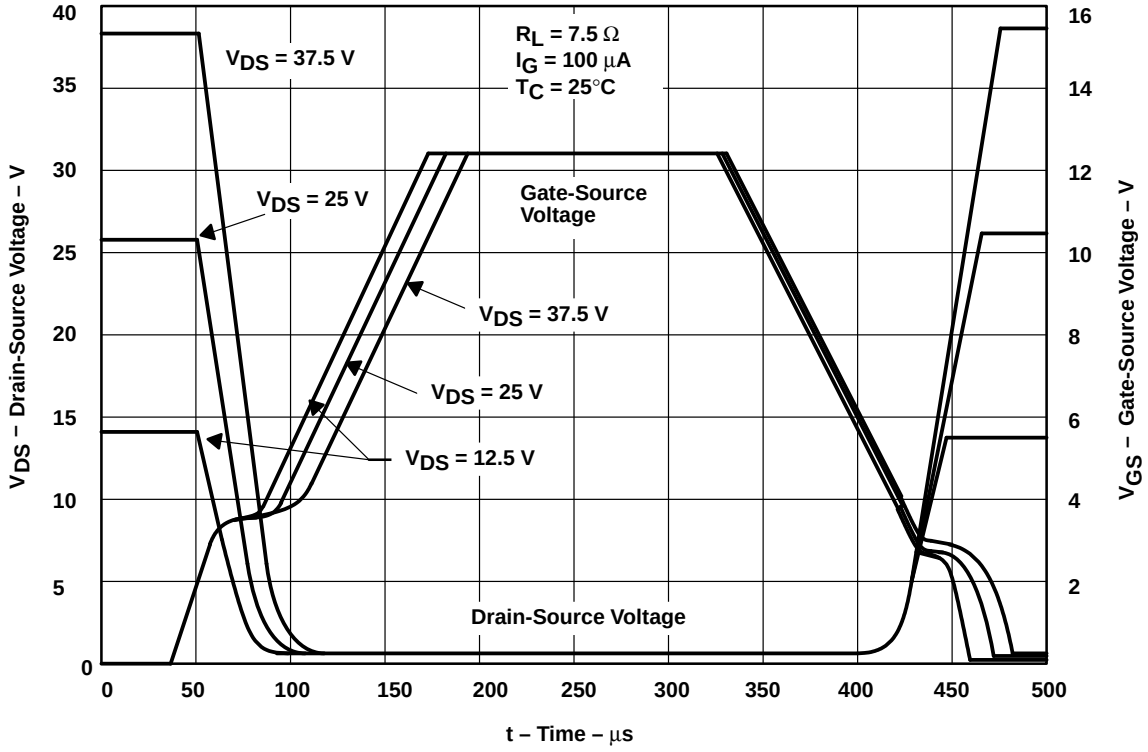


Figure 13. Resistive Switching Waveforms

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DRAIN-SOURCE VOLTAGE

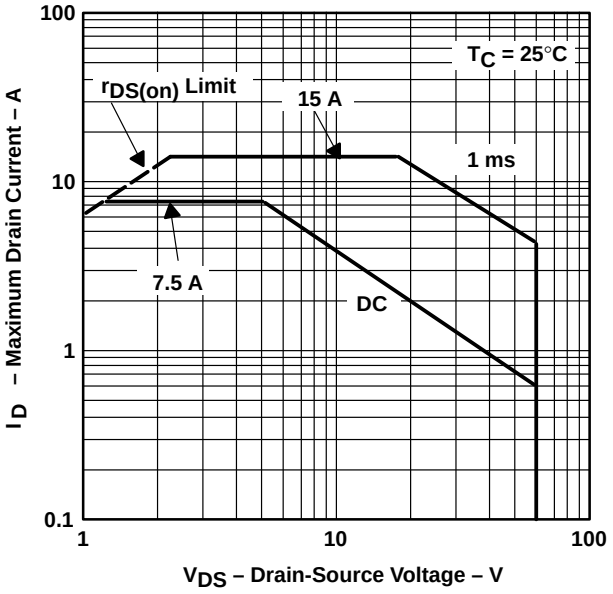


Figure 14

MAXIMUM PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

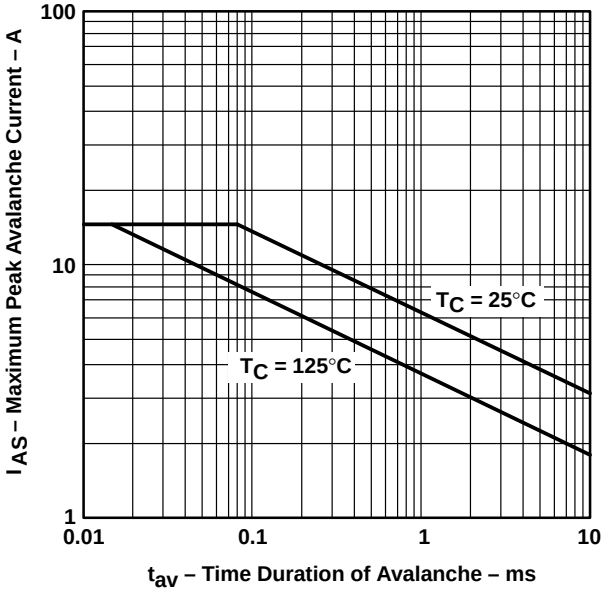
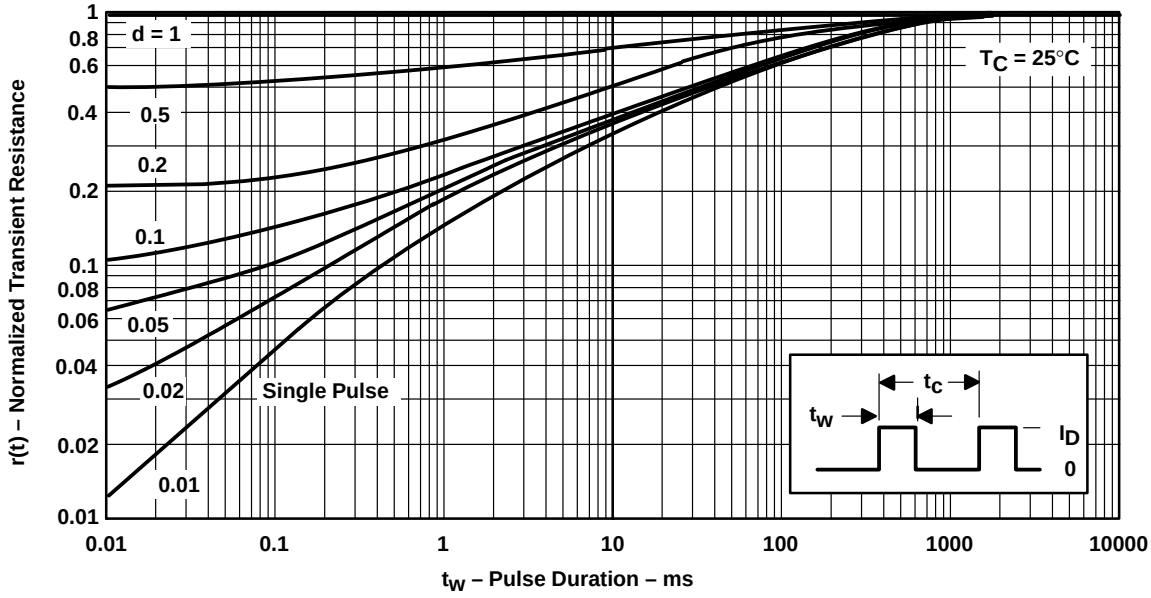


Figure 15

THERMAL INFORMATION

**NORMALIZED TRANSIENT THERMAL IMPEDANCE
vs
SQUARE-WAVE PULSE DURATION**



NOTES: $Z_{\theta JC}(t) = r(t)\ R_{\theta JC}$
t_W = pulse duration
t_C = period
d = duty cycle = t_W/t_C

Figure 16

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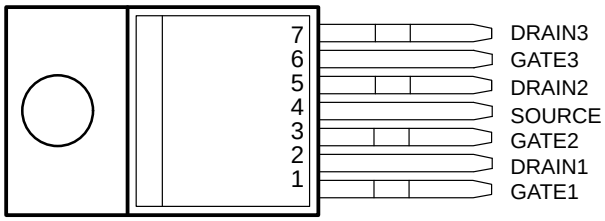
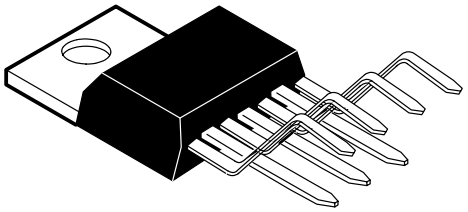
- **Three 7.5-A Independent Output Channels, Continuous Current Per Channel**
- **Low $r_{DS(on)}$ . . . 0.09 Ω Typical**
- **Output Voltage . . . 60 V**
- **Pulsed Current . . . 15 A Per Channel**
- **Avalanche Energy . . . 120 mJ**

KV PACKAGE
(TOP VIEW)



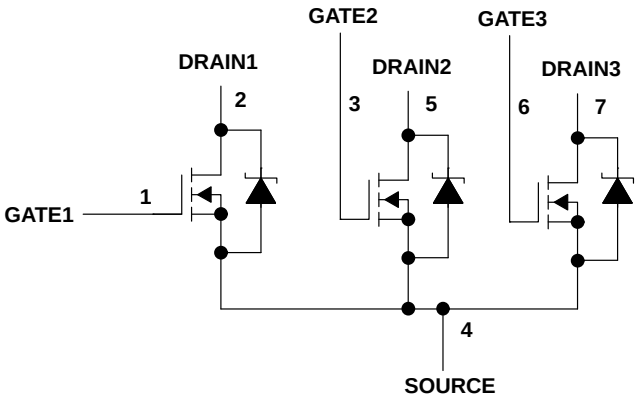


The tab is electrically connected to SOURCE.

description

The TPIC2301 is a monolithic power DMOS array that consists of three independent N-channel enhancement-mode DMOS transistors connected in a common-source configuration with open drains.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)

Drain-source voltage, V_{DS}	60 V
Gate-source voltage, V_{GS}	±20 V
Continuous source-drain diode current	7.5 A
Pulsed drain current, each output, all outputs on, I_D (see Note 1)	15 A
Continuous drain current, each output, all outputs on	7.5 A
Single-pulse avalanche energy, E_{AS} (see Figure 4)	120 mJ
Continuous power dissipation at (or below) T_A = 25°C (see Note 2)	2 W
Continuous power dissipation at (or below) T_C = 75°C, all outputs on (see Note 2)	50 W
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range, T_{stg}	–40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Pulse duration = 10 ms, duty cycle = 6%
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16 mW/°C. For operation above 75°C case temperature, and with all outputs conducting, derate linearly at the rate of 0.66 W/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded.

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)DS}$	Drain-source breakdown voltage	I_D = 1 µA, V_{GS} = 0			60			V
V_{TGS}	Gate-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}			1.2	1.75	2.4	V
$V_{DS(on)}$	Drain-source on-state voltage	I_D = 7.5 A, V_{GS} = 15 V, See Notes 3 and 4				0.68	0.94	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C			0.07	1	µA
			T_C = 125°C			1.3	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 20 V, V_{DS} = 0				10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{GS} = –20 V, V_{DS} = 0				10	100	nA
$r_{DS(on)}$	Static drain-source on-state resistance	V_{GS} = 15 V, I_D = 7.5 A, See Notes 3 and 4 and Figures 5 and 6	T_C = 25°C			0.09	0.125	Ω
			T_C = 125°C			0.15	0.21	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 5 A, See Notes 3 and 4			3.3	4.7		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 300 kHz				490		pF
C_{oss}	Short-circuit output capacitance, common source					285		
C_{rss}	Short-circuit reverse transfer capacitance, common source					90		

NOTES: 3. Technique should limit T_J – T_C to 10°C maximum.
4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{SD}	Forward on voltage	I_S = 7.5 A, V_{DS} = 48 V,	V_{GS} = 0, See Figure 1	di/dt = 100 A/µs,		0.8	1.3	V
t_{rr}	Reverse recovery time					200		ns
Q_{RR}	Total source-drain diode charge					1.5		µC

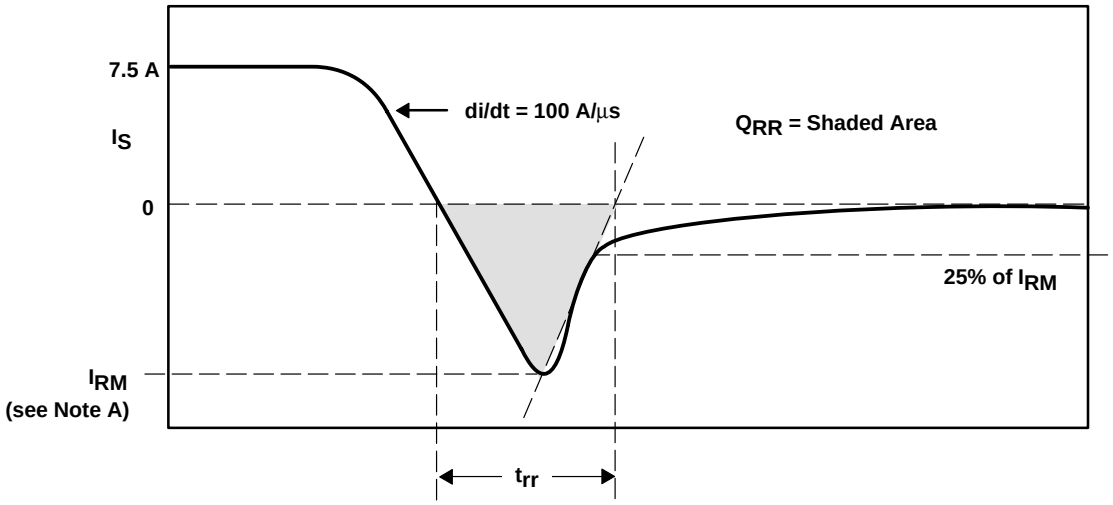
resistive-load switching characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, t_{dis} = 10 ns,	R_L = 6.7 Ω, See Figure 2	t_{en} = 10 ns,		12		ns
$t_{d(off)}$	Turn-off delay time					100		
t_r	Rise time					43		
t_f	Fall time					5		
Q_g	Total gate charge	V_{DS} = 48 V, See Figure 3	I_D = 2.5 A,	V_{GS} = 10 V,		13.6	18	nC
Q_{gs}	Gate-source charge					8.3	11	
Q_{gd}	Gate-drain charge					5.3	7	
L_D	Internal drain inductance					7		nH
L_S	Internal source inductance					7		

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power			62.5	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	All outputs with equal power			1.5	°C/W
		One output dissipating power			3.3	°C/W

PARAMETER MEASUREMENT INFORMATION



NOTE A: I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveforms of Source-Drain Diode

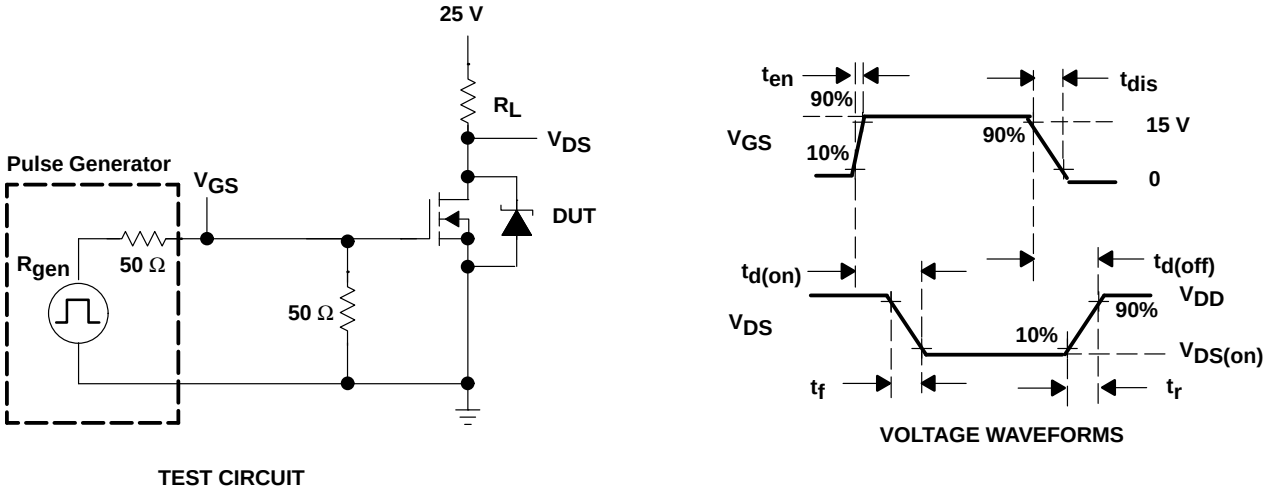


Figure 2. Resistive Switching

PARAMETER MEASUREMENT INFORMATION

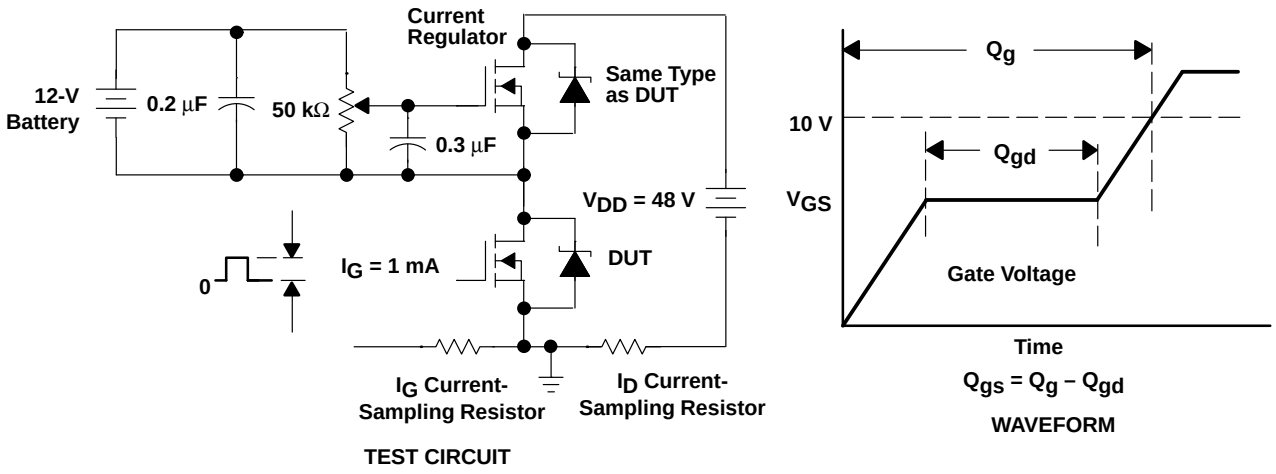
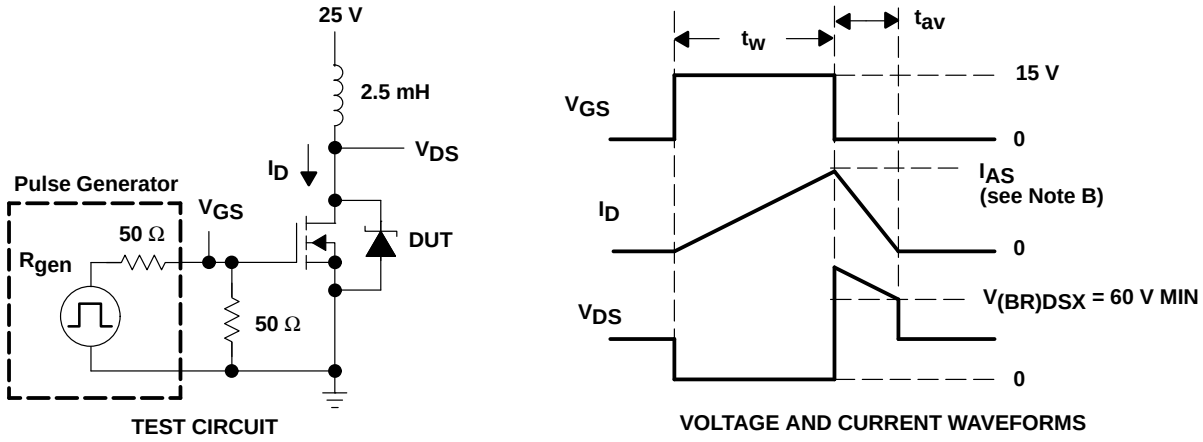


Figure 3. Gate-Charge Test Circuit and Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 7.5$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 120$ mJ min.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs CASE TEMPERATURE

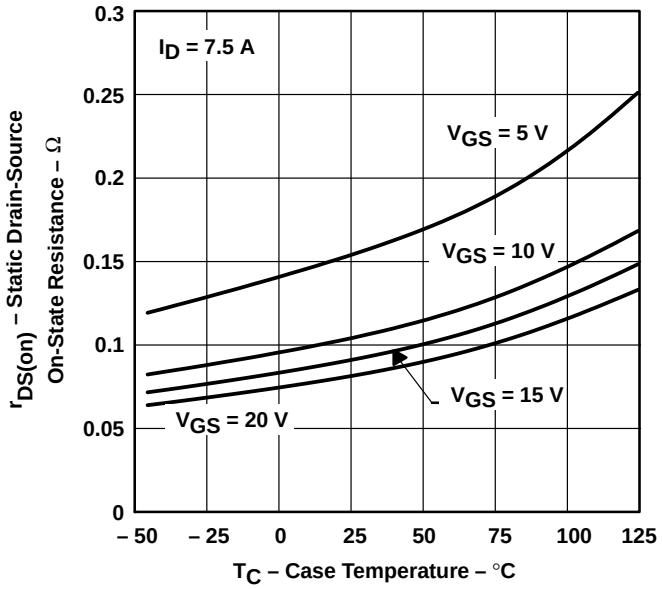


Figure 5

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

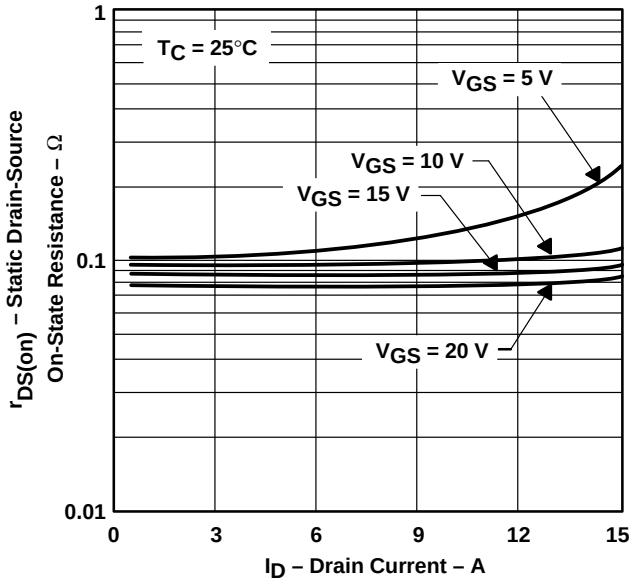


Figure 6

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

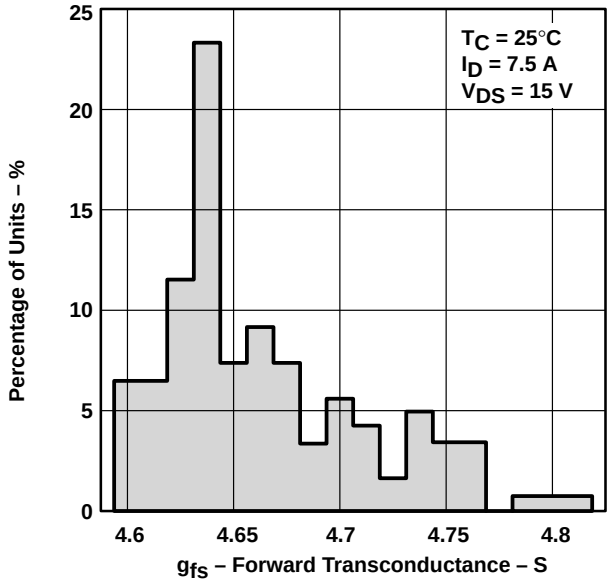


Figure 7

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

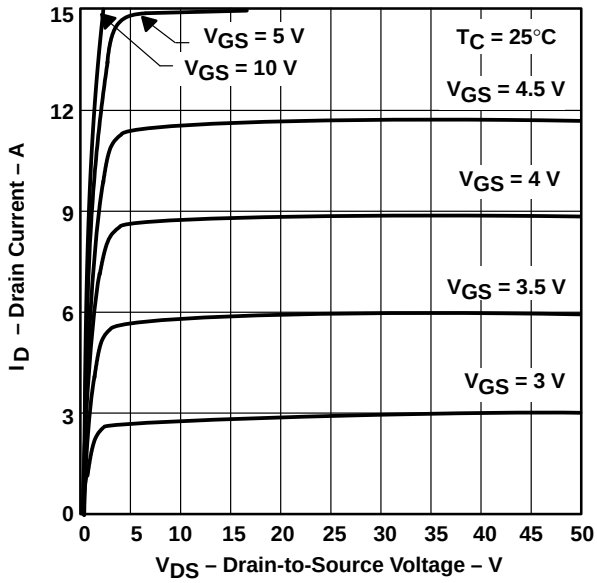


Figure 8

TYPICAL CHARACTERISTICS

GATE-SOURCE THRESHOLD VOLTAGE vs CASE TEMPERATURE

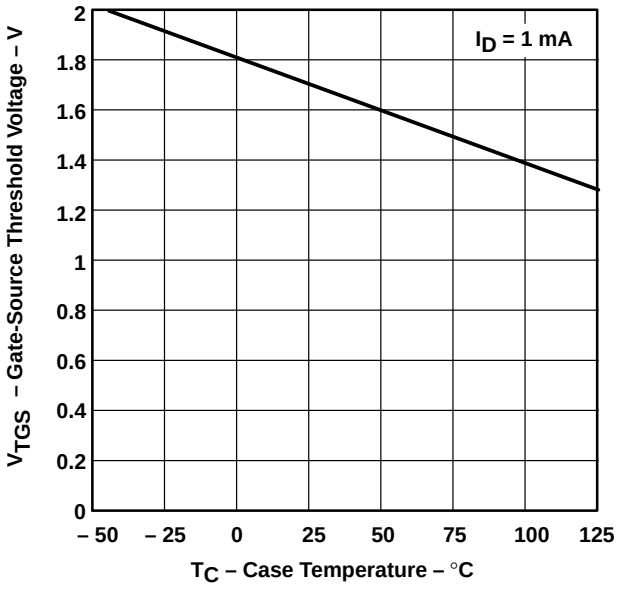


Figure 9

SOURCE-DRAIN DIODE CURRENT vs SOURCE-DRAIN VOLTAGE

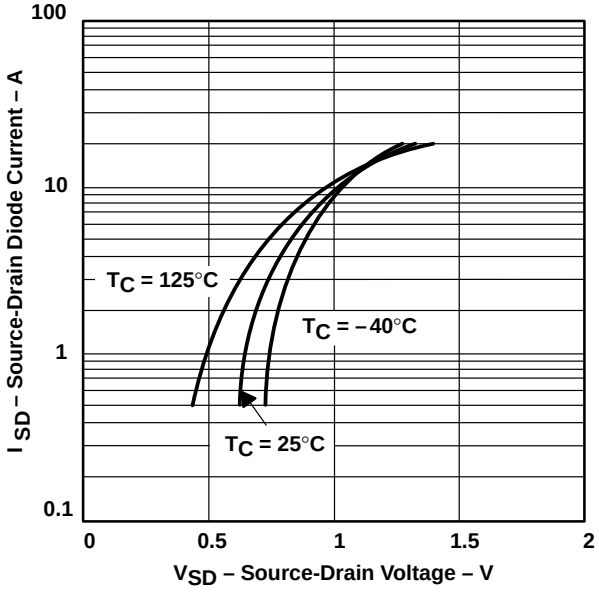


Figure 10

GATE-SOURCE VOLTAGE vs GATE CHARGE

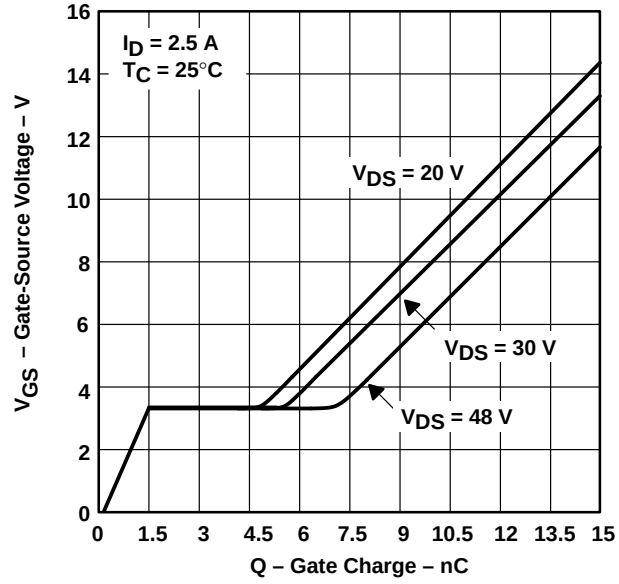


Figure 11

REVERSE RECOVERY TIME vs REVERSE di/dt

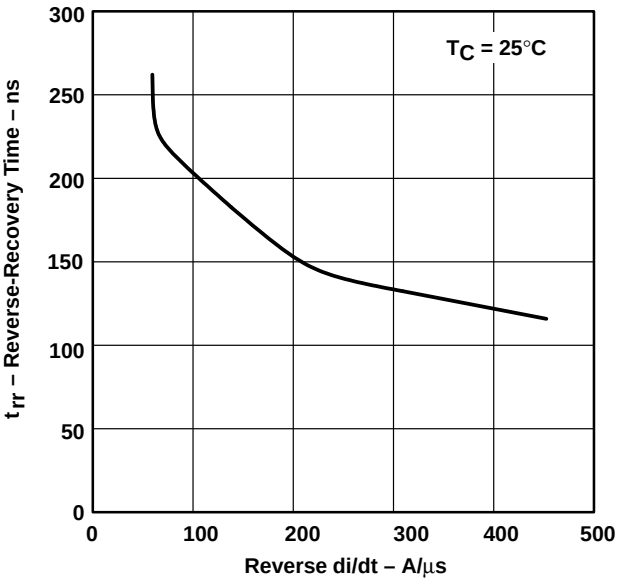


Figure 12

TYPICAL CHARACTERISTICS

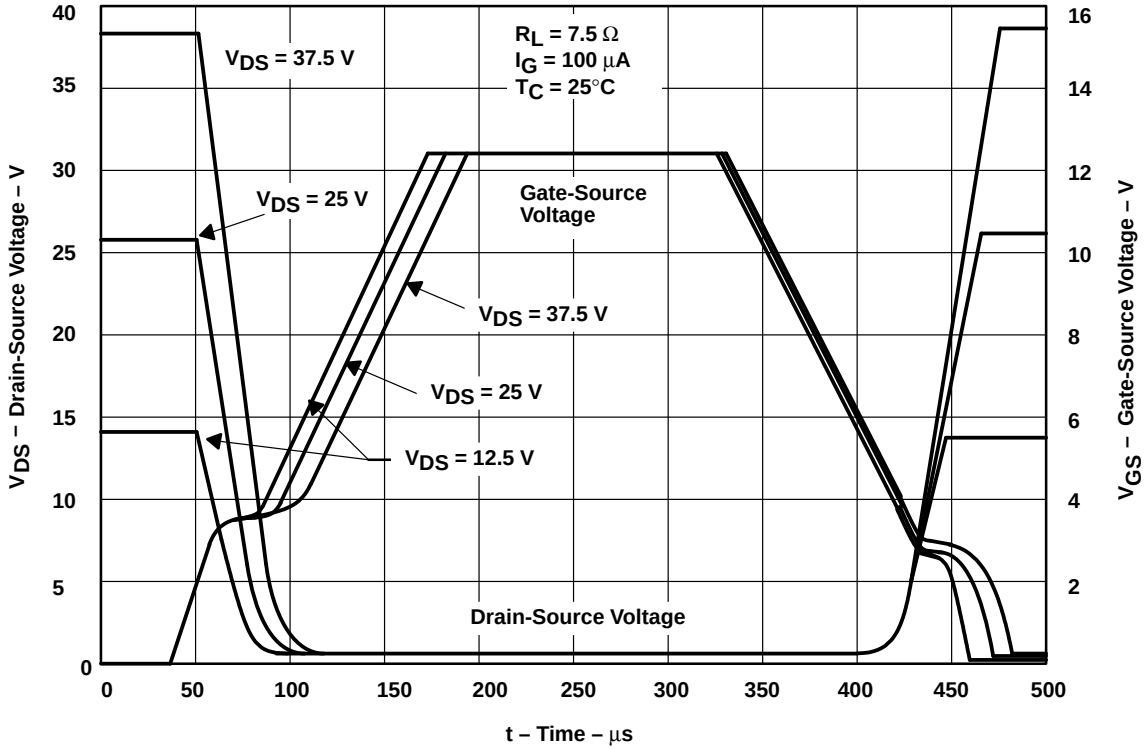


Figure 13. Resistive Switching Waveforms

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DRAIN-SOURCE VOLTAGE

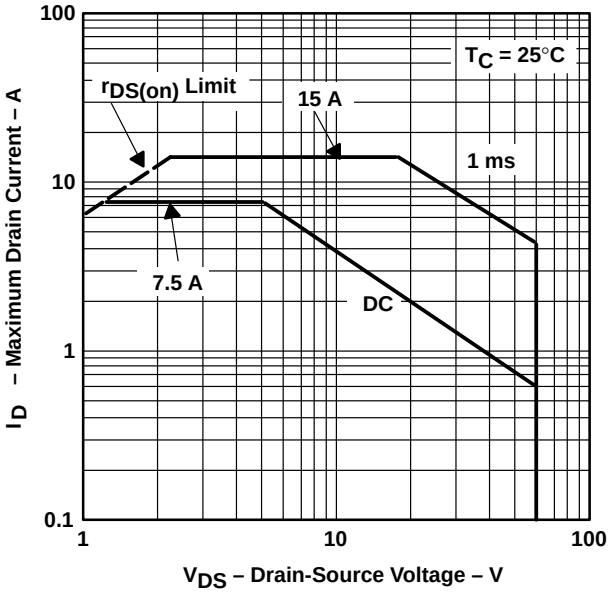


Figure 14

MAXIMUM PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

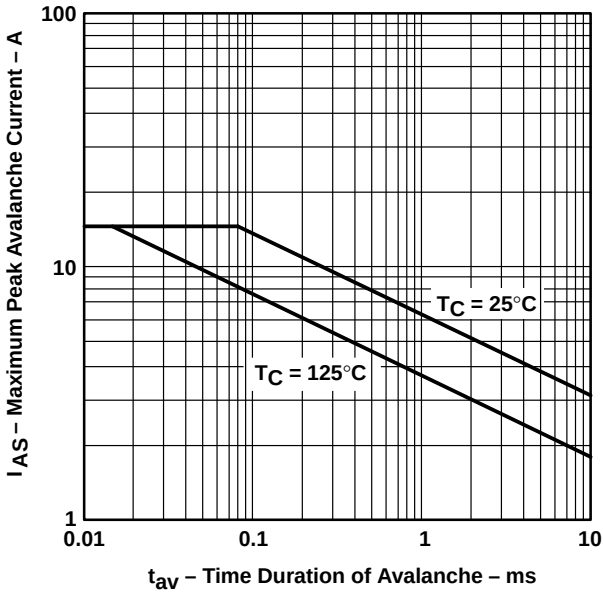
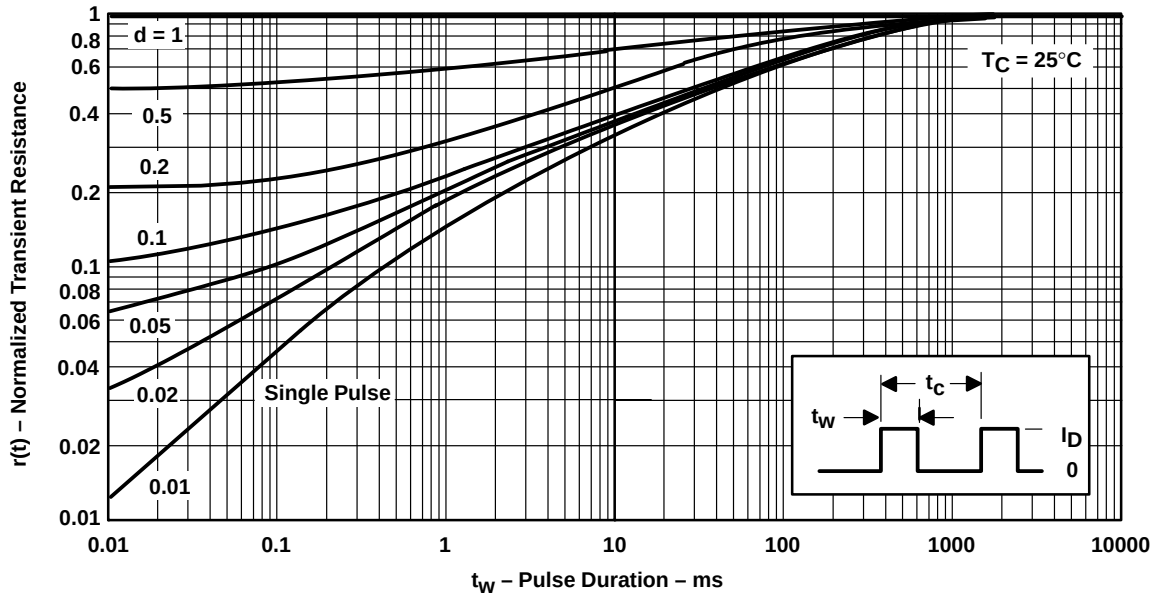


Figure 15

NORMALIZED TRANSIENT THERMAL IMPEDANCE vs SQUARE-WAVE PULSE DURATION



NOTES: $Z_{\theta JC}(t) = r(t) R_{\theta JC}$
t_W = pulse duration
t_C = period
d = duty cycle = t_W/t_C

Figure 16

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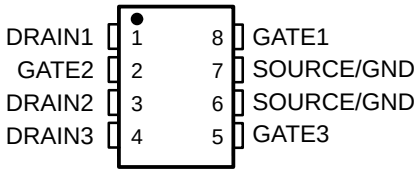
- **High-Voltage Outputs . . . 60 V**
- **Pulsed Current . . . 2.25 A Per Channel**
- **Fast Commutation Speed**
- **Direct Logic-Level Interface**

D PACKAGE
(TOP VIEW)

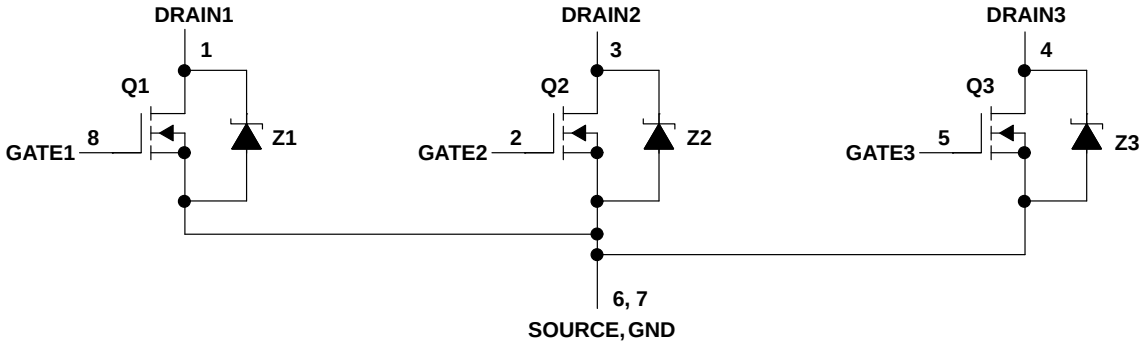


description

The TPIC2322L is a monolithic logic-level power DMOS array that consists of three electrically isolated N-channel enhancement-mode DMOS transistors configured with a common source and open drains.

The TPIC2322L is offered in a standard eight-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature range of –40°C to 125°C.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Gate-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage, V_{GS}	±20 V
Continuous drain current, each output, all outputs on, T_C = 25°C	0.75 A
Continuous source-to-drain diode current, T_C = 25°C	0.75 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	2.25 A
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figure 4)	30.4 mJ
Continuous total power dissipation at (or below) T_C = 25°C (see Figure 15)	0.95 W
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%.

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 μA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}, See Figure 5		1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain to GND breakdown voltage	Drain to GND current = 250 μA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 0.75 A, V_{GS} = 5 V, See Notes 2 and 3			0.45	0.53	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 0.75 A, V_{GS} = 0 See Notes 2 and 3 and Figure 12			0.85	1	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	μA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 16 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{SG} = 16 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	μA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 5 V, I_D = 0.75 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.6	0.7	Ω
			T_C = 125°C		0.94	1	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 0.5 A, See Notes 2 and 3 and Figure 9		0.75	0.9		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0, See Figure 11			115	145	pF
C_{oss}	Short-circuit output capacitance, common source				60	75	
C_{rss}	Short-circuit reverse transfer capacitance, common source				30	40	

NOTES: 2. Technique should limit T_J – T_C to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain diode characteristics, T_C = 25°C (see schematic diagram)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_F = 0.375 A, V_{DS} = 48 V, di/dt = 100 A/μs, See Figures 1 and 14		85		ns
Q_{RR}	Total diode charge			0.19		μC

resistive-load switching characteristics, T_C = 25°C

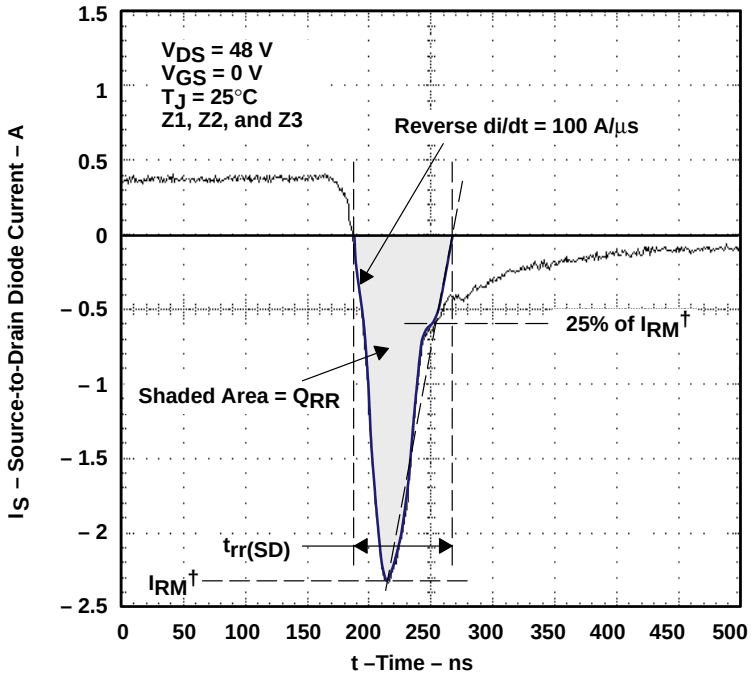
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 67 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		21	42	ns
$t_{d(off)}$	Turn-off delay time			26	52	
t_r	Rise time			14	28	
t_f	Fall time			13	26	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 0.375 A, V_{GS} = 5 V, See Figure 3		1.8	2.3	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.4	0.5	
Q_{gd}	Gate-to-drain charge			1.1	1.4	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance, See Note 4	All outputs with equal power		130		°C/W
$R_{\theta JP}$	Junction-to-pin thermal resistance			44		°C/W

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink.

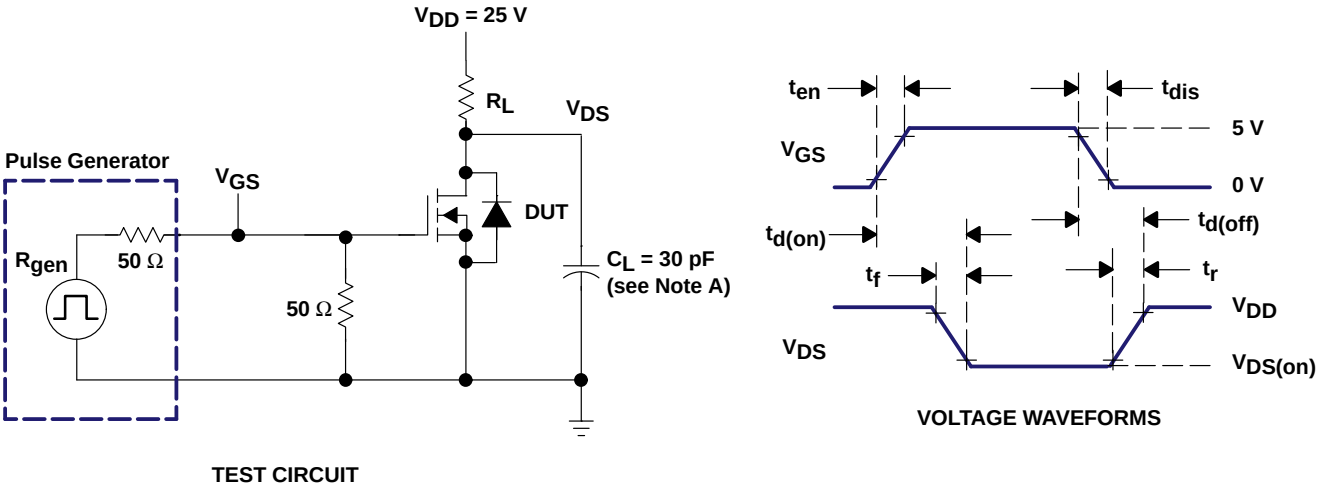
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

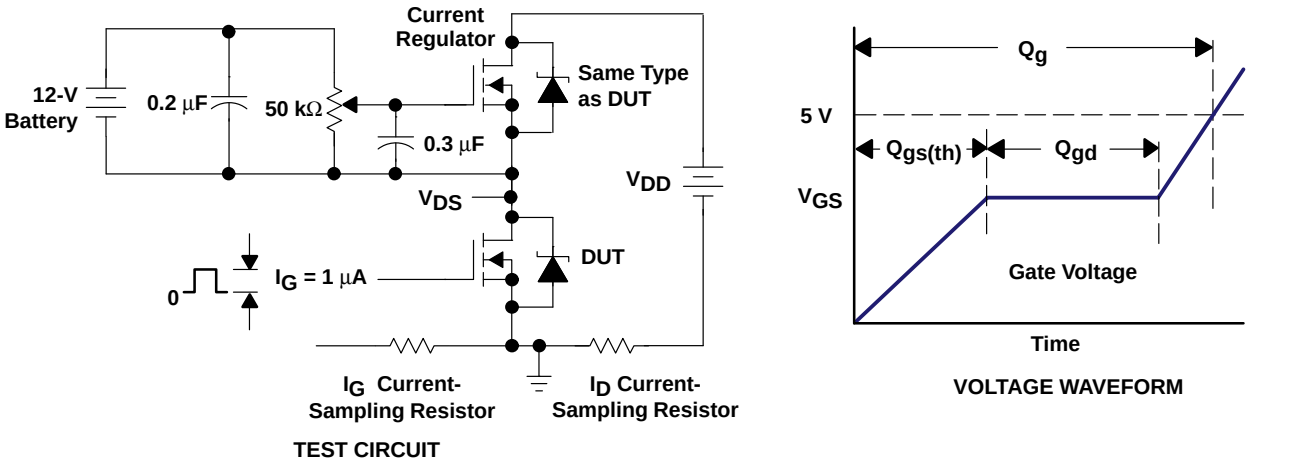
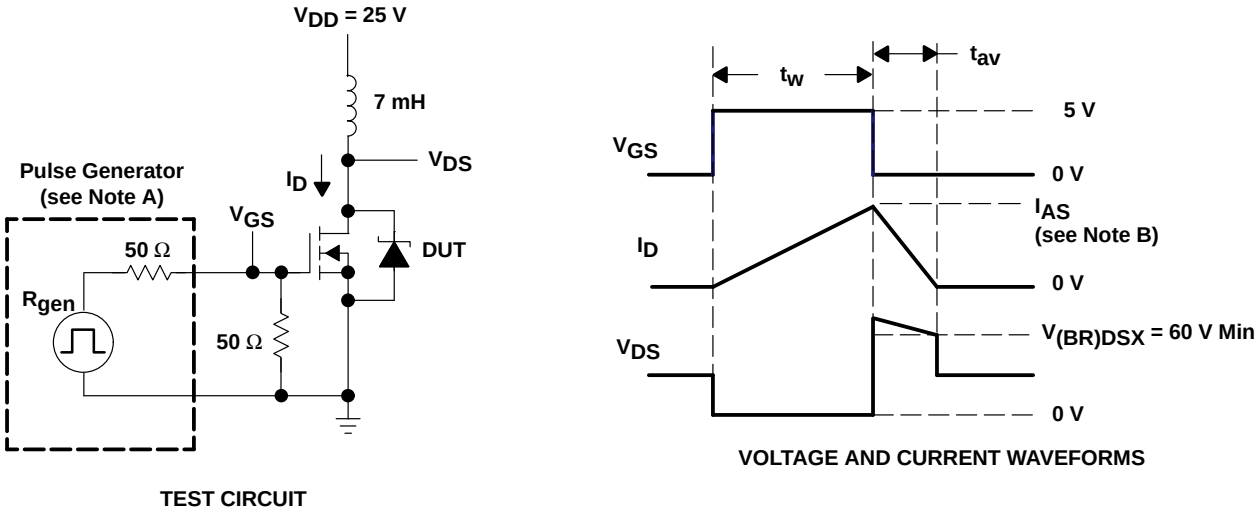


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 2.25$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 30.4$ mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

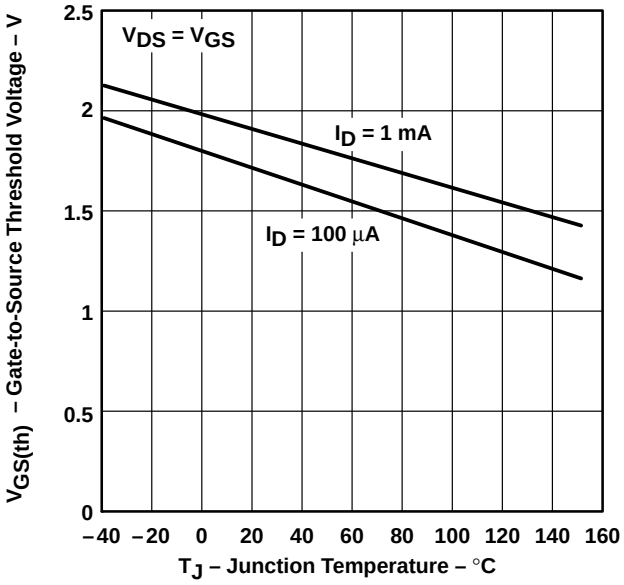


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

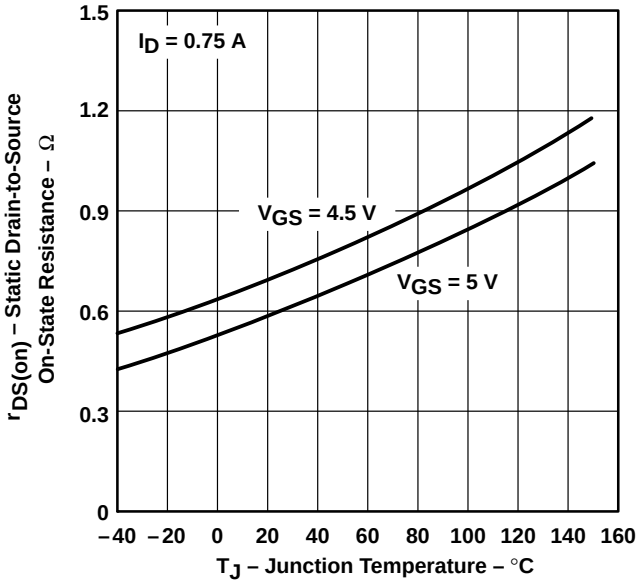


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

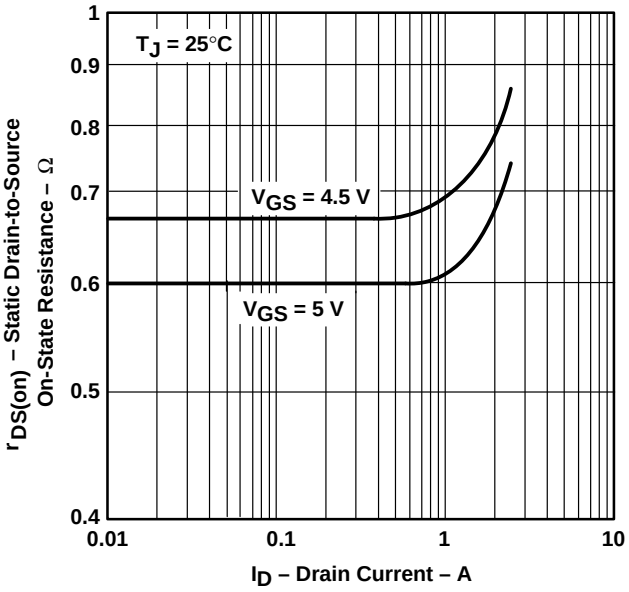


Figure 7

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

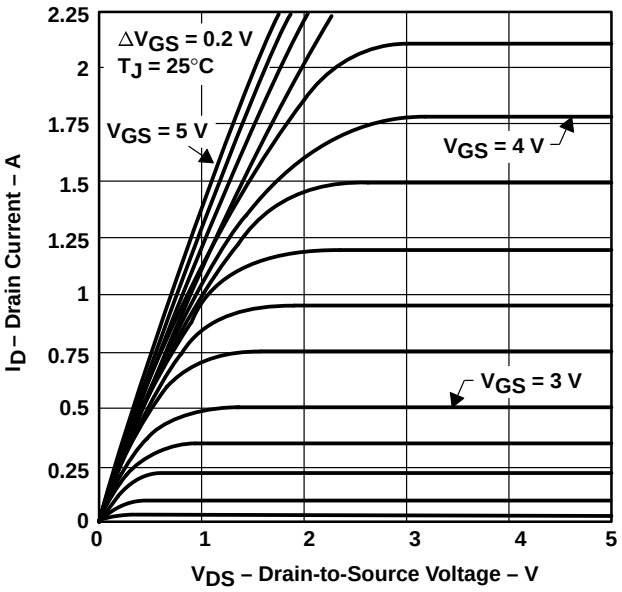


Figure 8

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

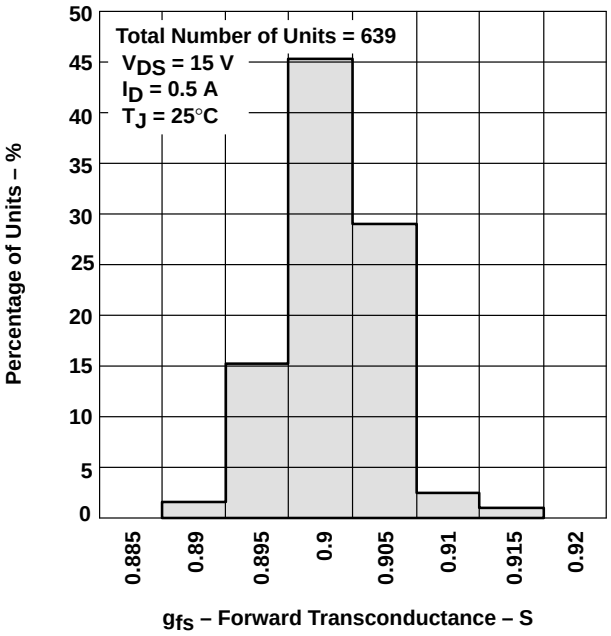


Figure 9

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

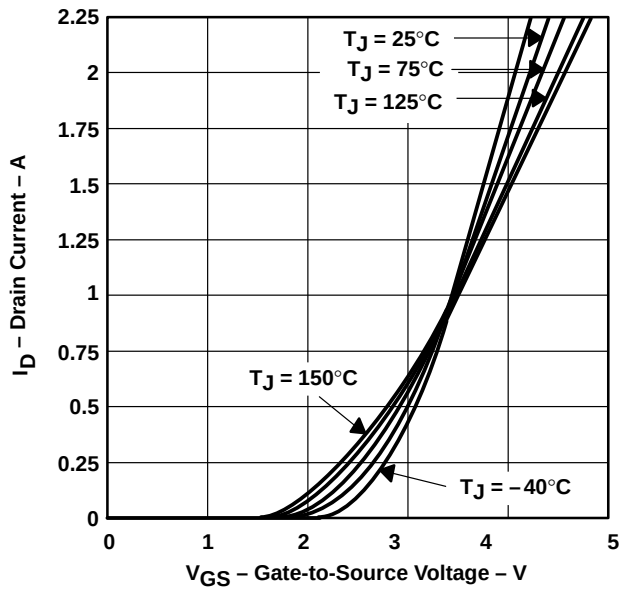


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

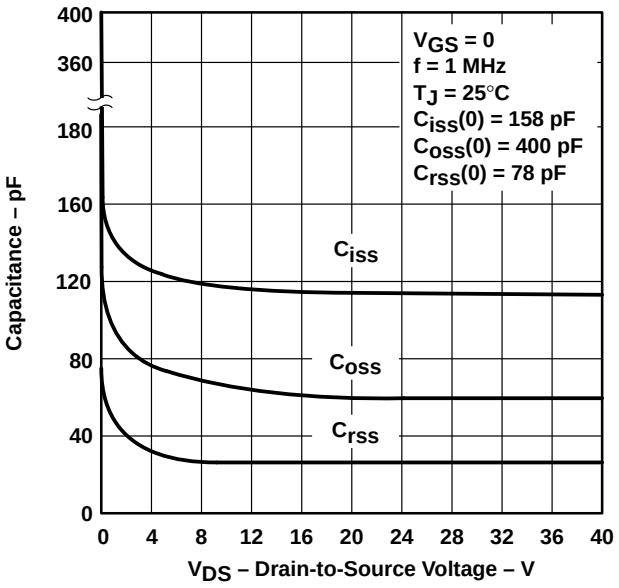


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

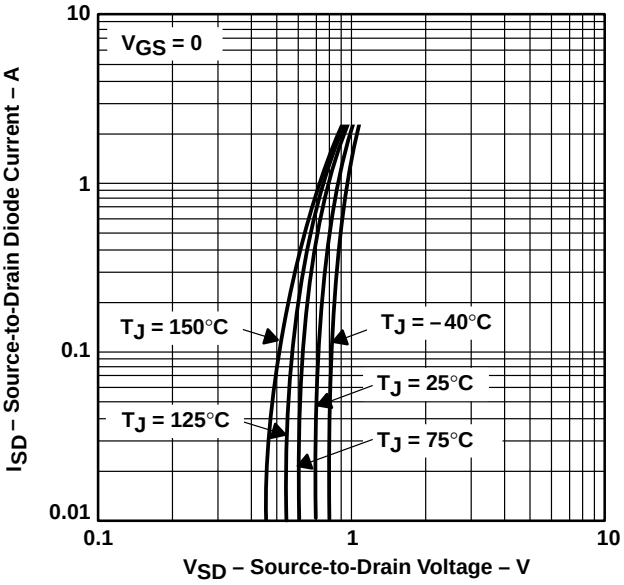


Figure 12

DRAIN-TO-SOURCE VOLTAGE AND GATE-TO-SOURCE VOLTAGE vs GATE CHARGE

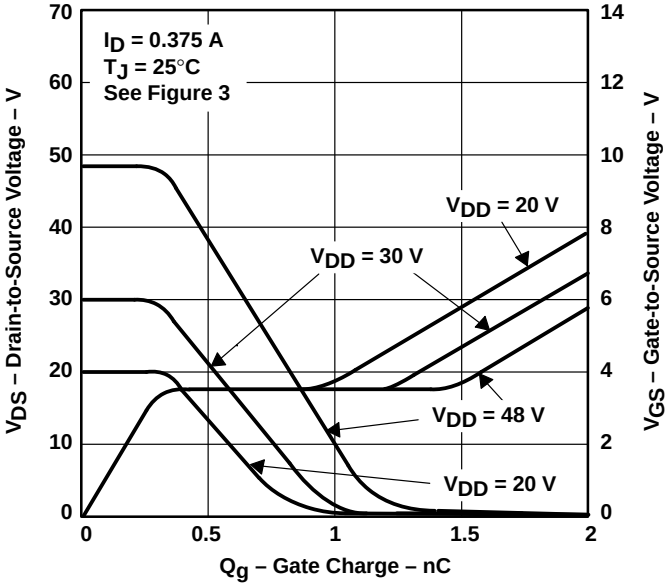


Figure 13

REVERSE-RECOVERY TIME vs REVERSE di/dt

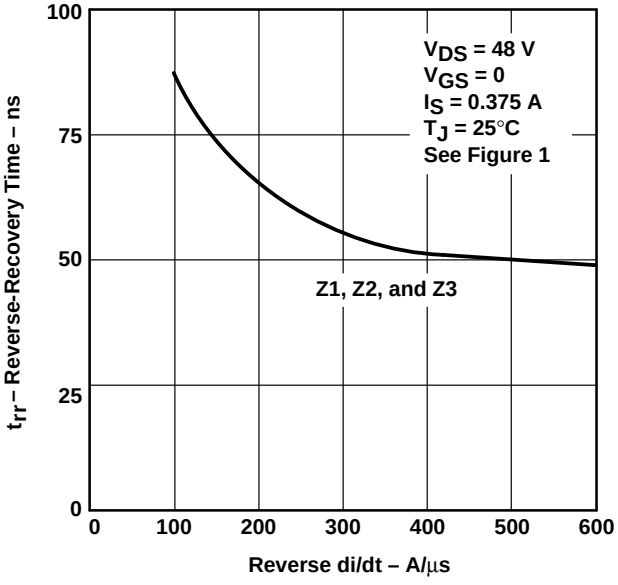
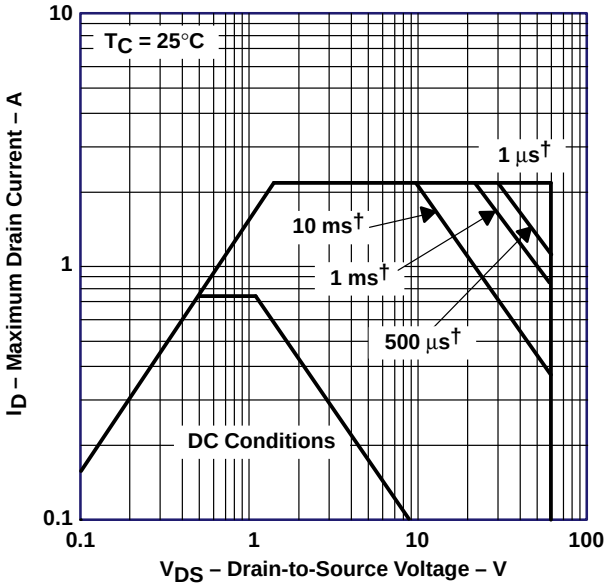


Figure 14

THERMAL INFORMATION

**MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE**



† Less than 2% duty cycle

Figure 15

**MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE**

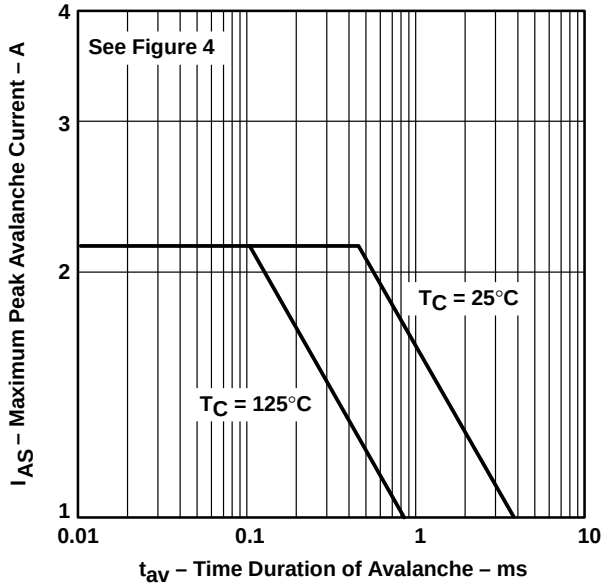
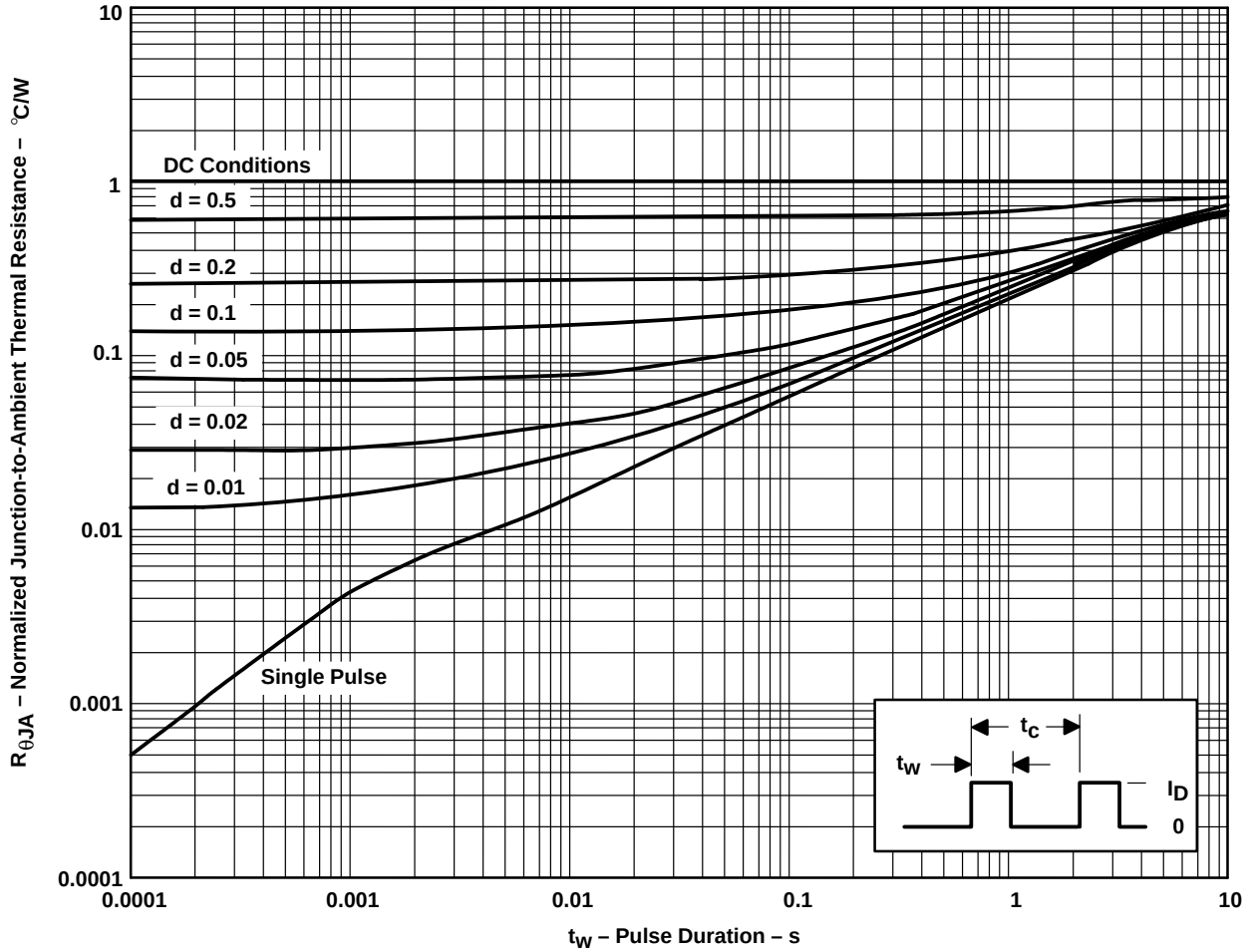


Figure 16

THERMAL INFORMATION

D PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



† Device mounted on FR4 printed-circuit board with no heat sink.

NOTES: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 17

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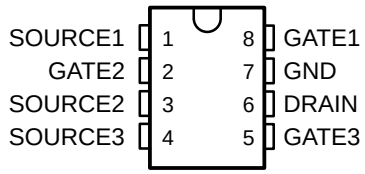
- **Low $r_{DS(on)}$ . . . 0.6 Ω Typ**
- **High-Voltage Outputs . . . 60 V**
- **Pulsed Current . . . 2.25 A Per Channel**
- **Fast Commutation Speed**
- **Direct Logic-Level Interface**

D PACKAGE
(TOP VIEW)

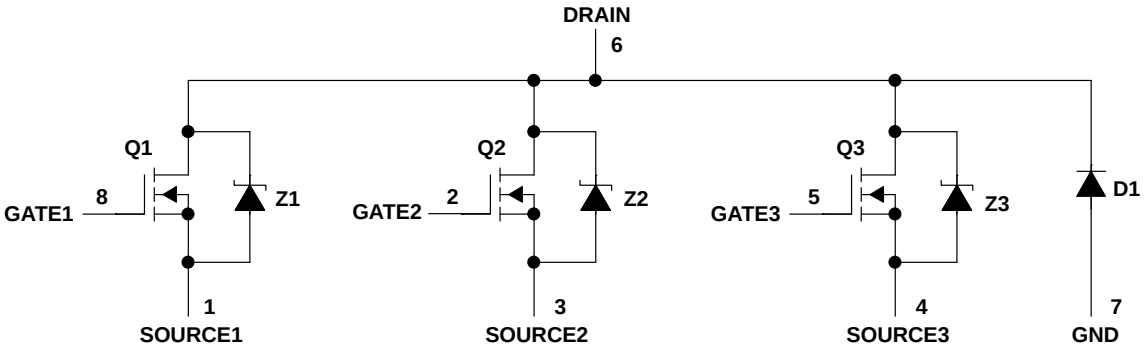


description

The TPIC3322L is a monolithic logic-level power DMOS transistor array that consists of three isolated N-channel enhancement-mode DMOS transistors configured with a common drain and open sources.

The TPIC3322L is offered in a standard 8-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature range of –40°C to 125°C.

schematic diagram



absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage, V_{GS}	±20 V
Continuous drain current, each output, all outputs on, T_C = 25°C	0.75 A
Continuous source-to-drain diode current, T_C = 25°C	0.75 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	2.25 A
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figure 4)	19 mJ
Continuous total power dissipation at (or below) T_C = 25°C (see Figure 15)	0.95 W
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%.

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 μA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}		1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1)	Drain-to-GND current = 250 μA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 0.75 A, V_{GS} = 5 V, See Notes 2 and 3			0.45	0.53	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 0.75 A, See Notes 2 and 3			1.8		V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 0.75 A, V_{GS} = 0, See Notes 2 and 3 and Figure 12			0.85	1	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	μA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 16 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{SG} = 16 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	μA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 5 V, I_D = 0.75 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.6	0.7	Ω
			T_C = 125°C		0.94	1	
g_{fs}	Forward transconductance	V_{DS} = 10 V, I_D = 0.5 A, See Notes 2 and 3 and Figure 9		0.75	0.9		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0, See Figure 11			115	145	pF
C_{oss}	Short-circuit output capacitance, common source				60	75	
C_{rss}	Short-circuit reverse transfer capacitance, common source				30	40	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{rr(SD)}$	Reverse-recovery time	I_S = 0.375 A, di/dt = 100 A/μs, See Figures 1 and 14 V_{GS} = 0, V_{DS} = 48 V,	Z1, Z2, Z3		30		ns
			D1		85		
Q_{RR}	Total diode charge		Z1, Z2, Z3		0.03		μC
			D1		0.19		

resistive-load switching characteristics, T_C = 25°C

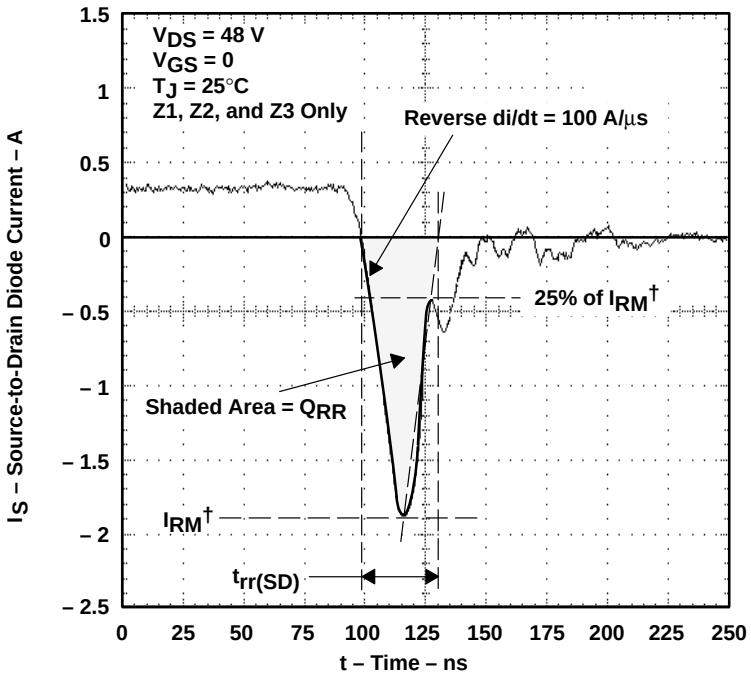
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, t_{f1} = 10 ns,	R_L = 67 Ω, See Figure 2	t_{r1} = 10 ns,		8	16	ns
$t_{d(off)}$	Turn-off delay time					12	24	
t_{r2}	Rise time					14	28	
t_{f2}	Fall time					13	26	
Q_g	Total gate charge	V_{DS} = 48 V, See Figure 3	I_D = 0.375 A,	V_{GS} = 5 V,		1.8	2.3	nC
$Q_{gs(th)}$	Threshold gate-to-source charge					0.4	0.5	
Q_{gd}	Gate-to-drain charge					1.1	1.4	
L_D	Internal drain inductance					5		nH
L_S	Internal source inductance					5		
R_g	Internal gate resistance					0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance, See Note 4	All outputs with equal power		130		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			44		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink.

PARAMETER MEASUREMENT INFORMATION

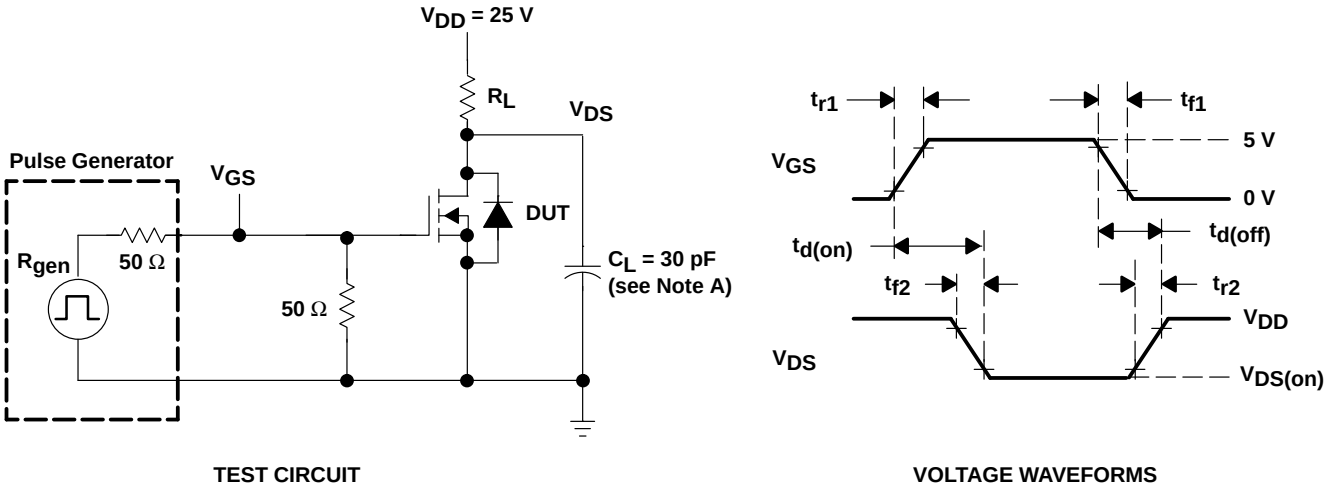


† I_{RM} = maximum recovery current

NOTE A. The above waveform represents D1 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

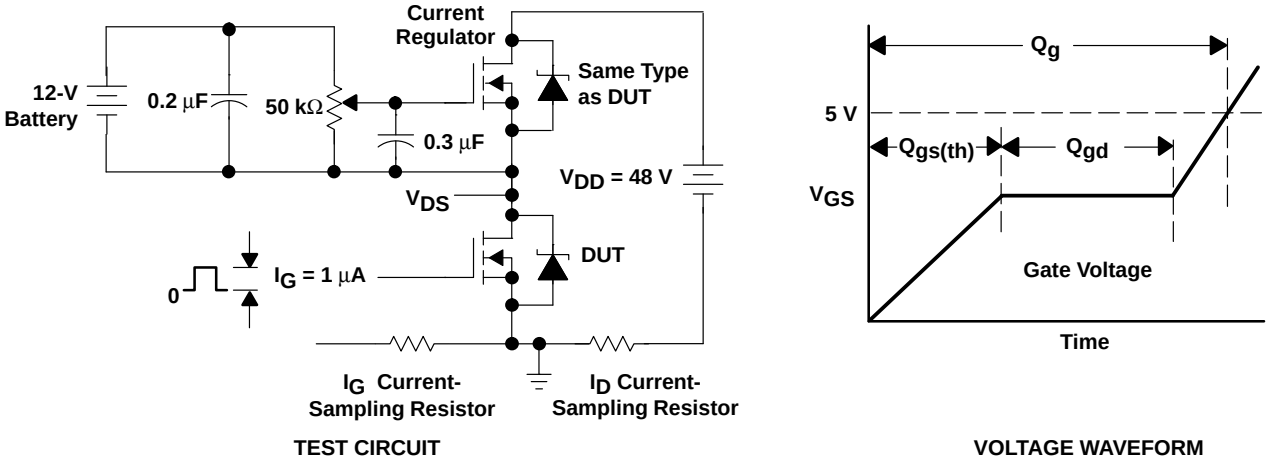
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

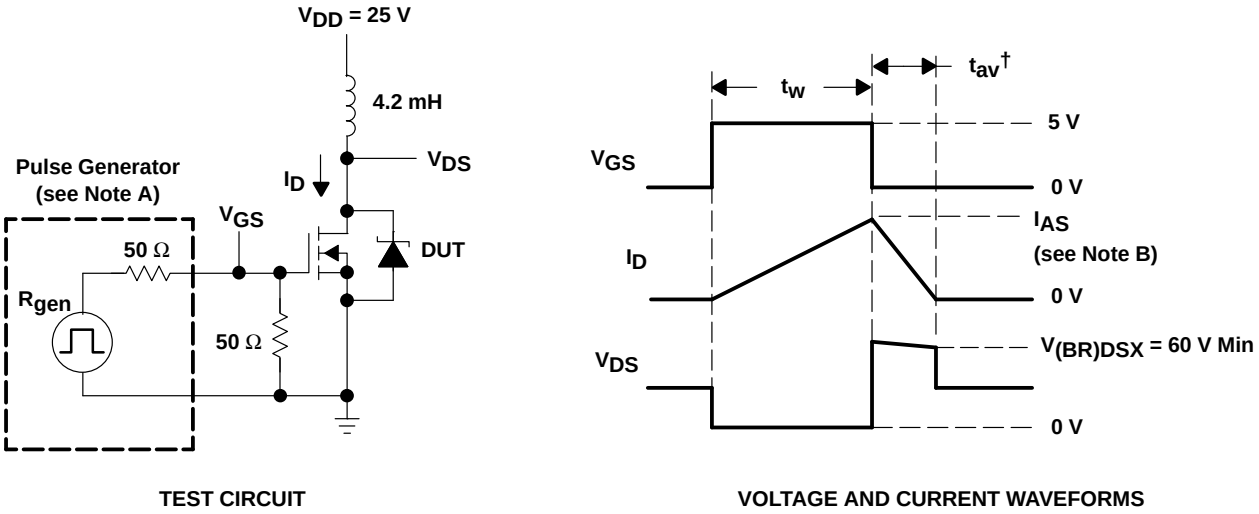
Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORM

Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT **VOLTAGE AND CURRENT WAVEFORMS**

† Non-JEDEC symbol for avalanche time

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 2.25$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 19$ mJ, where t_{av} = avalanche time.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

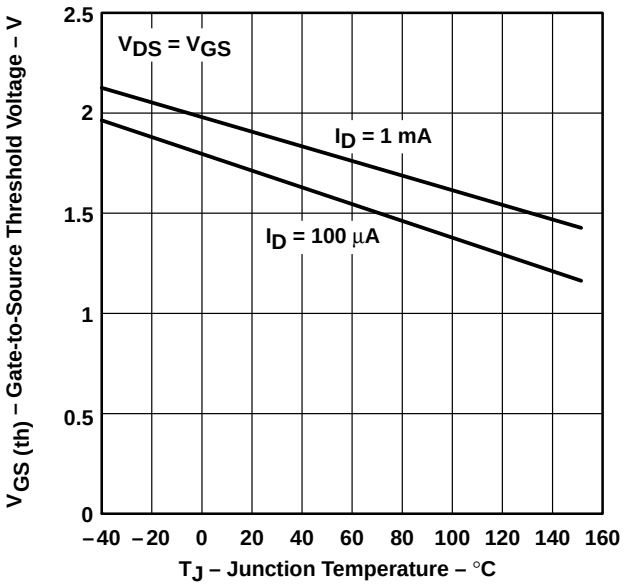


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

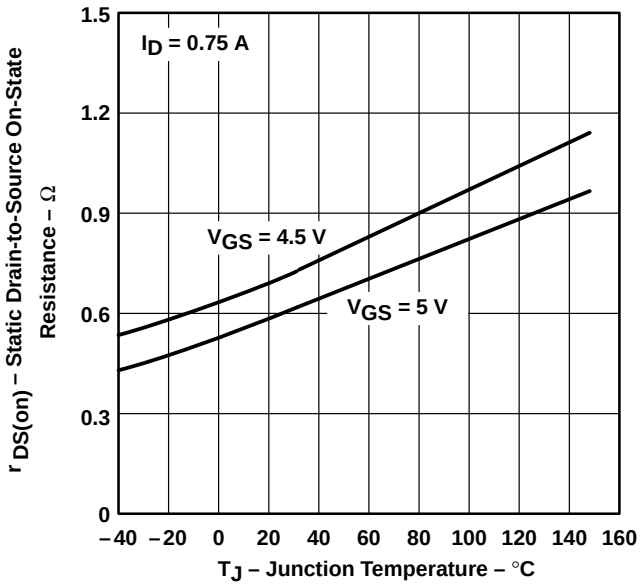


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

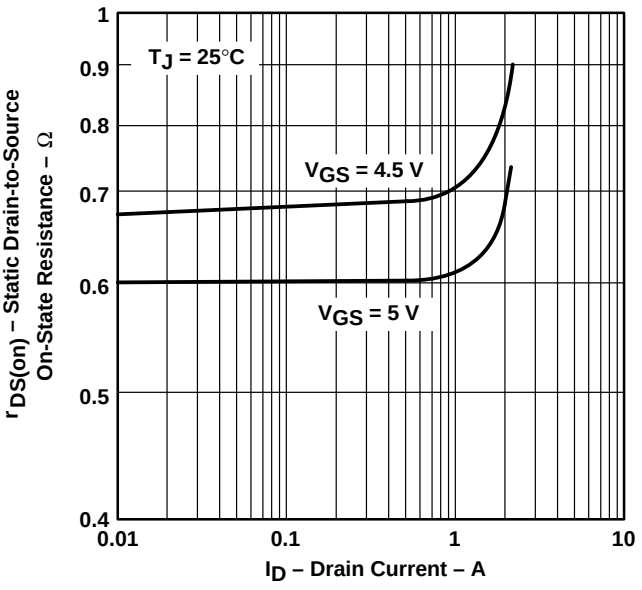


Figure 7

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

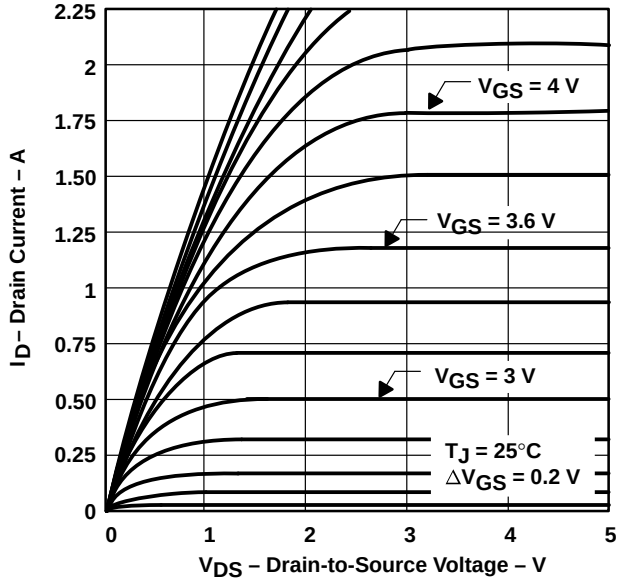


Figure 8

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

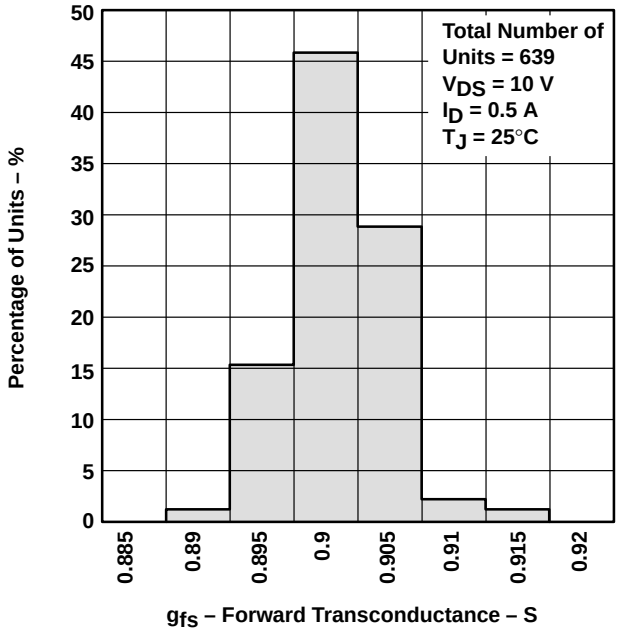


Figure 9

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

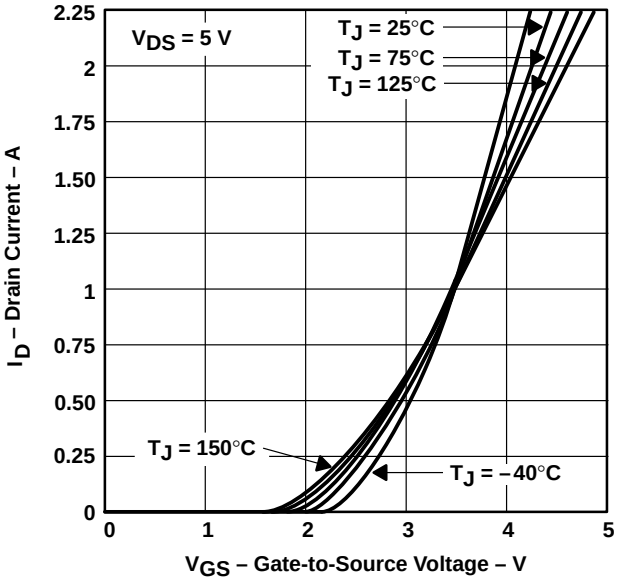


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

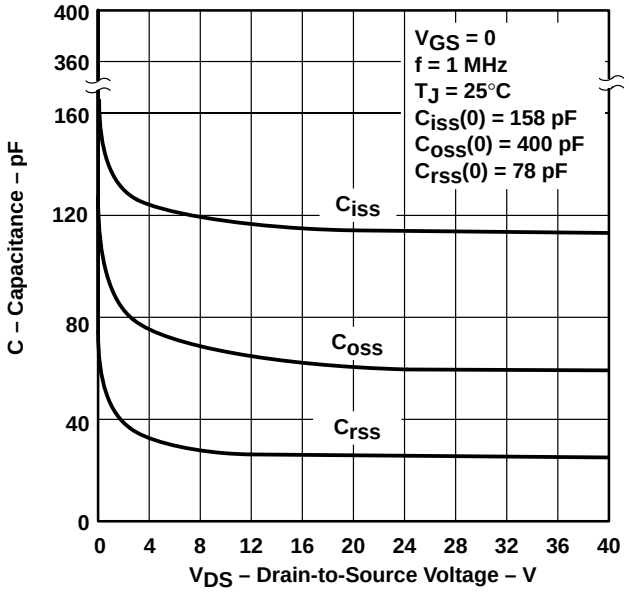


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

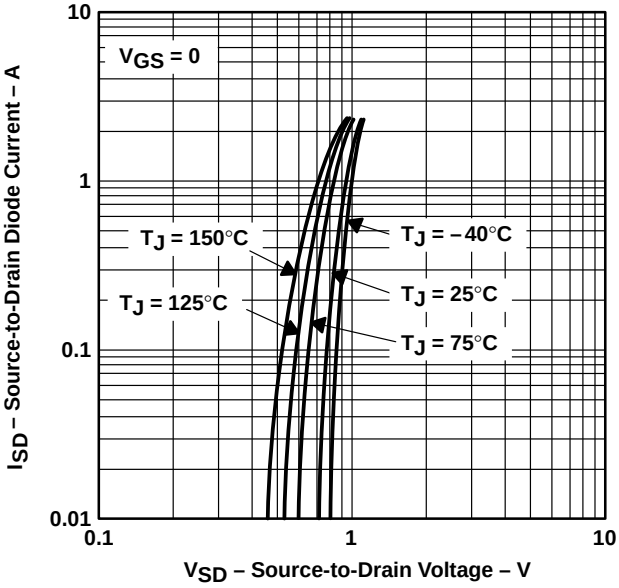


Figure 12

DRAIN-TO-SOURCE AND GATE-TO-SOURCE VOLTAGE vs GATE CHARGE

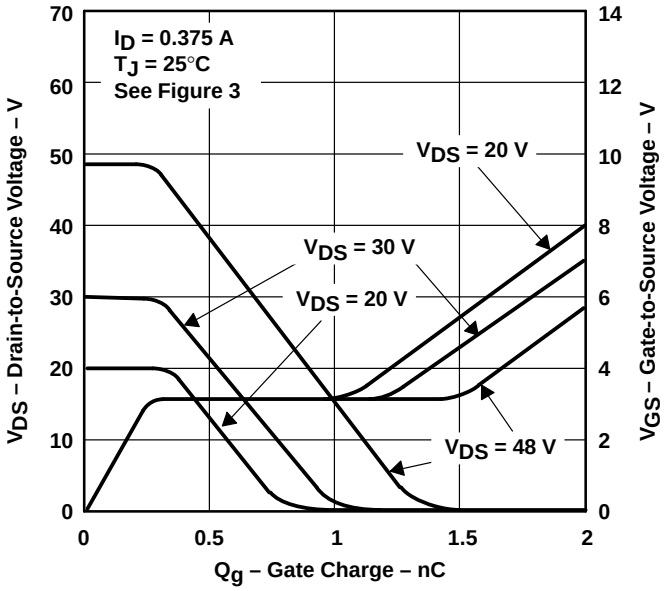


Figure 13

REVERSE-RECOVERY TIME vs REVERSE di/dt

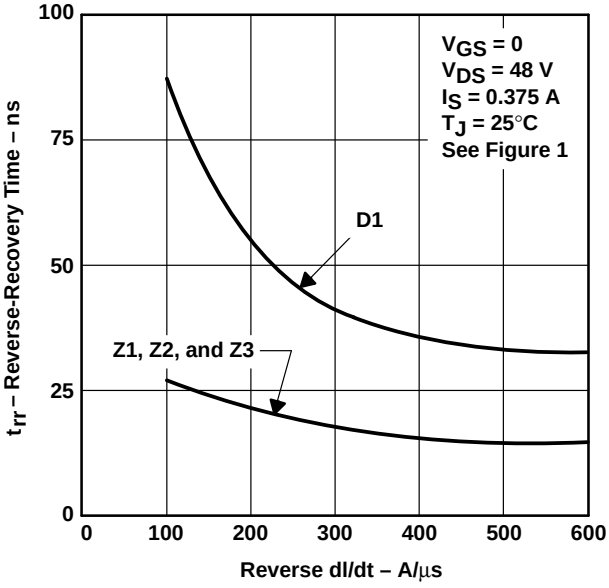
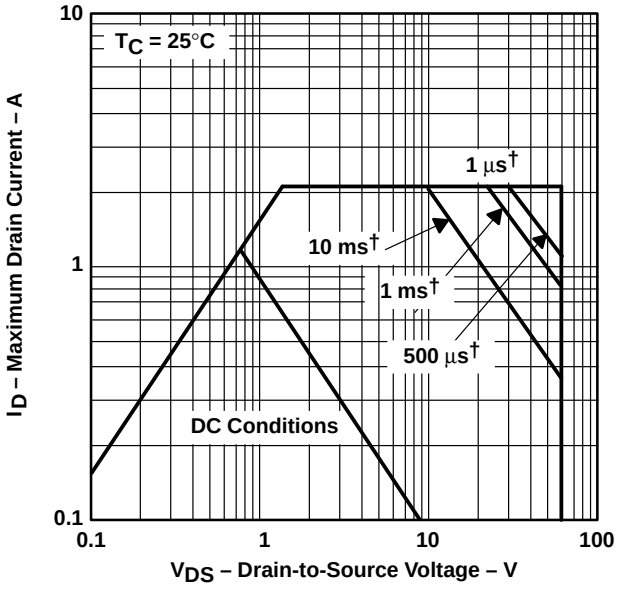


Figure 14

THERMAL INFORMATION

**MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE**



† Less than 2% duty cycle

Figure 15

**MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE**

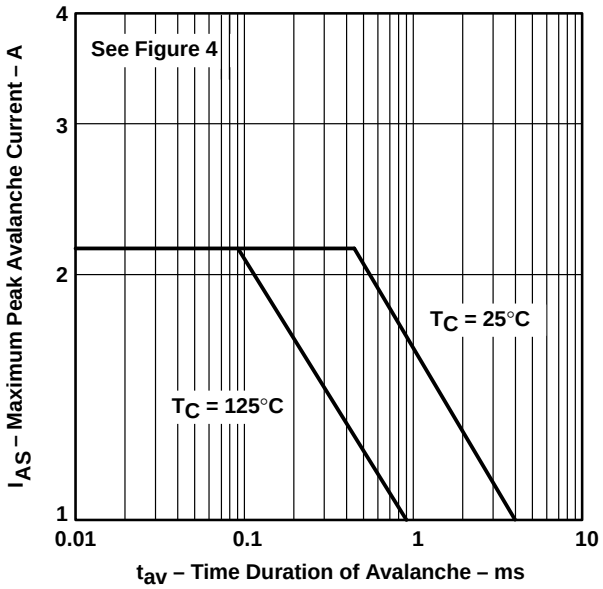
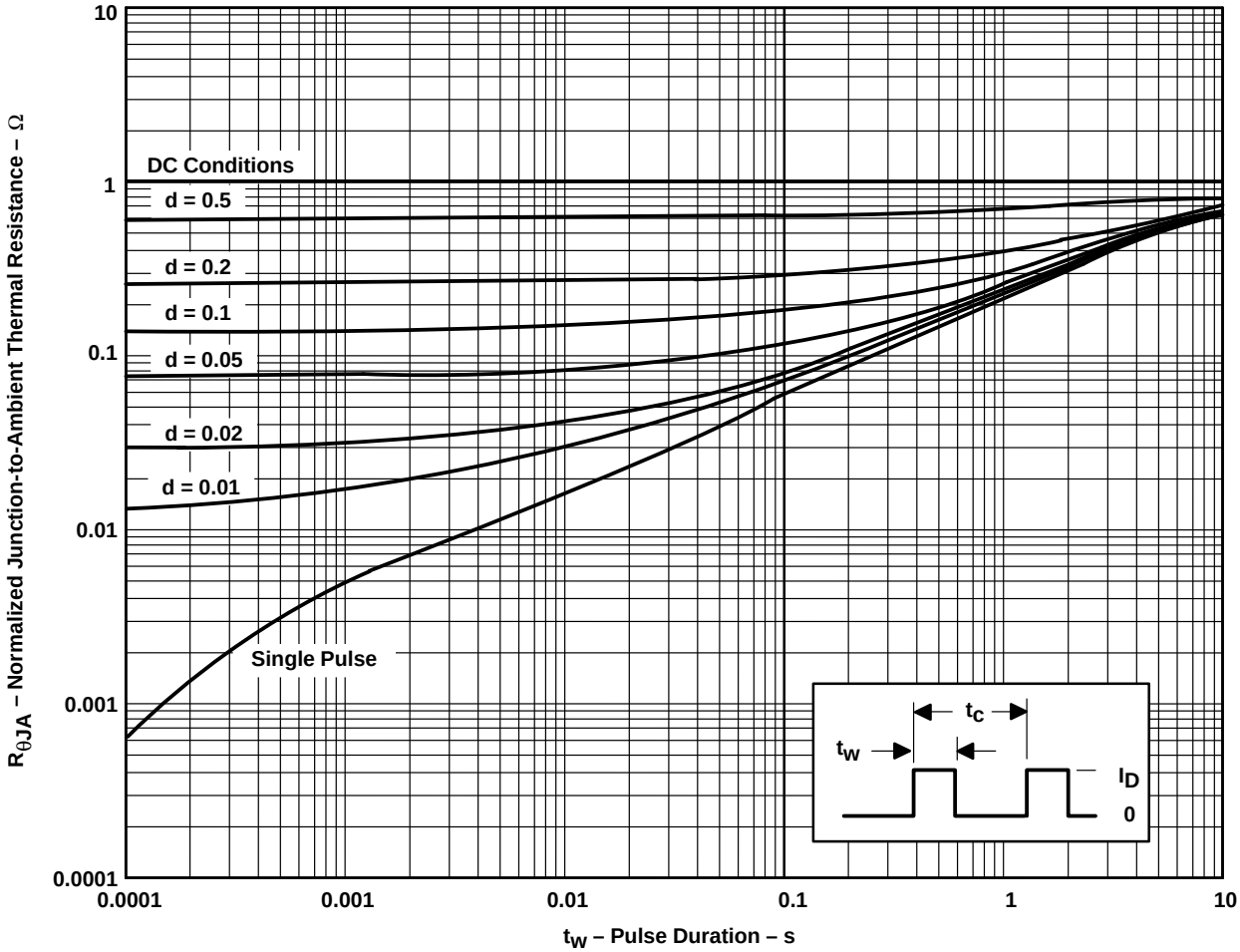


Figure 16

THERMAL INFORMATION

NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE† vs PULSE DURATION



† Device mounted on FR4 printed-circuit board with no heat sink.

NOTE A: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 17

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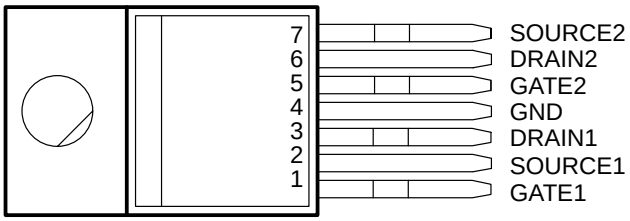
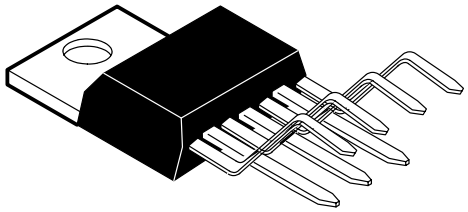
- **Two 7.5-A Independent Output Channels, Continuous Current Per Channel**
- **Low $r_{DS(on)}$ . . . 0.09 Ω Typical**
- **Output Voltage . . . 60 V**
- **Pulsed Current . . . 15 A Per Channel**
- **Avalanche Energy . . . 120 mJ**

KV PACKAGE
(TOP VIEW)





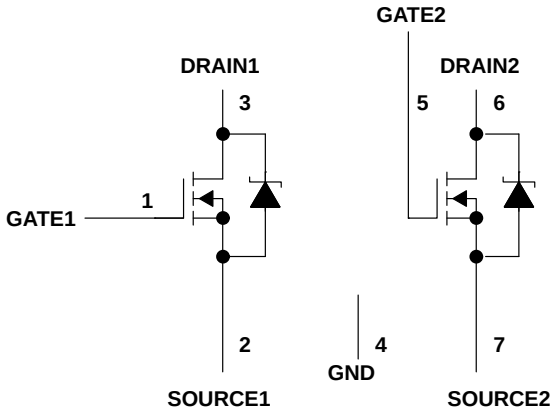
To ensure correct device operation, the source and the drain of the same transistor cannot simultaneously be taken below GND.

The tab is electrically connected to GND.

description

The TPIC5201 is a power monolithic DMOS array that consists of dual independent N-channel enhancement-mode DMOS transistors.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)

Drain-source voltage, V_{DS}	60 V
Source-GND voltage	60 V
Drain-GND voltage	60 V
Gate-source voltage, V_{GS}	±20 V
Continuous source-drain diode current	7.5 A
Pulsed drain current, each output, all outputs on, I_D (see Note 1)	15 A
Continuous drain current, each output, all outputs on	7.5 A
Single-pulse avalanche energy, E_{AS} (see Figure 4)	120 mJ
Continuous power dissipation at (or below) T_A = 25°C (see Note 2)	2 W
Continuous power dissipation at (or below) T_C = 75°C, all outputs on (see Note 2)	31 W
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range, T_{stg}	–40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Pulse duration = 10 ms, duty cycle = 6%
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16 mW/°C. For operation above 75°C case temperature, and with all outputs conducting, derate linearly at the rate of 0.42 W/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded.

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)DS}$	Drain-source breakdown voltage	I_D = 1 µA, V_{GS} = 0			60			V
V_{TGS}	Gate-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}			1.2	1.75	2.4	V
$V_{DS(on)}$	Drain-source on-state voltage	I_D = 7.5 A, V_{GS} = 15 V, See Notes 3 and 4				0.68	0.94	V
V_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{DS} = 0	T_C = 25°C			0.07	1	µA
			T_C = 125°C			1.3	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 20 V, V_{DS} = 0				10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{GS} = –20 V, V_{DS} = 0				10	100	nA
$r_{DS(on)}$	Static drain-source on-state resistance	V_{GS} = 15 V, I_D = 7.5 A, See Notes 3 and 4 and Figures 5 and 6	T_C = 25°C			0.09	0.125	Ω
			T_C = 125°C			0.15	0.21	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 5 A, See Notes 3 and 4			2.5	4.7		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 300 kHz				490		pF
C_{oss}	Short-circuit output capacitance, common source					285		
C_{rss}	Short-circuit reverse transfer capacitance, common source					90		

NOTES: 3. Technique should limit $T_J – T_C$ to 10°C maximum.
4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{SD}	Forward on voltage	I_S = 7.5 A, di/dt = 100 A/µs, See Figure 1	V_{GS} = 0, V_{DS} = 48 V,		0.8	1.3	V
t_{rr}	Reverse-recovery time				200		ns
Q_{RR}	Total source-drain diode charge				1.5		µC

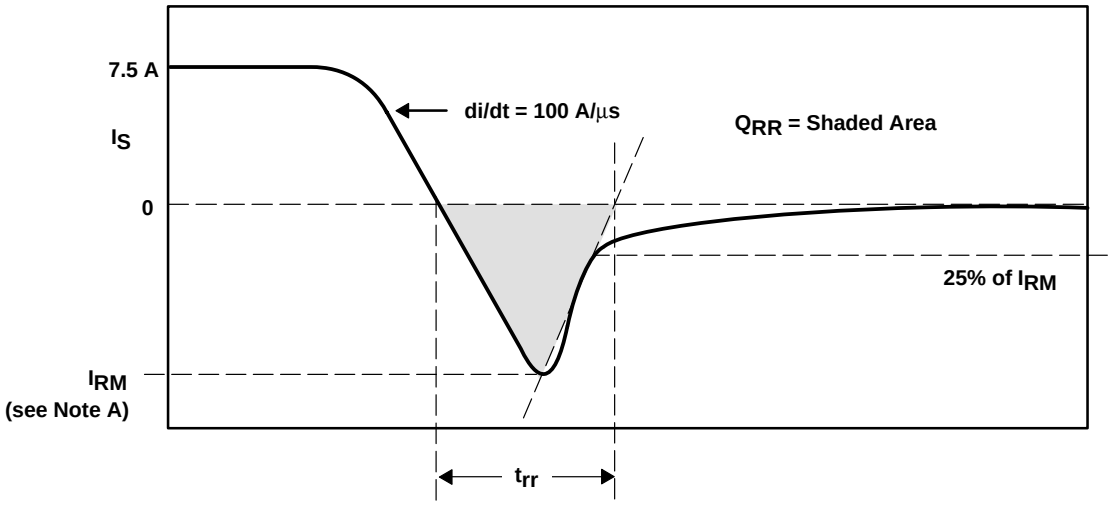
resistive-load switching characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, t_{dis} = 10 ns,	R_L = 6.7 Ω, See Figure 2	t_{en} = 10 ns,		12		ns
t_r	Rise time					43		
$t_{d(off)}$	Turn-off delay time					100		
t_f	Fall time					5		
Q_g	Total gate charge	V_{DD} = 48 V, See Figure 3	I_D = 2.5 A,	V_{GS} = 15,		13.6	18	nC
Q_{gs}	Gate-source charge					8.3	11	
Q_{gd}	Gate-drain charge					5.3	7	
L_D	Internal drain inductance					7		nH
L_S	Internal source inductance					7		

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	All outputs with equal power			62.5	°C/W
$R_{θJC}$	Junction-to-case thermal resistance	All outputs with equal power			2.4	°C/W
		One output dissipating power			3.3	°C/W

PARAMETER MEASUREMENT INFORMATION



NOTE A: I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveforms of Source-Drain Diode

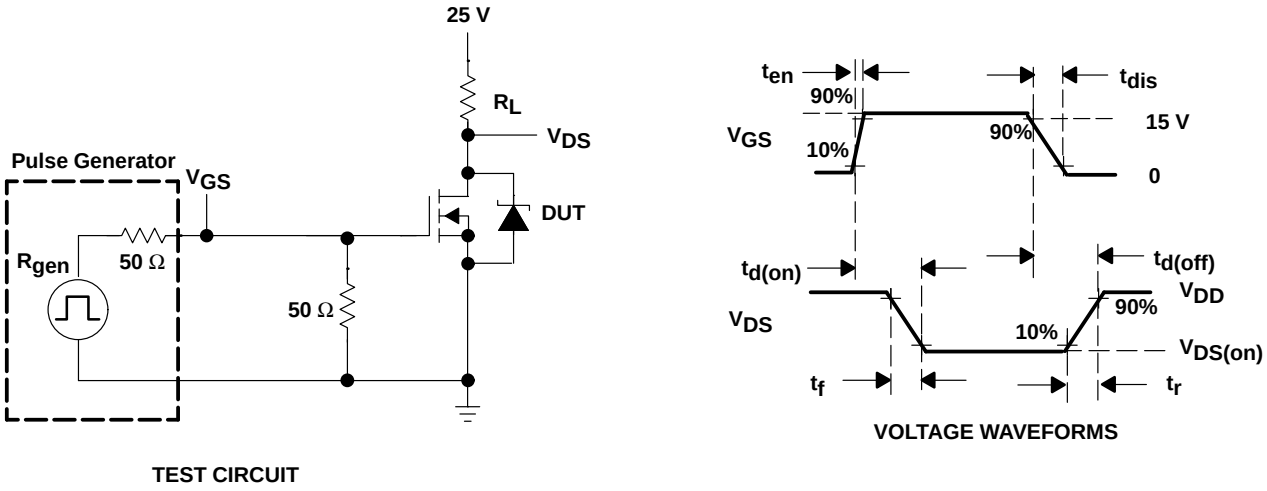


Figure 2. Resistive Switching

PARAMETER MEASUREMENT INFORMATION

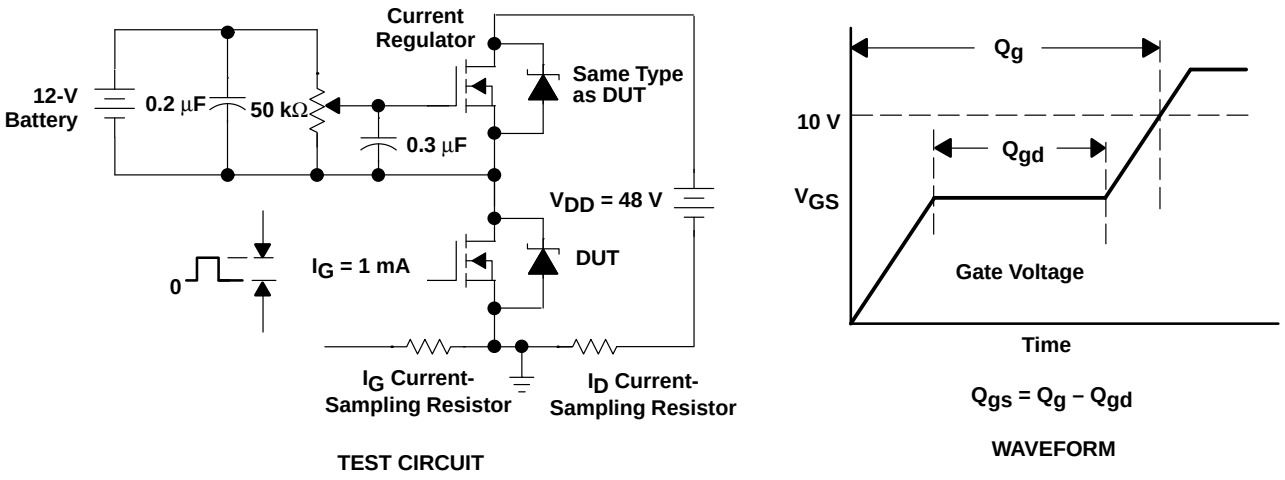
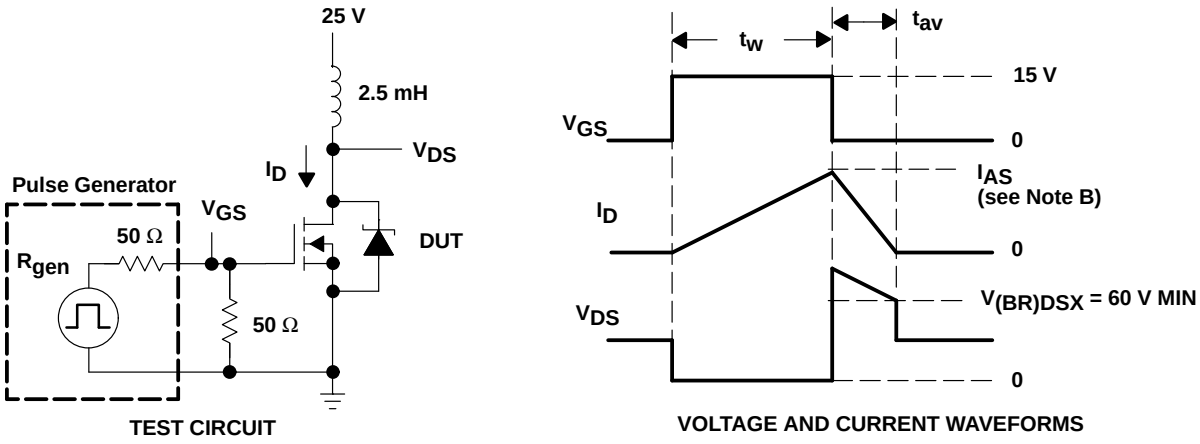


Figure 3. Gate Charge Test Circuit and Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_W) is increased until peak current $I_{AS} = 7.5$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 120$ mJ min.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs CASE TEMPERATURE

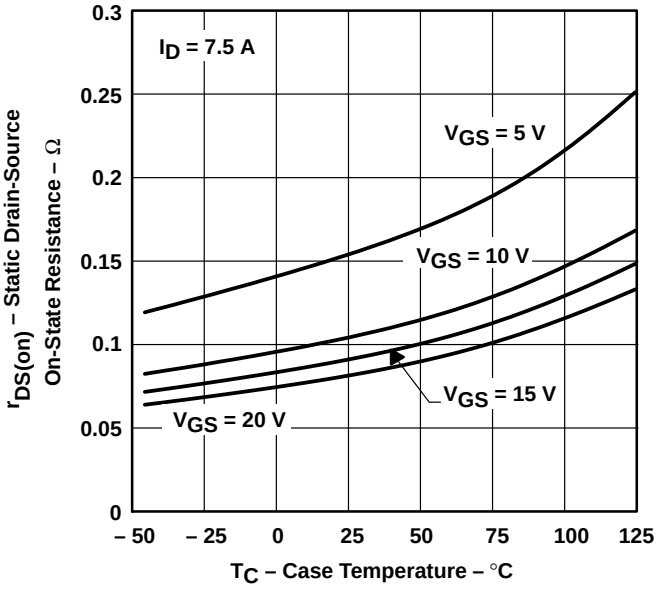


Figure 5

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

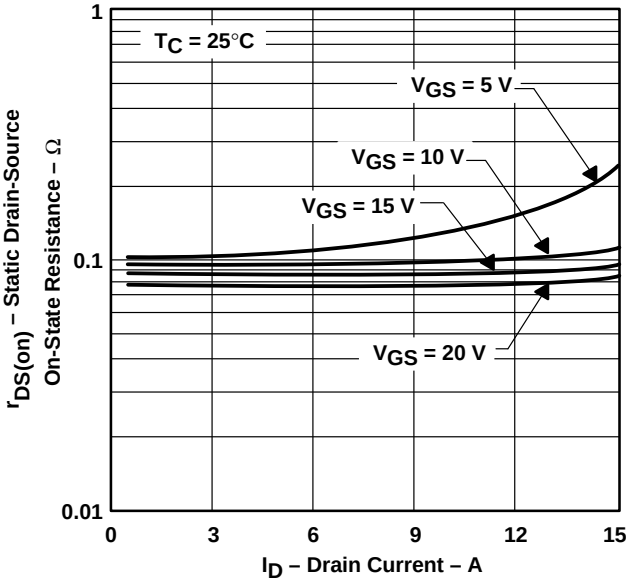


Figure 6

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

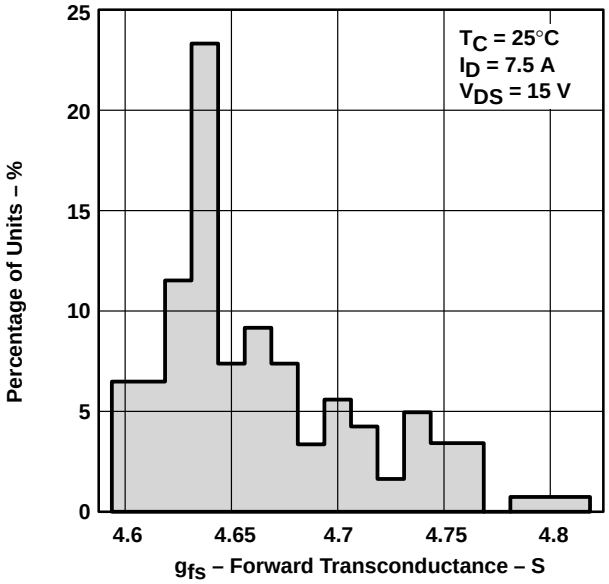


Figure 7

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

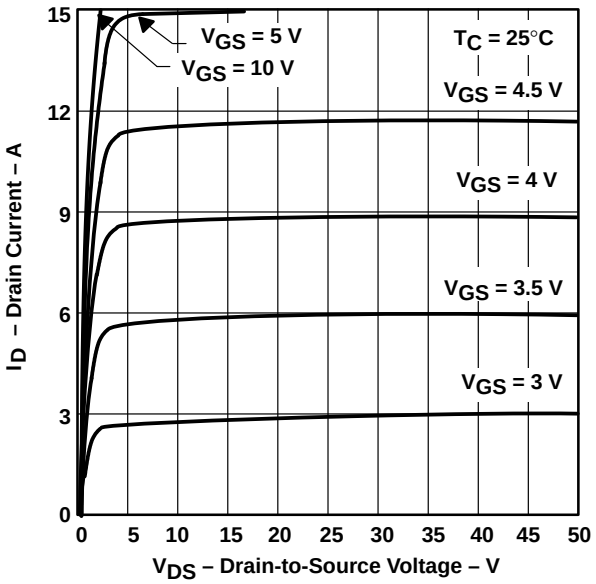


Figure 8

TYPICAL CHARACTERISTICS

GATE-SOURCE THRESHOLD VOLTAGE vs CASE TEMPERATURE

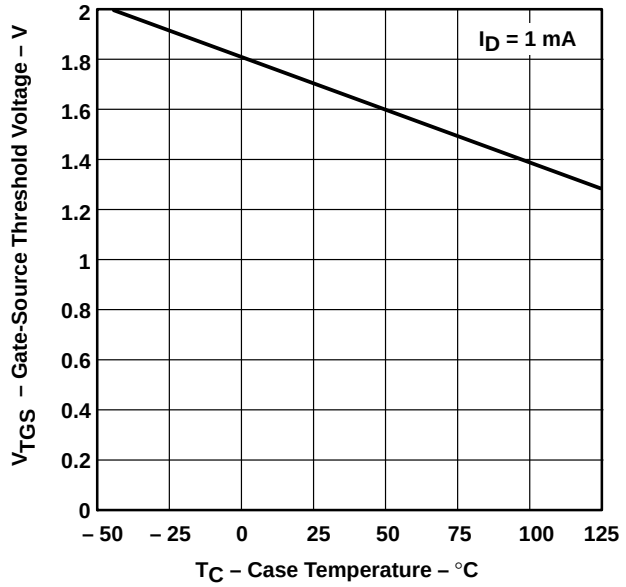


Figure 9

SOURCE-DRAIN DIODE CURRENT vs SOURCE-DRAIN VOLTAGE

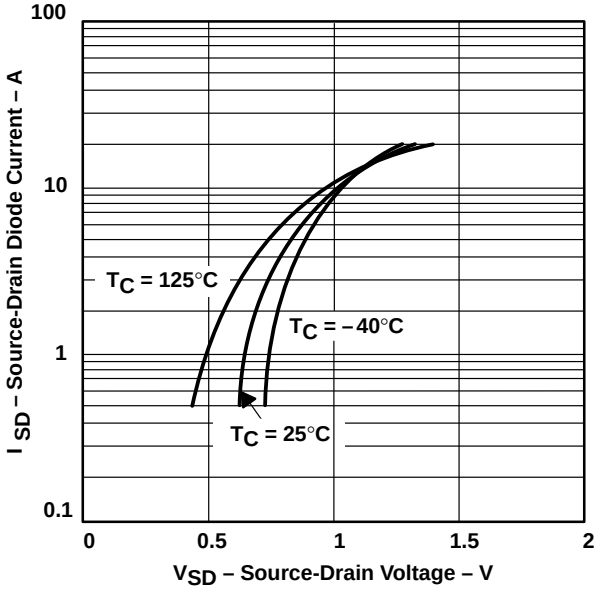


Figure 10

GATE-SOURCE VOLTAGE vs GATE CHARGE

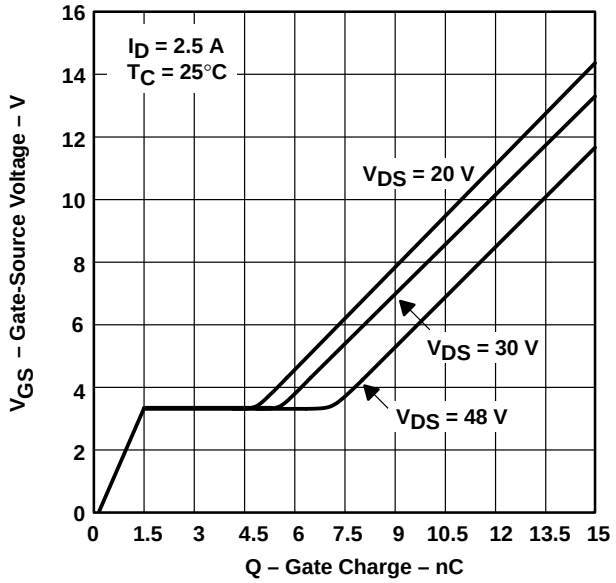


Figure 11

REVERSE-RECOVERY TIME vs REVERSE di/dt

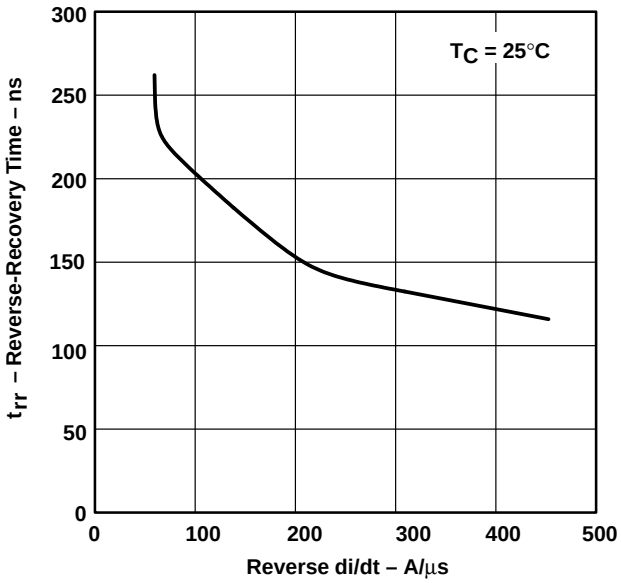


Figure 12

TYPICAL CHARACTERISTICS

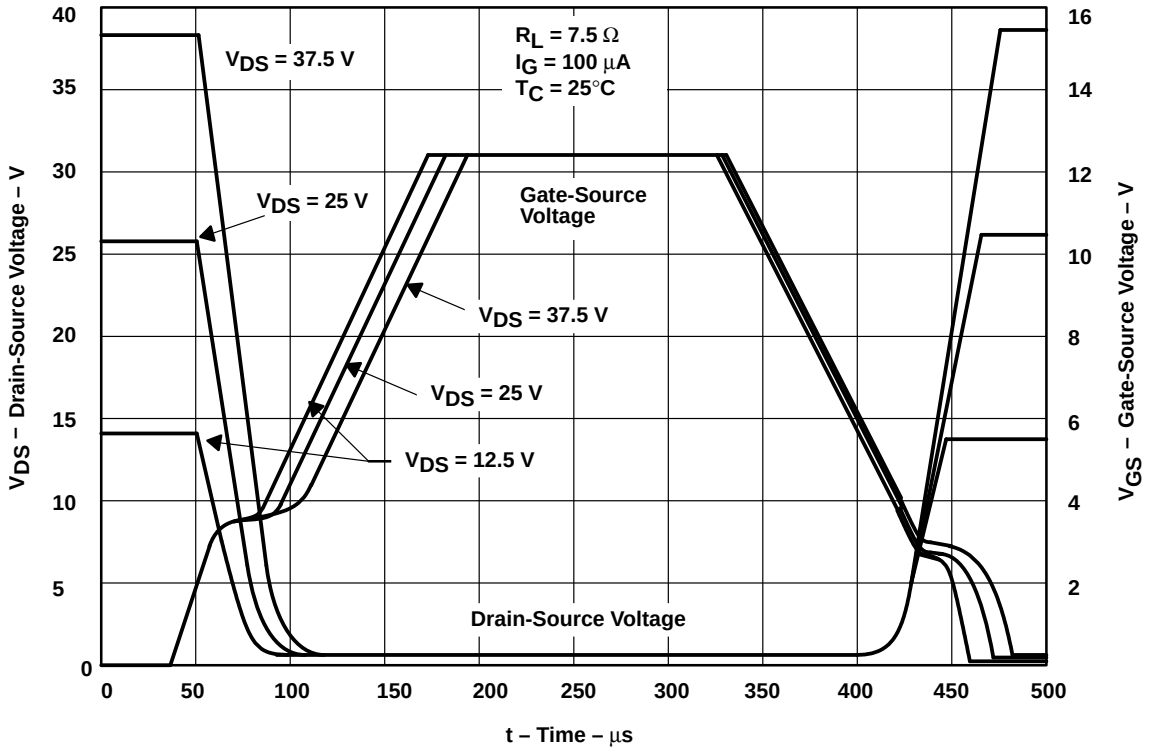


Figure 13. Resistive Switching Waveforms

THERMAL INFORMATION

**MAXIMUM DRAIN CURRENT
vs
DRAIN-SOURCE VOLTAGE**

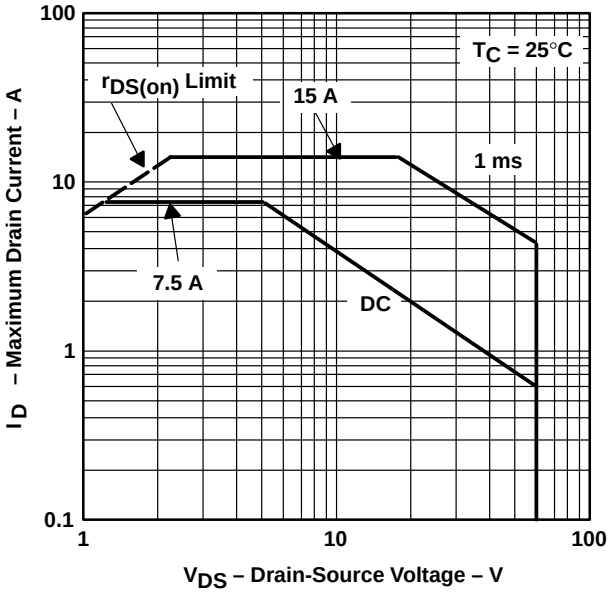


Figure 14

**MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE**

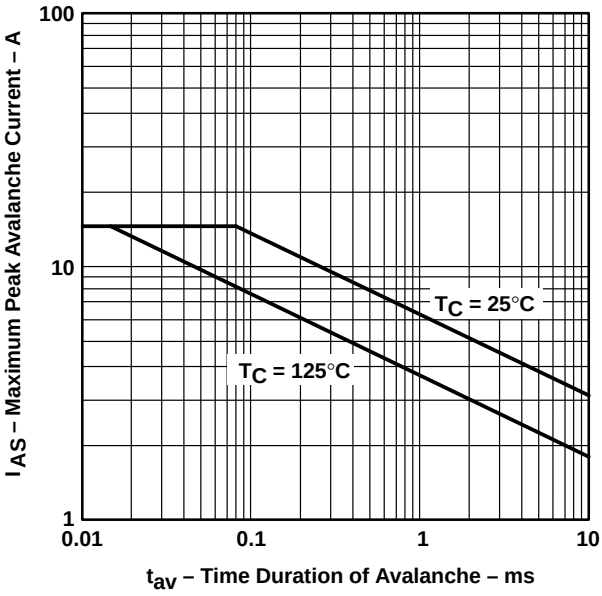
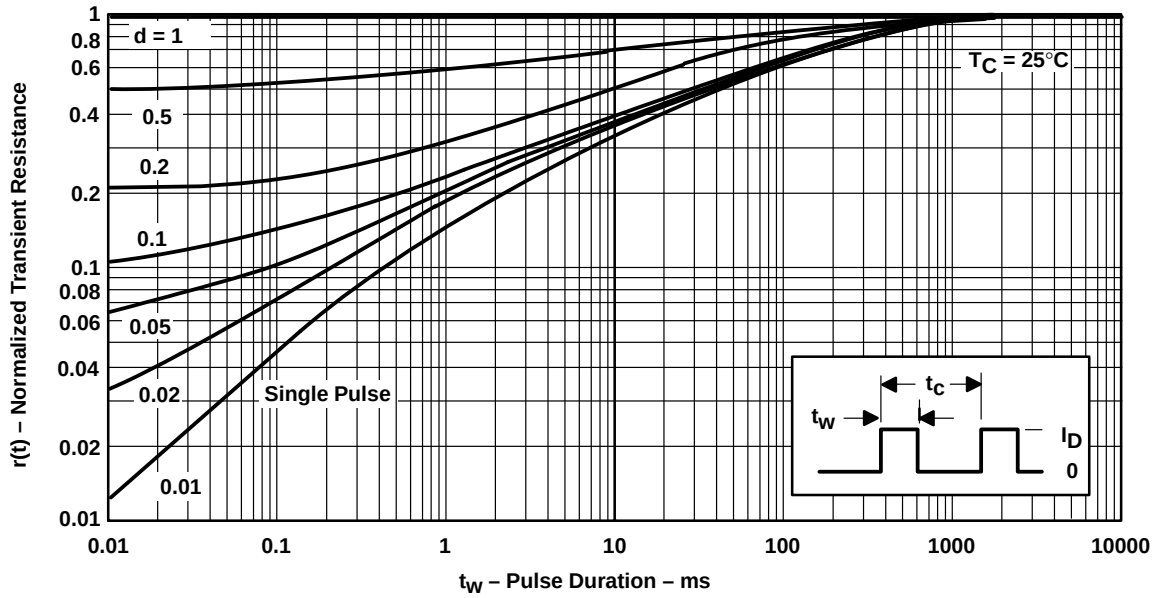


Figure 15

**NORMALIZED TRANSIENT THERMAL IMPEDANCE
vs
SQUARE-WAVE PULSE DURATION**



NOTES: $Z_{\theta JC}(t) = r(t)\ R_{\theta JC}$
t_w = pulse duration
t_c = period
d = duty cycle = t_w/t_c

Figure 16

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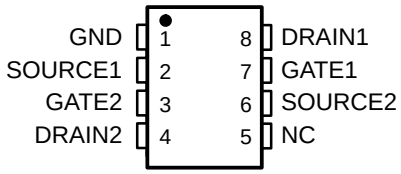
- **Low $r_{DS(on)}$ . . . 0.38 Ω Typ**
- **Voltage Output . . . 60 V**
- **Input Protection Circuitry . . . 18 V**
- **Pulsed Current . . . 3 A Per Channel**
- **Extended ESD Capability . . . 4000 V**
- **Direct Logic-Level Interface**

D PACKAGE
(TOP VIEW)



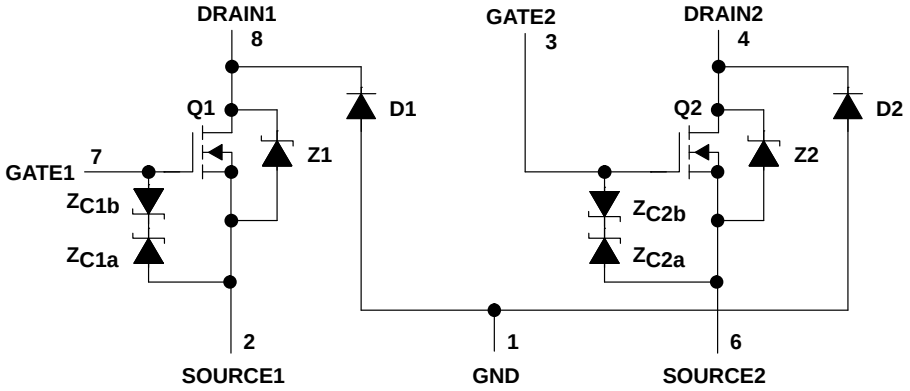
NC – No internal connection

description

The TPIC5223L is a monolithic gate-protected logic-level power DMOS array that consists of two electrically isolated independent N-channel enhancement-mode DMOS transistors. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-kΩ resistor.

The TPIC5223L is offered in a standard eight-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature of –40°C to 125°C.

schematic



NOTE A: For correct operation, no terminal may be taken below GND.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage range, V_{GS}	–9 V to 18 V
Continuous drain current, each output, T_C = 25°C	1 A
Continuous source-to-drain diode current, T_C = 25°C	1 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	3 A
Continuous gate-to-source zener diode current, T_C = 25°C	±50 mA
Pulsed gate-to-source zener-diode current, T_C = 25°C	±500 mA
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figures 4 and 16)	108 mJ
Continuous total power dissipation, T_C = 25°C (see Figure 15)	0.95 W
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 μA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}, See Figure 5		1.5	2.05	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	I_{GS} = 250 μA		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	I_{SG} = 250 μA		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND current = 250 μA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1 A, V_{GS} = 5 V, See Notes 2 and 3			0.375	0.425	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1 A, V_{GS} = 0 (Z1, Z2), See Notes 2 and 3 and Figure 12			0.85	1.2	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 1 A (D1, D2), See Notes 2 and 3			3		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	μA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	V_{GS} = 15 V, V_{DS} = 0			20	200	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	V_{SG} = 5 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	μA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 5 V, I_D = 1 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.38	0.43	Ω
			T_C = 125°C		0.61	0.65	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 500 mA, See Notes 2 and 3 and Figure 9		1.2	1.49		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz, See Figure 11			150	190	pF
C_{oss}	Short-circuit output capacitance, common source				100	125	
C_{rss}	Short-circuit reverse transfer capacitance, common source				40	50	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 500 mA, V_{GS} = 0, See Figures 1 and 14 V_{DS} = 48 V, di/dt = 100 A/μs,	Z1 and Z2		50		ns
			D1 and D2		210		
Q_{RR}	Total diode charge		Z1 and Z2		50		nC
			D1 and D2		800		

resistive-load switching characteristics, T_C = 25°C

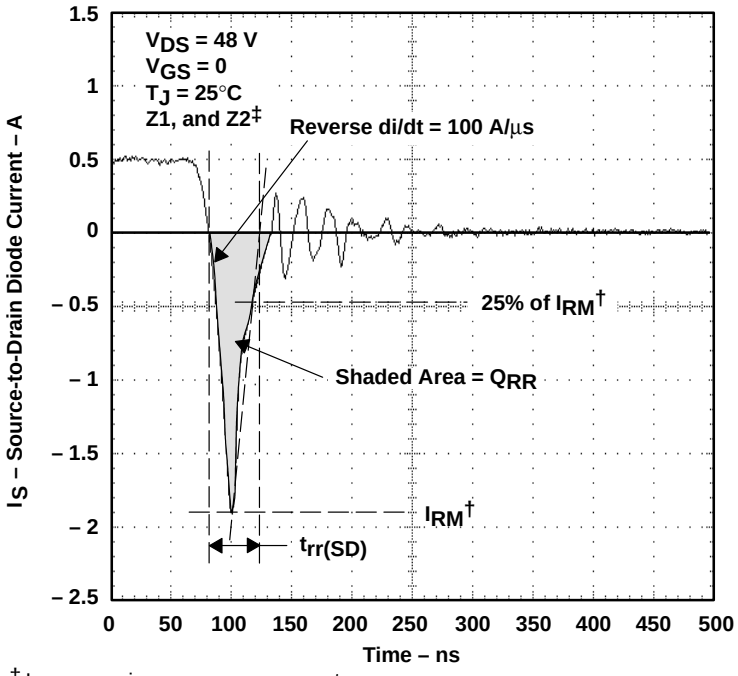
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 50 Ω, t_{r1} = 10 ns, t_{f1} = 10 ns, See Figure 2		34	70	ns
$t_{d(off)}$	Turn-off delay time			20	40	
t_{r1}	Rise time			28	55	
t_{f2}	Fall time			15	30	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 500 mA, V_{GS} = 5 V, See Figure 3		3.1	3.8	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.5	0.6	
Q_{gd}	Gate-to-drain charge			1.9	2.3	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	See Notes 4 and 7		130		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	See Notes 5 and 7		78.6		
$R_{\theta JP}$	Junction-to-pin thermal resistance	See Notes 6 and 7		34		

NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink.
5. Package mounted on a 24 in^2, 4-layer FR4 printed-circuit board.
6. Package mounted in intimate contact with infinite heatsink.
7. All outputs with equal power

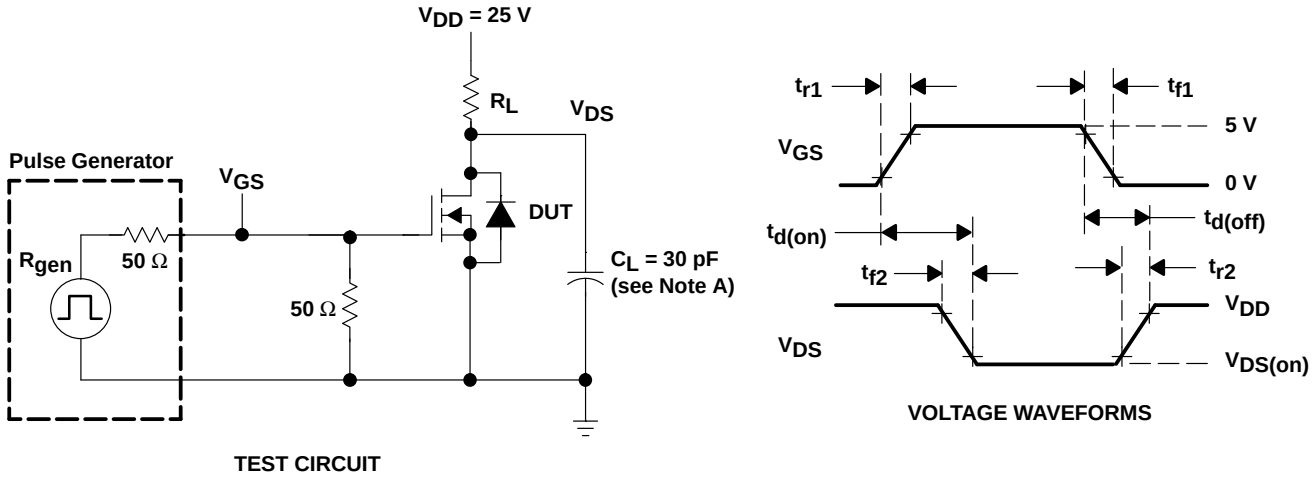
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current
‡ The above waveform is representative of D1 and D2 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION

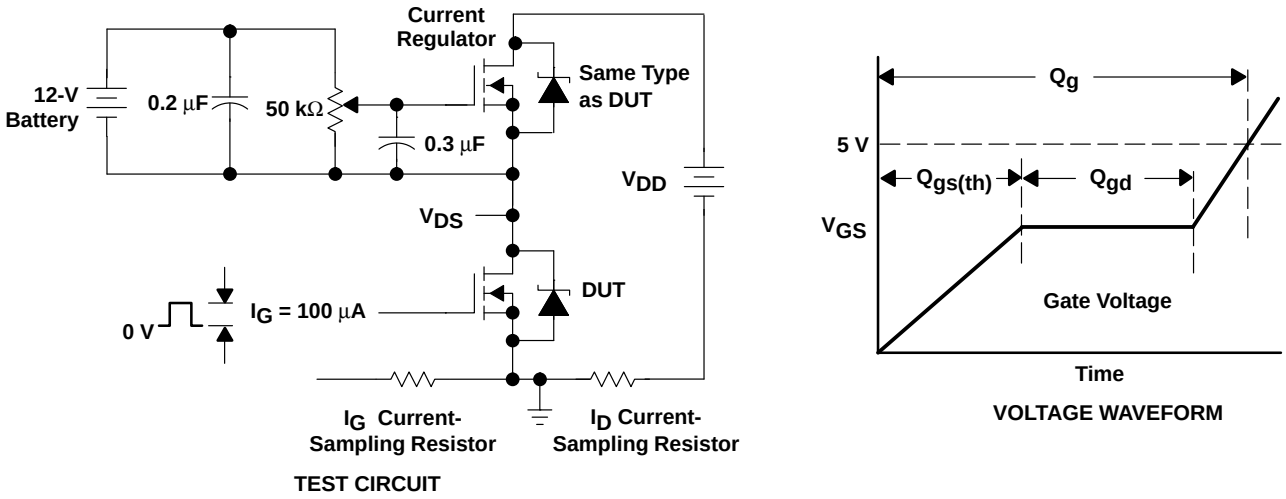


TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

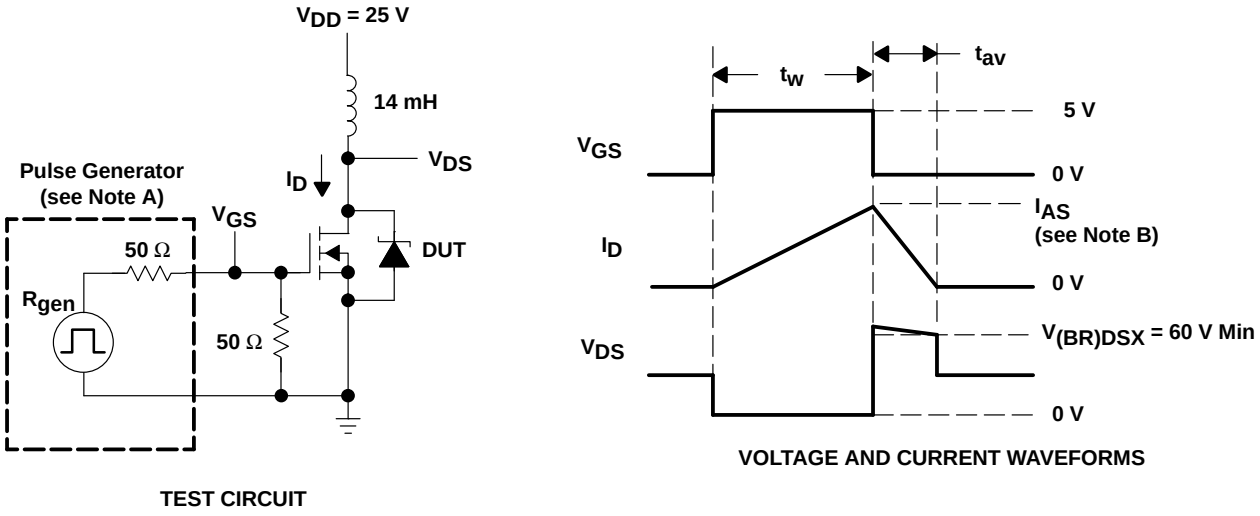


TEST CIRCUIT

VOLTAGE WAVEFORM

Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_W) is increased until peak current I_{AS} = 3 A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2}$ = 108 mJ, where t_{av} = avalanche time.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

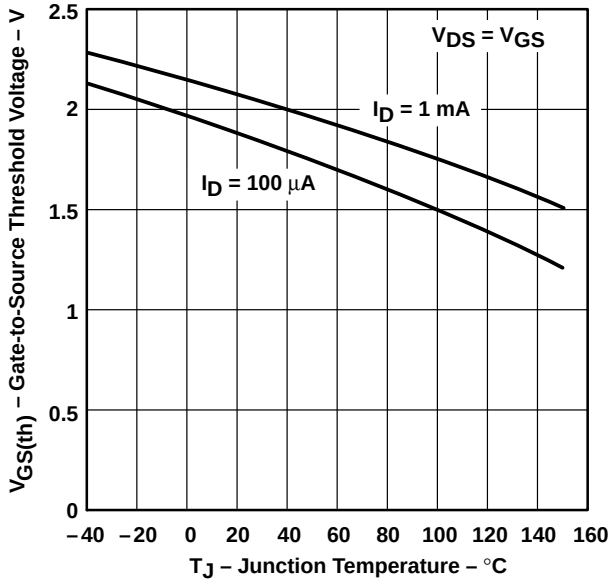


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

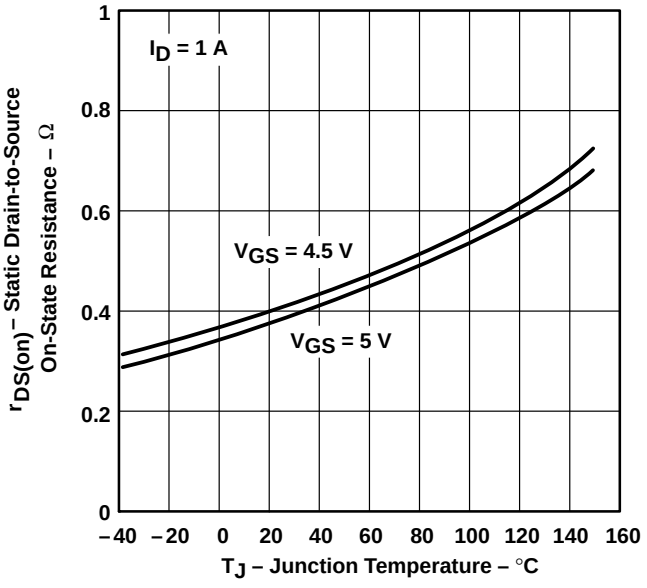


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

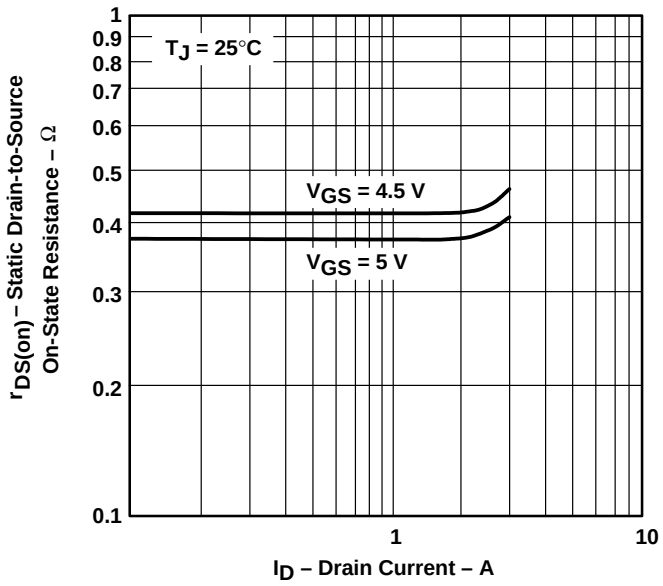


Figure 7

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

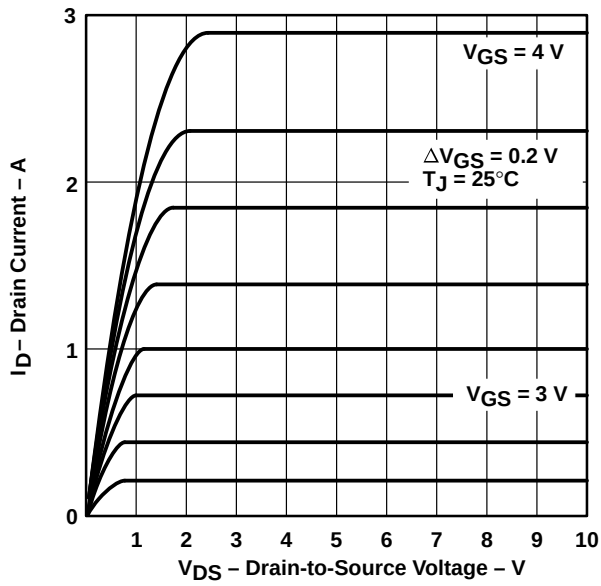


Figure 8

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

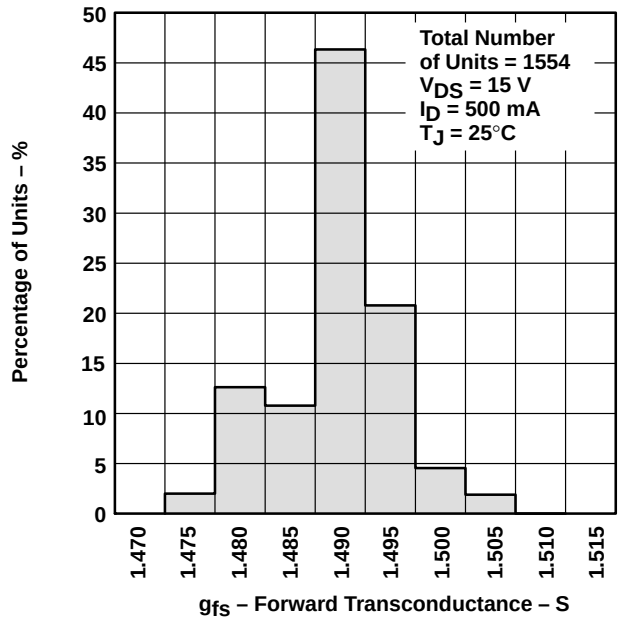


Figure 9

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

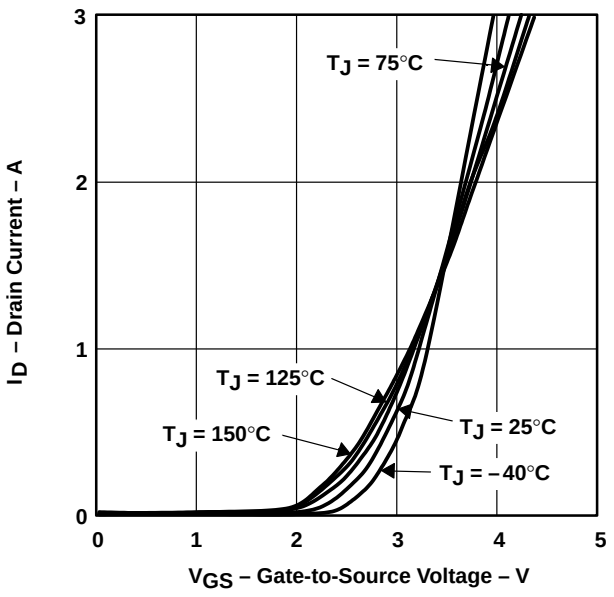


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

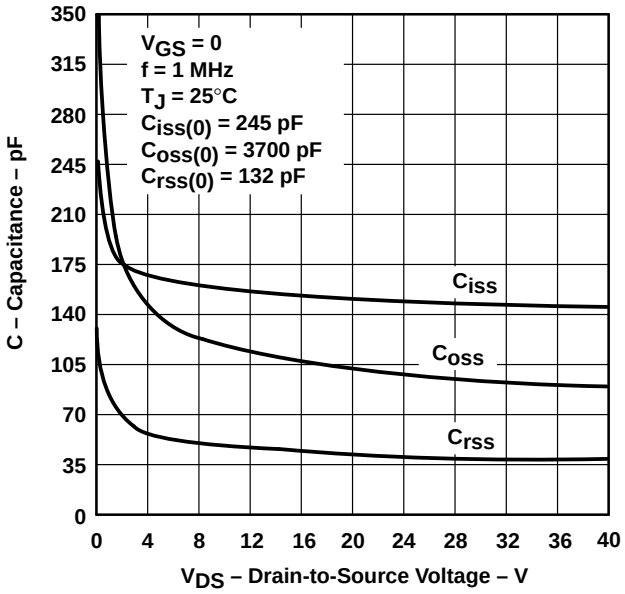


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

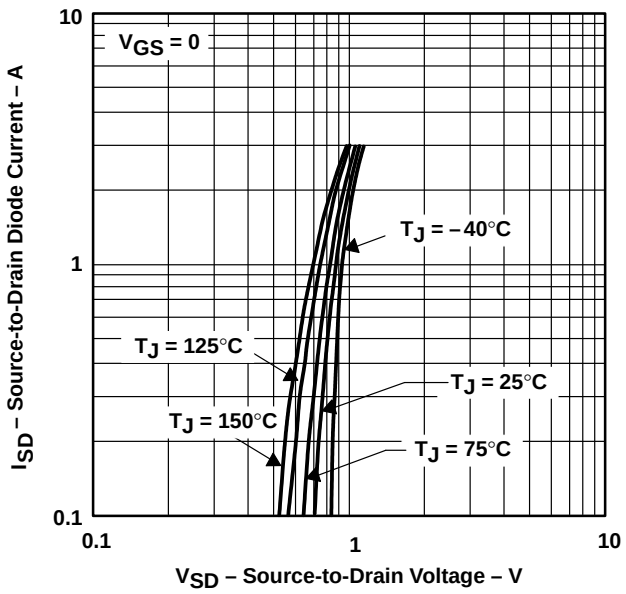


Figure 12

DRAIN-TO-SOURCE VOLTAGE AND GATE-TO-SOURCE VOLTAGE vs GATE CHARGE

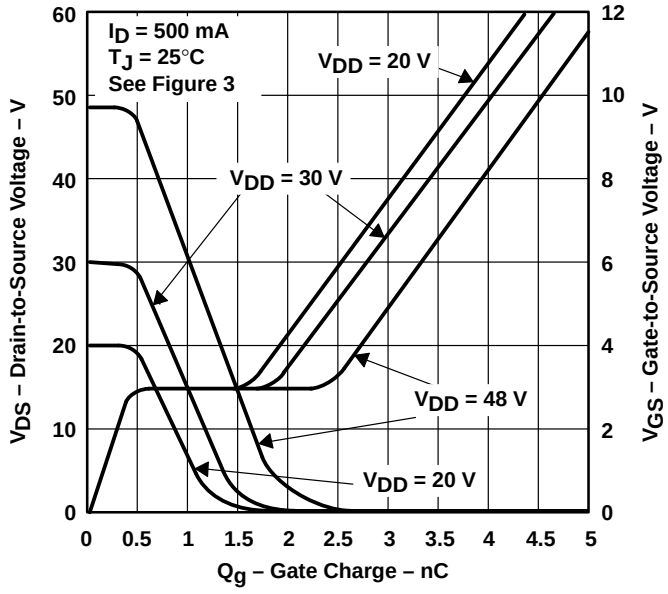


Figure 13

REVERSE-RECOVERY TIME vs REVERSE di/dt

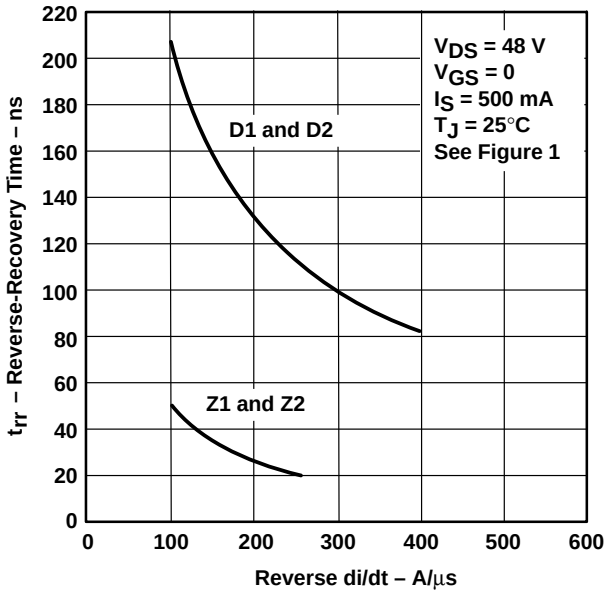
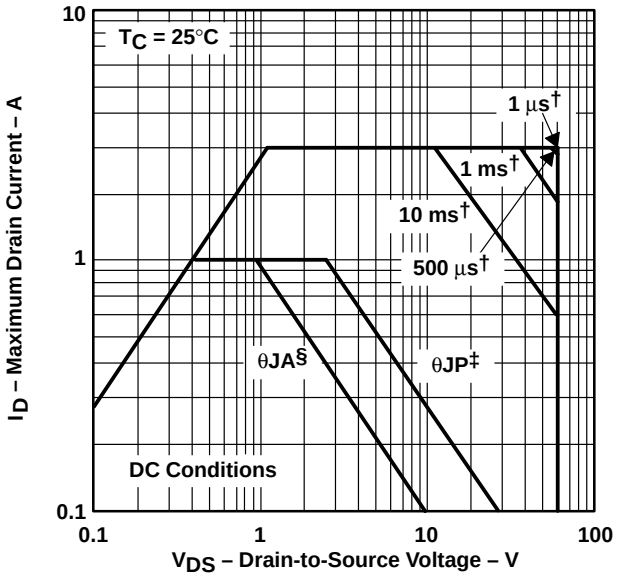


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle
‡ Device mounted in intimate contact with infinite heatsink.
§ Device mounted on FR4 printed-circuit board with no heatsink.

Figure 15

MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

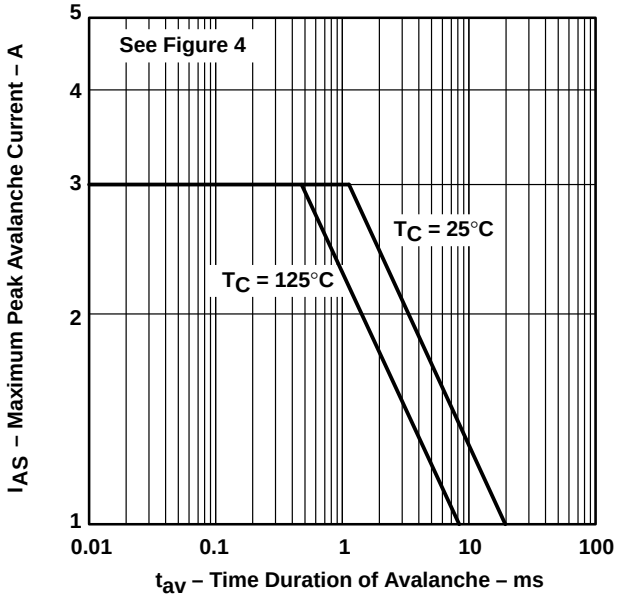
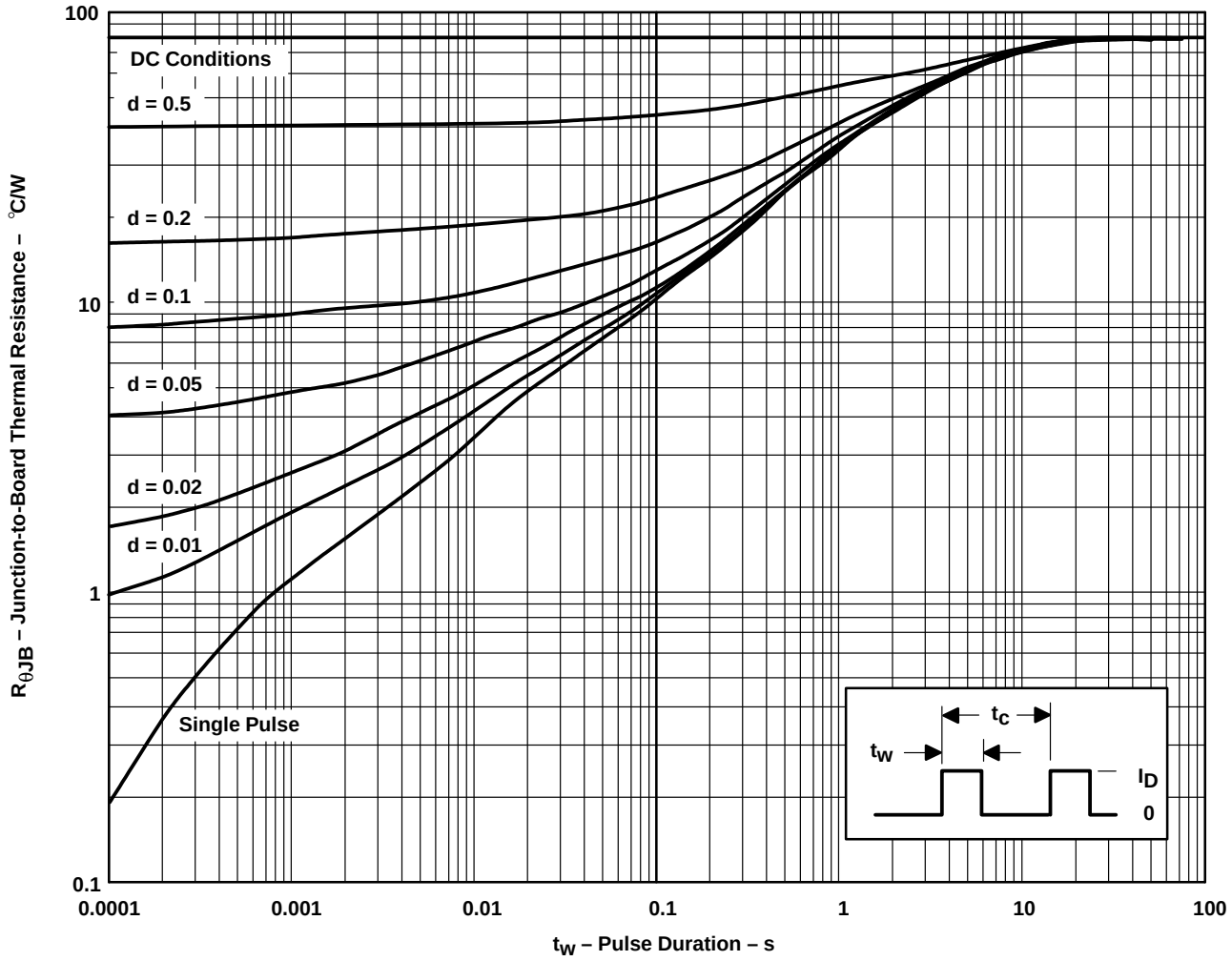


Figure 16

THERMAL INFORMATION

D PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
vs
PULSE DURATION



† Device mounted on 24 in^2, 4-layer FR4 printed-circuit board with no heatsink.

NOTE A: $Z_{\theta B}(t) = r(t)\ R_{\theta JB}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 17

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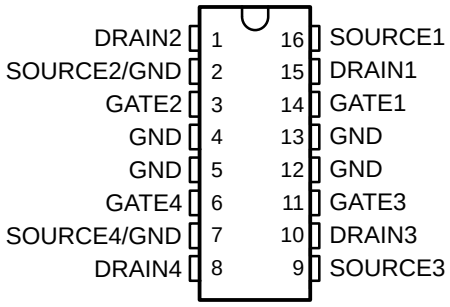
- **Low $r_{DS(on)}$ . . . 0.3 Ω Typ**
- **High Voltage Output . . . 60 V**
- **Extended ESD Capability . . . 4000 V**
- **Pulsed Current . . . 10 A Per Channel**
- **Fast Commutation Speed**

description

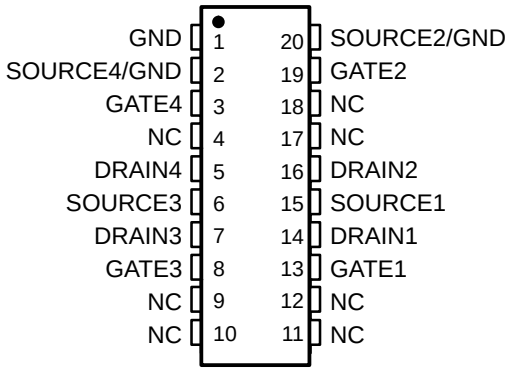
The TPIC5401 is a monolithic gate-protected power DMOS array that consists of four N-channel enhancement-mode DMOS transistors, two of which are configured with a common source. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-kΩ resistor.

The TPIC5401 is offered in a 16-pin thermally enhanced dual-in-line (NE) package and a 20-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature range of –40°C to 125°C.

NE PACKAGE
(TOP VIEW)

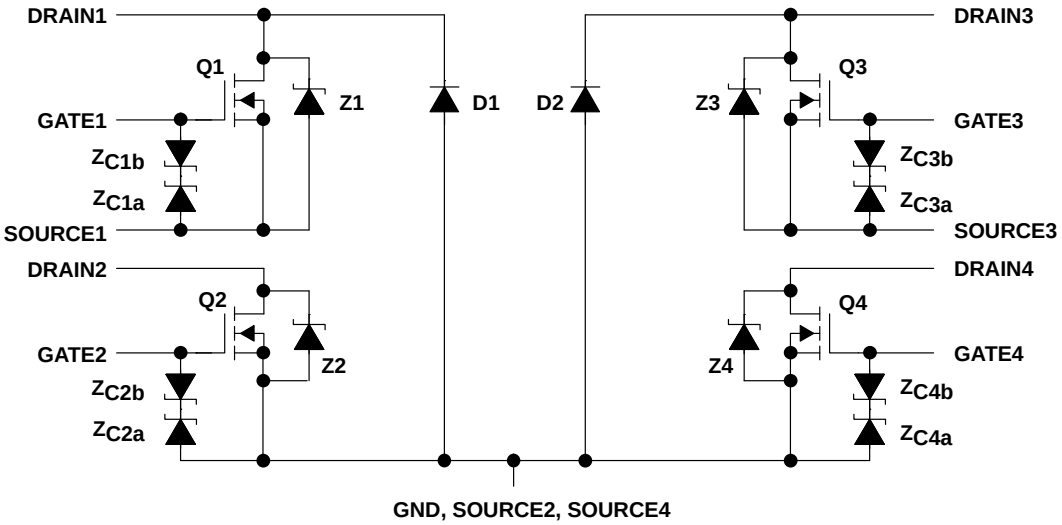


DW PACKAGE
(TOP VIEW)



NC – No internal connection

schematic



NOTE: For correct operation, no terminal pin may be taken below GND.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q2, Q4)	60 V
Gate-to-source voltage range, V_{GS}	–9 V to 18 V
Continuous drain current, each output, T_C = 25°C: DW package	1.7 A
NE package	2 A
Continuous source-to-drain diode current, T_C = 25°C	2 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	10 A
Continuous gate-to-source zener-diode current, T_C = 25°C	±50 mA
Pulsed gate-to-source zener-diode current, T_C = 25°C	±500 mA
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figures 4, 15, and 16)	21 mJ
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1389 mW	11.1 mW/°C	279 mW
NE	2075 mW	16.6 mW/°C	415 mW

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}, See Figure 5		1.5	1.85	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	I_{GS} = 250 µA		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	I_{SG} = 250 µA		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 2 A, V_{GS} = 10 V, See Notes 2 and 3			0.6	0.7	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 2 A, V_{GS} = 0 (Z1, Z2, Z3, Z4), See Notes 2 and 3 and Figure 12			1	1.2	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 2 A (D1, D2), See Notes 2 and 3			7.5		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	V_{GS} = 15 V, V_{DS} = 0			20	200	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	V_{SG} = 5 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 10 V, I_D = 2 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.3	0.35	Ω
			T_C = 125°C		0.47	0.5	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 1 A, See Notes 2 and 3 and Figure 9		1.6	1.9		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz, See Figure 11			220	275	pF
C_{oss}	Short-circuit output capacitance, common source				120	150	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				100	125	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 1 A, V_{GS} = 0, See Figures 1 and 14 V_{DS} = 48 V, di/dt = 100 A/µs,	Z1 and Z3		120		ns
			Z2 and Z4		280		
			D1 and D2		260		
Q_{RR}	Total diode charge		Z1 and Z3		0.12		µC
			Z2 and Z4		0.9		
			D1 and D2		2.2		

resistive-load switching characteristics, T_C = 25°C

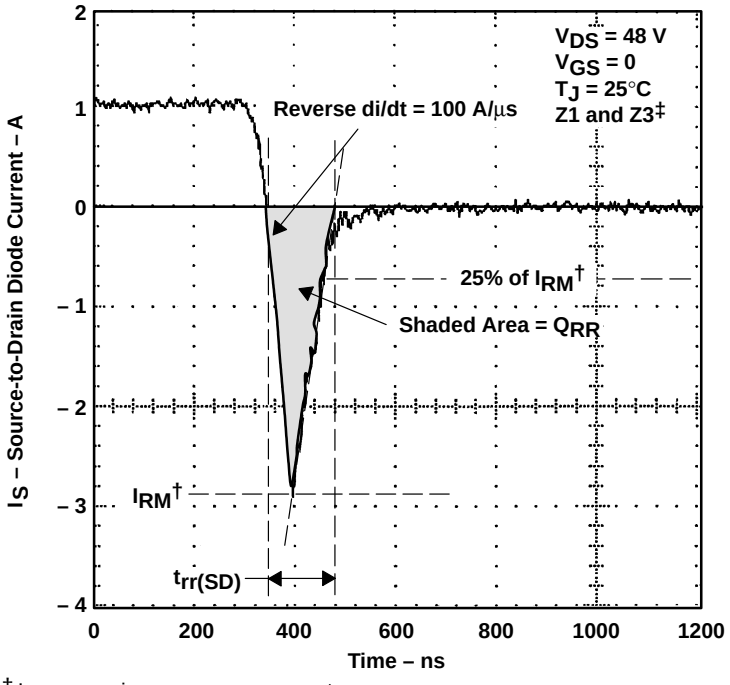
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 25 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		32	65	ns
$t_{d(off)}$	Turn-off delay time			40	80	
t_r	Rise time			15	30	
t_f	Fall time			25	50	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 1 A, V_{GS} = 10 V, See Figure 3		6.6	8	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.8	1	
Q_{gd}	Gate-to-drain charge			2.6	3.2	
L_d	Internal drain inductance			5		nH
L_s	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistances

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (see Note 4)	DW	All outputs with equal power		90		°C/W
		NE			60		
$R_{\theta JB}$	Junction-to-board thermal resistance	DW			53		
$R_{\theta JC}$	Junction-to-case thermal resistance	DW			30		
$R_{\theta JP}$	Junction-to-pin thermal resistance	NE			25		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heatsink.

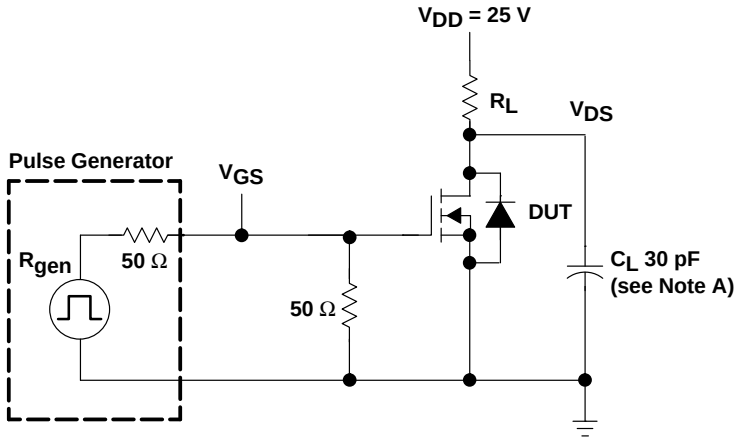
PARAMETER MEASUREMENT INFORMATION



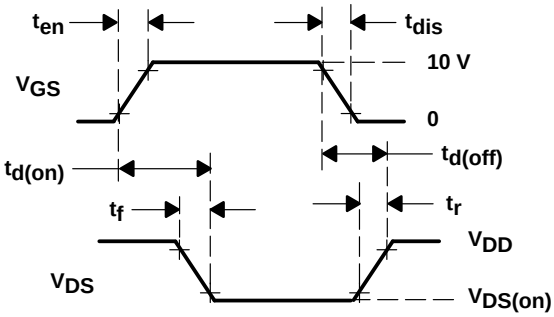
† I_{RM} = maximum recovery current
‡ The above waveform is representative of Z2, Z4, D1, and D2 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



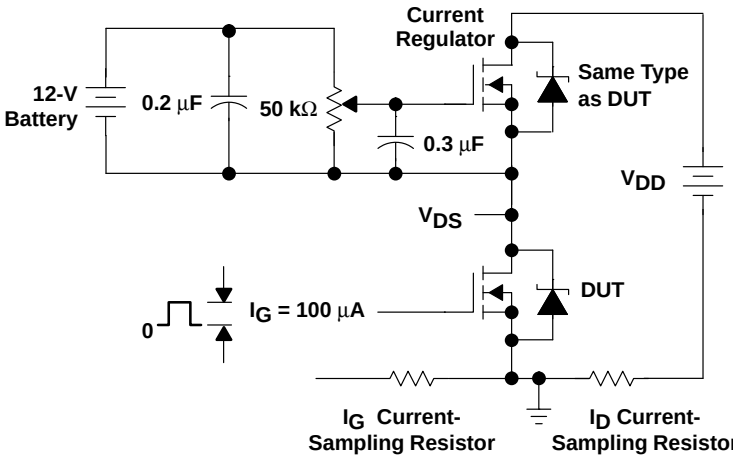
TEST CIRCUIT



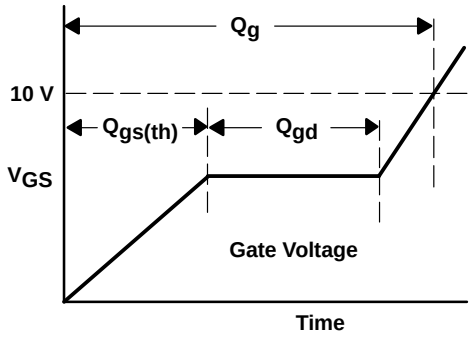
VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms



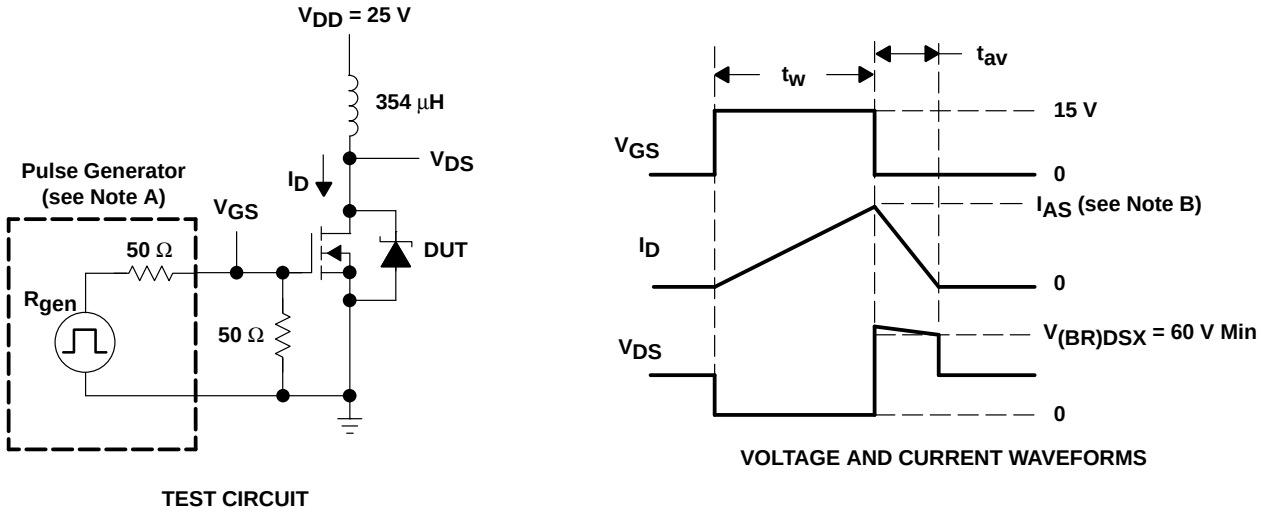
TEST CIRCUIT



WAVEFORM

Figure 3. Gate-Charge Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 10$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 21$ mJ.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

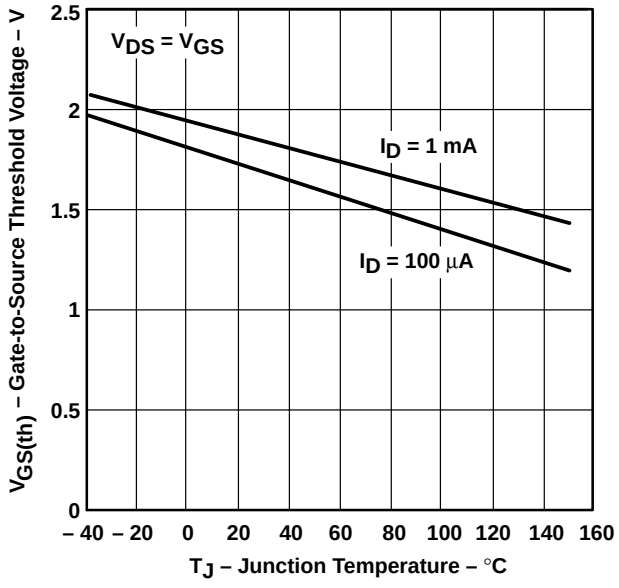


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

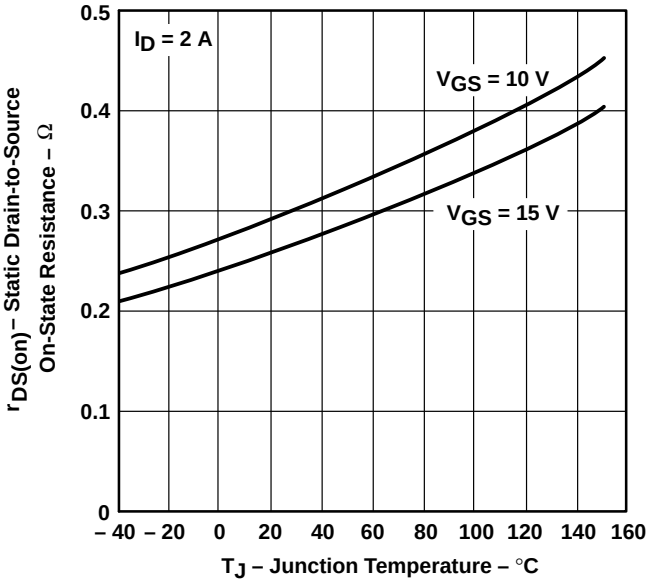


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

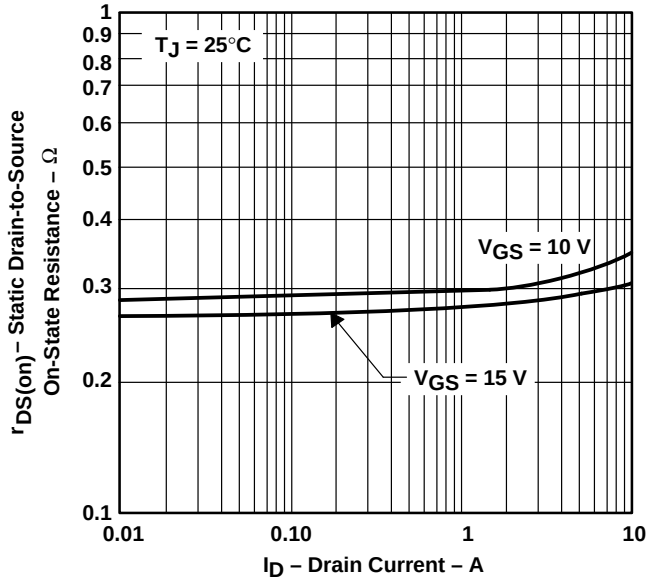


Figure 7

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

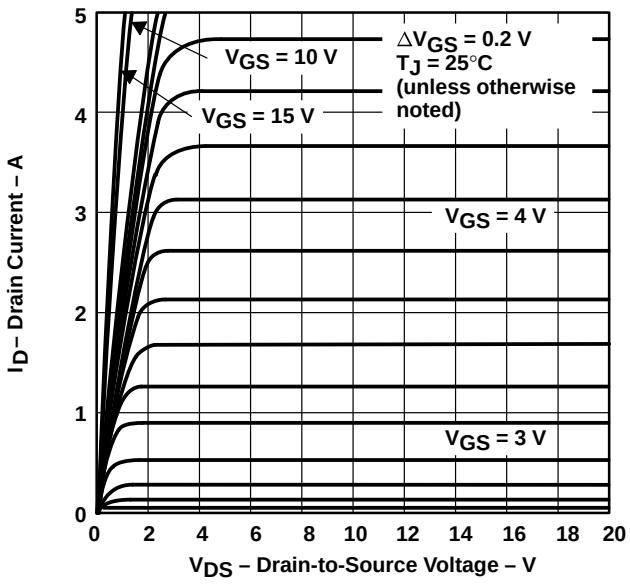


Figure 8

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

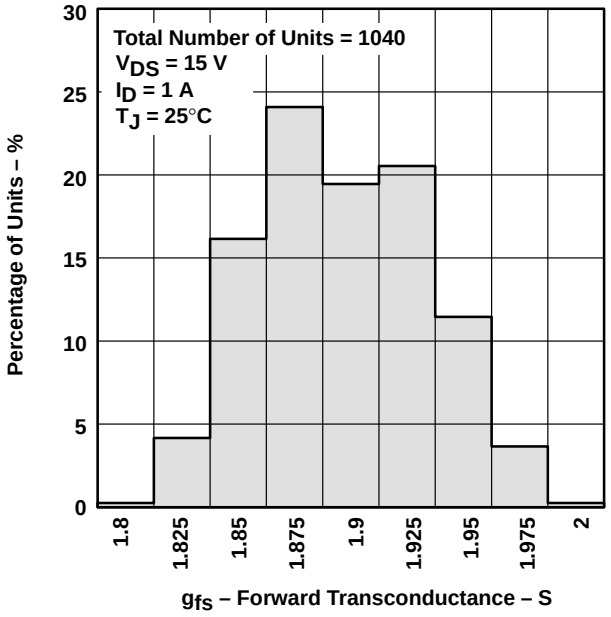


Figure 9

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

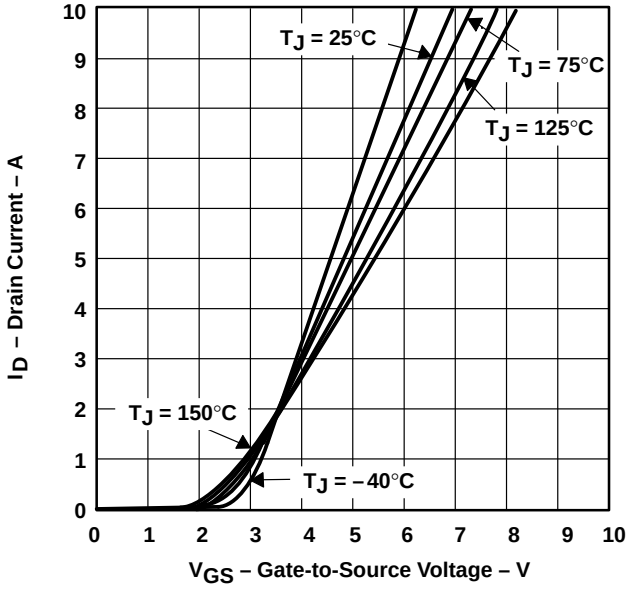


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

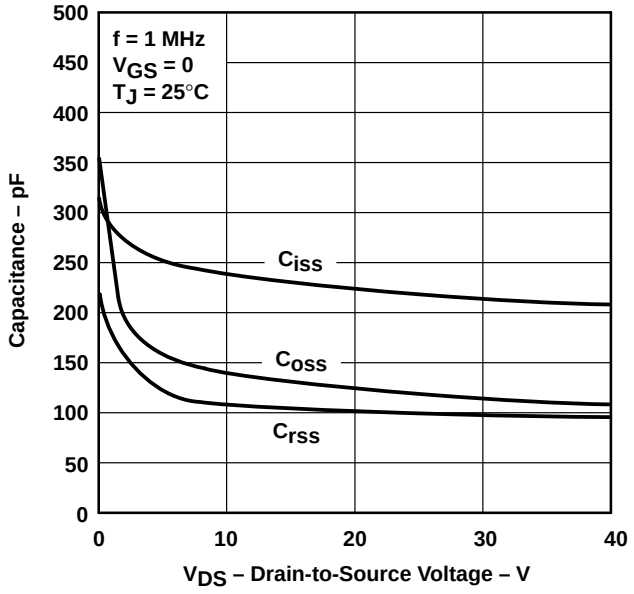


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

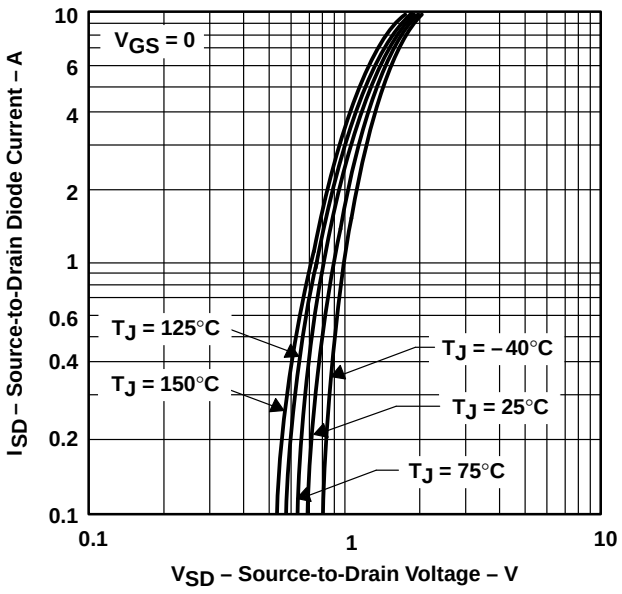


Figure 12

DRAIN-TO-SOURCE VOLTAGE AND GATE-TO-SOURCE VOLTAGE vs GATE CHARGE

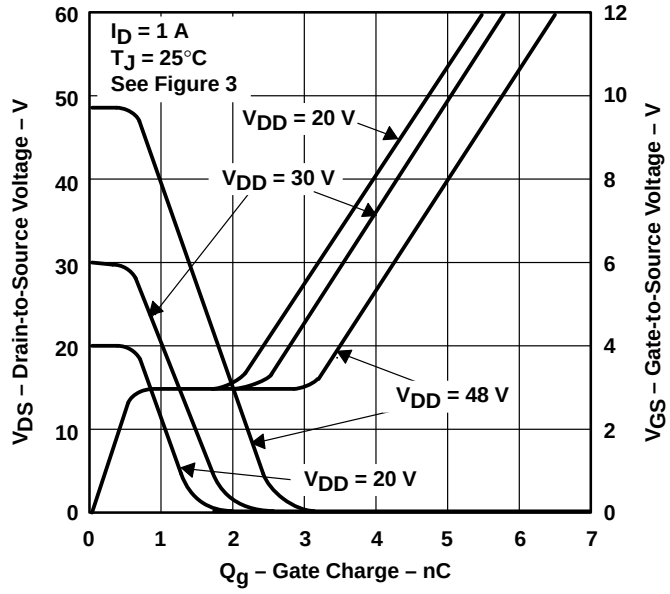


Figure 13

REVERSE-RECOVERY TIME vs REVERSE di/dt

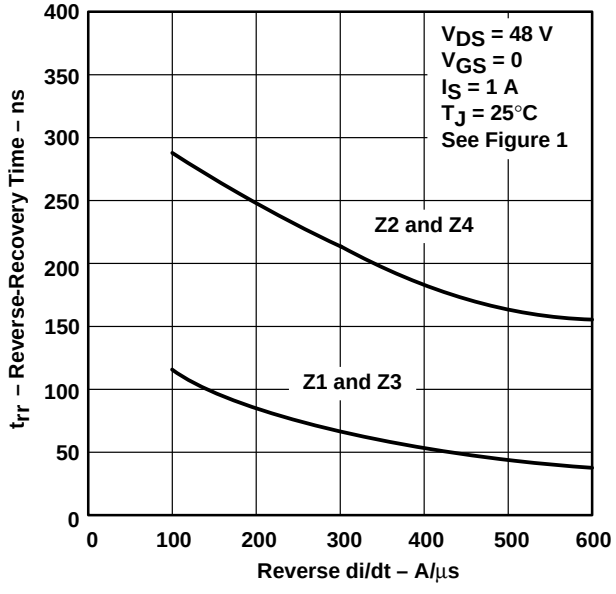
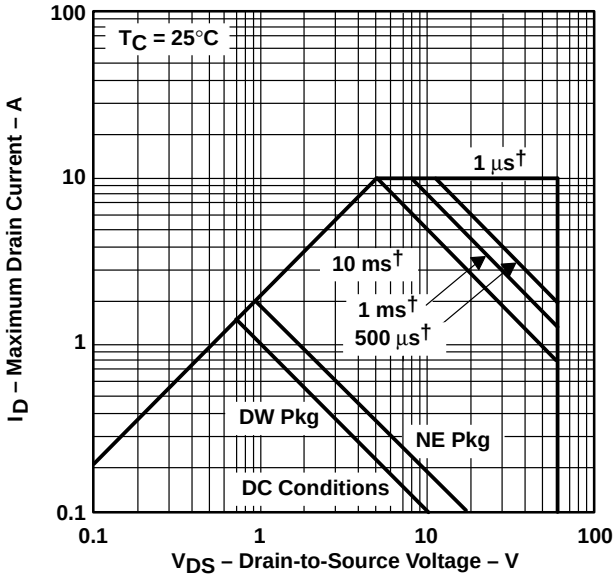


Figure 14

THERMAL INFORMATION

**MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE**



† Less than 2% duty cycle

Figure 15

**MAXIMUM PEAK-AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE**

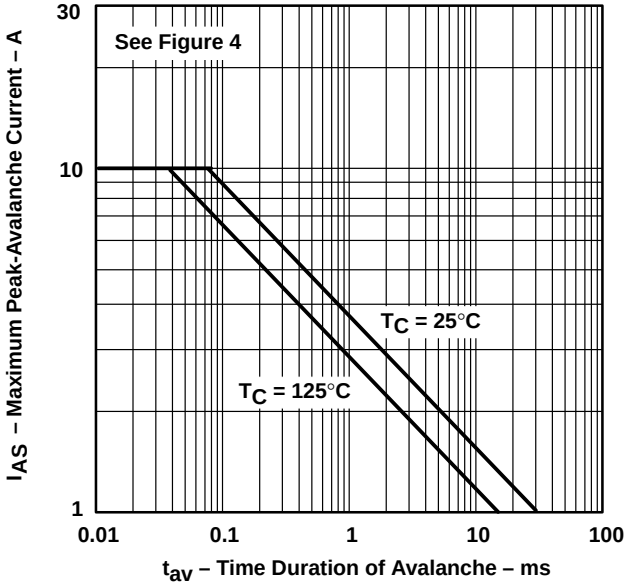
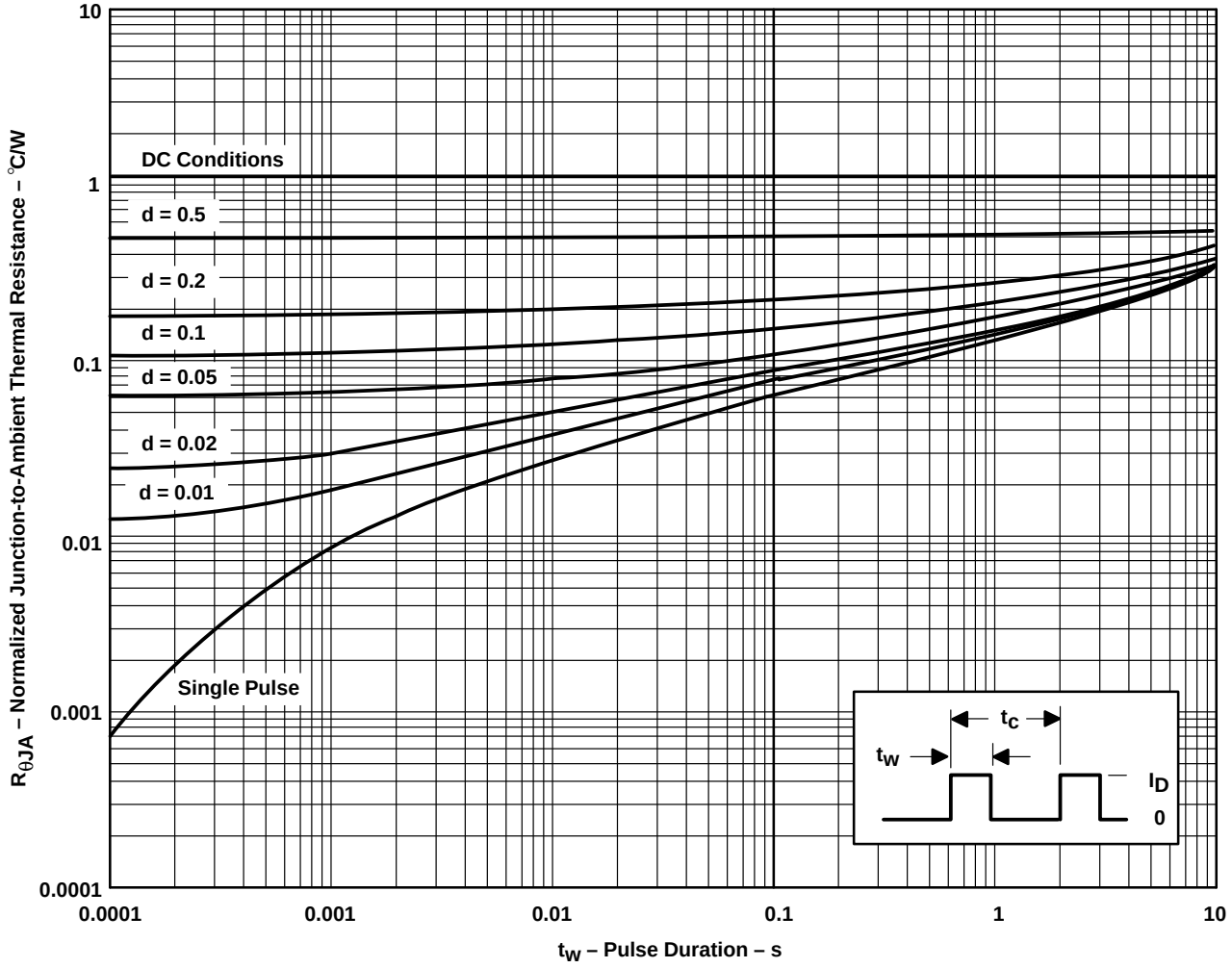


Figure 16

THERMAL INFORMATION

NE PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



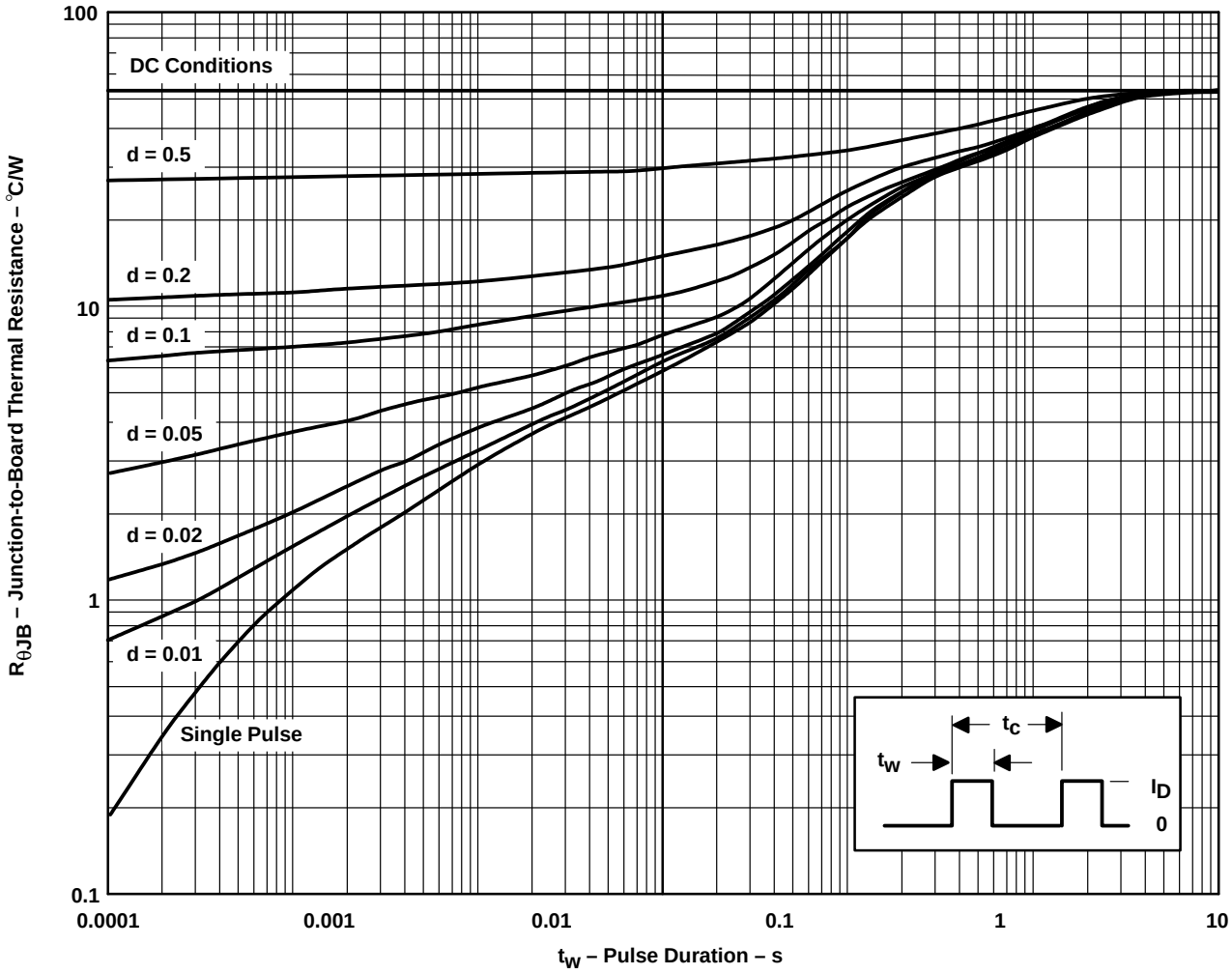
† Device mounted on FR4 printed-circuit board with no heatsink.

NOTE A: $Z_{\theta JA}(t) = r(t)\ R_{\theta JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 17

THERMAL INFORMATION

DW PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
vs
PULSE DURATION



† Device mounted on 24 in^2, 4-layer FR4 printed-circuit board with no heatsink.

NOTE A: $Z_{\theta JB}(t) = r(t)\ R_{\theta JB}$
t_W = pulse duration
t_c = cycle time
d = duty cycle = t_W/t_c

Figure 18

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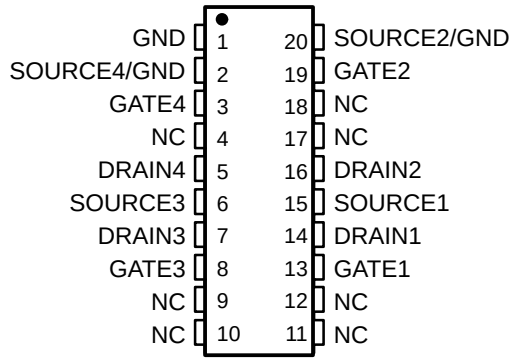
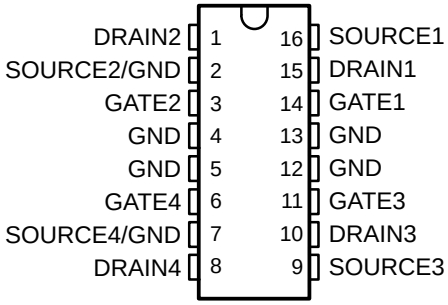
- **Low $r_{DS(on)}$ . . . 0.4 Ω Typ**
- **Voltage Output . . . 60 V**
- **Input Protection Circuitry . . . 18 V**
- **Pulsed Current . . . 3 A Per Channel**
- **Extended ESD Capability . . . 4000 V**
- **Direct Logic-Level Interface**

DW PACKAGE
(TOP VIEW)



NE PACKAGE
(TOP VIEW)



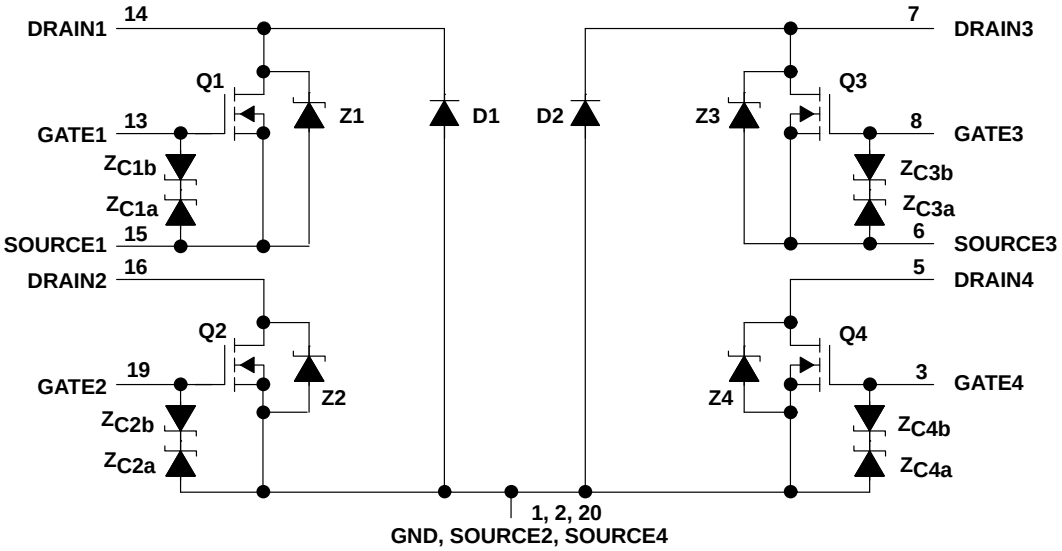
NC – No internal connection

description

The TPIC5421L is a monolithic gate-protected logic-level power DMOS array that consists of four electrically isolated N-channel enhancement-mode DMOS transistors, two of which are configured with common source. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-kΩ resistor.

The TPIC5421L is offered in a 20-pin wide-body surface-mount (DW) package and a 16-pin thermally-enhanced dual-in-line (NE) package and is characterized for operation over the case temperature of –40°C to 125°C.

schematic



NOTE A: For correct operation, no terminal may be taken below GND.
Pin numbers shown are for the DW package.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q2, Q4)	60 V
Gate-to-source voltage range, V_{GS}	–9 V to 18 V
Continuous drain current, each output, T_C = 25°C: NE package	1.5 A
DW package	1 A
Continuous source-to-drain diode current, T_C = 25°C	1 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	3 A
Continuous gate-to-source zener-diode current, T_C = 25°C	±50 mA
Pulsed gate-to-source zener-diode current, T_C = 25°C	±500 mA
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figures 4 and 16)	180 mJ
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1125 mW	9.0 mW/°C	225 mW
NE	2075 mW	16.6 mW/°C	415 mW

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}, See Figure 5		1.5	1.85	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	I_{GS} = 250 µA		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	I_{SG} = 250 µA		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1 A, V_{GS} = 5 V, See Notes 2 and 3			0.4	0.475	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1 A, V_{GS} = 0 (Z1, Z2, Z3, Z4), See Notes 2 and 3 and Figure 12			0.9	1.1	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 1 A (D1, D2), See Notes 2 and 3			4.6		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	V_{GS} = 15 V, V_{DS} = 0			20	200	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	V_{SG} = 5 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 5 V, I_D = 1 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.4	0.475	Ω
			T_C = 125°C		0.65	0.68	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 0.5 A, See Notes 2 and 3 and Figure 9		1.25	1.4		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0, See Figure 11			220	275	pF
C_{oss}	Short-circuit output capacitance, common source				120	150	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				100	125	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 0.5 A, V_{GS} = 0, See Figures 1 and 14	Z1 and Z3		55		ns
		V_{DS} = 48 V, di/dt = 100 A/µs,	Z2 and Z4		150		
			D1 and D2		200		
Q_{RR}	Total diode charge		Z1 and Z3		0.06		µC
			Z2 and Z4		0.3		
			D1 and D2		0.7		

resistive-load switching characteristics, T_C = 25°C

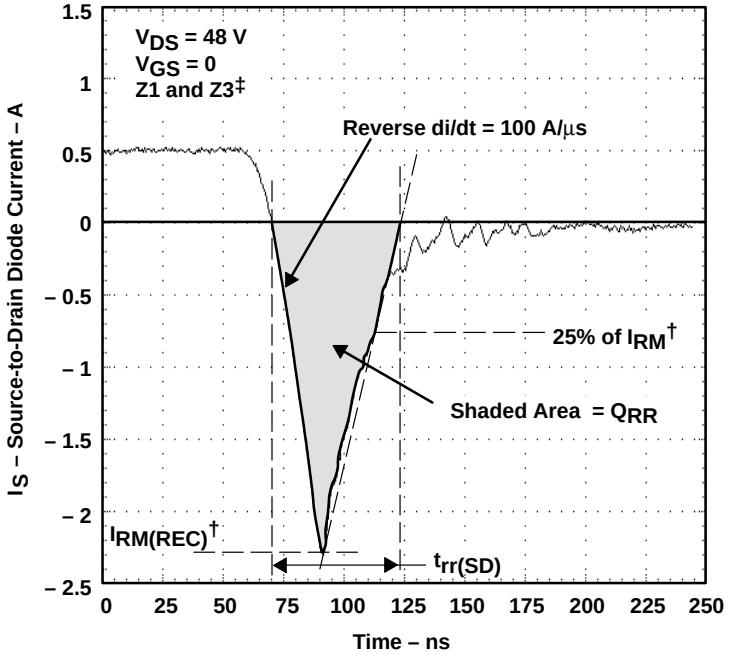
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, t_{f1} = 10 ns,	R_L = 25 Ω, See Figure 2	t_{r1} = 10 ns,		25	50	ns
$t_{d(off)}$	Turn-off delay time					20	40	
t_{r2}	Rise time					21	42	
t_{f2}	Fall time					9	18	
Q_g	Total gate charge	V_{DS} = 48 V, See Figure 3	I_D = 0.5 A,	V_{GS} = 5 V,		3.9	5	nC
$Q_{gs(th)}$	Threshold gate-to-source charge					0.55	0.8	
Q_{gd}	Gate-to-drain charge					2.5	3.6	
L_D	Internal drain inductance					5		nH
L_S	Internal source inductance					5		
R_g	Internal gate resistance					0.25		Ω

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	DW package	See Notes 4 and 6		90		°C/W
		NE package			60		
$R_{\theta JB}$	Junction-to-board thermal resistance	DW package	See Notes 4 and 6		53		
$R_{\theta JP}$	Junction-to-pin thermal resistance	DW package	See Notes 5 and 6		30		
		NE package			25		

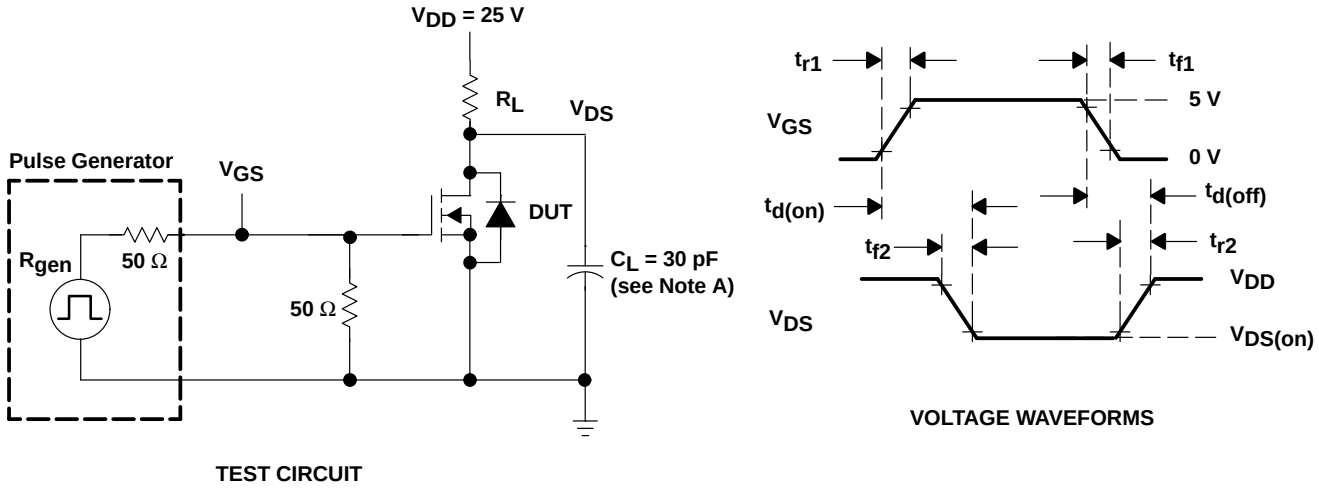
NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink.
5. Package mounted in intimate contact with infinite heatsink.
6. All outputs with equal power

PARAMETER MEASUREMENT INFORMATION



† $I_{RM(REC)}$ = maximum recovery current
‡ The above waveform is representative of Z2, Z4, D1, and D2 in shape only.

Figure 1. Reverse-Recovery-Current Waveforms of Source-to-Drain Diode



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

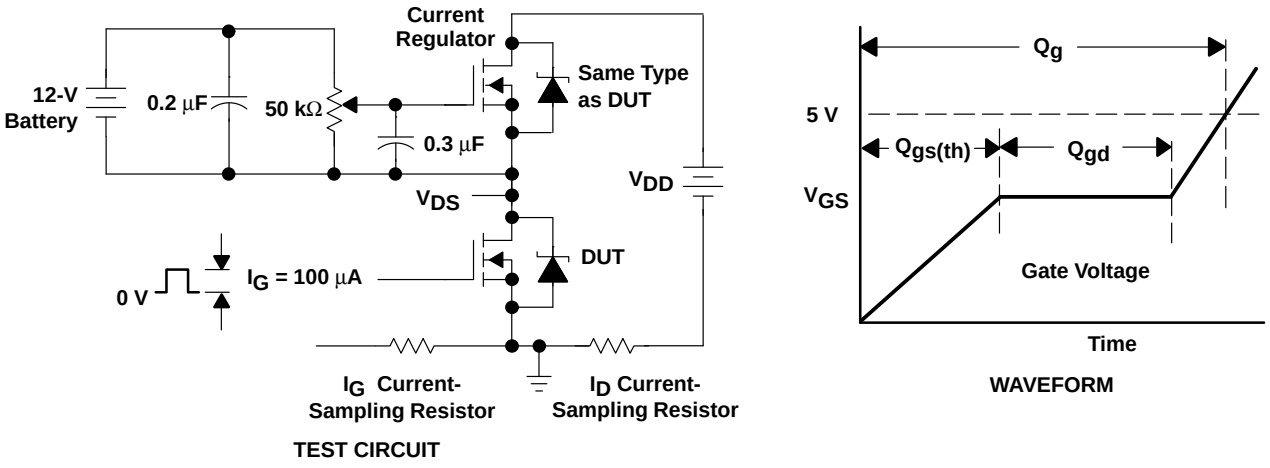
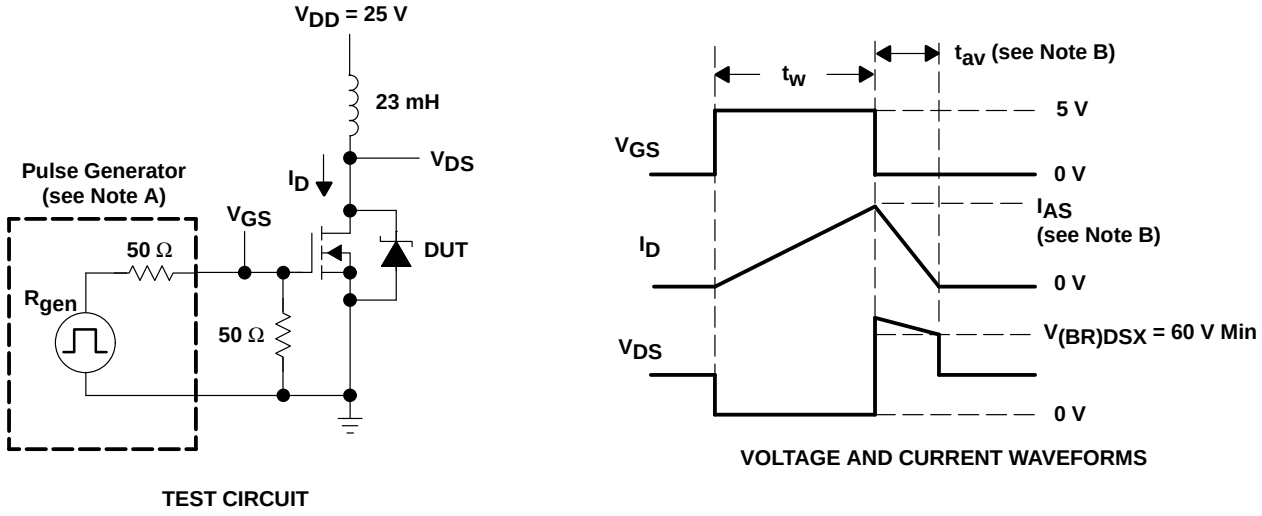


Figure 3. Gate-Charge Test Circuit and Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_W) is increased until peak current $I_{AS} = 3$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 180$ mJ,
where t_{av} = avalanche time

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

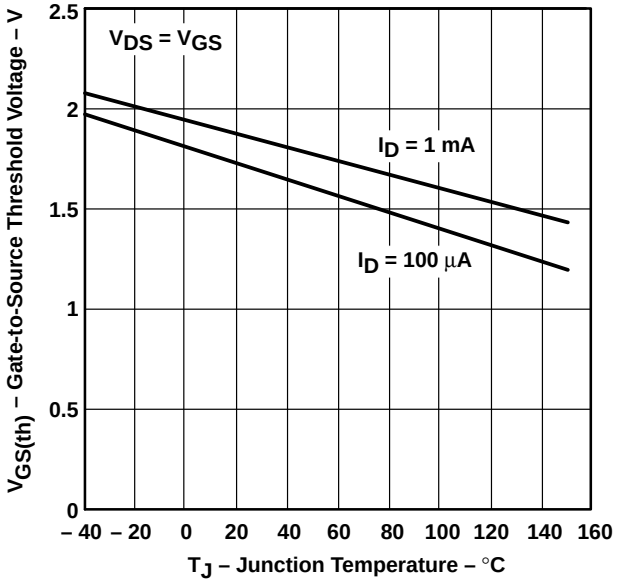


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
CASE TEMPERATURE

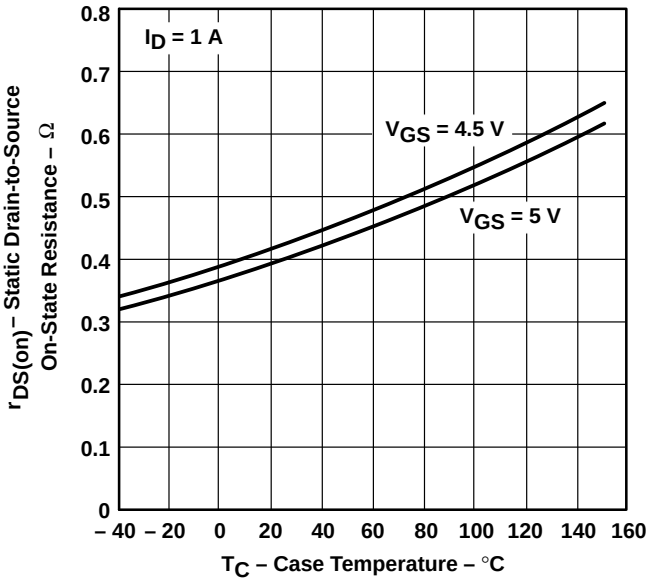


Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

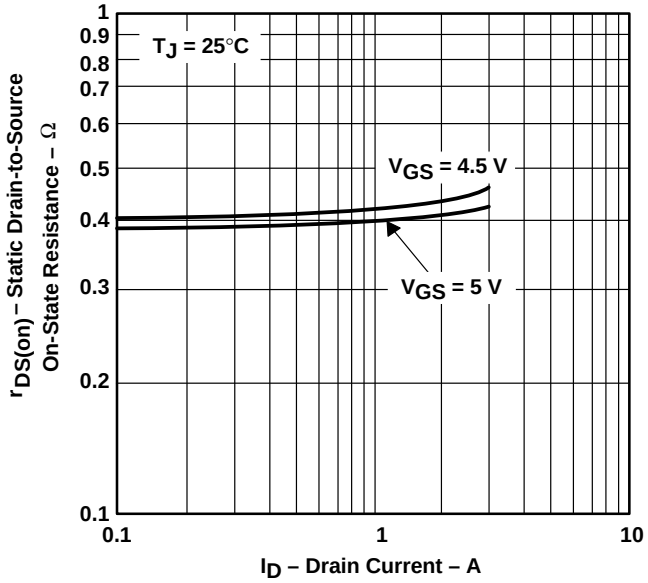


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

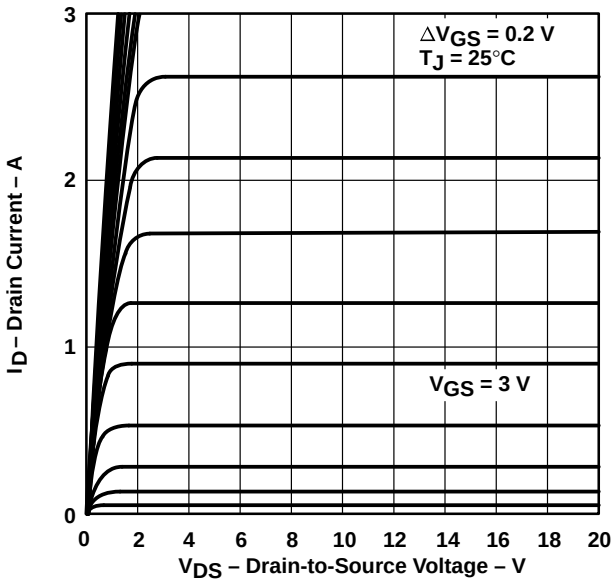


Figure 8

TYPICAL CHARACTERISTICS

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

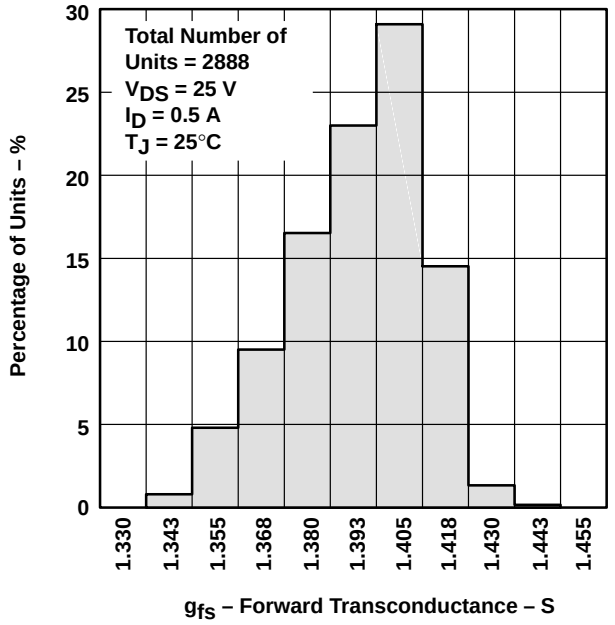


Figure 9

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

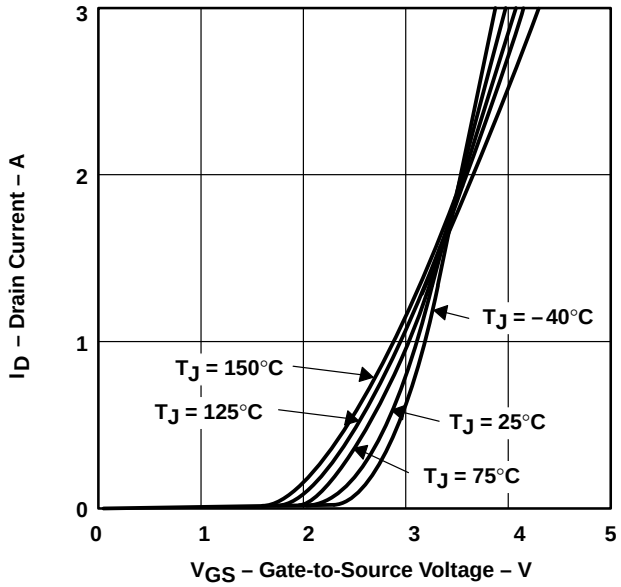


Figure 10

CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

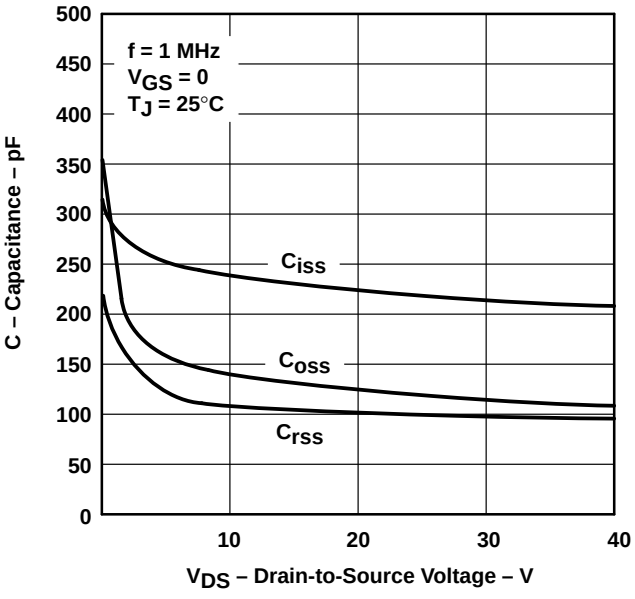


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

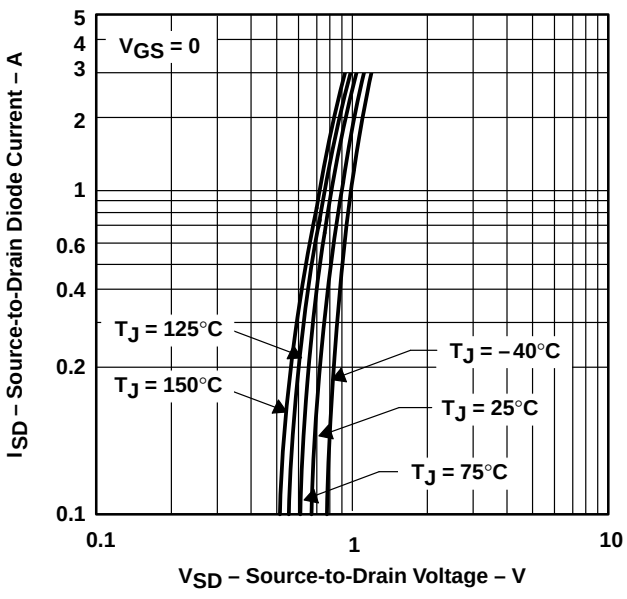


Figure 12

TYPICAL CHARACTERISTICS

DRAIN-TO-SOURCE VOLTAGE AND GATE-TO-SOURCE VOLTAGE vs GATE CHARGE

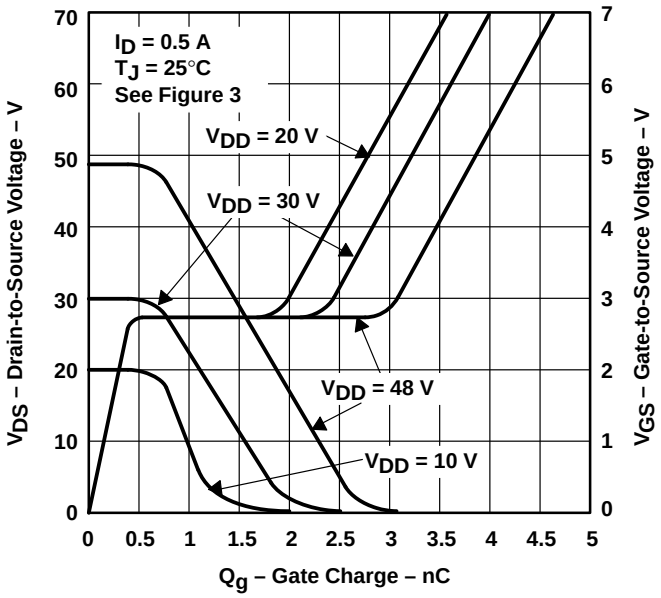


Figure 13

REVERSE-RECOVERY TIME vs REVERSE di/dt

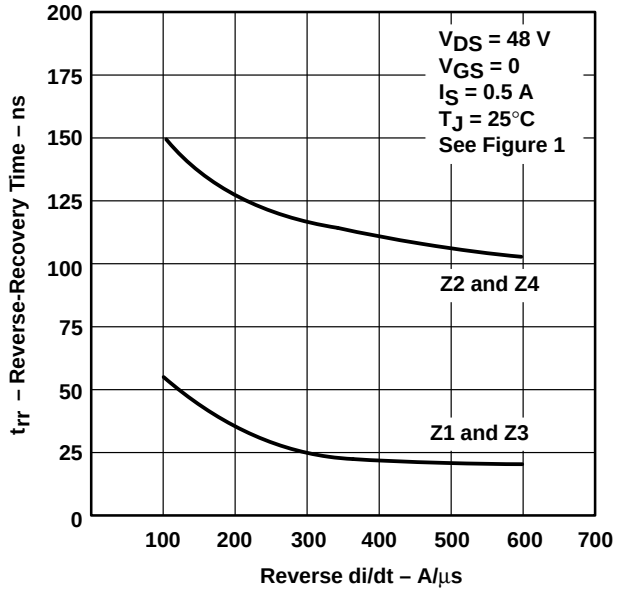
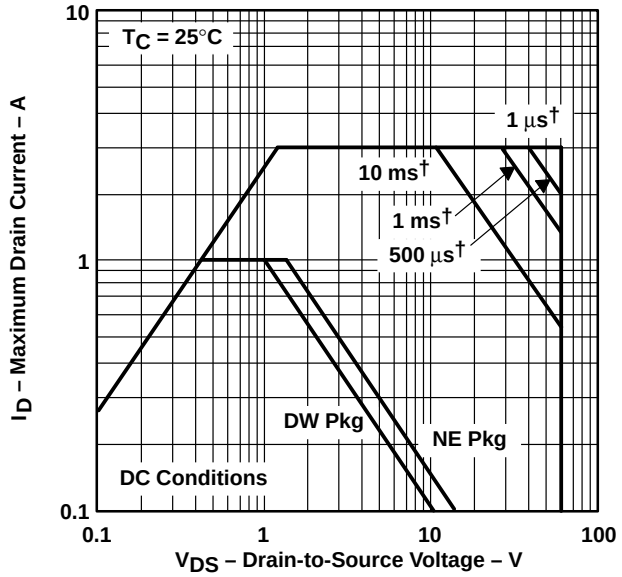


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle

Figure 15

MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

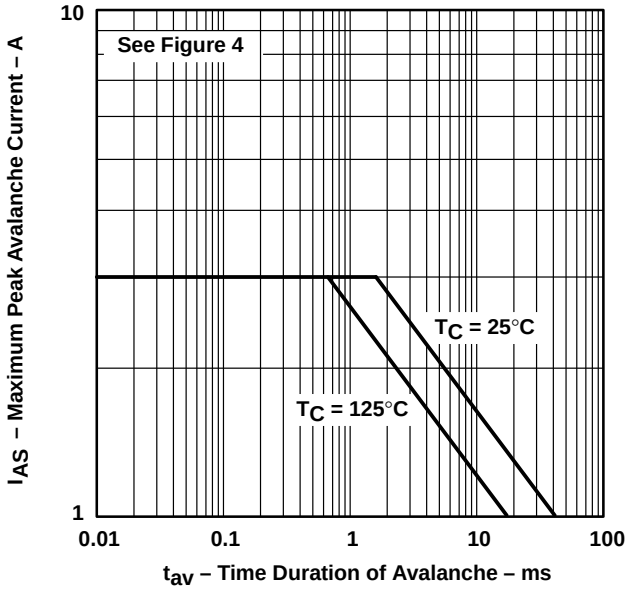
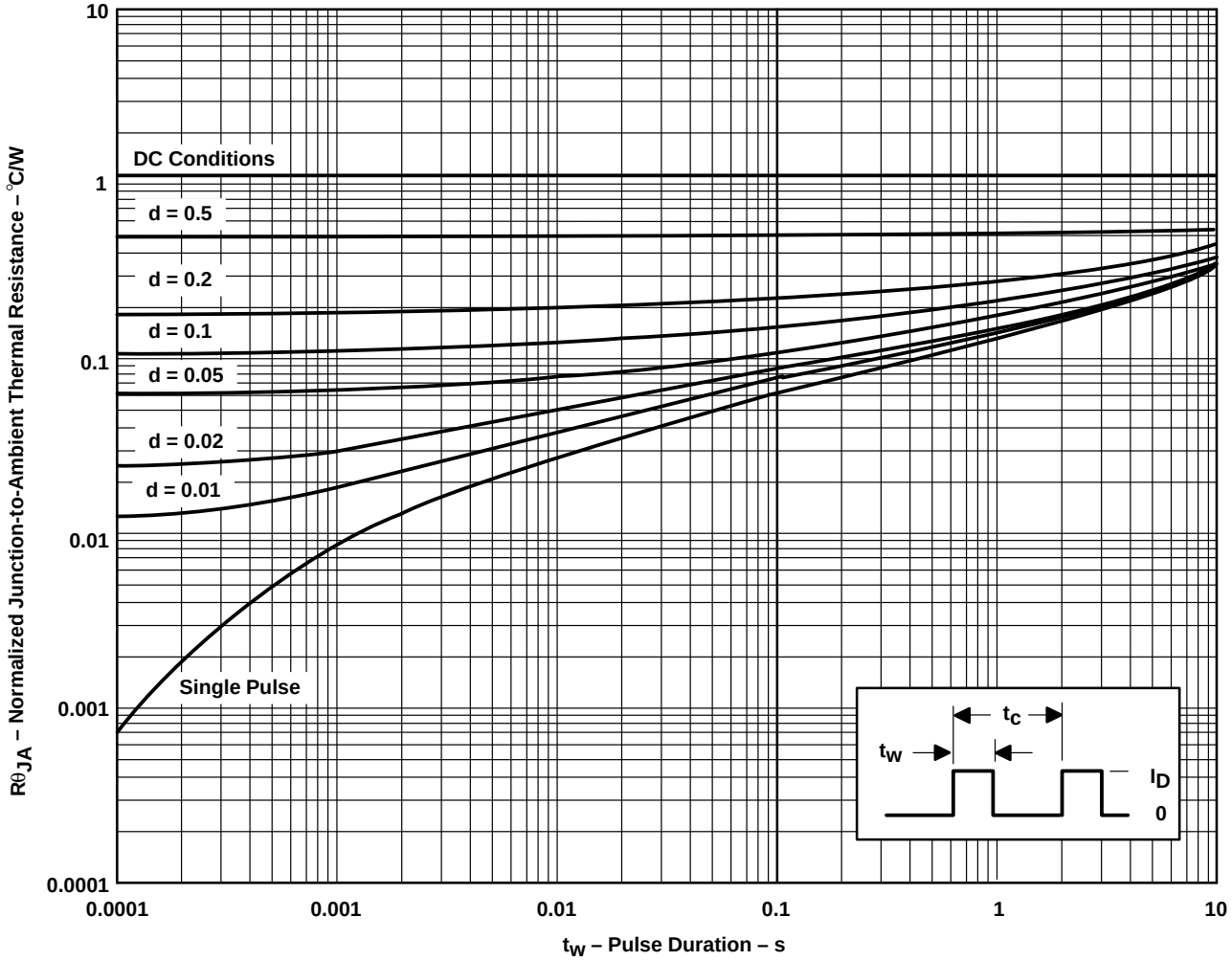


Figure 16

THERMAL INFORMATION

NE PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



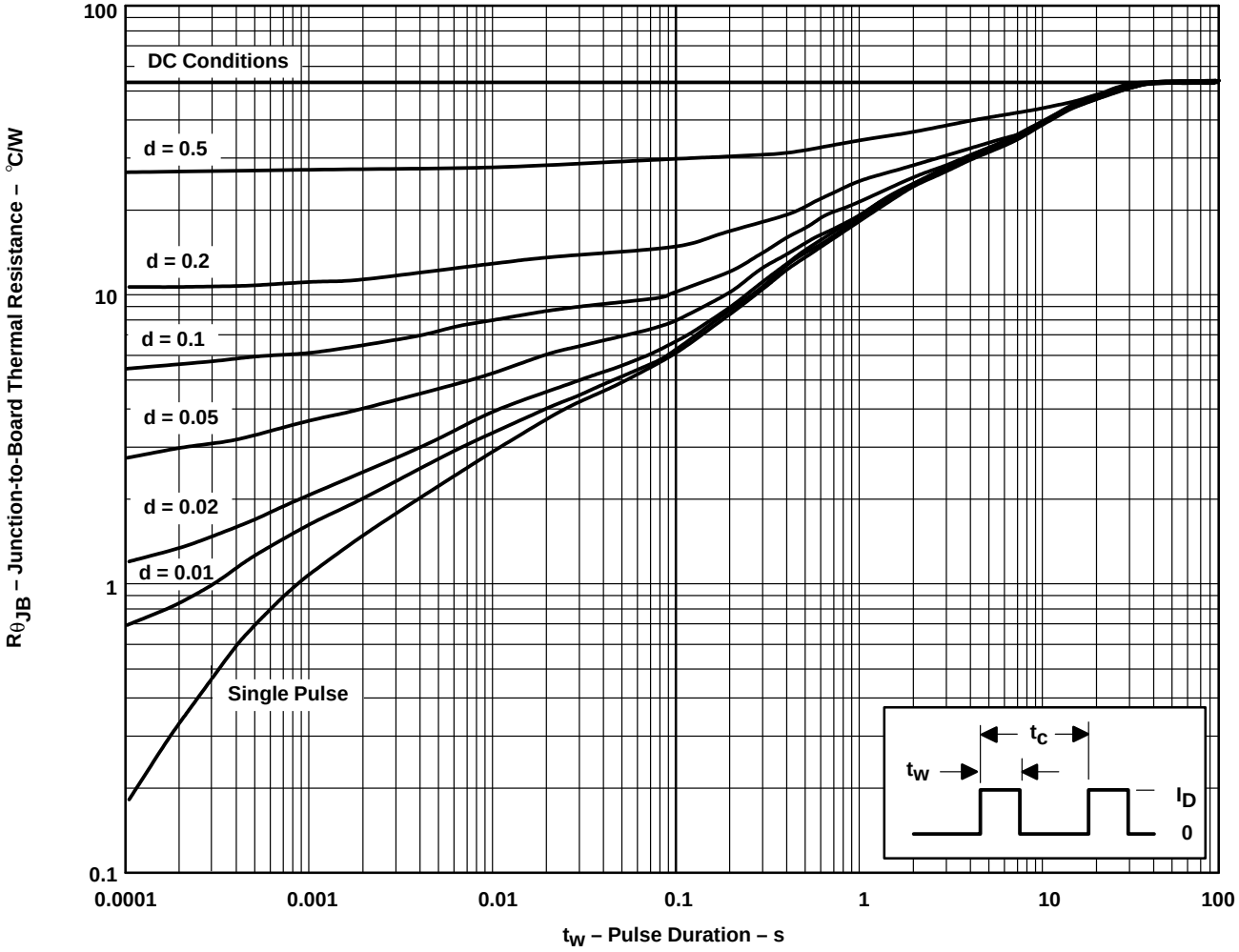
† Device mounted on FR4 printed-circuit board with no heatsink.

NOTES A: $Z_{\theta JA}(t) = r(t)\ R_{\theta JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 17

THERMAL INFORMATION

DW PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
vs
PULSE DURATION



† Device mounted on a 24 in^2, 4-layer FR4 printed-circuit board with no heatsink.

NOTES A: $Z_{\theta JB}(t) = r(t)\ R_{\theta JB}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 18

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- **Low $r_{DS(on)}$ . . . 1 Ω Typ**
- **Output Short-Circuit Protection**
- **Avalanche Energy . . . 75 mJ**
- **Eight 350-mA DMOS Outputs**
- **50-V Switching Capability**
- **Four Distinct Function Modes**
- **Low Power Consumption**

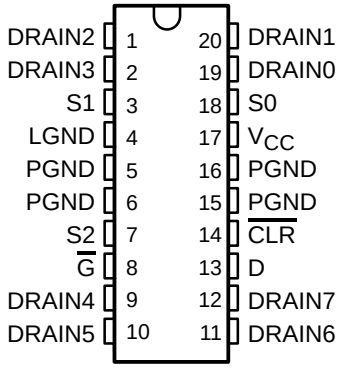
description

This power logic 8-bit addressable latch controls open-drain DMOS-transistor outputs and is designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and decoders or demultiplexers. This is a multifunctional device capable of operating as eight addressable latches or an 8-line demultiplexer with active-low DMOS outputs. Each open-drain DMOS transistor features an independent chopping current-limiting circuit to prevent damage in the case of a short circuit.

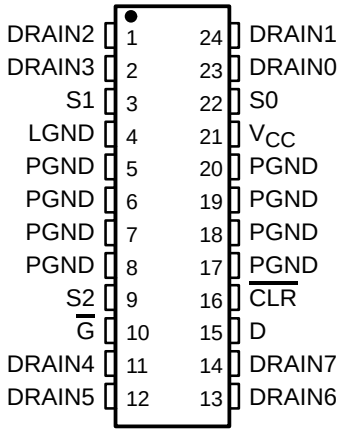
Four distinct modes of operation are selectable by controlling the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in (D) terminal is written into the addressed latch. The addressed DMOS-transistor output inverts the data input with all unaddressed DMOS-transistor outputs remaining in their previous states. In the memory mode, all DMOS-transistor outputs remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latch, enable $\overline{G}$ should be held high (inactive) while the address lines are changing. In the 8-line demultiplexing mode, the addressed output is inverted with respect to the D input and all other outputs are high. In the clear mode, all outputs are high and unaffected by the address and data inputs.

Separate power ground (PGND) and logic ground (LGND) terminals are provided to facilitate maximum system flexibility. All PGND terminals are internally connected, and each PGND terminal must be externally connected to the power system ground in order to minimize parasitic impedance. A single-point connection between LGND and PGND must be made externally in a manner that reduces crosstalk between the logic and load circuits.

NE PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS			OUTPUT OF ADDRESSED DRAIN	EACH OTHER DRAIN	FUNCTION
$\overline{CLR}$	$\overline{G}$	D			
H	L	H	L	Q_{io}	Addressable Latch
H	L	L	H	Q_{io}	
H	H	X	Q_{io}	Q_{io}	Memory
L	L	H	L	H	8-Line Demultiplexer
L	L	L	H	H	
L	H	X	H	H	Clear

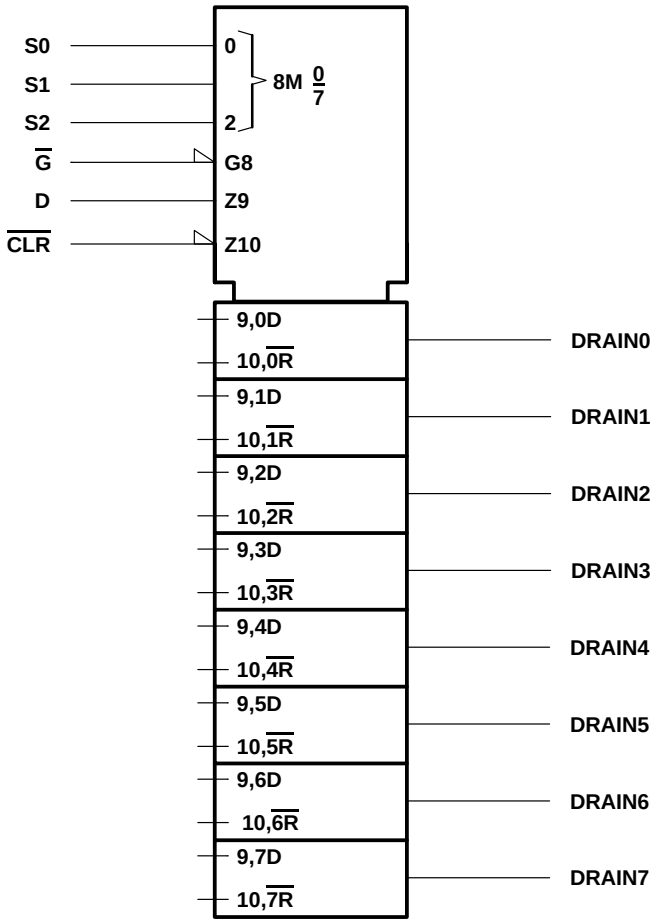
LATCH SELECTION TABLE

SELECT INPUTS			DRAIN ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

description (continued)

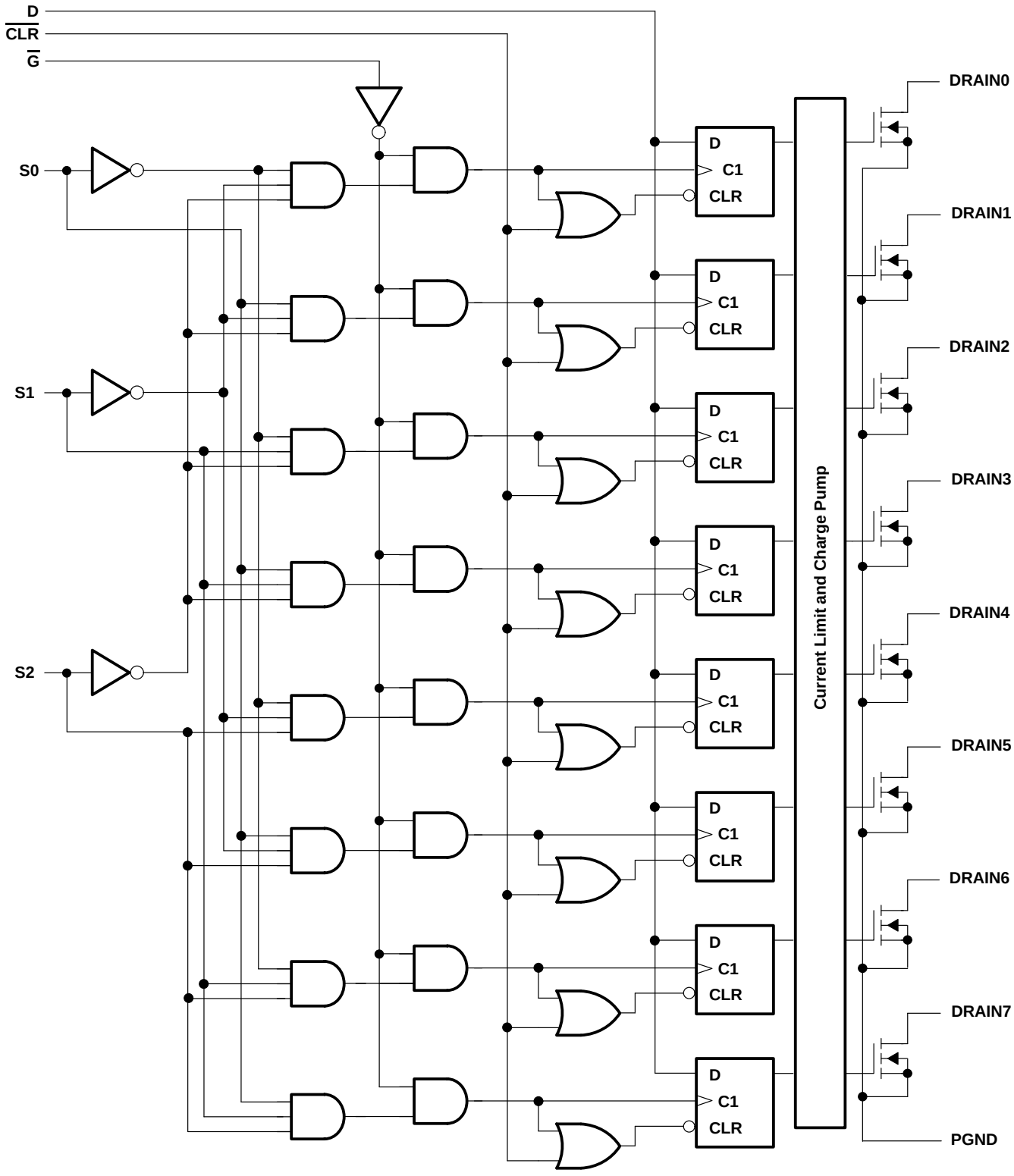
The TPIC6A259 is offered in a thermally-enhanced dual-in-line (NE) package and a wide-body, surface-mount (DW) package. The TPIC6A259 is characterized for operation over the operating case temperature range of –40°C to 125°C.

logic symbol†

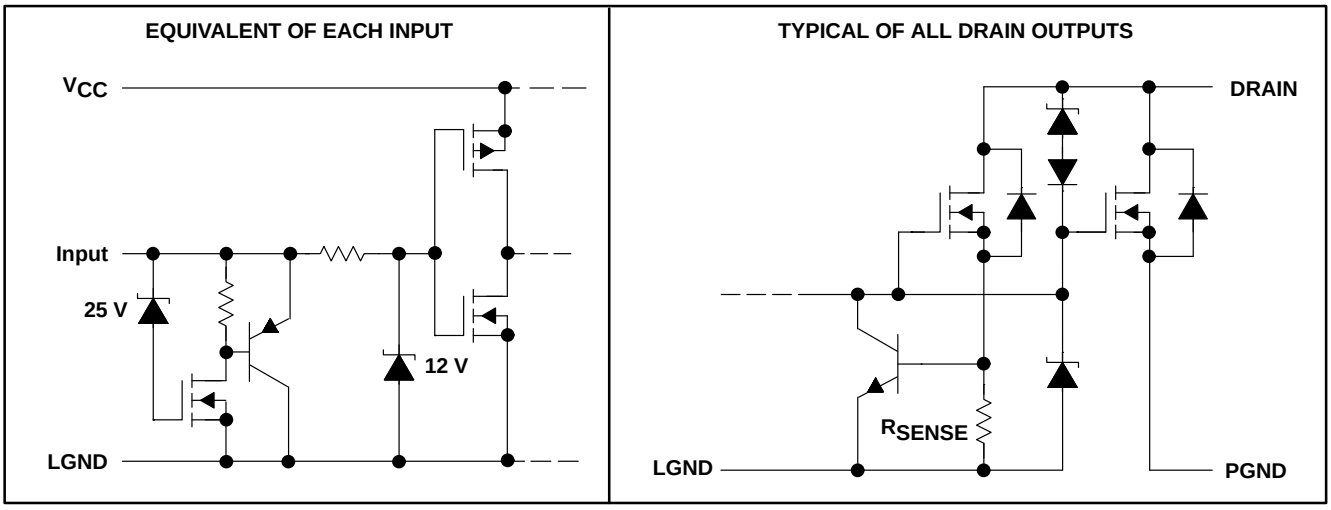


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	–0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	50 V
Continuous source-to-drain diode anode current	1 A
Pulsed source-to-drain diode anode current (see Note 3)	2 A
Pulsed drain current, each output, all outputs on, I_D, T_C = 25°C (see Note 3)	1.1 A
Continuous drain current, each output, all outputs on, I_D, T_C = 25°C	350 mA
Peak drain current single output, T_C = 25°C (see Note 3)	1.1 A
Single-pulse avalanche energy, E_{AS} (see Figure 6)	75 mJ
Avalanche current, I_{AS} (see Note 4)	600 mA
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to LGND and PGND.
2. Each power DMOS source is internally connected to PGND.
3. Pulse duration ≤ 100 µs, and duty cycle ≤ 2%.
4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 210 mH, and I_{AS} = 600 mA (see Figure 6).

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1750 mW	14 mW/°C	350 mW
NE	2500 mW	20 mW/°C	500 mW

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}	V_{CC}	V
Low-level input voltage, V_{IL}	0	0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	–1.8	0.6	A
Setup time, D high before $\overline{G}\uparrow$, t_{su} (see Figure 2)	10		ns
Hold time, D high before $\overline{G}\uparrow$, t_h (see Figure 2)	5		ns
Pulse duration, t_w (see Figure 2)	15		ns
Operating case temperature, T_C	–40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 1 mA			50			V
V_{SD}	Source-to-drain diode forward voltage	I_F = 350 mA,	See Note 3			0.8	1.1	V
I_{IH}	High-level input current	$V_I = V_{CC}$					1	µA
I_{IL}	Low-level input current	V_I = 0					–1	µA
I_{CC}	Logic supply current	I_O = 0,	$V_I = V_{CC}$ or 0			0.5	5	mA
I_{OK}	Output current at which chopping starts	T_C = 25°C,	See Note 5 and Figures 3 and 4		0.6	0.8	1.1	A
$I_{(nom)}$	Nominal current	$V_{DS(on)}$ = 0.5 V, V_{CC} = 5 V,	$I_{(nom)} = I_D$, T_C = 85°C, See Notes 5, 6, and 7			350		mA
I_D	Off-state drain current	V_{DS} = 40 V,	T_C = 25°C			0.1	1	µA
		V_{DS} = 40 V,	T_C = 125°C			0.2	5	
$r_{DS(on)}$	Static drain-to-source on-state resistance	I_D = 350 mA,	T_C = 25°C	See Notes 5 and 6 and Figures 9 and 10		1	1.5	Ω
		I_D = 350 mA,	T_C = 125°C			1.7	2.5	

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output from D	C_L = 30 pF,	I_D = 350 mA, See Figures 1, 2, and 11		30		ns
t_{PLH}	Propagation delay time, low- to high-level output from D				125		ns
t_r	Rise time, drain output				60		ns
t_f	Fall time, drain output				30		ns
t_a	Reverse-recovery-current rise time	I_F = 350 mA,	di/dt = 20 A/µs, See Notes 5 and 6 and Figure 5		100		ns
t_{rr}	Reverse-recovery time				300		ns

NOTES: 3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

thermal resistance

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case	DW	All eight outputs with equal power		10	°C/W
		NE			10	
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW	All eight outputs with equal power		50	°C/W
		NE			50	

PARAMETER MEASUREMENT INFORMATION

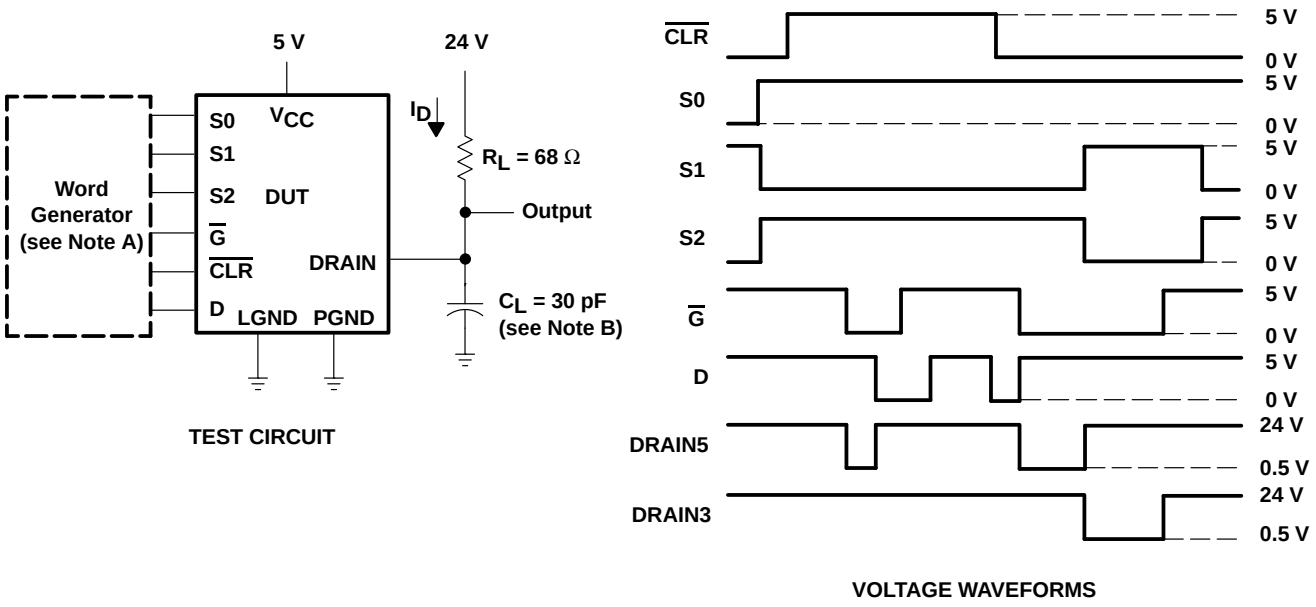


Figure 1. Typical Operation Mode

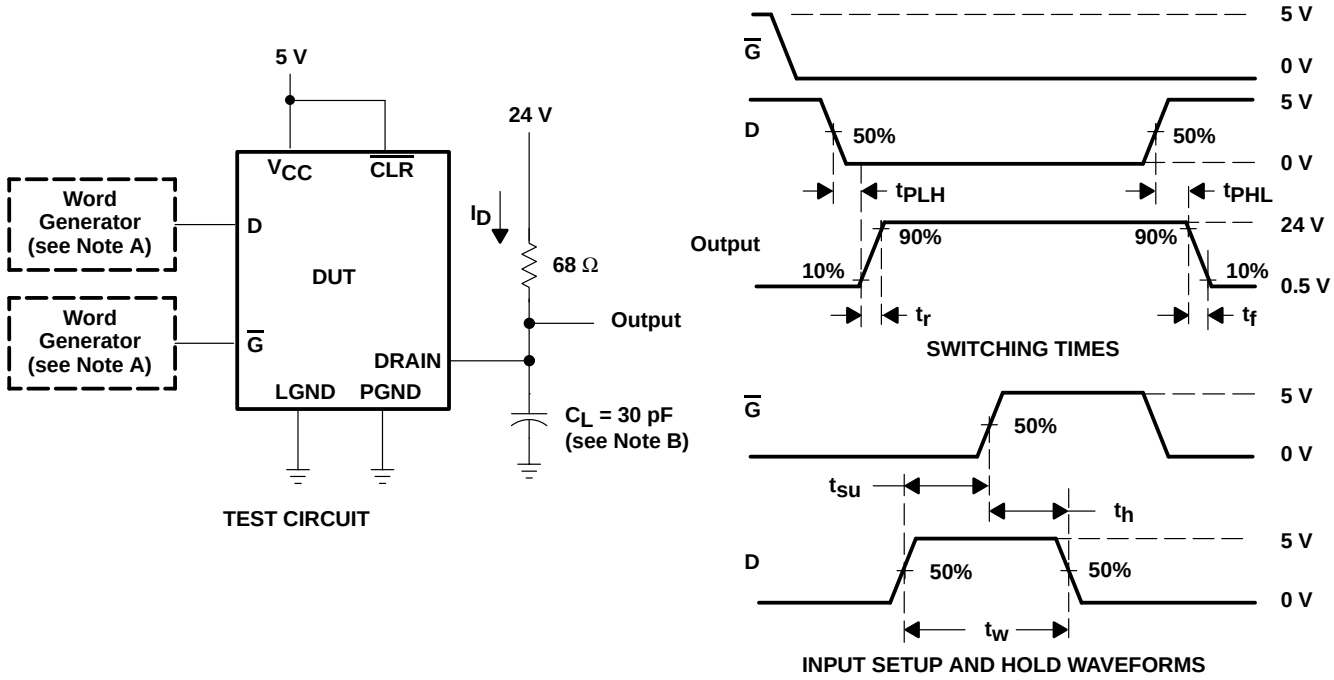
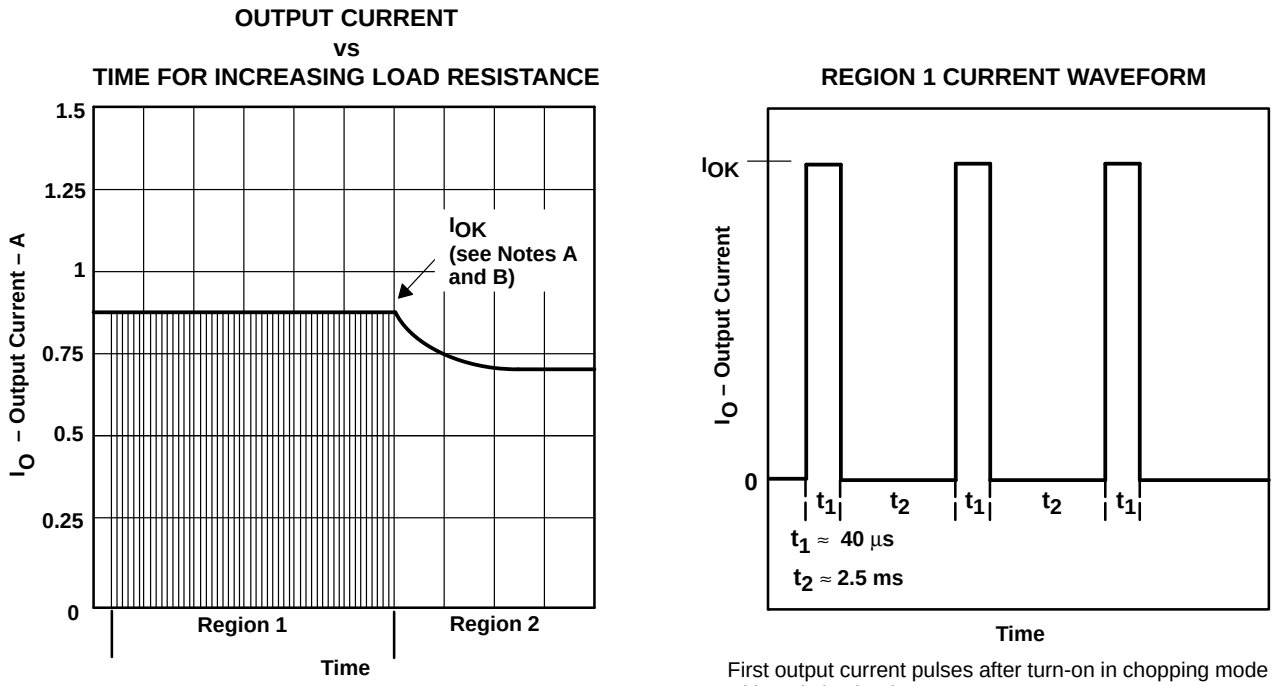


Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



First output current pulses after turn-on in chopping mode with resistive load.

NOTES: A. Figure 3 illustrates the output current characteristics of the device energizing a load having initially low, increasing resistance, e.g., an incandescent lamp. In region 1, chopping occurs and the peak current is limited to I_{OK}. In region 2, output current is continuous. The same characteristics occur in reverse order when the device energizes a load having an initially high, decreasing resistance.
B. Region 1 duty cycle is approximately 2%.

Figure 3. Chopping-Mode Characteristics

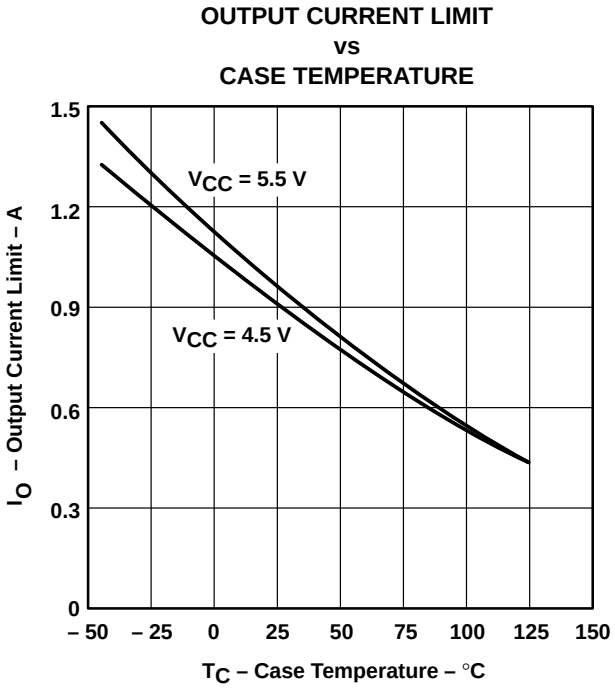
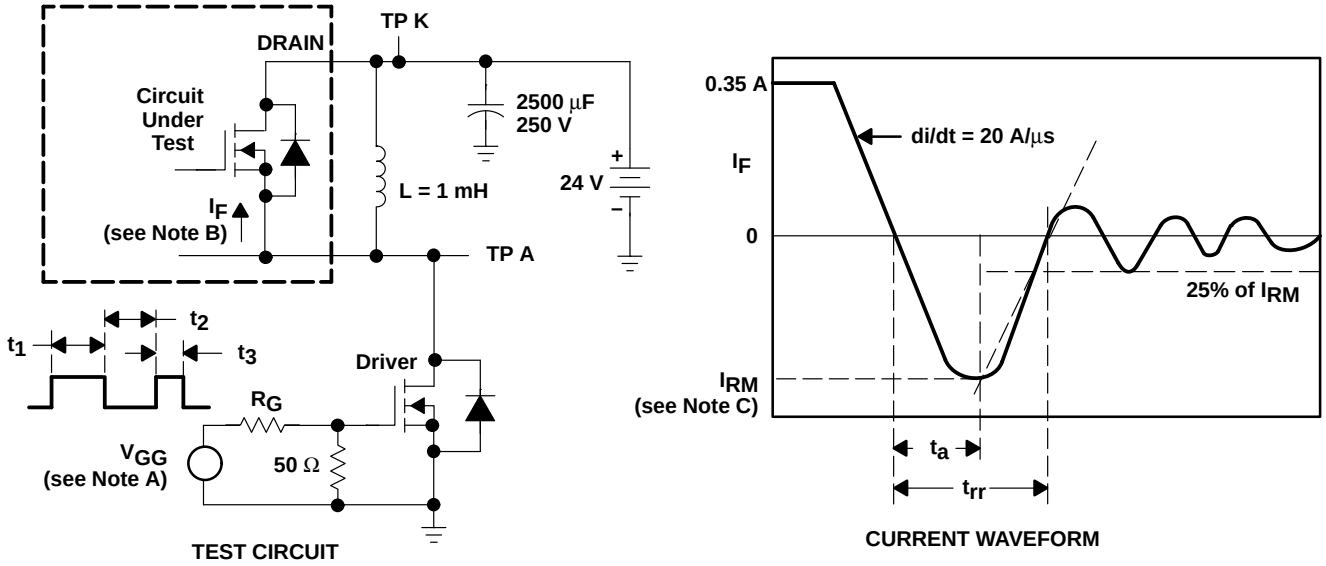


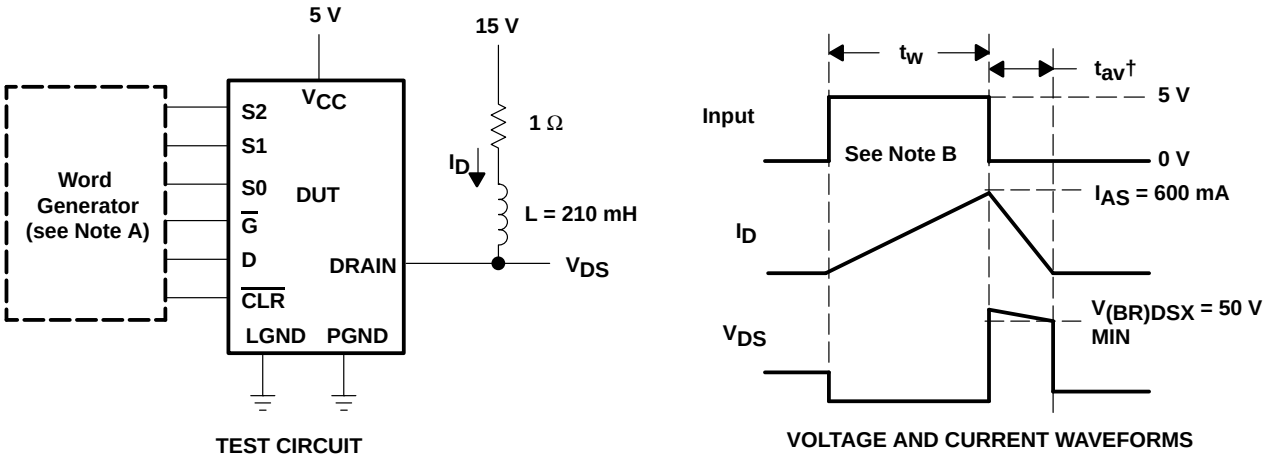
Figure 4

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/μs. A V_{GG} double-pulse train is used to set I_F = 0.35 A, where t_1 = 10 μs, t_2 = 7 μs, and t_3 = 3 μs.
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
C. I_{RM} = maximum recovery current

Figure 5. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



† Non-JEDEC symbol for avalanche time.

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, Z_O = 50 Ω.
B. Input pulse duration, t_w, is increased until peak current I_{AS} = 600 mA.
Energy test level is defined as $E_{AS} = (I_{AS} \times V_{(BR)DSX} \times t_{av})/2$ = 75 mJ.

Figure 6. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

MAXIMUM CONTINUOUS DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

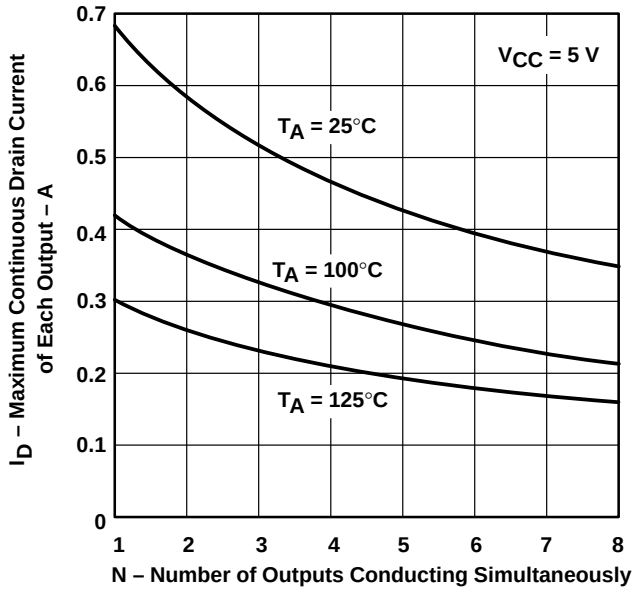


Figure 7

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

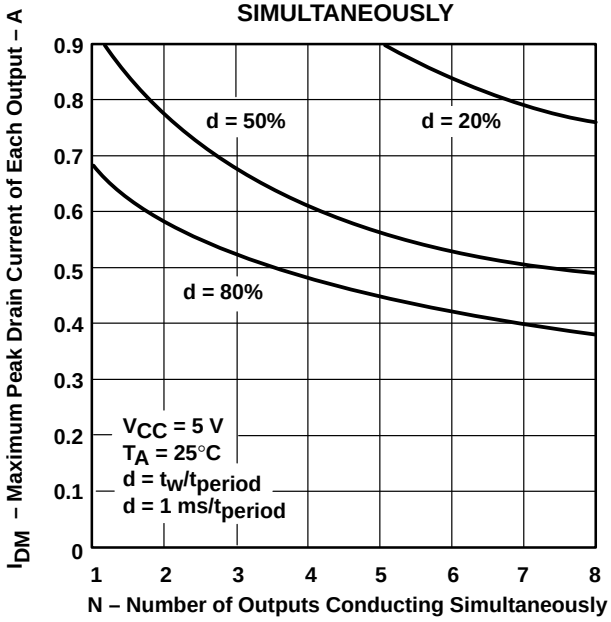


Figure 8

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

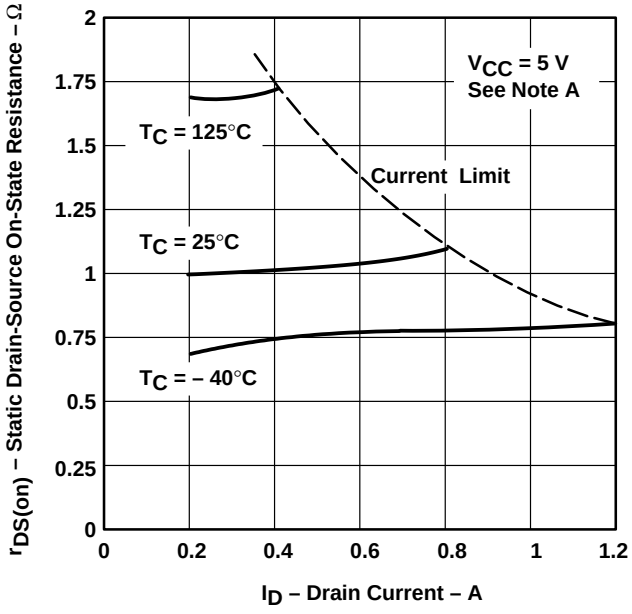


Figure 9

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

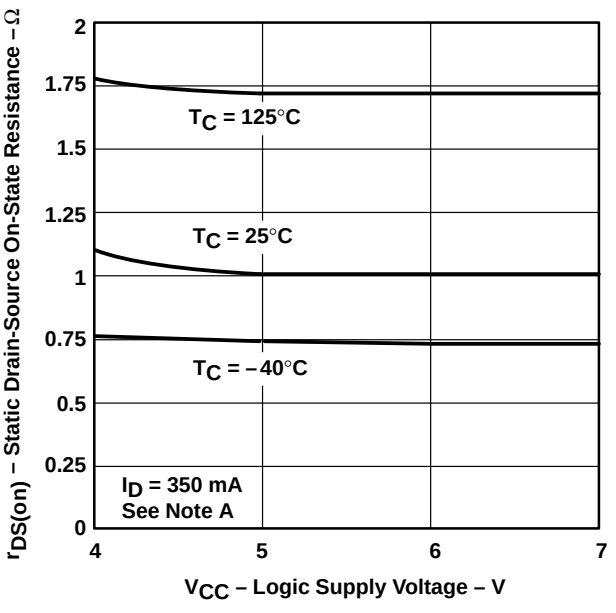
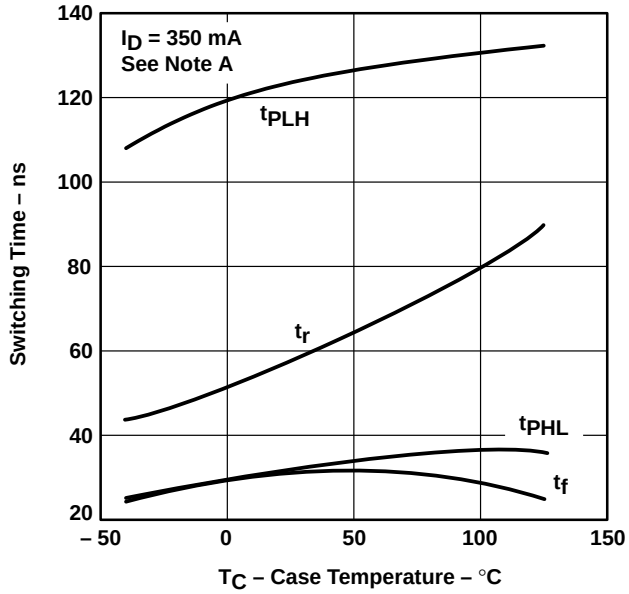


Figure 10

NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

TYPICAL CHARACTERISTICS

SWITCHING TIME vs CASE TEMPERATURE

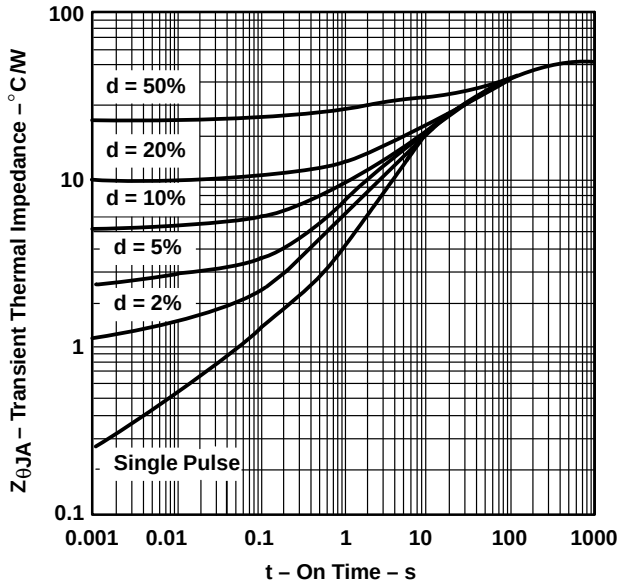


NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 11

THERMAL INFORMATION

NE PACKAGE TRANSIENT THERMAL IMPEDANCE vs ON TIME



The single-pulse curve represents measured data. The curves for various pulse durations are based on the following equation:

$$Z_{\theta JA} = \left| \frac{t_w}{t_c} \right| R_{\theta JA} + \left| 1 - \frac{t_w}{t_c} \right| Z_\theta(t_w + t_c) + Z_\theta(t_w) - Z_\theta(t_c)$$

Where:

$Z_\theta(t_w)$ = the single-pulse thermal impedance for t = t_w seconds

$Z_\theta(t_c)$ = the single-pulse thermal impedance for t = t_c seconds

$Z_\theta(t_w + t_c)$ = the single-pulse thermal impedance for t = $t_w + t_c$ seconds

$d = t_w/t_c$

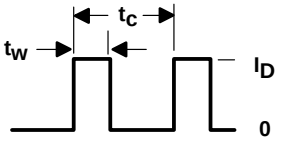


Figure 12

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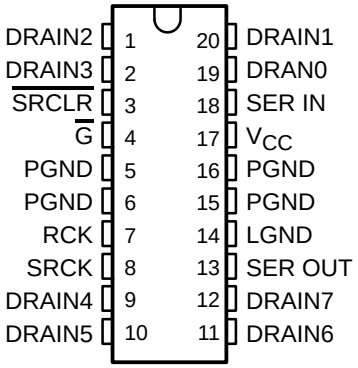
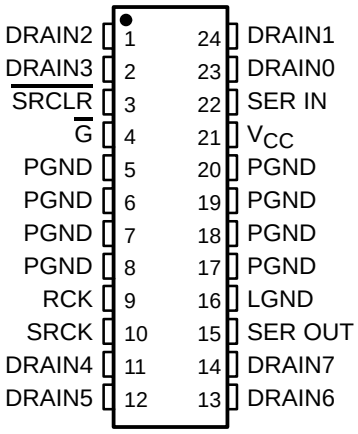
- **Low $r_{DS(on)}$ . . . 1 Ω Typ**
- **Output Short-Circuit Protection**
- **Avalanche Energy . . . 75 mJ**
- **Eight 350-mA DMOS Outputs**
- **50-V Switching Capability**
- **Devices Are Cascadable**
- **Low Power Consumption**

NE PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



description

The TPIC6A595 is a monolithic, high-voltage, high-current power logic 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads. Each open-drain DMOS transistor features an independent chopping current-limiting circuit to prevent damage in the case of a short circuit.

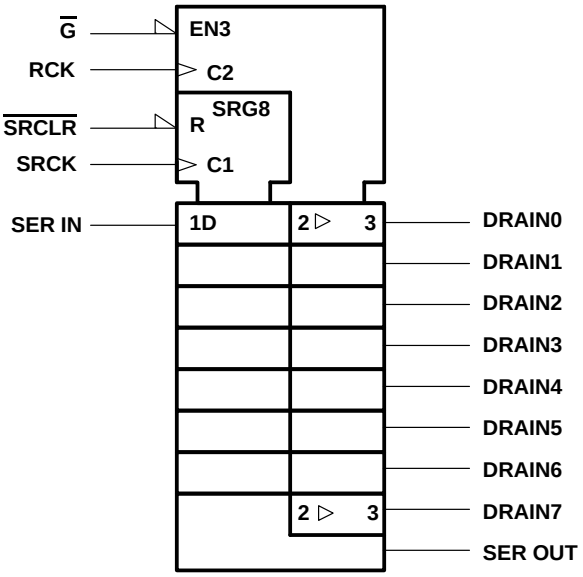
This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit, D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear ($\overline{\text{SRCLR}}$) is high. When $\overline{\text{SRCLR}}$ is low, the input shift register is cleared. When output enable ($\overline{\text{G}}$) is held high, all data in the output buffers is held low and all drain outputs are off. When $\overline{\text{G}}$ is held low, data from the storage register is transparent to the output buffers. The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices.

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and a 350-mA continuous sink current capability. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink current capability.

Separate power ground (PGND) and logic ground (LGND) terminals are provided to facilitate maximum system flexibility. All PGND terminals are internally connected, and each PGND terminal must be externally connected to the power system ground in order to minimize parasitic impedance. A single-point connection between LGND and PGND must be made externally in a manner that reduces crosstalk between the logic and load circuits.

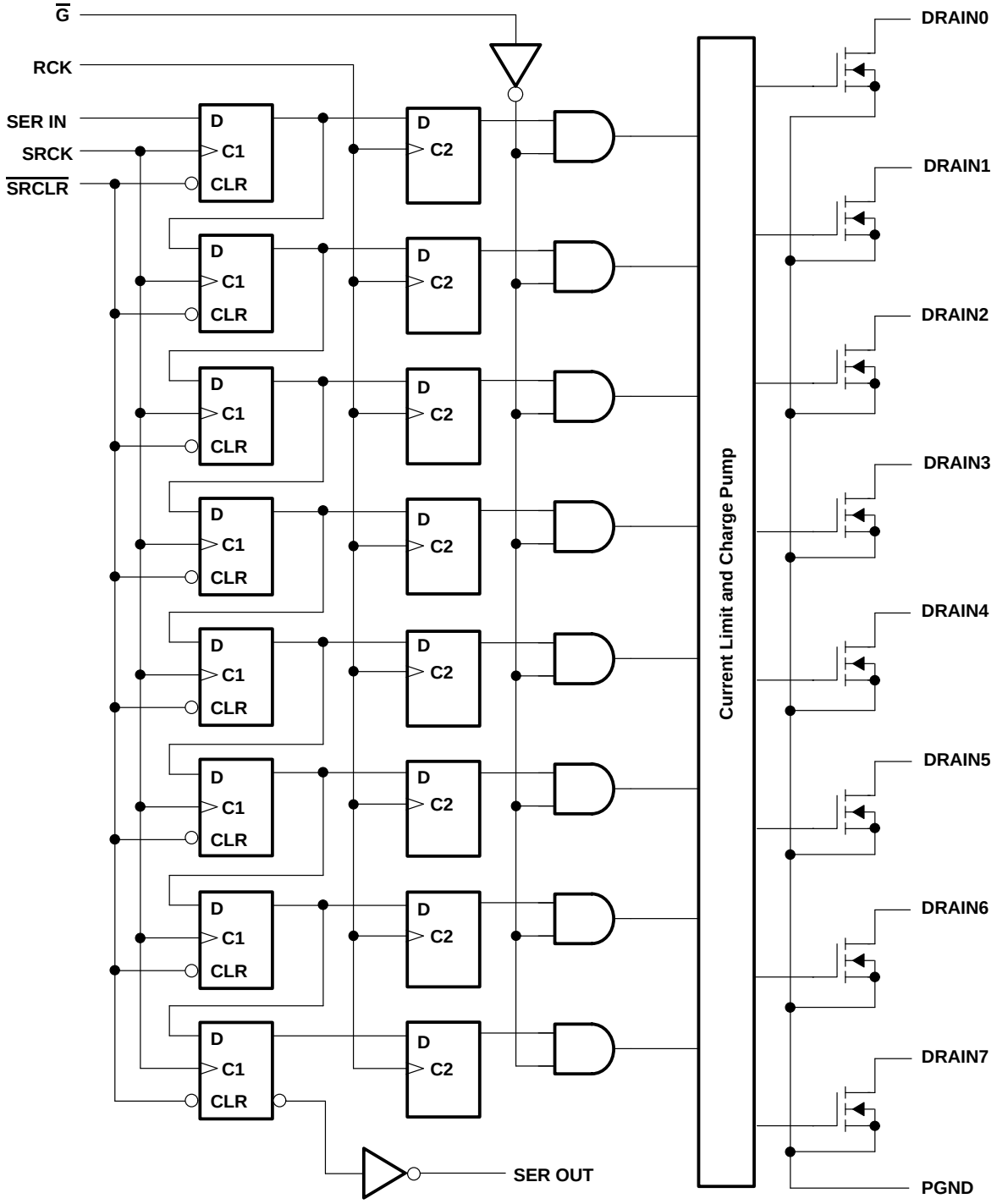
The TPIC6A595 is offered in a thermally-enhanced dual-in-line (NE) package and a wide-body surface-mount (DW) package. The TPIC6A595 is characterized for operation over the operating case temperature range of –40°C to 125°C.

logic symbol†

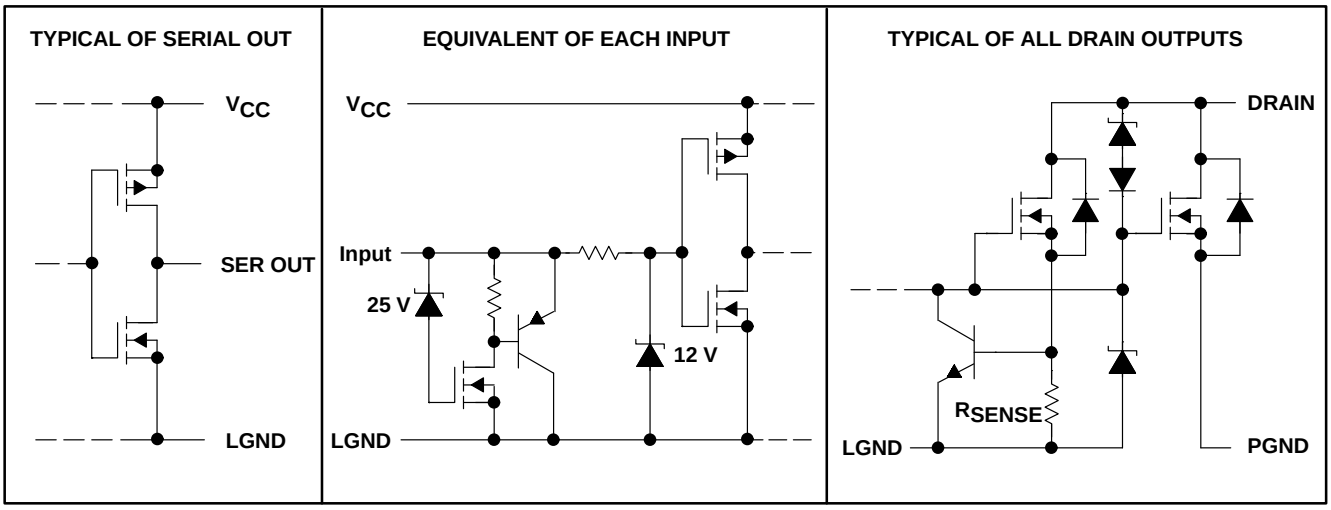


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	–0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	50 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current (see Note 3)	2 A
Pulsed drain current, each output, all outputs on, I_{Dn}, T_A = 25°C (see Note 3)	1.1 A
Continuous drain current, each output, all outputs on, I_{Dn}, T_A = 25°C	350 mA
Peak drain current, single output, T_A = 25°C (see Note 3)	1.1 A
Single-pulse avalanche energy, E_{AS} (see Figure 6)	75 mJ
Avalanche current, I_{AS} (see Note 4)	600 mA
Continuous total dissipation	See Dissipation Rating Table
Operating case temperature range, T_C	–40°C to 125°C
Operating virtual junction temperature range, T_J	–40°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to LGND and PGND.
2. Each power DMOS source is internally connected to PGND.
3. Pulse duration ≤ 100 µs and duty cycle ≤ 2 %.
4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 210 mH, I_{AS} = 600 mA (see Figure 6).

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1750 mW	14 mW/°C	350 mW
NE	2500 mW	20 mW/°C	500 mW

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}	V_{CC}	V
Low-level input voltage, V_{IL}	0	0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	–1.8	0.6	A
Setup time, SER IN high before SRCK↑, t_{su} (see Figure 2)	10		ns
Hold time, SER IN high after SRCK↑, t_h (see Figure 2)	10		ns
Pulse duration, t_w (see Figure 2)	20		ns
Operating case temperature, T_C	–40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 1 mA		50			V
V_{SD}	Source-to-drain diode forward voltage	I_F = 350 mA,	See Note 3		0.8	1.1	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = –20 µA		V_{CC}–0.1	V_{CC}		V
		I_{OH} = –4 mA		V_{CC}–0.5	V_{CC}–0.2		
V_{OL}	Low-level output voltage, SER OUT	I_{OL} = 20 µA			0	0.1	V
		I_{OL} = 4 mA			0.2	0.5	
I_{IH}	High-level input current	$V_I = V_{CC}$				1	µA
I_{IL}	Low-level input current	V_I = 0				–1	µA
$I_{O(chop)}$	Output current at which chopping starts	T_C = 25°C, See Note 5 and Figures 3 and 4		0.6	0.8	1.1	A
I_{CC}	Logic supply current	I_O = 0,	$V_I = V_{CC}$ or 0		0.5	5	mA
$I_{CC(FRQ)}$	Logic supply current at frequency	f_{SRCK} = 5 MHz, $V_I = V_{CC}$ or 0,	I_O = 0, V_{CC} = 5 V, C_L = 30 pF, See Figure 7		1.3		mA
$I_{(nom)}$	Nominal current	$V_{DS(on)}$ = 0.5 V, V_{CC} = 5 V,	$I_{(nom)} = I_D$, T_C = 85°C, See Notes 5, 6, and 7		350		mA
I_D	Drain current, off-state	V_{DS} = 40 V,	T_C = 25°C		0.1	1	µA
		V_{DS} = 40 V,	T_C = 125°C		0.2	5	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 350 mA,	T_C = 25°C; See Notes 5 and 6 and Figures 10 and 11		1	1.5	Ω
		I_D = 350 mA,	T_C = 125°C		1.7	2.5	
		I_D = 350 mA,	T_C = 40°C				

NOTES: 3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

switching characteristics, V_{CC} = 5 V, T_C = 25°C

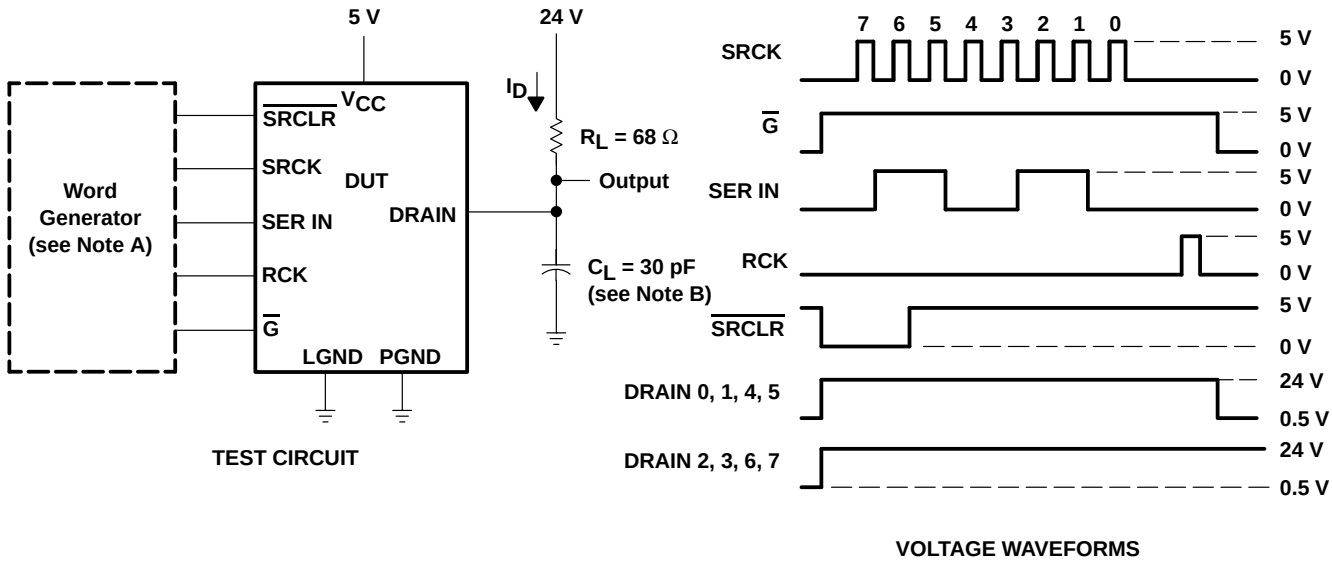
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$	C_L = 30 pF, I_D = 350 mA, See Figures 1, 2, and 12		30		ns
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$			125		ns
t_r	Rise time, drain output			60		ns
t_f	Fall time, drain output			30		ns
t_a	Reverse-recovery-current rise time	I_F = 350 mA, di/dt = 20 A/µs, See Notes 5 and 6 and Figure 5		100		ns
t_{rr}	Reverse-recovery time			300		ns

NOTES: 5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal resistance

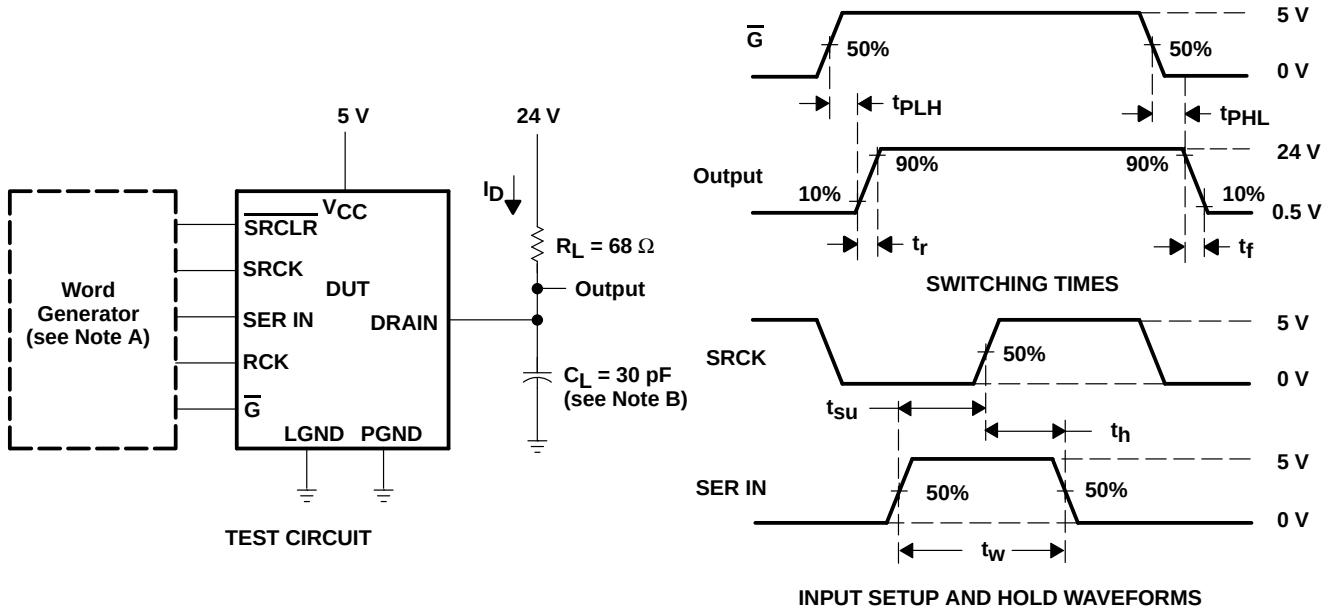
PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case	DW	All eight outputs with equal power		10	°C/W
		NE			10	
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW	All eight outputs with equal power		50	°C/W
		NE			50	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

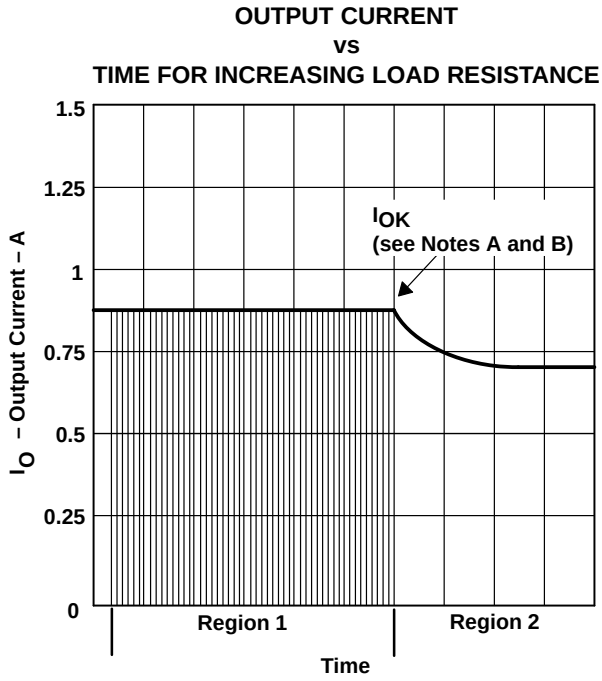
Figure 1. Resistive Load Operation

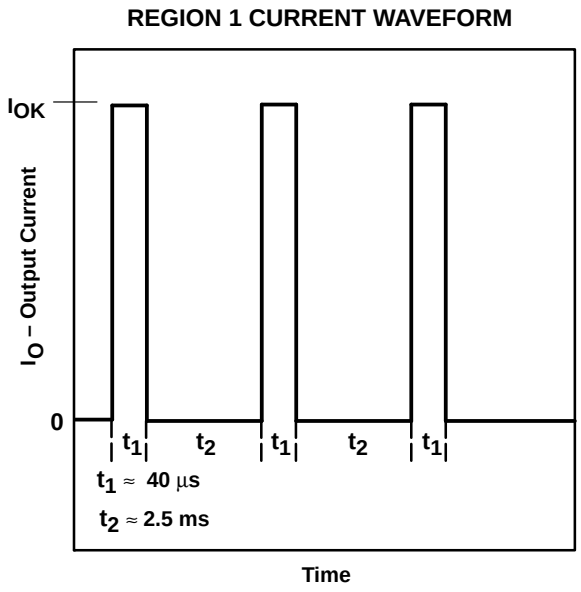


NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION





First output current pulses after turn-on in chopping mode with resistive load.

NOTES: A. Figure 3 illustrates the output current characteristics of the device energizing a load having initially low, increasing resistance, e.g., an incandescent lamp. In region 1, chopping occurs and the peak current is limited to I_{OK}. In region 2, output current is continuous. The same characteristics occur in reverse order when the device energizes a load having an initially high, decreasing resistance.
B. Region 1 duty cycle is approximately 2%.

Figure 3. Chopping-Mode Characteristics

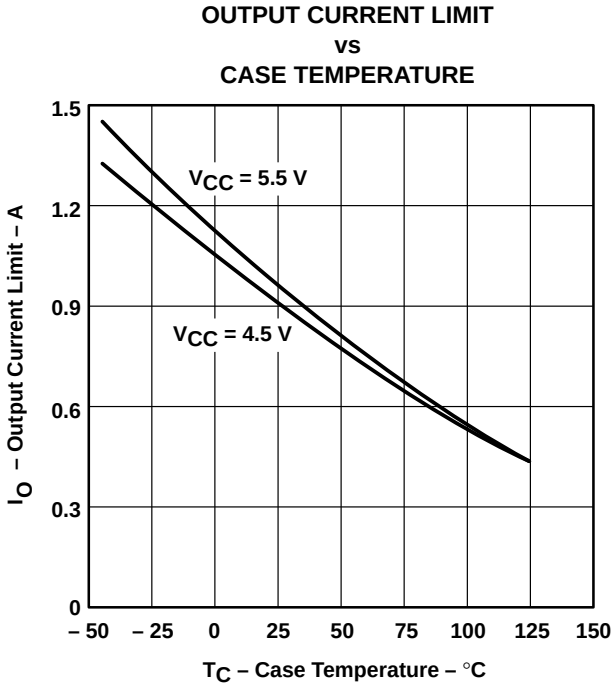
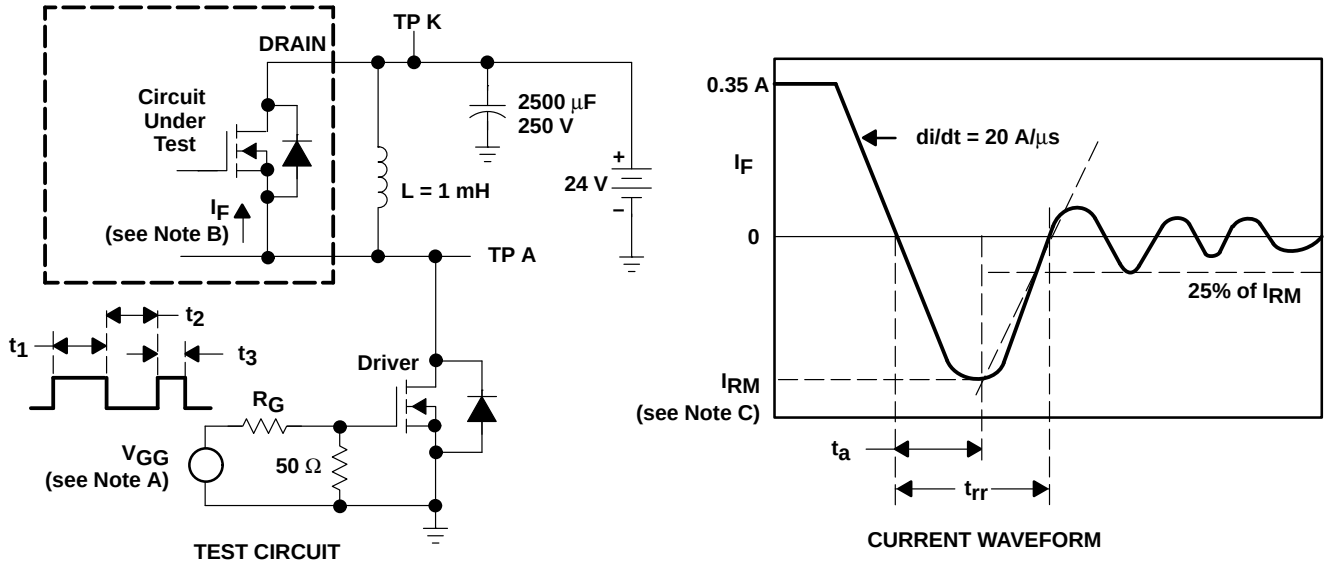


Figure 4

PARAMETER MEASUREMENT INFORMATION

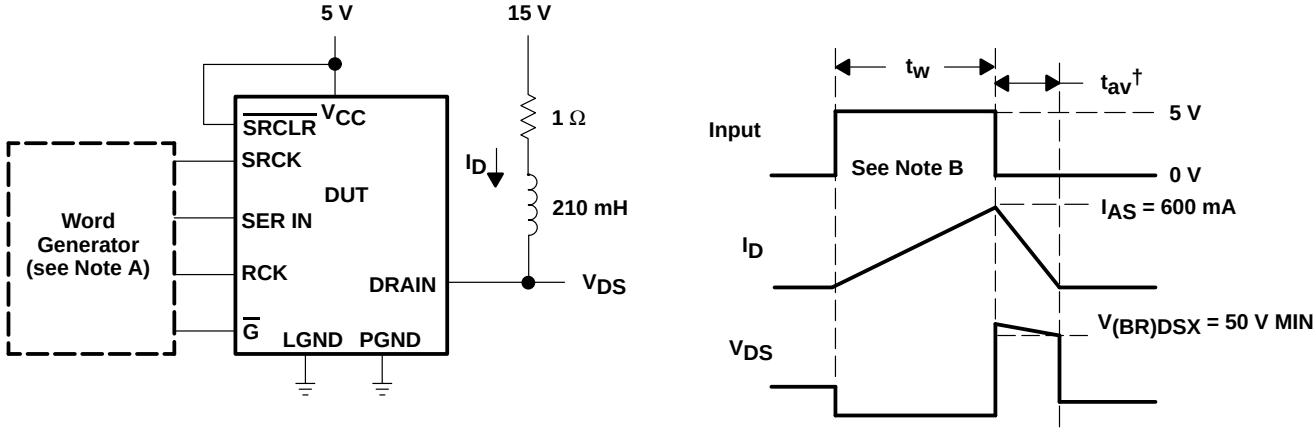


NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/μs. A V_{GG} double-pulse train is used to set I_F = 0.35 A, where t_1 = 10 μs, t_2 = 7 μs, and t_3 = 3 μs.

B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

C. I_{RM} = maximum recovery current

Figure 5. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



† Non JEDEC symbol for avalanche time.

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, Z_O = 50 Ω.

B. Input pulse duration, t_w, is increased until peak current I_{AS} = 600 mA.
Energy test level is defined as $E_{AS} = (I_{AS} \times V_{(BR)DSX} \times t_{av})/2$ = 75 mJ.

Figure 6. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREQUENCY

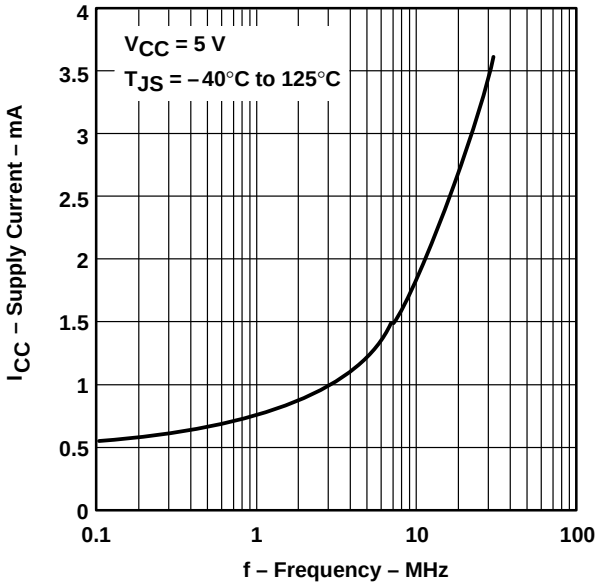


Figure 7

MAXIMUM CONTINUOUS DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

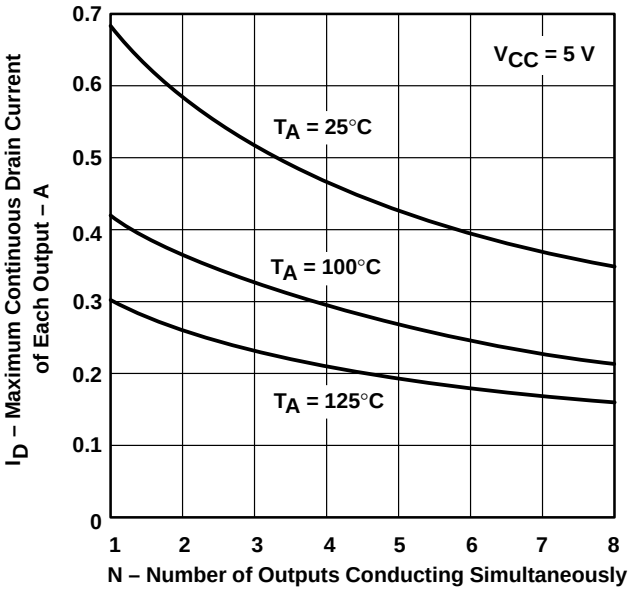


Figure 8

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

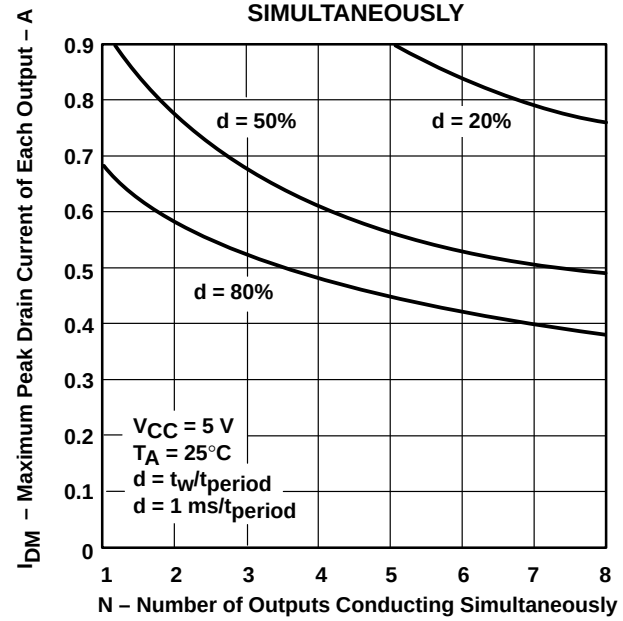
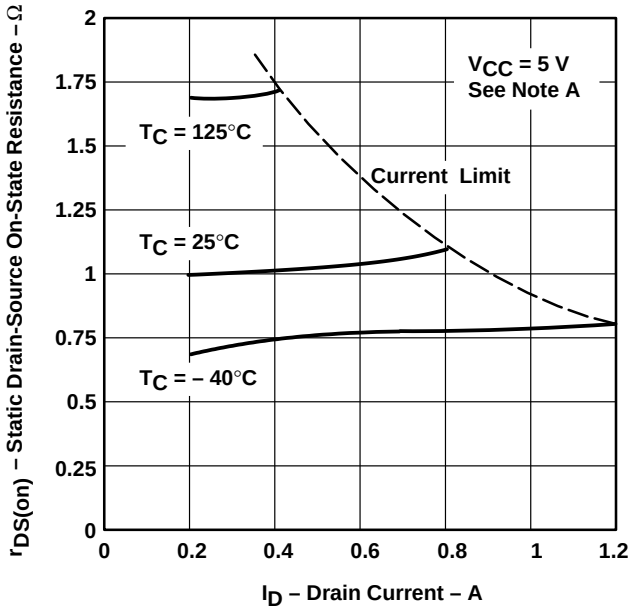


Figure 9

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT



NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 10

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

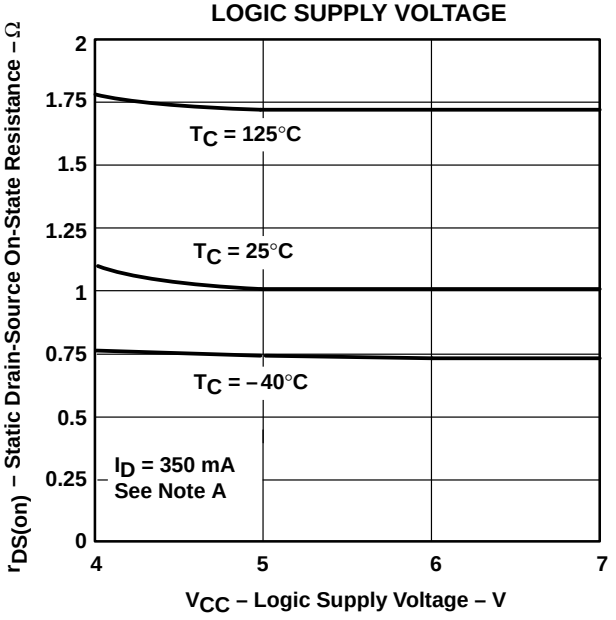


Figure 11

SWITCHING TIME vs CASE TEMPERATURE

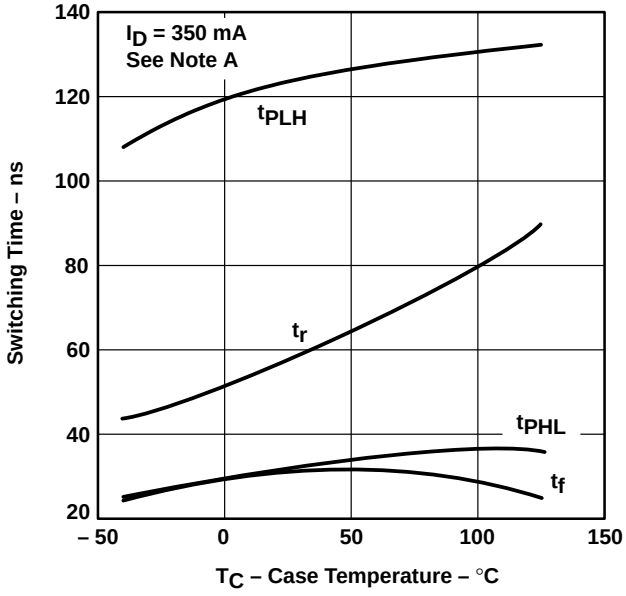
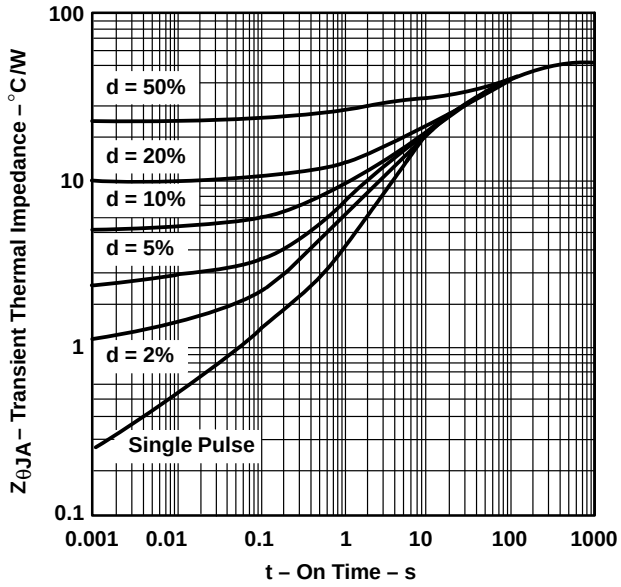


Figure 12

NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

THERMAL INFORMATION

NE PACKAGE TRANSIENT THERMAL IMPEDANCE vs ON TIME



The single-pulse curve represents measured data. The curves for various pulse durations are based on the following equation:

$$Z_{\theta JA} = \left| \frac{t_w}{t_c} \right| R_{\theta JA} + \left| 1 - \frac{t_w}{t_c} \right| Z_\theta(t_w + t_c) + Z_\theta(t_w) - Z_\theta(t_c)$$

Where:

$Z_\theta(t_w)$ = the single-pulse thermal impedance for t = t_w seconds

$Z_\theta(t_c)$ = the single-pulse thermal impedance for t = t_c seconds

$Z_\theta(t_w + t_c)$ = the single-pulse thermal impedance for t = $t_w + t_c$ seconds

$d = t_w/t_c$

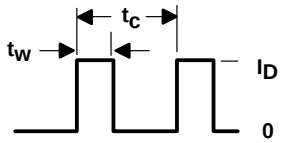


Figure 13

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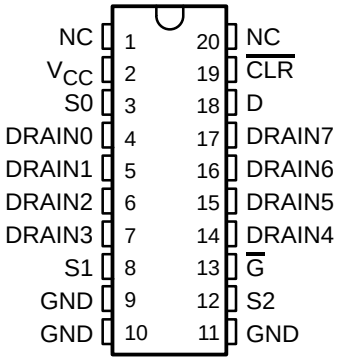
- **Low $r_{DS(on)}$ . . . 5 Ω Typical**
- **Avalanche Energy . . . 30 mJ**
- **Eight Power DMOS-Transistor Outputs of 150-mA Continuous Current**
- **500-mA Typical Current-Limiting Capability**
- **Output Clamp Voltage . . . 50 V**
- **Four Distinct Function Modes**
- **Low Power Consumption**

DW OR N PACKAGE
(TOP VIEW)



NC – No internal connection

description

This power logic 8-bit addressable latch controls open-drain DMOS-transistor outputs and is designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and decoders or demultiplexers. This is a multi-functional device capable of storing single-line data in eight addressable latches and 3-to-8 decoder or demultiplexer with active-low DMOS outputs.

Four distinct modes of operation are selectable by controlling the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in (D) terminal is written into the addressed latch. The addressed DMOS-transistor output inverts the data input with all unaddressed DMOS-transistor outputs remaining in their previous states. In the memory mode, all DMOS-transistor outputs remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latch, enable $\overline{G}$ should be held high (inactive) while the address lines are changing. In the 3-to-8 decoding or demultiplexing mode, the addressed output is inverted with respect to the D input and all other outputs are off. In the clear mode, all outputs are off and unaffected by the address and data inputs. When data is low for a given output, the DMOS-transistor output is off. When data is high, the DMOS-transistor output has sink-current capability.

FUNCTION TABLE

INPUTS			OUTPUT OF ADDRESSED DRAIN	EACH OTHER DRAIN	FUNCTION
$\overline{CLR}$	$\overline{G}$	D			
H	L	H	L	Q_{io}	Addressable Latch
H	L	L	H	Q_{io}	
H	H	X	Q_{io}	Q_{io}	Memory
L	L	H	L	H	8-Line Demultiplexer
L	L	L	H	H	
L	H	X	H	H	Clear

LATCH SELECTION TABLE

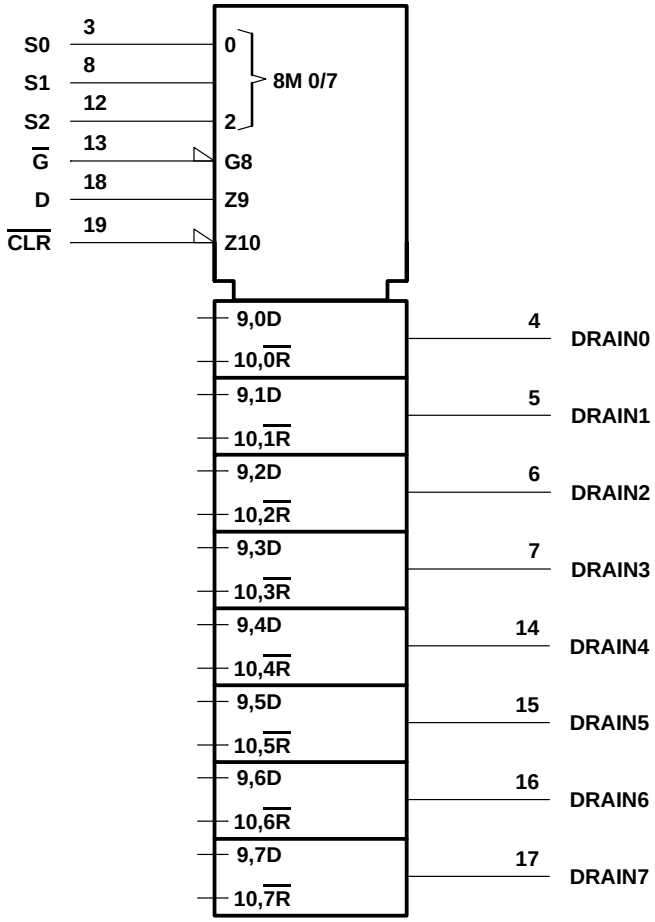
SELECT INPUTS			DRAIN ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H = high level, L = low level

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink-current capability. Each output provides a 500-mA typical current limit at T_C = 25°C. The current limit decreases as the junction temperature increases for additional device protection.

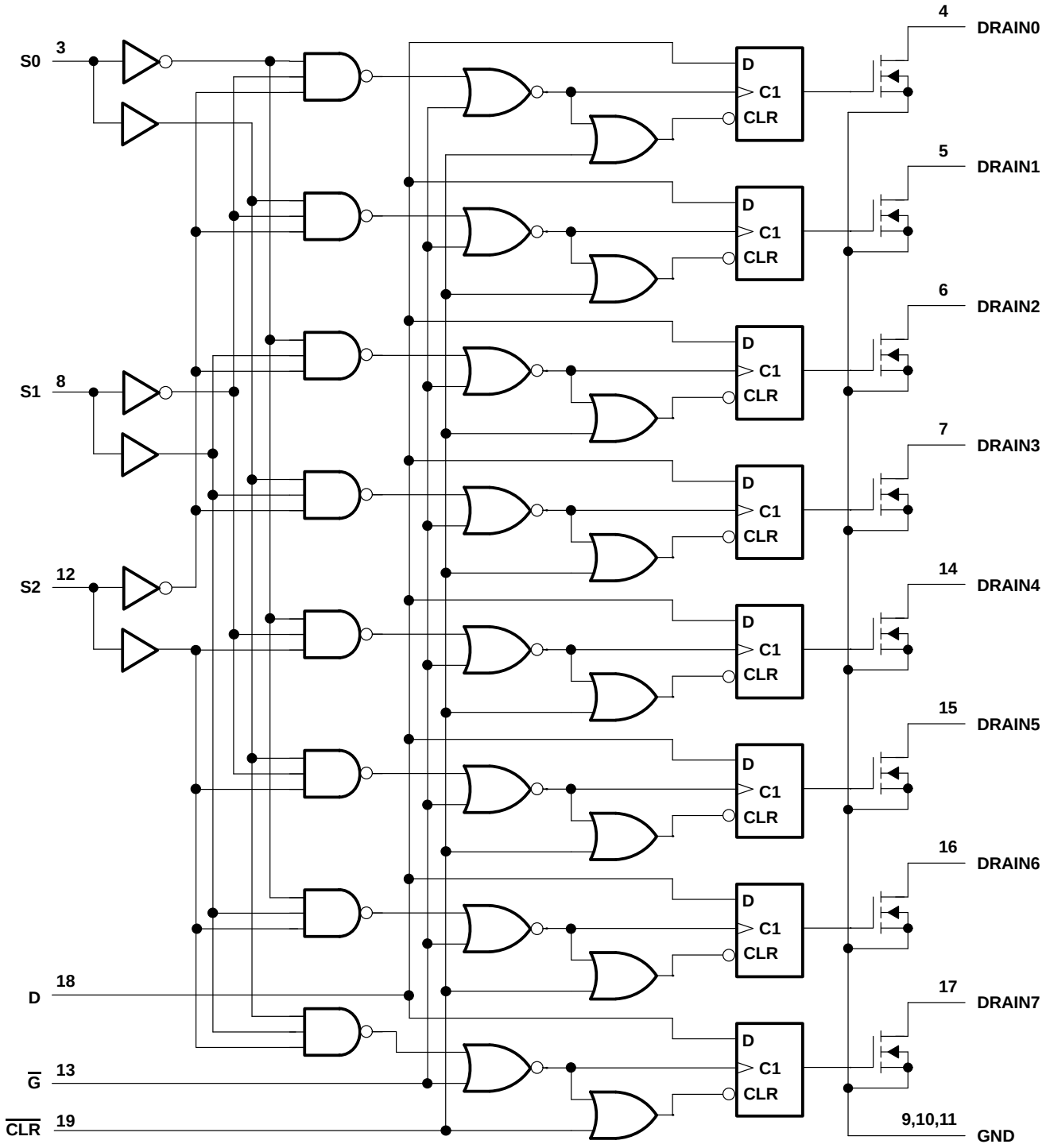
The TPIC6B259 is characterized for operation over the operating case temperature range of −40°C to 125°C.

logic symbol†

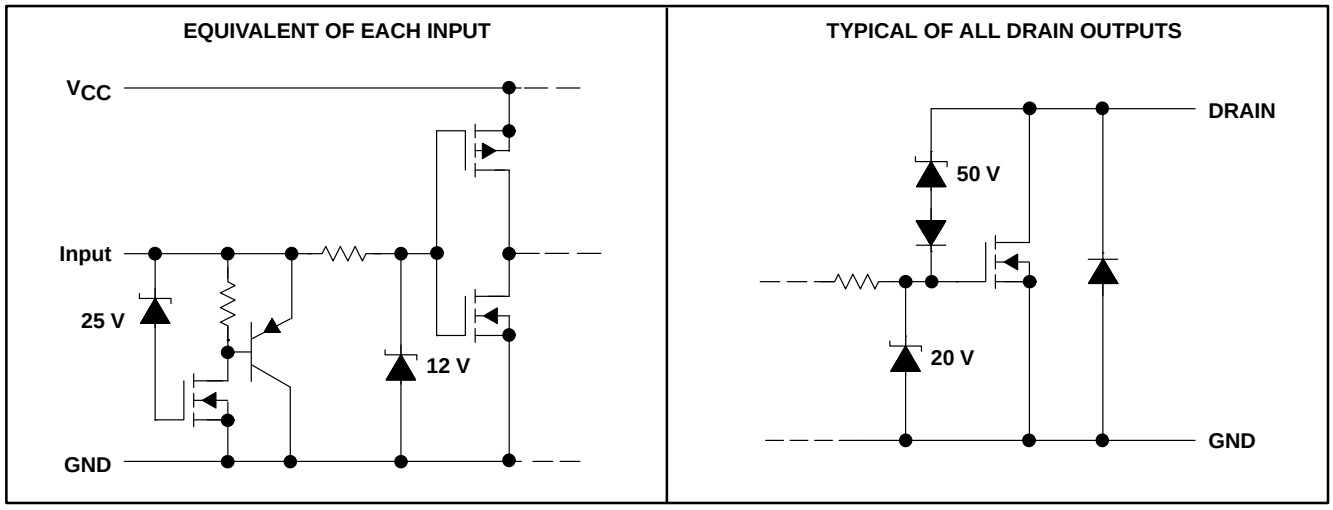


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	–0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	50 V
Continuous source-to-drain diode anode current	500 mA
Pulsed source-to-drain diode anode current (see Note 3)	1 A
Pulsed drain current, each output, all outputs on, I_D, T_C = 25°C (see Note 3)	500 mA
Continuous drain current, each output, all outputs on, I_D, T_C = 25°C	150 mA
Peak drain current single output, I_{DM}, T_C = 25°C (see Note 3)	500 mA
Single-pulse avalanche energy, E_{AS} (see Figure 4)	30 mJ
Avalanche current, I_{AS} (see Note 4)	500 mA
Continuous total dissipation	See Dissipating Rating Table
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Each power DMOS source is internally connected to GND.
3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 200 mH, I_{AS} = 0.5 A (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25°C$	$T_C = 125°C$ POWER RATING
DW	1389 mW	11.1 mW/°C	278 mW
N	1050 mW	10.5 mW/°C	263 mW

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V
Low-level input voltage, V_{IL}		0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	–500	500	mA
Setup time, D high before $\overline{G}\uparrow$, t_{su} (see Figure 2)	20		ns
Hold time, D high after $\overline{G}\uparrow$, t_h (see Figure 2)	20		ns
Pulse duration, t_w (see Figure 2)	40		ns
Operating case temperature, T_C	–40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 1 mA			50			V
V_{SD}	Source-to-drain diode forward voltage	I_F = 100 mA				0.85	1	V
I_{IH}	High-level input current	V_{CC} = 5.5 V,	$V_I = V_{CC}$				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V,	V_I = 0				–1	µA
I_{CC}	Logic supply current	V_{CC} = 5.5 V	All outputs off			20	100	µA
			All outputs on			150	300	
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, $I_N = I_D$, See Notes 5, 6, and 7		T_C = 85°C,		90		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V,	V_{CC} = 5.5 V			0.1	5	µA
		V_{DS} = 40 V,	V_{CC} = 5.5 V,	T_C = 125°C		0.15	8	
$r_{DS(on)}$	Static drain-to-source on-state resistance	I_D = 100 mA,	V_{CC} = 4.5 V	See Notes 5 and 6 and Figures 6 and 7		4.2	5.7	Ω
		I_D = 100 mA, T_C = 125°C	V_{CC} = 4.5 V,			6.8	9.5	
		I_D = 350 mA,	V_{CC} = 4.5 V			5.5	8	

switching characteristics, V_{CC} = 5 V, T_C = 25°C

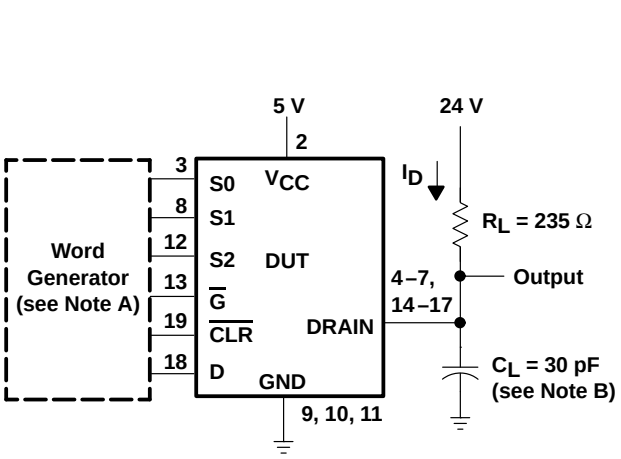
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from D	C_L = 30 pF, See Figures 1, 2, and 8	I_D = 100 mA,		150		ns
t_{PHL}	Propagation delay time, high-to-low-level output from D				90		ns
t_r	Rise time, drain output				200		ns
t_f	Fall time, drain output				200		ns
t_a	Reverse-recovery-current rise time	I_F = 100 mA, See Notes 5 and 6 and Figure 3	di/dt = 20 A/µs,		100		ns
t_{rr}	Reverse-recovery time				300		

NOTES: 3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

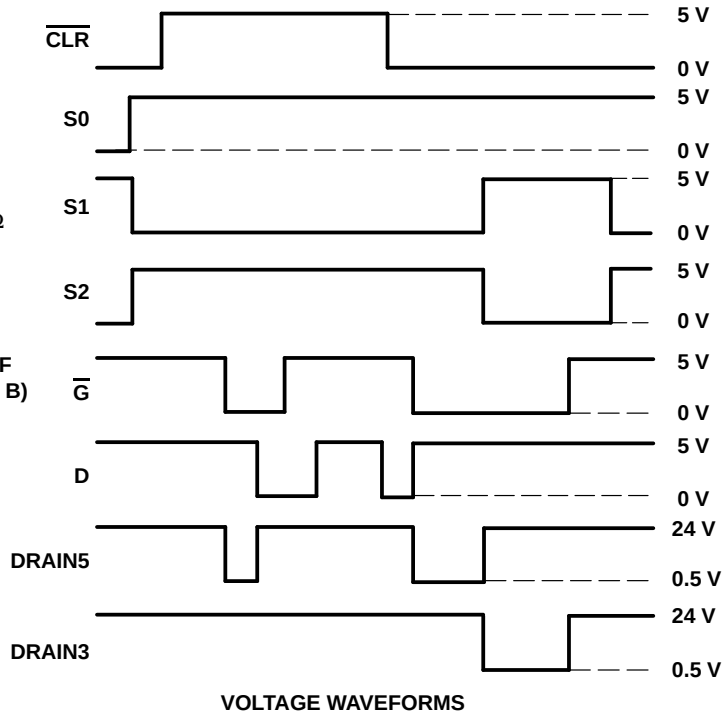
thermal resistance

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance junction-to-ambient	DW package	All 8 outputs with equal power		90	°C/W
		N package			95	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

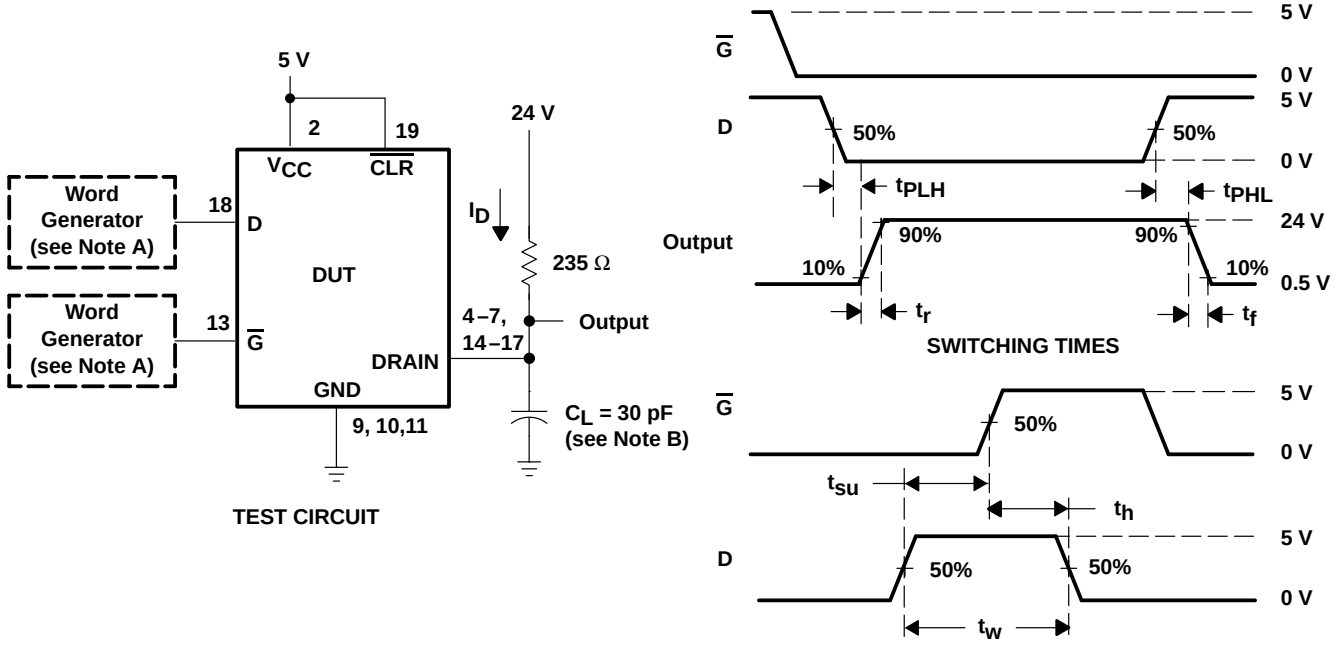


VOLTAGE WAVEFORMS

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

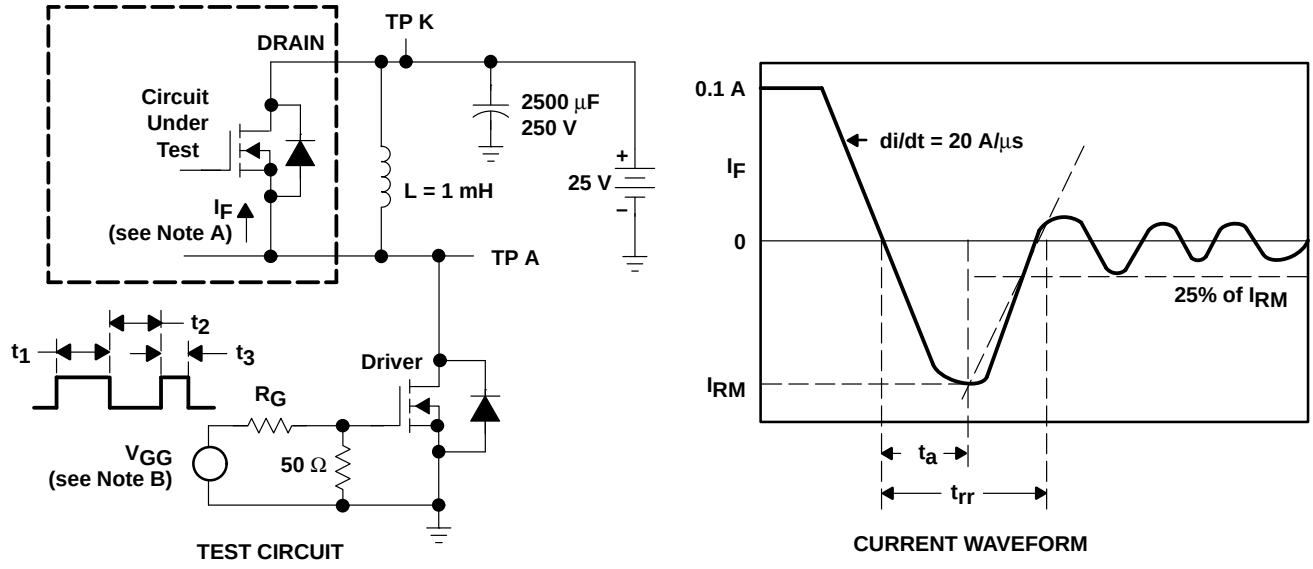
Figure 1. Resistive-Load Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

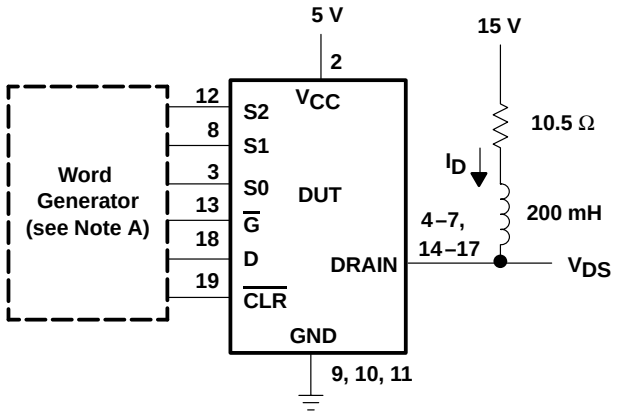
Figure 2. Test Circuit, Switching Times, and Voltage Waveforms



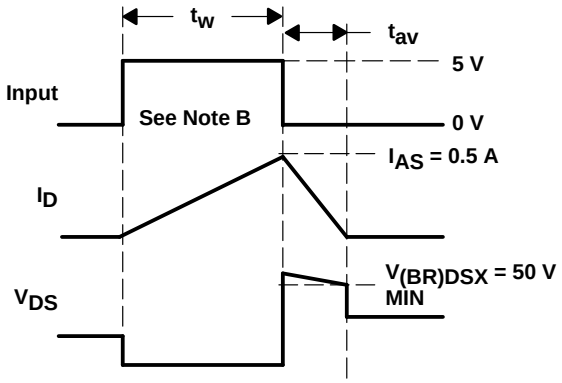
NOTES: A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
B. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/μs. A V_{GG} double-pulse train is used to set $I_F = 0.1$ A, where $t_1 = 10$ μs, $t_2 = 7$ μs, and $t_3 = 3$ μs.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration, t_w, is increased until peak current $I_{AS} = 0.5$ A.
Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 30$ mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

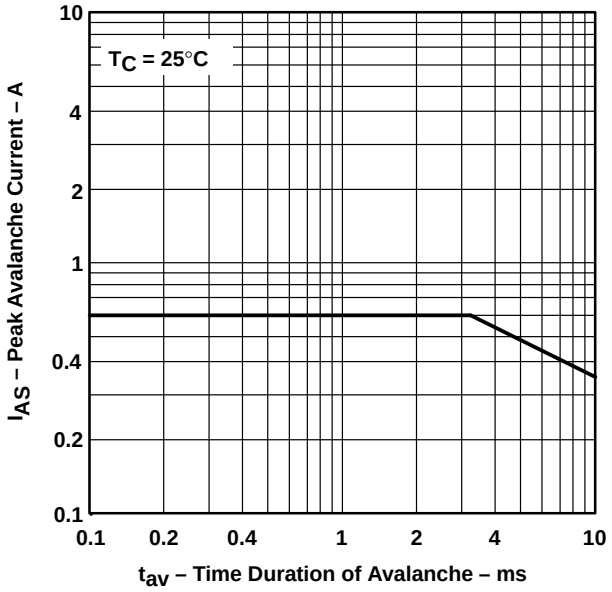
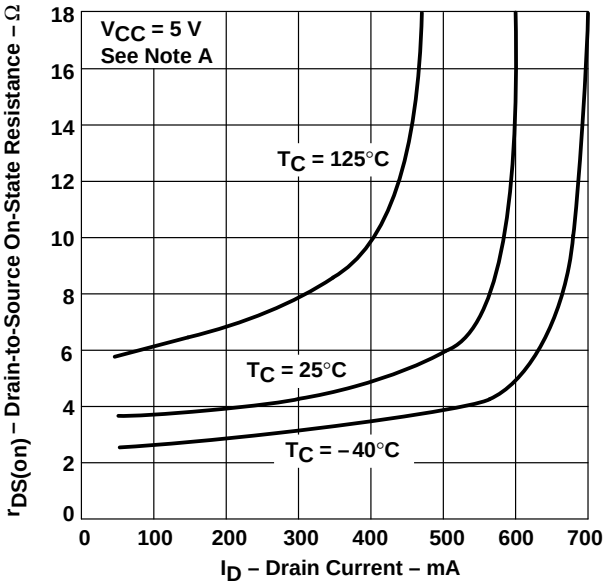


Figure 5

DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT



NOTE C. Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

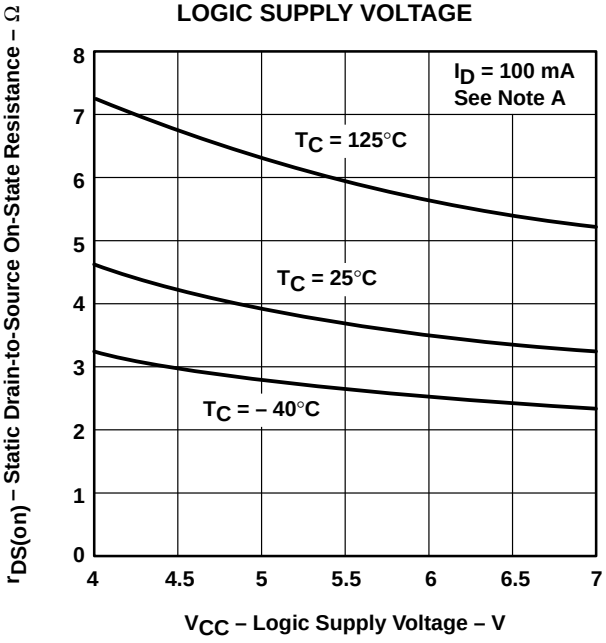


Figure 7

SWITCHING TIME vs CASE TEMPERATURE

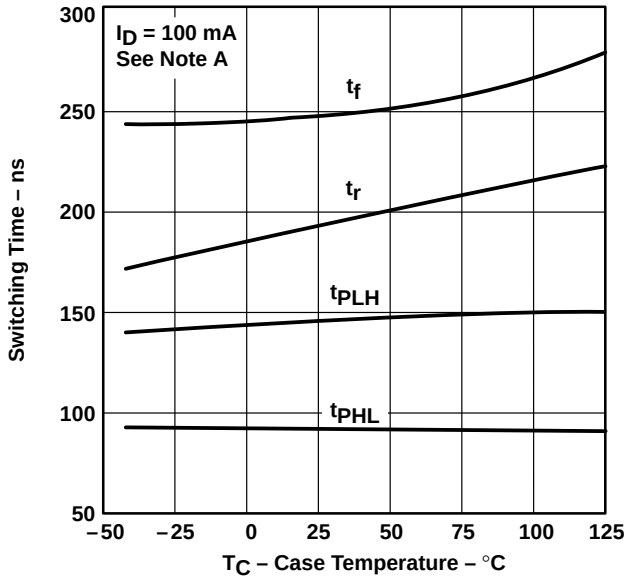


Figure 8

NOTE D. Technique should limit $T_J - T_C$ to 10°C maximum.

THERMAL INFORMATION

MAXIMUM CONTINUOUS DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

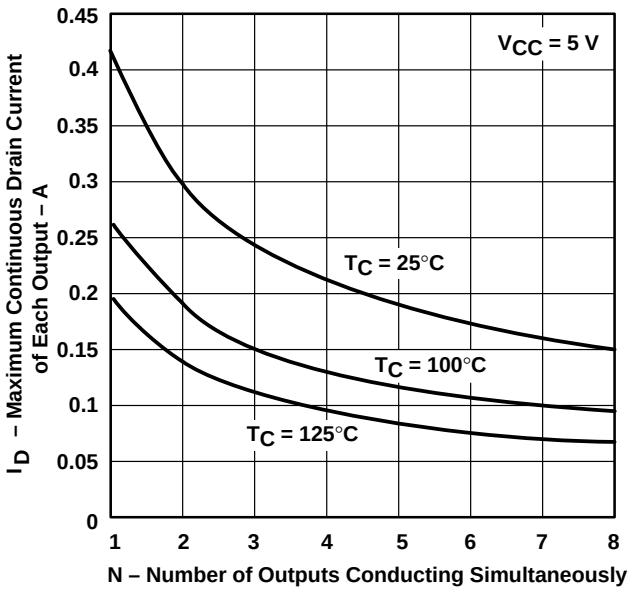


Figure 9

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

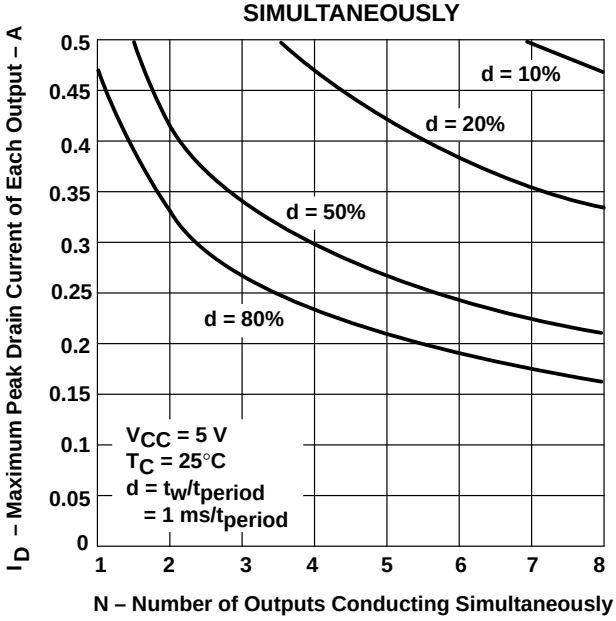


Figure 10

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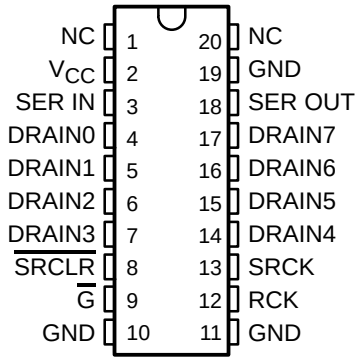
- **Low $r_{DS(on)}$ . . . 5 Ω Typical**
- **Avalanche Energy . . . 30 mJ**
- **Eight Power DMOS-Transistor Outputs of 150-mA Continuous Current**
- **500-mA Typical Current-Limiting Capability**
- **Output Clamp Voltage . . . 50 V**
- **Devices Are Cascadable**
- **Low Power Consumption**

DW OR N PACKAGE
(TOP VIEW)



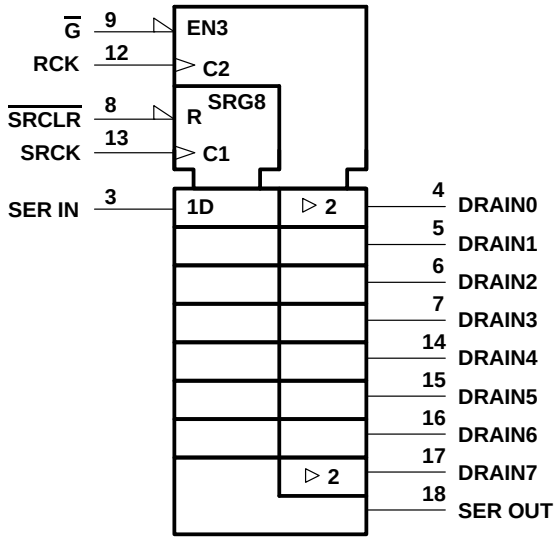
NC – No internal connection

description

The TPIC6B595 is a monolithic, high-voltage, medium-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear ($\overline{SRCLR}$) is high. When $\overline{SRCLR}$ is low, the input shift register is cleared. When output enable ($\overline{G}$) is held high, all data in the output buffers is held low and all drain outputs are off. When $\overline{G}$ is held low, data from the storage register is transparent to the output buffers. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink-current capability. The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices.

logic symbol†

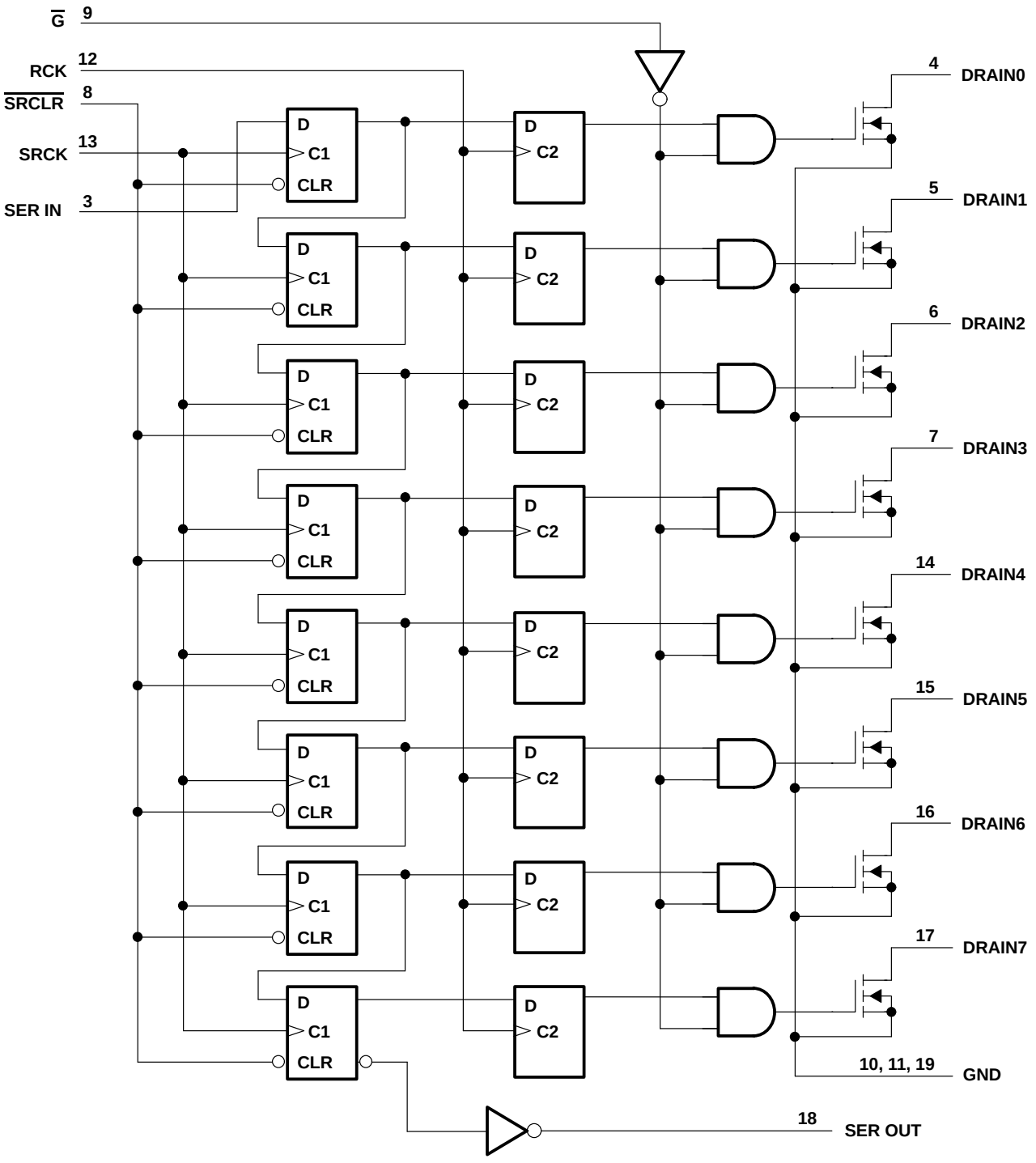


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

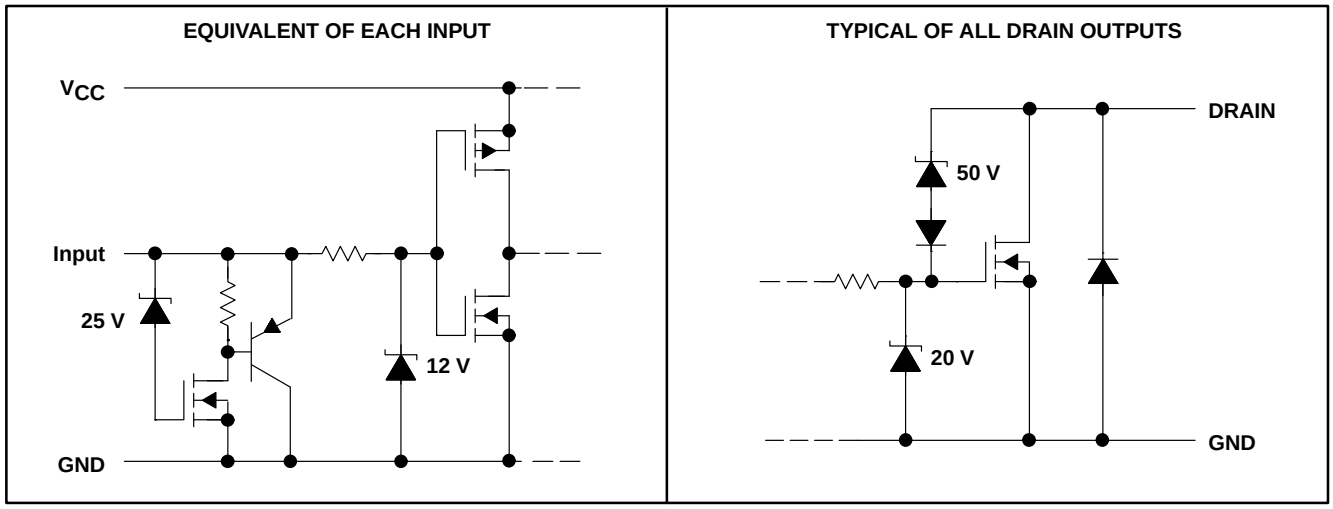
Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink-current capability. Each output provides a 500-mA typical current limit at T_C = 25°C. The current limit decreases as the junction temperature increases for additional device protection.

The TPIC6B595 is characterized for operation over the operating case temperature range of −40°C to 125°C.

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	–0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	50 V
Continuous source-to-drain diode anode current	500 mA
Pulsed source-to-drain diode anode current (see Note 3)	1 A
Pulsed drain current, each output, all outputs on, I_D, T_C = 25°C (see Note 3)	500 mA
Continuous drain current, each output, all outputs on, I_D, T_C = 25°C	150 mA
Peak drain current single output, I_{DM},T_C = 25°C (see Note 3)	500 mA
Single-pulse avalanche energy, E_{AS} (see Figure 4)	30 mJ
Avalanche current, I_{AS} (see Note 4)	500 mA
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Each power DMOS source is internally connected to GND.
3. Pulse duration ≤ 100 μs and duty cycle ≤ 2%.
4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 200 mH, I_{AS} = 0.5 A (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1389 mW	11.1 mW/°C	278 mW
N	1050 mW	10.5 mW/°C	263 mW

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V
Low-level input voltage, V_{IL}		0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	–500	500	mA
Setup time, SER IN high before SRCK↑, t_{su} (see Figure 2)	20		ns
Hold time, SER IN high after SRCK↑, t_h (see Figure 2)	20		ns
Pulse duration, t_w (see Figure 2)	40		ns
Operating case temperature, T_C	–40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 1 mA		50			V
V_{SD}	Source-to-drain diode forward voltage	I_F = 100 mA			0.85	1	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = –20 µA, V_{CC} = 4.5 V		4.4	4.49		V
		I_{OH} = –4 mA, V_{CC} = 4.5 V		4	4.2		
V_{OL}	Low-level output voltage, SER OUT	I_{OL} = 20 µA, V_{CC} = 4.5 V			0.005	0.1	V
		I_{OL} = 4 mA, V_{CC} = 4.5 V			0.3	0.5	
I_{IH}	High-level input current	V_{CC} = 5.5 V, V_I = V_{CC}				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V, V_I = 0				–1	µA
I_{CC}	Logic supply current	V_{CC} = 5.5 V	All outputs off		20	100	µA
			All outputs on		150	300	
$I_{CC(FRQ)}$	Logic supply current at frequency	f_{SRCK} = 5 MHz, C_L = 30 pF, All outputs off,	See Figures 2 and 6		0.4	5	mA
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, I_N = I_D, T_C = 85°C	See Notes 5, 6, and 7		90		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V, V_{CC} = 5.5 V			0.1	5	µA
		V_{DS} = 40 V, V_{CC} = 5.5 V, T_C = 125°C			0.15	8	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 100 mA, V_{CC} = 4.5 V	See Notes 5 and 6 and Figures 7 and 8		4.2	5.7	Ω
		I_D = 100 mA, T_C = 125°C, V_{CC} = 4.5 V			6.8	9.5	
		I_D = 350 mA, V_{CC} = 4.5 V			5.5	8	

NOTES: 3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
5. Technique should limit T_J – T_C to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

switching characteristics, V_{CC} = 5 V, T_C = 25°C

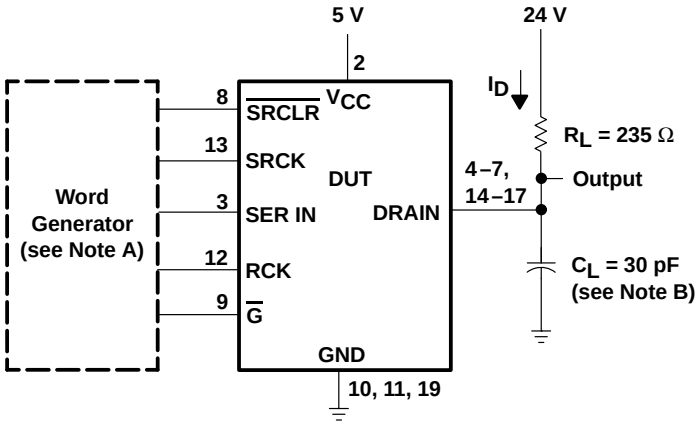
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$	C_L = 30 pF, I_D = 100 mA, See Figures 1, 2, and 9		150		ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$			90		ns
t_r	Rise time, drain output			200		ns
t_f	Fall time, drain output			200		ns
t_a	Reverse-recovery-current rise time	I_F = 100 mA, di/dt = 20 A/µs, See Notes 5 and 6 and Figure 3		100		ns
t_{rr}	Reverse-recovery time			300		

NOTES: 5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

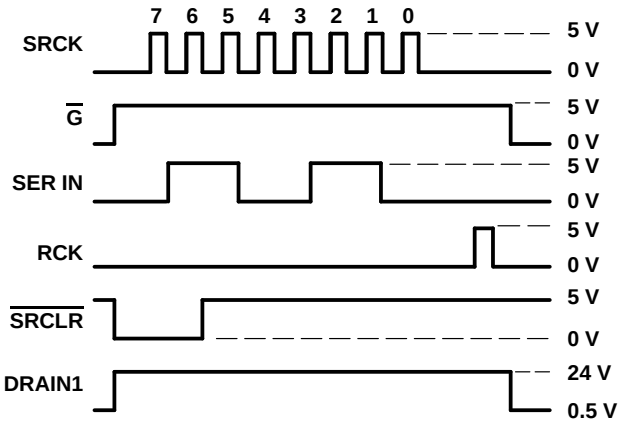
thermal resistance

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW package	All 8 outputs with equal power		90	°C/W
		N package			95	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

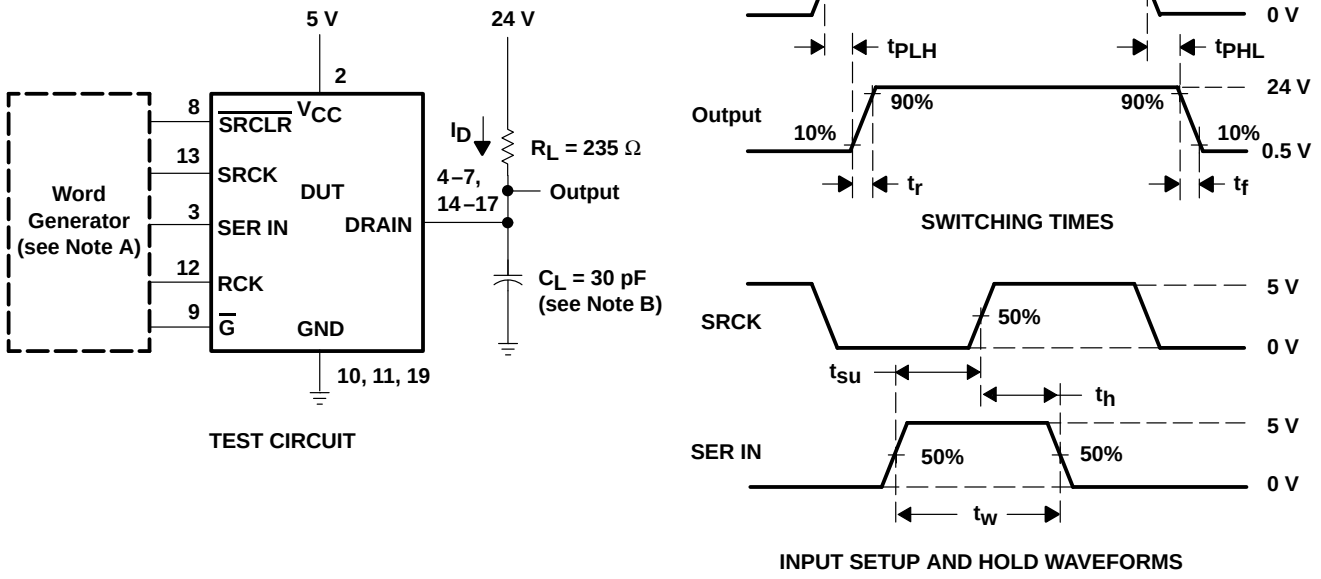


VOLTAGE WAVEFORMS

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, t_w = 300 ns, pulsed repetition rate (PRR) = 5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

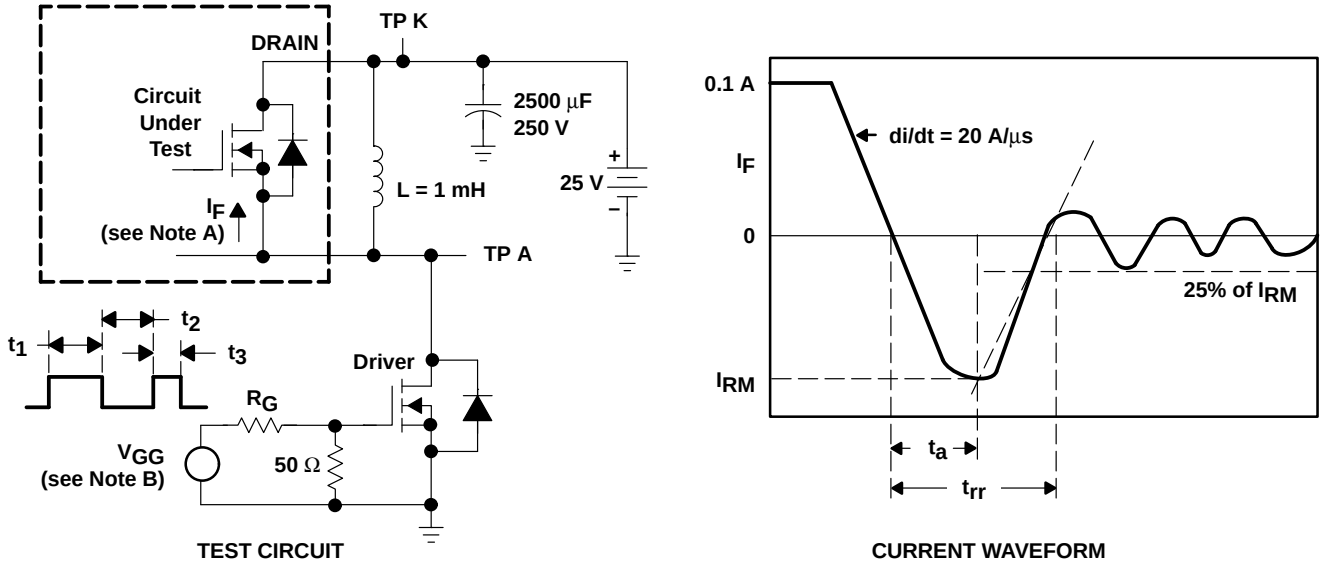
Figure 1. Resistive-Load Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

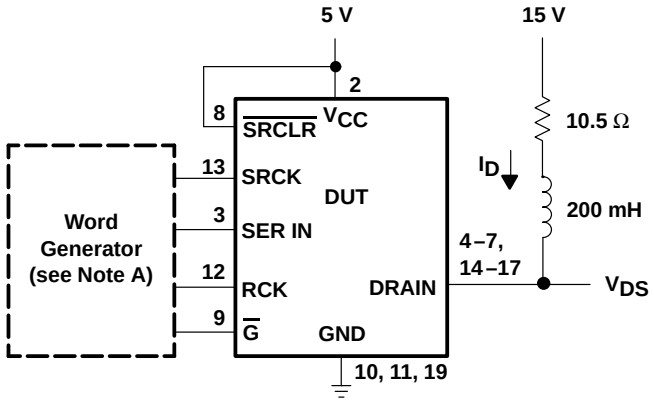
Figure 2. Test Circuit, Switching Times, and Voltage Waveforms



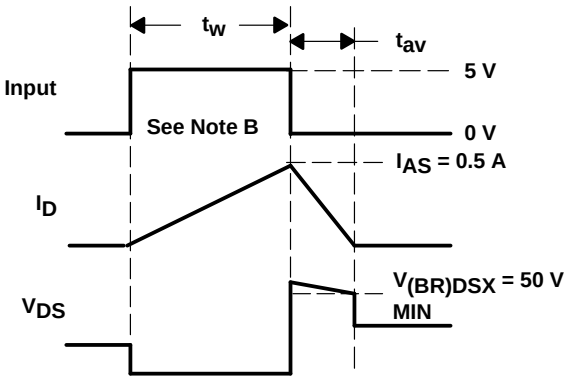
NOTES: A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
B. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/μs. A V_{GG} double-pulse train is used to set $I_F = 0.1$ A, where $t_1 = 10$ μs, $t_2 = 7$ μs, and $t_3 = 3$ μs.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



SINGLE-PULSE AVALANCHE ENERGY TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration, t_W, is increased until peak current $I_{AS} = 0.5$ A.
Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 30$ mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

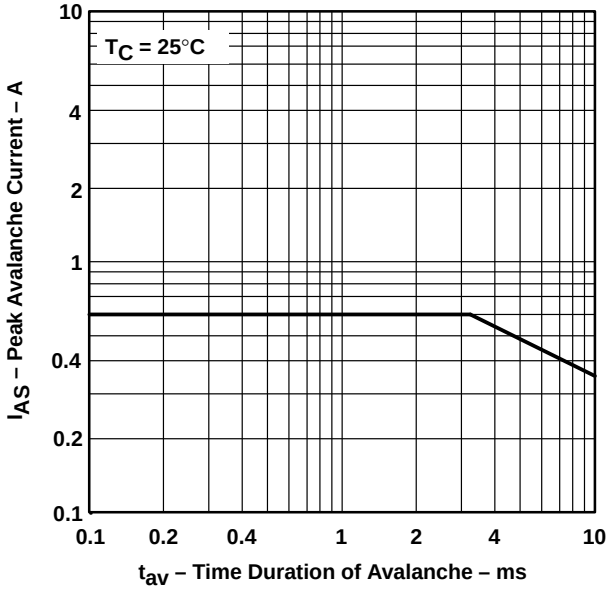


Figure 5

SUPPLY CURRENT vs FREQUENCY

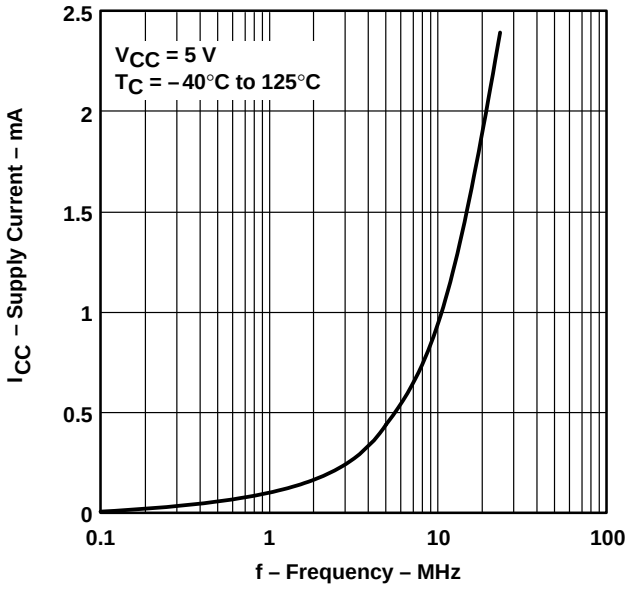


Figure 6

TYPICAL CHARACTERISTICS

DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

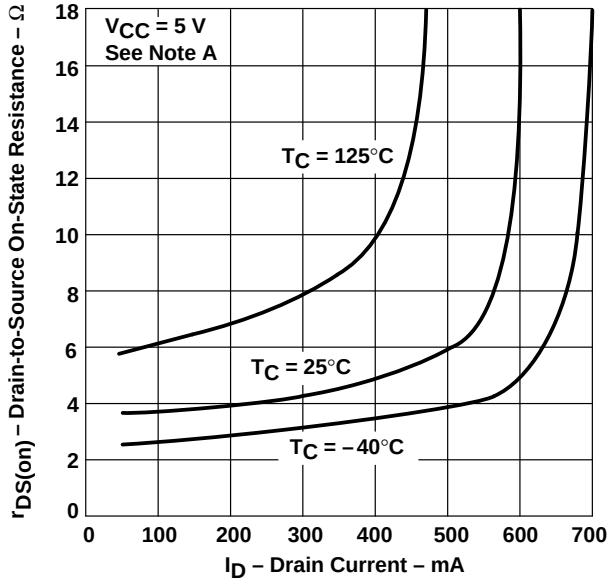


Figure 7

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

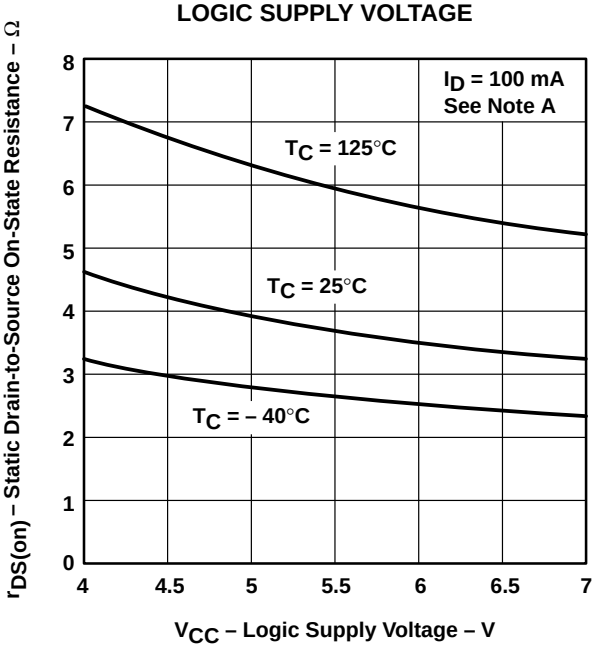


Figure 8

SWITCHING TIME vs CASE TEMPERATURE

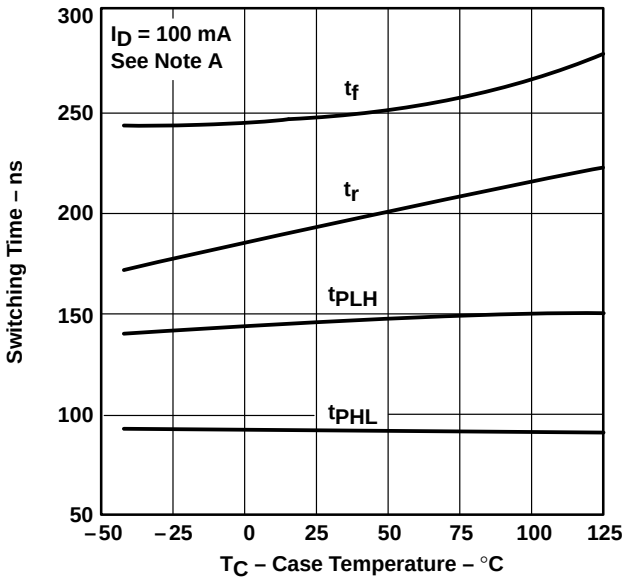


Figure 9

NOTE C. Technique should limit $T_J - T_C$ to 10°C maximum.

THERMAL INFORMATION

MAXIMUM CONTINUOUS DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

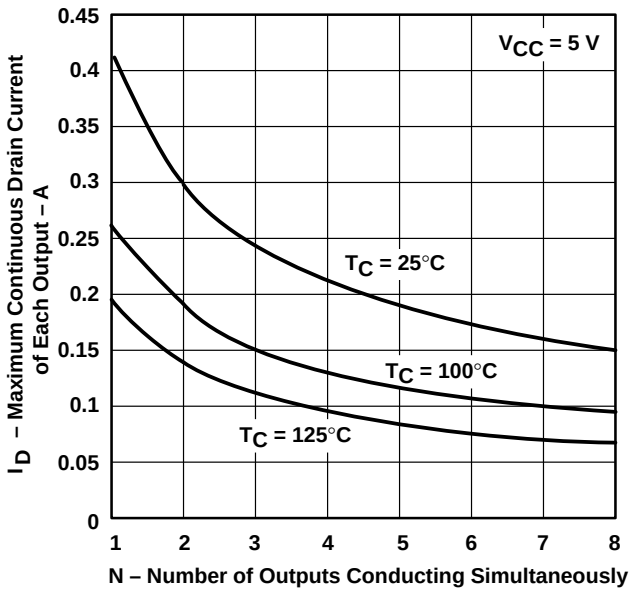


Figure 10

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

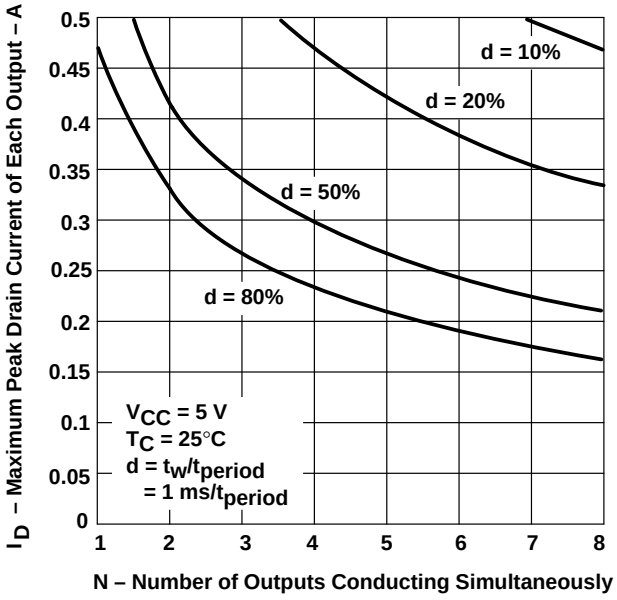


Figure 11

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