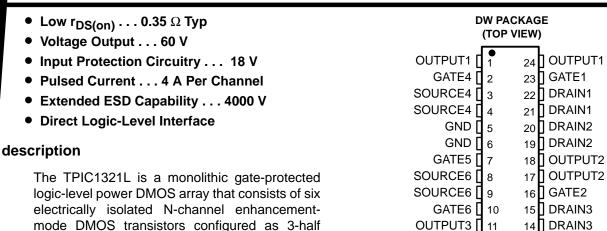
OUTPUT3

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14 DRAIN3

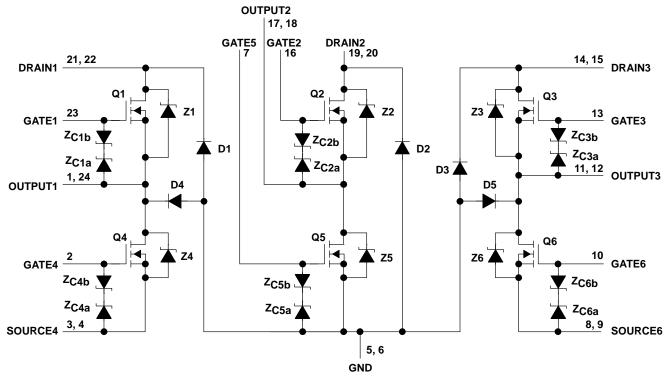
13 GATE3



high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to $4000 \, \text{V}$ of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-k Ω resistor.

The TPIC1321L is offered in a 24-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature of -40°C to 125°C.

schematic



NOTE A: For correct operation, no terminal may be taken below GND.

mode DMOS transistors configured as 3-half

H-bridges. Each transistor features integrated

TPIC1321L 3-HALF H-BRIDGE GATE-PROTECTED LOGIC-LEVEL POWER DMOS ARRAY

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absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V _{DS}	60 V
Output-to-GND voltage	60 V
Drain-to-GND voltage	100 V
SOURCE4, SOURCE6-to-GND voltage	60 V
Gate-to-source voltage range, V _{GS}	9 V to 18 V
Continuous drain current, each output, T _C = 25°C	1.25 A
Continuous source-to-drain diode current, T _C = 25°C	1.25 A
Pulsed drain current, each output, I _{max} , T _C = 25°C (see Note 1 and Figure 15)	4 A
Continuous gate-to-source zener-diode current, T _C = 25°C	±50 mA
Pulsed gate-to-source zener-diode current, T _C = 25°C	±500 mA
Single-pulse avalanche energy, E _{AS.} T _C = 25°C (see Figures 4 and 16)	96 mJ
Continuous total dissipation, T _C = 25°C (see Figure 15)	1.39 W
Operating virtual junction temperature range, T _J	. −40°C to 150°C
Operating case temperature range, T _C	. −40°C to 125°C
Storage temperature range	. −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	26000

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%



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electrical characteristics, $T_C = 25^{\circ}C$ (unless otherwise noted)

	PARAMETER	TEST COND	ITIONS	MIN	TYP	MAX	UNIT
V(BR)DSX	Drain-to-source breakdown voltage	$I_D = 250 \mu A$,	V _{GS} = 0	60			V
V _{GS(th)}	Gate-to-source threshold voltage	I _D = 1 mA, See Figure 5	$V_{DS} = V_{GS}$	1.5	1.75	2.2	>
V _(BR) GS	Gate-to-source breakdown voltage	I _{GS} = 250 μA		18			V
V _(BR) SG	Source-to-gate breakdown voltage	I _{SG} = 250 μA		9			V
V _(BR)	Reverse drain-to-GND breakdown voltage (across D1, D2, D3, D4, D5)	Drain-to-GND curren	t = 250 μA	100			V
V _{DS(on)}	Drain-to-source on-state voltage	I _D = 1.25 A, V _{GS} = 5 V, See Notes 2 and 3			0.44	0.5	V
V _{F(SD)}	Forward on-state voltage, source-to-drain	I _S = 1.25 A, V _{GS} = 0 (Z1 – Z6), See Notes 2 and 3 and Figure 12			0.9	1.1	V
VF	Forward on-state voltage, GND-to-drain	I _D = 1.25 A (D1 – D5) See Notes 2 and 3			4		V
l	Zoro goto voltago drain gurrent	V _{DS} = 48 V,	T _C = 25°C		0.05	1	μΑ
IDSS	Zero-gate-voltage drain current	V _{GS} = 0	T _C = 125°C		0.5	10	μΑ
IGSSF	Forward-gate current, drain short circuited to source	$V_{GS} = 15 V$,	$V_{DS} = 0$		20	200	nA
IGSSR	Reverse-gate current, drain short circuited to source	$V_{SG} = 5 V$	$V_{DS} = 0$		10	100	nA
lu	Leakage current, drain-to-GND	VDGND = 48 V	T _C = 25°C		0.05	1	μA
llkg	Leakage current, drain to GND	VDGND = 40 V	T _C = 125°C		0.5	10	μΛ
(DC()	Static drain-to-source on-state resistance	V _{GS} = 5 V, I _D = 1.25 A,	T _C = 25°C		0.35	0.4	Ω
rDS(on)	otatic drain to source on state resistance	See Notes 2 and 3 and Figures 6 and 7	T _C = 125°C		0.57	0.6	32
9fs	Forward transconductance	V _{DS} = 15 V, I _D = 625 mA, See Notes 2 and 3 and Figure 9		1.6	1.74		S
C _{iss}	Short-circuit input capacitance, common source				200	250	
Coss	Short-circuit output capacitance, common source	$V_{DS} = 25 V$,	$V_{GS} = 0$,		175	220	pF
C _{rss}	Short-circuit reverse-transfer capacitance, common source	f = 1 MHz,	See Figure 11		40	75	ν.

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.

source-to-drain and GND-to-drain diode characteristics, $T_C = 25^{\circ}C$

	PARAMETER TEST CONDITIONS				MIN	TYP	MAX	UNIT
t _{rr}	Reverse-recovery time	$I_S = 625 \text{ mA},$	V _{DS} = 48 V,	71 72 and 72		45		ns
Q _{RR}	Total diode charge	VGS = 0, See Figures 1 and 14	di/dt = 100 A/μs,	Z1, Z2, and Z3		50		nC

^{3.} These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

TPIC1321L 3-HALF H-BRIDGE GATE-PROTECTED LOGIC-LEVEL POWER DMOS ARRAY

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resistive-load switching characteristics, T_C = 25°C

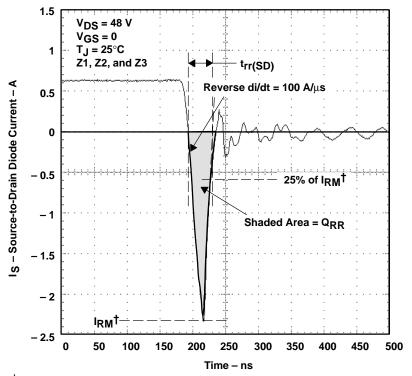
	PARAMETER	7	TEST CONDITION	NS	MIN	TYP	MAX	UNIT									
t _{d(on)}	Turn-on delay time					34	70										
td(off)	Turn-off delay time	V _{DD} = 25 V,	$R_L = 40 \Omega$,	$t_{en} = 10 \text{ ns},$		80	150	ns									
t _r	Rise time		See Figure 2			28	55	115									
t _f	Fall time					15	30										
Qg	Total gate charge					4.6	5.8										
Q _{gs(th)}	Threshold gate-to-source charge	V _{DS} = 48 V,								V _{DS} = 48 V, See Figure 3		$I_D = 625 \text{ mA},$	$V_{GS} = 5 V$,		0.7	0.88	nC
Q _{gd}	Gate-to-drain charge	e coo r iguilo c				2.5	3.13										
L _D	Internal drain inductance					5		-11									
LS	Internal source inductance					5		nΗ									
Rg	Internal gate resistance					0.25		Ω									

thermal resistance

	PARAMETER TEST CONDITIONS				MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	See Notes 4 and 7		90		
$R_{\theta JB}$	Junction-to-board thermal resistance	See Notes 5 and 7		44.5		°C/W
$R_{\theta JP}$	Junction-to-pin thermal resistance	See Notes 6 and 7		28		

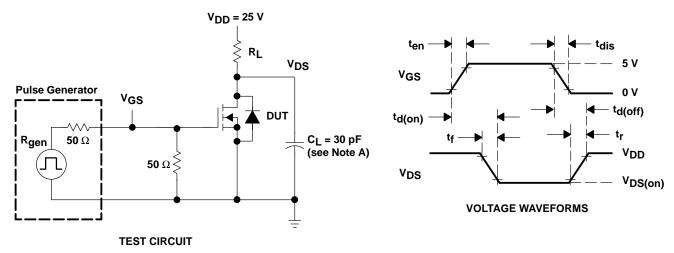
NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink.

- 5. Package mounted on a 24 in², 4-layer FR4 printed-circuit board.
- 6. Package mounted in intimate contact with infinite heatsink.
- 7. All outputs with equal power



† I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms



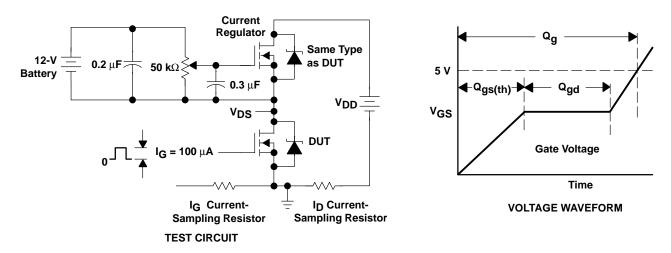
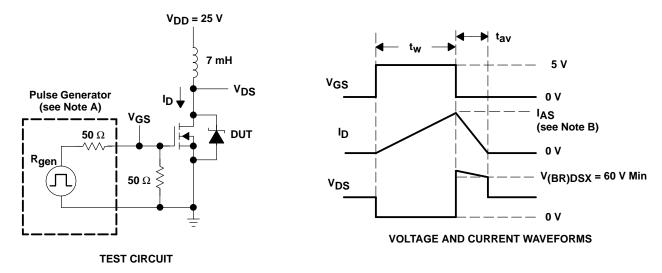


Figure 3. Gate-Charge Test Circuit and Voltage Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50 \Omega$.

B. Input pulse duration (t_W) is increased until peak current $I_{AS} = 4$ A.

Energy test level is defined as E_{AS} = $\frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2}$ = 96 mJ.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

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TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE

JUNCTION TEMPERATURE 2.5 VGS(th) - Gate-to-Source Threshold Voltage - V $V_{DS} = V_{GS}$ $I_D = 1 \text{ mA}$ 1.5 $I_D = 100 \, \mu A$ 0.5 -40 - 2040 60 80 100 120 140 160

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE

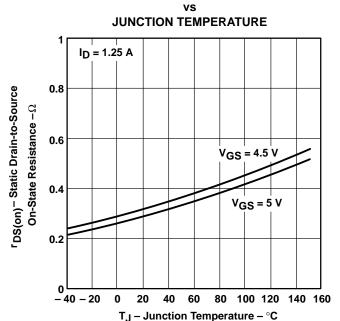
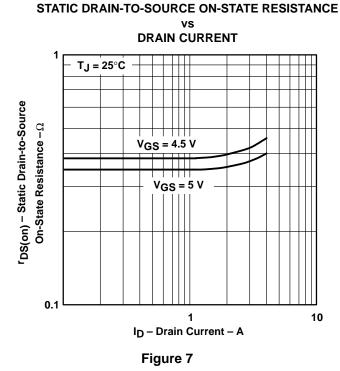


Figure 5

T_J - Junction Temperature - °C



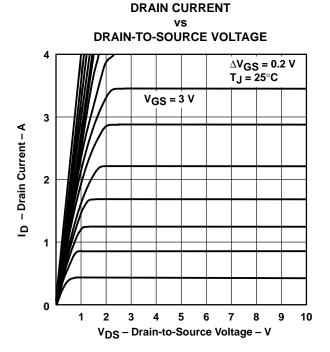


Figure 6

Figure 8

TYPICAL CHARACTERISTICS

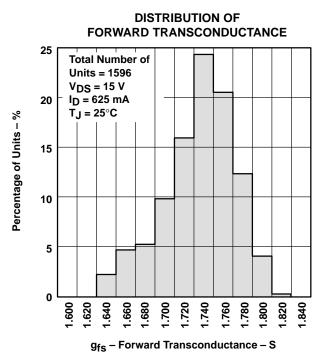


Figure 9

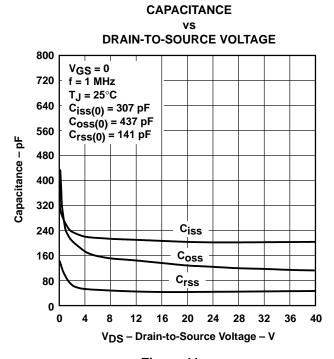


Figure 11

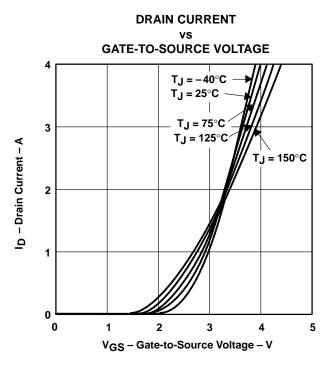
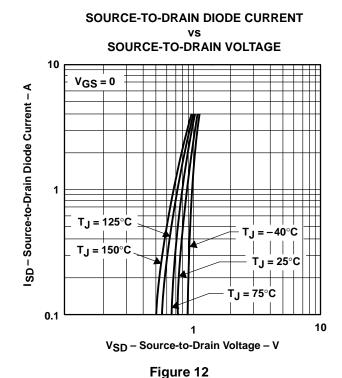


Figure 10



TYPICAL CHARACTERISTICS

DRAIN-TO-SOURCE VOLTAGE AND GATE-TO-SOURCE VOLTAGE

GATE CHARGE 60 12 I_D = 625 mA $\bar{T_J} = 25^{\circ}C$ See Figure 3 50 10 VDS - Drain-to-Source Voltage - V VGS - Gate-to-Source Voltage - V $V_{DD} = 20 V$ 40 8 $V_{DD} = 30 V$ 30 20 $V_{DD} = 48 V$ 10 V_{DD} = 20 V 0 0 3 4 7 2 5 6 8

Figure 13

REVERSE-RECOVERY TIME

Q_g – Gate Charge – nC

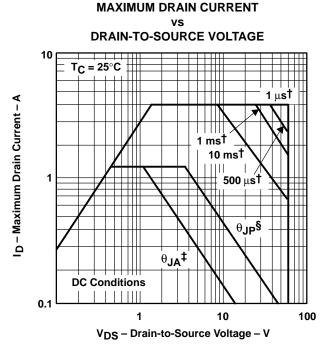
REVERSE di/dt 50 45 trr - Reverse-Recovery Time - ns 40 Z₁, Z₂, and Z₃ 35 30 25 20 15 V_{DS} = 48 V $V_{GS} = 0$ 10 Is = 625 mA 5 T_J = 25°C See Figure 1 300 400 600 0 100 200 500 Reverse di/dt – A/ μ s

Figure 14



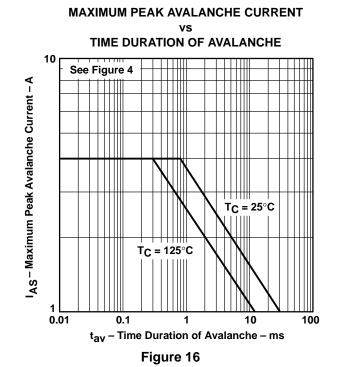
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THERMAL INFORMATION



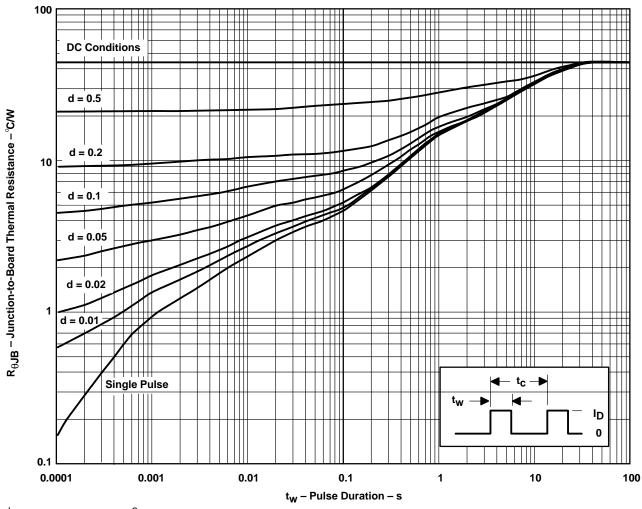
- †Less than 2% duty cycle
- [‡] Device mounted on FR4 printed-circuit board with no heatsink.
- § Device mounted in intimate contact with infinite heatsink.

Figure 15



THERMAL INFORMATION

DW PACKAGE† JUNCTION-TO-BOARD THERMAL RESISTANCE vs PULSE DURATION



† Device mounted on 24 in², 4-layer FR4 printed-circuit board with no heatsink.

NOTE A: $Z_{\theta B}(t) = r(t) R_{\theta JB}$ $t_W = \text{pulse duration}$ $t_C = \text{cycle time}$ $d = \text{duty cycle} = t_W/t_C$

Figure 17



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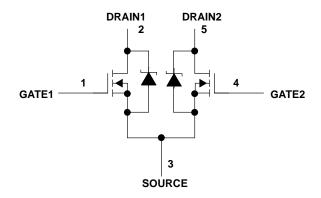
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- Two 7.5-A Independent Output Channels, Continuous Current Per Channel
- Low r_{DS(on)} . . . 0.09 Ω Typical
- Output Voltage . . . 60 V
- Pulsed Current . . . 15 A Per Channel
- Avalanche Energy . . . 120 mJ

description

The TPIC2202 is a monolithic power DMOS array that consists of two independent N-channel enhancement-mode DMOS transistors connected in a common-source configuration with open drains.

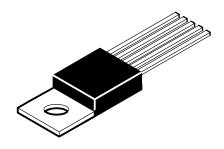
schematic



KC PACKAGE (TOP VIEW)



The tab is electrically connected to SOURCE.



absolute maximum ratings over operating case temperature range (unless otherwise noted)

Drain-source voltage, V _{DS}	60 V
Gate-source voltage, V _{GS}	±20 V
Continuous source-drain diode current	7.5 A
Pulsed drain current, each output, all outputs on, ID (see Note 1)	
Continuous drain current, each output, all outputs on	7.5 A
Single-pulse avalanche energy, E _{AS} (see Figure 4)	120 mJ
Continuous power dissipation at (or below) T _A = 25°C (see Note 2)	2 W
Continuous power dissipation at (or below) T _C = 75°C, all outputs on (see Note 2)	
Operating virtual junction temperature range, T _J	-40°C to 150°C
Operating case temperature range, T _C	-40°C to 125°C
Storage temperature range, T _{stq}	-40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

NOTES: 1. Pulse duration = 10 ms, duty cycle = 6%

2. For operation above 25°C free-air temperature, derate linearly at the rate of 16 mW/°C. For operation above 75°C case temperature, and with all outputs conducting, derate linearly at the rate of 0.42 W/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded.



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electrical characteristics, $T_C = 25^{\circ}C$ (unless otherwise noted)

	PARAMETER		TEST COND	ITIONS		MIN	TYP	MAX	UNIT
V _{(BR)DS}	Drain-source breakdown voltage	$I_D = 1 \mu A$,	$V_{GS} = 0$			60			V
VTGS	Gate-source threshold voltage	$I_D = 1 \text{ mA},$	$V_{DS} = V_{GS}$			1.2	1.75	2.4	V
V _{DS(on)}	Drain-source on-state voltage	$I_D = 7.5 A,$	V _{GS} = 15 V,	V _{GS} = 15 V, See Notes 3 and 4			0.68	0.94	V
Inna	Zero-gate-voltage drain current	\/= 0 - 49 \/	Vaa – 0		T _C = 25°C		0.07	1	^
IDSS	Zero-gate-voltage drain current	$V_{DS} = 48 \text{ V},$	VGS = 0		T _C = 125°C		1.3	10	μΑ
IGSSF	Forward gate current, drain short circuited to source	V _{GS} = 20 V,	$V_{DS} = 0$				10	100	nA
I _{GSSR}	Reverse gate current, drain short circuited to source	$V_{GS} = -20 \text{ V},$	V _{DS} = 0				10	100	nA
r=0()	Static drain-source on-state	$V_{GS} = 15 \text{ V},$	$T_{CS} = 15 \text{ V}, I_{D} = 7.5 \text{ A}, T_{C} = 25^{\circ}\text{C}$				0.09	0.125	Ω
rDS(on)	resistance	See Notes 3 an	d 4 and Figure	$\frac{1}{4}$ and Figures 5 and 6 $T_C = 125^{\circ}C$			0.15	0.21	52
9fs	Forward transconductance	$V_{DS} = 15 V$,	I _D = 5 A,	See Note:	s 3 and 4	2.5	4.7		S
C _{iss}	Short-circuit input capacitance, common source						490		
C _{oss}	Short-circuit output capacitance, common source	V _{DS} = 25 V,	V _{GS} = 0, f = 300 kHz			285		pF	
C _{rss}	Short-circuit reverse transfer capacitance, common source						90		

NOTES: 3. Technique should limit $T_J - T_C$ to 10°C maximum.

source-drain diode characteristics, $T_C = 25^{\circ}C$

	PARAMETER		TEST CONDITI	MIN	TYP	MAX	UNIT	
V _{SD}	Forward on voltage	. 754		11/11 400 A/ -		0.8	1.3	V
t _{rr}	Reverse recovery time	$I_S = 7.5 A,$ $V_{DS} = 48 V,$		di/dt = 100 A/μs,		200		ns
Q _{RR}	Total source-drain diode charge	103 10 1,				1.5		μС

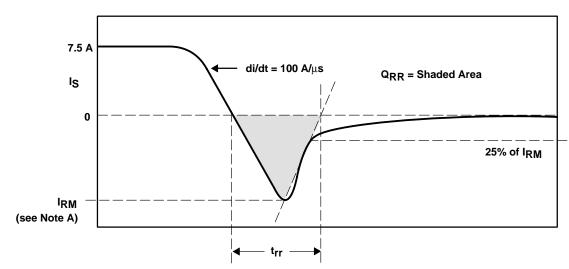
resistive-load switching characteristics, $T_C = 25^{\circ}C$

	PARAMETER	1	TEST CONDITION	NS	MIN	TYP	MAX	UNIT
t _{d(on)}	Turn-on delay time					12		
td(off)	Turn-off delay time	$V_{DD} = 25 \text{ V},$	$R_L = 6.7 \Omega$,	$t_{en} = 10 \text{ ns},$		100		ns
t _r	Rise time	$t_{dis} = 10 \text{ ns},$	See Figure 2			43		115
tf	Fall time					5		
Qg	Total gate charge					13.6	18	
Qgs	Gate-source charge	V _{DD} = 48 V, See Figure 3	$I_D = 2.5 A,$	$V_{GS} = 10 V$,		8.3	11	nC
Q _{gd}	Gate-drain charge	gui o o				5.3	7	
L _D	Internal drain inductance					7		nH
LS	Internal source inductance					7		ш

thermal resistance

	PARAMETER TEST CONDITIONS			TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power			62.5	°C/W
R _θ JC	lunction to cope thermal registeres	All outputs with equal power			2.4	°C/W
	Junction-to-case thermal resistance	One output dissipating power			3.3	°C/W

^{4.} These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.



NOTE A: I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveforms of Source-Drain Diode

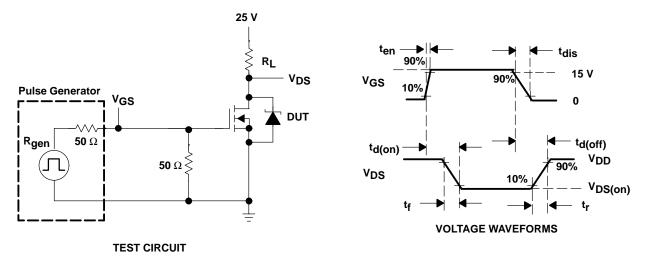


Figure 2. Test Circuit and Voltage Waveforms, Resistive Switching

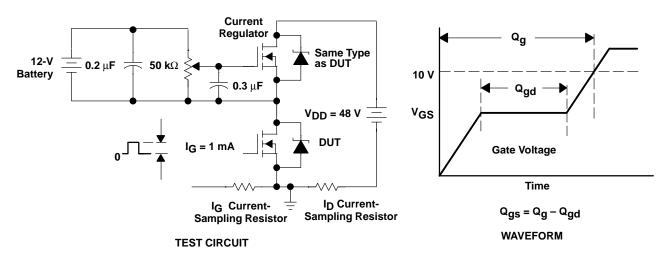
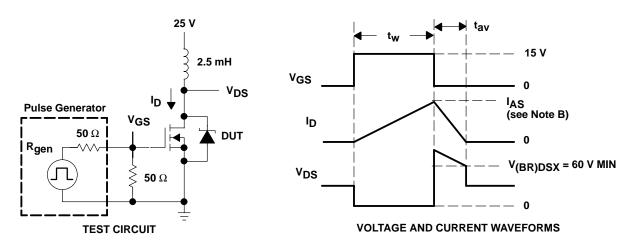


Figure 3. Gate Charge Test Circuit and Waveform



NOTES: A. The pulse generator has the following characteristics: $t_f \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50$ Ω .

B. Input pulse duration (t_W) is increased until peak current IAS = 7.5 A.

Energy test level is defined as
$$E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 120 \text{ mJ min.}$$

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE

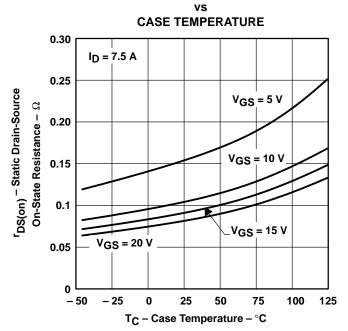


Figure 5

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

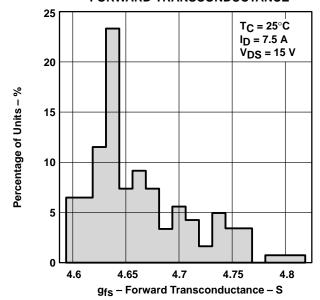


Figure 7

STATIC DRAIN-SOURCE ON-STATE RESISTANCE

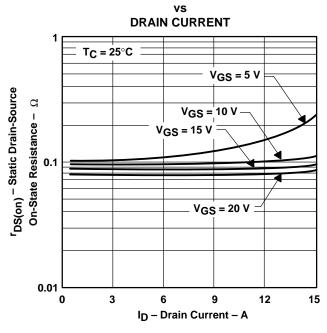


Figure 6

DRAIN CURRENT

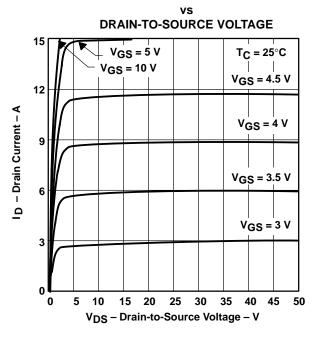


Figure 8

TYPICAL CHARACTERISTICS

GATE-SOURCE THRESHOLD VOLTAGE vs **CASE TEMPERATURE** V_{TGS} - Gate-Source Threshold Voltage - V $I_D = 1 \text{ mA}$ 1.8 1.6 1.4 1.2 1 0.8 0.6 0.4 0.2 0 - 50 - 25 25 50 75 100 125 T_C - Case Temperature - °C



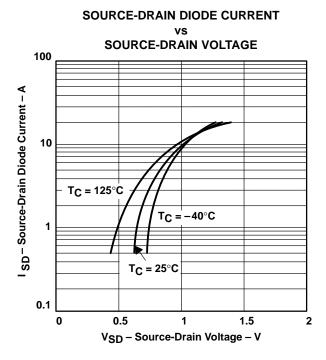


Figure 10

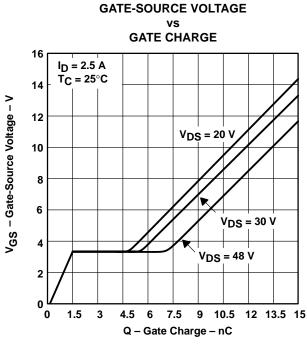


Figure 11

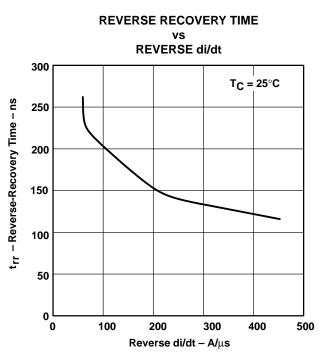


Figure 12

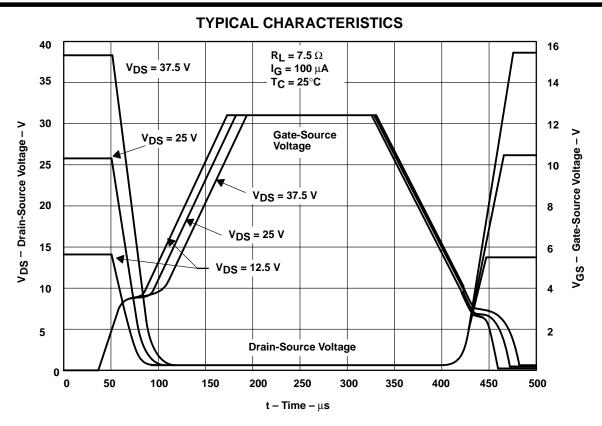


Figure 13. Resistive Switching Waveforms

THERMAL INFORMATION

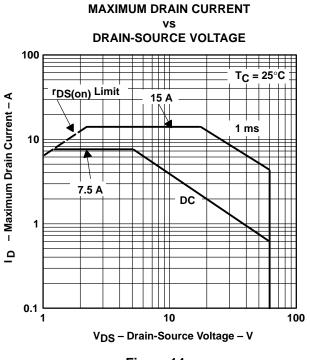


Figure 14

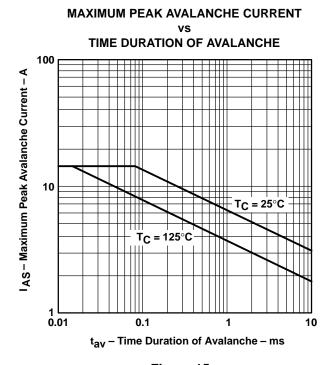
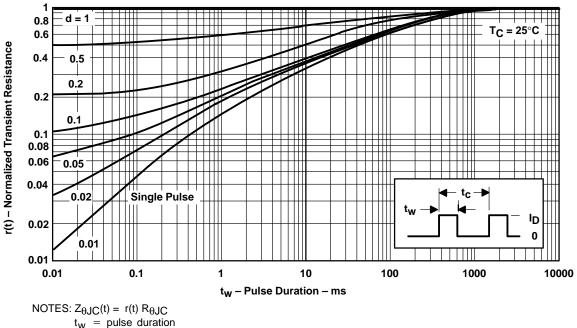


Figure 15

THERMAL INFORMATION

NORMALIZED TRANSIENT THERMAL IMPEDANCE vs SQUARE-WAVE PULSE DURATION



NOTES: $Z_{\theta JC}(t) = r(t) R_{\theta JC}$ $t_W = \text{pulse duration}$ $t_C = \text{period}$ $d = \text{duty cycle} = t_W/t_C$

Figure 16

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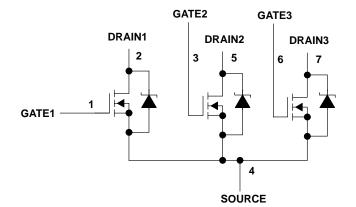
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- Three 7.5-A Independent Output Channels, Continuous Current Per Channel
- Low $r_{DS(on)} \dots 0.09 \Omega$ Typical
- Output Voltage . . . 60 V
- Pulsed Current . . . 15 A Per Channel
- Avalanche Energy . . . 120 mJ

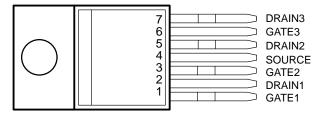
description

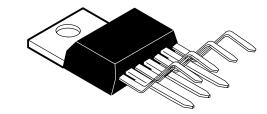
The TPIC2301 is a monolithic power DMOS array that consists of three independent N-channel enhancement-mode DMOS transistors connected in a common-source configuration with open drains.

schematic



KV PACKAGE (TOP VIEW)





The tab is electrically connected to SOURCE.

absolute maximum ratings over operating case temperature range (unless otherwise noted)

Drain-source voltage, V _{DS}	60 V
Gate-source voltage, V _{GS}	±20 V
Continuous source-drain diode current	7.5 A
Pulsed drain current, each output, all outputs on, I _D (see Note 1)	15 A
Continuous drain current, each output, all outputs on	7.5 A
Single-pulse avalanche energy, EAS (see Figure 4)	120 mJ
Continuous power dissipation at (or below) T _A = 25°C (see Note 2)	2 W
Continuous power dissipation at (or below) T _C = 75°C, all outputs on (see Note 2)	50 W
Operating virtual junction temperature range, T _J	-40°C to 150°C
Operating case temperature range, T _C	-40°C to 125°C
Storage temperature range, T _{stq}	-40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

NOTES: 1. Pulse duration = 10 ms, duty cycle = 6%

2. For operation above 25°C free-air temperature, derate linearly at the rate of 16 mW/°C. For operation above 75°C case temperature, and with all outputs conducting, derate linearly at the rate of 0.66 W/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded.

SLIS018 - SEPTEMBER 1992

electrical characteristics, $T_C = 25^{\circ}C$ (unless otherwise noted)

	PARAMETER		TEST COND	ITIONS		MIN	TYP	MAX	UNIT
V _{(BR)DS}	Drain-source breakdown voltage	$I_D = 1 \mu A$,	$V_{GS} = 0$			60			V
VTGS	Gate-source threshold voltage	$I_D = 1 \text{ mA},$	$V_{DS} = V_{GS}$			1.2	1.75	2.4	V
V _{DS(on)}	Drain-source on-state voltage	$I_D = 7.5 A,$	V _{GS} = 15 V,	V _{GS} = 15 V, See Notes 3 and 4			0.68	0.94	V
Inna	Zero-gate-voltage drain current	\/= a - 49 \/	Vaa - 0		T _C = 25°C		0.07	1	
IDSS	Zero-gate-voltage drain current	$V_{DS} = 48 \text{ V},$	VGS = 0		T _C = 125°C		1.3	10	μΑ
IGSSF	Forward gate current, drain short circuited to source	V _{GS} = 20 V,	V _{DS} = 0				10	100	nA
IGSSR	Reverse gate current, drain short circuited to source	$V_{GS} = -20 \text{ V},$	V _{DS} = 0				10	100	nA
r=0()	Static drain-source on-state	$V_{GS} = 15 \text{ V},$	$I_{CS} = 15 \text{ V}, I_{D} = 7.5 \text{ A}, T_{C} = 25^{\circ}\text{C}$		$T_C = 25^{\circ}C$		0.09	0.125	Ω
rDS(on)	resistance	See Notes 3 an	See Notes 3 and 4 and Figures 5 and 6 $T_C = 1$				0.15	0.21	52
9fs	Forward transconductance	$V_{DS} = 15 V$,	I _D = 5 A,	See Note	s 3 and 4	3.3	4.7		S
C _{iss}	Short-circuit input capacitance, common source						490		
C _{oss}	Short-circuit output capacitance, common source	V _{DS} = 25 V,	V _{GS} = 0, f = 300 kHz			285		pF	
C _{rss}	Short-circuit reverse transfer capacitance, common source				,		90		

NOTES: 3. Technique should limit $T_J - T_C$ to 10°C maximum.

source-drain diode characteristics, $T_C = 25^{\circ}C$

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V _{SD}	Forward on voltage	. 75 4		11/11 400 4/ -		0.8	1.3	V
t _{rr}	Reverse recovery time	I _S = 7.5 A, V _{DS} = 48 V,	V _{GS} = 0, See Figure 1	di/dt = 100 A/μs,		200		ns
Q _{RR}	Total source-drain diode charge	103 = 10 1,	Goo : .ga.o :			1.5		μС

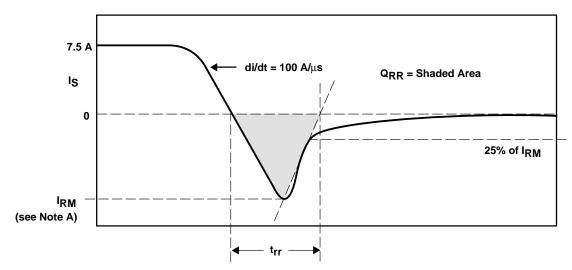
resistive-load switching characteristics, $T_C = 25^{\circ}C$

	PARAMETER	1	EST CONDITION	NS	MIN	TYP	MAX	UNIT
t _d (on)	Turn-on delay time					12		
td(off)	Turn-off delay time	V _{DD} = 25 V,	$R_L = 6.7 \Omega$,	$t_{en} = 10 \text{ ns},$		100		ns
t _r	Rise time	t _{dis} = 10 ns,	See Figure 2			43		115
tf	Fall time]				5		
Qg	Total gate charge					13.6	18	
Qgs	Gate-source charge	V _{DS} = 48 V, See Figure 3	$I_D = 2.5 A,$	$V_{GS} = 10 \text{ V},$		8.3	11	nC
Q _{gd}	Gate-drain charge	Occ rigare o				5.3	7	
L _D	Internal drain inductance					7		nH
LS	Internal source inductance					7		ıп

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power			62.5	°C/W
Pa in	Junction-to-case thermal resistance	All outputs with equal power			1.5	°C/W
R ₀ JC	Junction-to-case thermal resistance	One output dissipating power			3.3	°C/W

^{4.} These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.



NOTE A: I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveforms of Source-Drain Diode

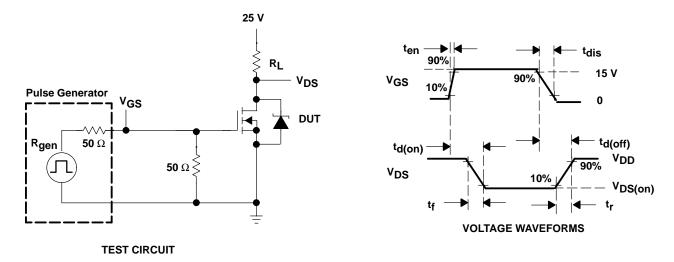


Figure 2. Resistive Switching

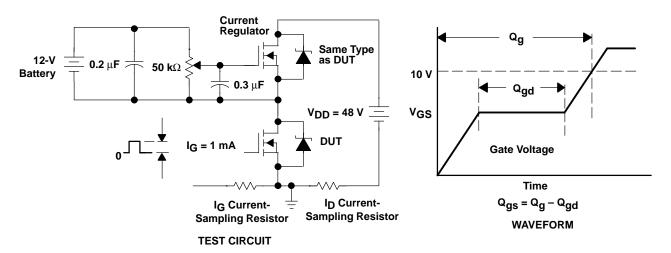
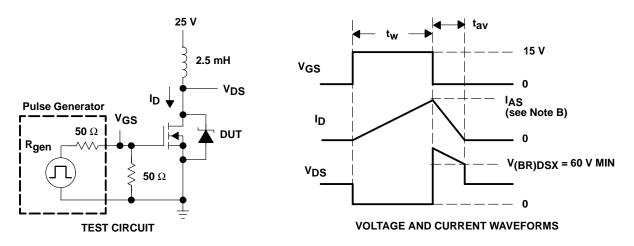


Figure 3. Gate-Charge Test Circuit and Waveform



NOTES: A. The pulse generator has the following characteristics: $t_f \le 10$ ns, $t_f \le 10$ ns, $t_O = 50 \Omega$.

B. Input pulse duration (t_W) is increased until peak current $I_{AS} = 7.5 \text{ A}$.

Energy test level is defined as
$$E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 120 \text{ mJ min.}$$

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE

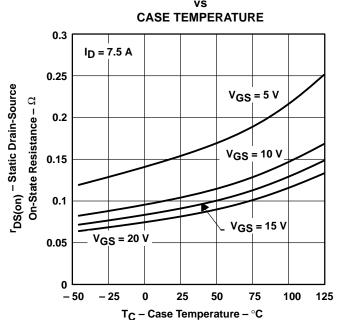


Figure 5

STATIC DRAIN-SOURCE ON-STATE RESISTANCE

DRAIN CURRENT

Figure 6

ID - Drain Current - A

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

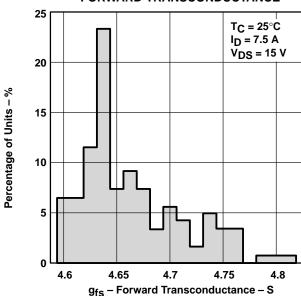


Figure 7

DRAIN CURRENT vs

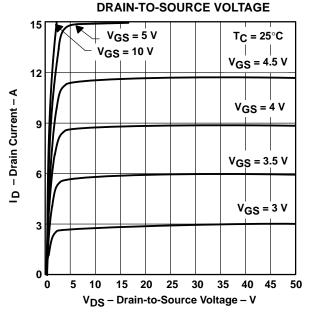


Figure 8

TYPICAL CHARACTERISTICS

GATE-SOURCE THRESHOLD VOLTAGE vs **CASE TEMPERATURE** V_{TGS} - Gate-Source Threshold Voltage - V $I_D = 1 \text{ mA}$ 1.8 1.6 1.4 1.2 1 0.8 0.6 0.4 0.2 0 - 50 - 25 25 50 75 100 125 T_C - Case Temperature - °C

Figure 9

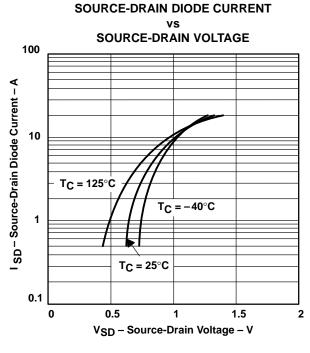


Figure 10

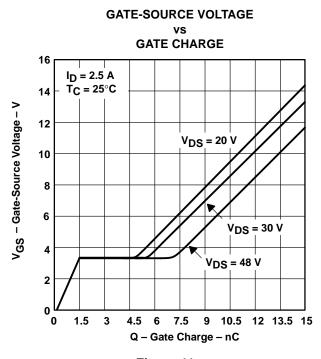


Figure 11

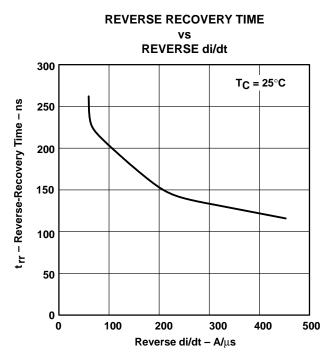


Figure 12

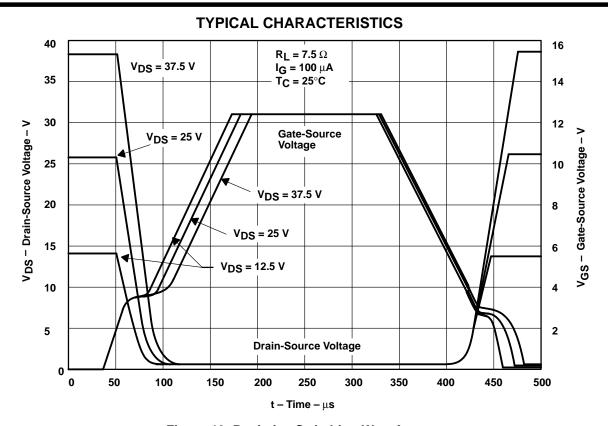
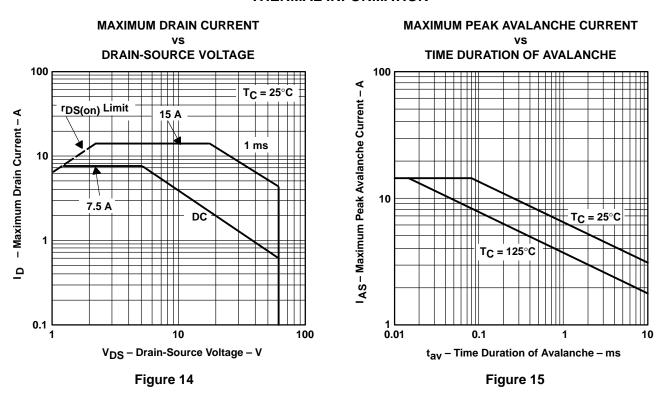


Figure 13. Resistive Switching Waveforms

THERMAL INFORMATION



NORMALIZED TRANSIENT THERMAL IMPEDANCE

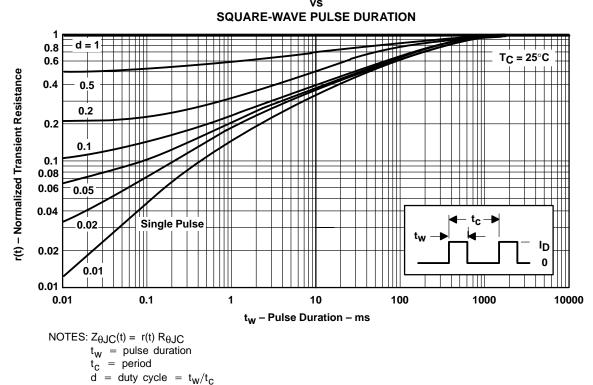


Figure 16



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TPIC2322L 3-CHANNEL COMMON-SOURCE LOGIC-LEVEL POWER DMOS ARRAY

SLIS036A - JUNE 1994 - REVISED OCTOBER 1994

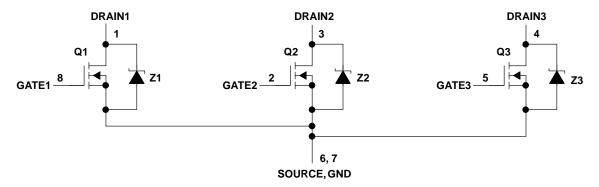
 Low r_{DS(on)} . . . 0.6 Ω Typ **D PACKAGE** (TOP VIEW) High-Voltage Outputs . . . 60 V Pulsed Current . . . 2.25 A Per Channel DRAIN1 8 GATE1 **Fast Commutation Speed** SOURCE/GND GATE2 DRAIN2 [6 SOURCE/GND Direct Logic-Level Interface DRAIN3 GATE3 5

description

The TPIC2322L is a monolithic logic-level power DMOS array that consists of three electrically isolated N-channel enhancement-mode DMOS transistors configured with a common source and open drains.

The TPIC2322L is offered in a standard eight-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature range of -40° C to 125° C.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V _{DS}	60 V
Gate-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage, V _{GS}	±20 V
Continuous drain current, each output, all outputs on, T _C = 25°C	0.75 A
Continuous source-to-drain diode current, T _C = 25°C	0.75 A
Pulsed drain current, each output, I _{max} , T _C = 25°C (see Note 1 and Figure 15)	2.25 A
Single-pulse avalanche energy, E _{AS} , T _C = 25°C (see Figure 4)	30.4 mJ
Continuous total power dissipation at (or below) T _C = 25°C (see Figure 15)	0.95 W
Operating virtual junction temperature range, T _J	–40°C to 150°C
Operating case temperature range, T _C	–40°C to 125°C
Storage temperature range	65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%.



SLIS036A - JUNE 1994 - REVISED OCTOBER 1994

electrical characteristics, $T_C = 25^{\circ}C$ (unless otherwise noted)

	PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V _{(BR)DSX}	Drain-to-source breakdown voltage	$I_D = 250 \mu A$,	V _{GS} = 0	60			V
V _{GS(th)}	Gate-to-source threshold voltage	I _D = 1 mA, See Figure 5	$V_{DS} = V_{GS}$,	1.5	1.85	2.2	V
V _(BR)	Reverse drain to GND breakdown voltage	Drain to GND current	t = 250 μA	100			V
V _{DS(on)}	Drain-to-source on-state voltage	I _D = 0.75 A, See Notes 2 and 3	$V_{GS} = 5 V$,		0.45	0.53	V
VF(SD)	Forward on-state voltage, source-to-drain	I _S = 0.75 A, See Notes 2 and 3 a	VGS = 0 nd Figure 12		0.85	1	V
1	Zana mata vialtama dunin numant	V _{DS} = 48 V, V _{GS} = 0	T _C = 25°C		0.05	1	^
IDSS	Zero-gate-voltage drain current		I	T _C = 125°C		0.5	10
IGSSF	Forward gate current, drain short circuited to source	V _{GS} = 16 V,	$V_{DS} = 0$		10	100	nA
IGSSR	Reverse gate current, drain short circuited to source	V _{SG} = 16 V,	V _{DS} = 0		10	100	nA
lu.	Lookaga aurrant drain to CND	\/= 0.15 - 48 \/	T _C = 25°C		0.05	1	^
llkg	Leakage current, drain-to-GND	V _{DGND} = 48 V	T _C = 125°C		0.5	10	μΑ
" "	Static drain-to-source on-state resistance	V _{GS} = 5 V, I _D = 0.75 A,	T _C = 25°C		0.6	0.7	Ω
^r DS(on)	Static draffice-source off-state resistance	See Notes 2 and 3 and Figures 6 and 7	T _C = 125°C		0.94	1	32
9fs	Forward transconductance	V _{DS} = 15 V, See Notes 2 and 3 a	I _D = 0.5 A, nd Figure 9	0.75	0.9		S
C _{iss}	Short-circuit input capacitance, common source				115	145	
C _{oss}	Short-circuit output capacitance, common source	1 20	$V_{GS} = 0$,		60	75	pF
C _{rss}	Short-circuit reverse transfer capacitance, common source	f = 1 MHz,	See Figure 11		30	40	Ρ'

source-to-drain diode characteristics, $T_C = 25^{\circ}C$ (see schematic diagram)

	PARAMETER	TEST C	MIN	TYP	MAX	UNIT	
t _{rr}	Reverse-recovery time	I _F = 0.375 A,	V _{DS} = 48 V,		85		ns
Q _{RR}	Total diode charge	di/dt = 100 A/μs,	See Figures 1 and 14		0.19		μC

NOTES: 2. Technique should limit T_J – T_C to 10°C maximum.

3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

resistive-load switching characteristics, T_C = 25°C

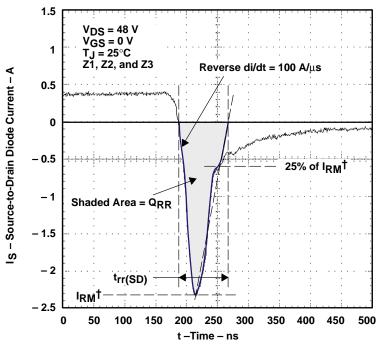
	PARAMETER	1	TEST CONDITIONS			TYP	MAX	UNIT				
t _d (on)	Turn-on delay time					21	42					
td(off)	Turn-off delay time	V _{DD} = 25 V,	$R_L = 67 \Omega$,	$t_{en} = 10 \text{ ns},$		26	52	no				
t _r	Rise time	$t_{dis} = 10 \text{ ns},$	See Figure 2			14	28	ns				
t _f	Fall time					13	26					
Qg	Total gate charge					1.8	2.3					
Q _{gs(th)}	Threshold gate-to-source charge	V _{DS} = 48 V, See Figure 3	$I_D = 0.375 A,$	$V_{GS} = 5 V$,		0.4	0.5	nC				
Q _{gd}	Gate-to-drain charge	occ i iguic o	Goo'r iguro o	Goorigaloo	Goorigaloo	Goo'r igure o			1.	1.1	1.4	
L _D	Internal drain inductance					5		ni i				
LS	Internal source inductance					5		nH				
Rg	Internal gate resistance					0.25		Ω				

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance, See Note 4	All outputs with equal power		130		°C/W
$R_{\theta JP}$	Junction-to-pin thermal resistance			44		°C/W

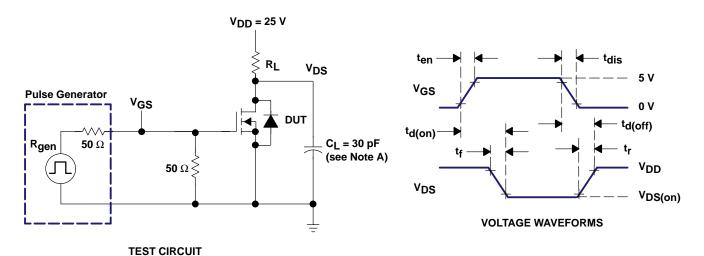
NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink.

PARAMETER MEASUREMENT INFORMATION



†I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

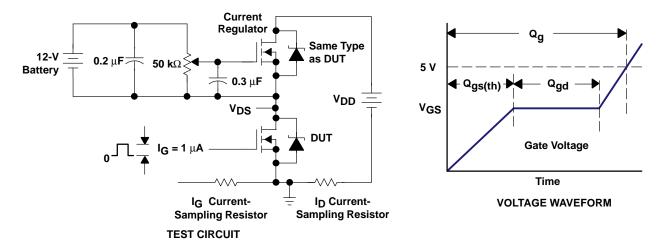
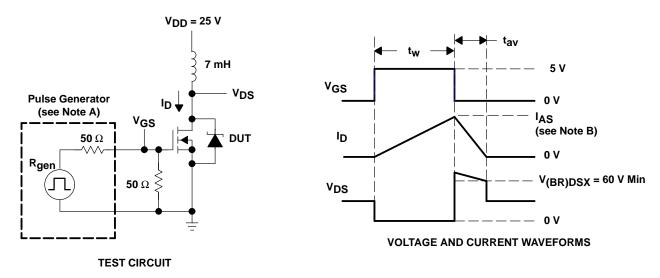


Figure 3. Gate-Charge Test Circuit and Voltage Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_O = 50 \Omega$.

B. Input pulse duration (t_W) is increased until peak current IAS = 2.25 A.

Energy test level is defined as $E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 30.4 \text{ mJ}.$

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

JUNCTION TEMPERATURE 2.5 V_{DS} = V_{GS} I_D = 1 mA 1.5 I_D = 100 μA 1.5 -40 -20 0 20 40 60 80 100 120 140 160 T_J - Junction Temperature - °C

Figure 5

GATE-TO-SOURCE THRESHOLD VOLTAGE

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE

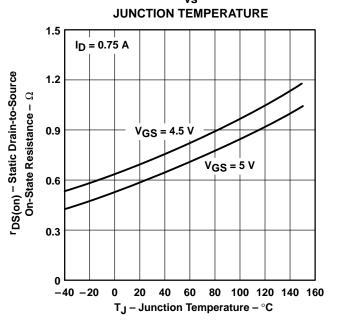


Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE

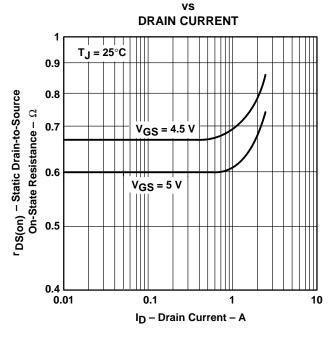


Figure 7

DRAIN-TO-SOURCE VOLTAGE 2.25 △VGS = 0.2 V T_J = 25°C 2 1.75 V_{GS} = 5 V V_{GS} = 4 V ⁻⁾ ID- Drain Current - A 1.5 1.25 1 0.75 **VGS = 3 V** 0.5 0.25 0 0 V_{DS} - Drain-to-Source Voltage - V

DRAIN CURRENT

Figure 8

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

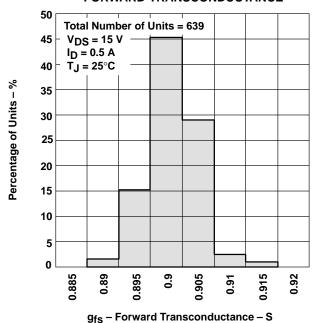


Figure 9

DRAIN CURRENT vs

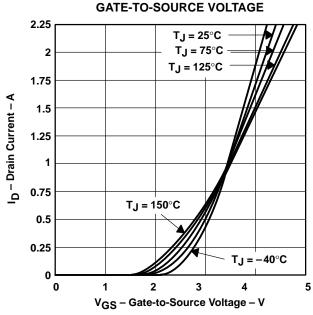


Figure 10

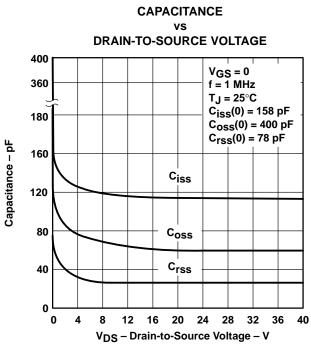


Figure 11

DRAIN-TO-SOURCE VOLTAGE AND GATE-TO-SOURCE VOLTAGE

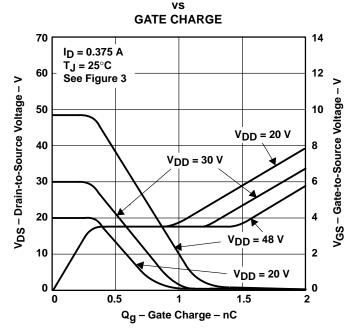


Figure 13

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

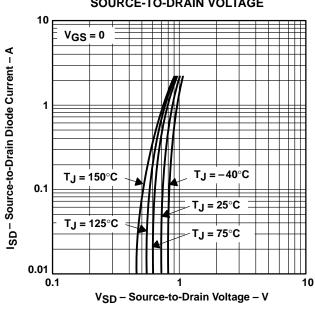


Figure 12

REVERSE-RECOVERY TIME

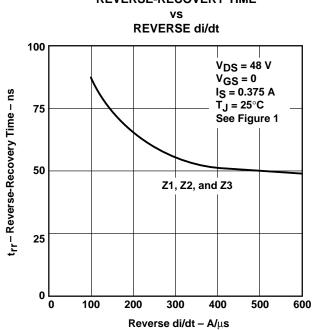
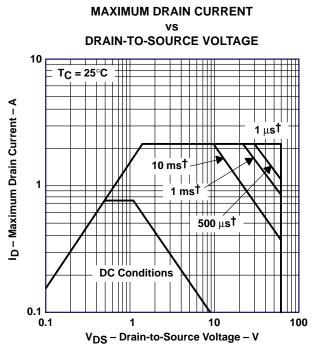


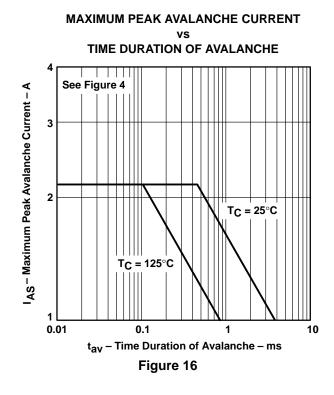
Figure 14

THERMAL INFORMATION



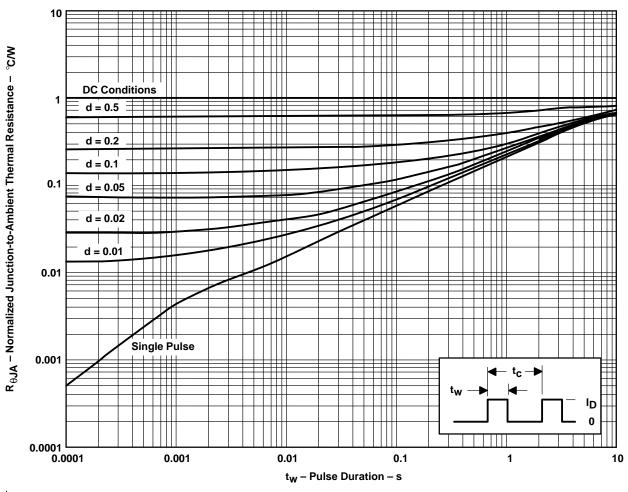
†Less than 2% duty cycle

Figure 15



THERMAL INFORMATION

D PACKAGE† NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE vs PULSE DURATION



† Device mounted on FR4 printed-circuit board with no heat sink.

NOTES: $Z_{\theta A}(t) = r(t) R_{\theta JA}$ $t_W = \text{pulse duration}$ $t_C = \text{cycle time}$

 $d = duty cycle = t_W/t_C$

Figure 17

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TPIC3322L 3-CHANNEL COMMON-DRAIN LOGIC-LEVEL POWER DMOS ARRAY

SLIS035B - JUNE 1994 - REVISED SEPTEMBER 1995

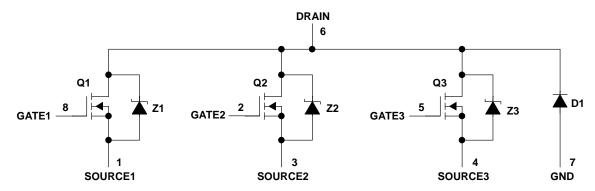
 Low r_{DS(on)} 0.6 Ω Typ High-Voltage Outputs 60 V 	D PACKAGE (TOP VIEW)
 Pulsed Current 2.25 A Per Channel Fast Commutation Speed 	SOURCE1 1 8 GATE1 GATE2 2 7 GND
Direct Logic-Level Interface	SOURCE2 3 6 DRAIN SOURCE3 4 5 GATE3

description

The TPIC3322L is a monolithic logic-level power DMOS transistor array that consists of three isolated N-channel enhancement-mode DMOS transistors configured with a common drain and open sources.

The TPIC3322L is offered in a standard 8-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature range of -40° C to 125° C.

schematic diagram



absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V _{DS}	
Drain-to-GND voltage	
Gate-to-source voltage, V _{GS}	
Continuous drain current, each output, all outputs on, T _C = 25°C	0.75 A
Continuous source-to-drain diode current, T _C = 25°C	0.75 A
Pulsed drain current, each output, I _{max} , T _C = 25°C (see Note 1 and Figure 15)	2.25 A
Single-pulse avalanche energy, E _{AS} , T _C = 25°C (see Figure 4)	19 mJ
Continuous total power dissipation at (or below) T _C = 25°C (see Figure 15)	0.95 W
Operating virtual junction temperature range, T _J	40°C to 150°C
Operating case temperature range, T _C	40°C to 125°C
Storage temperature range, T _{stq}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%.



SLIS035B – JUNE 1994 – REVISED SEPTEMBER 1995

electrical characteristics, $T_C = 25^{\circ}C$ (unless otherwise noted)

PARAMETER TEST CONDITIONS			ITIONS	MIN	TYP	MAX	UNIT
V(BR)DSX	Drain-to-source breakdown voltage	$I_D = 250 \mu\text{A},$	V _{GS} = 0	60			V
VGS(th)	Gate-to-source threshold voltage	$I_D = 1 \text{ mA},$	$V_{DS} = V_{GS}$	1.5	1.85	2.2	V
V _(BR)	Reverse drain-to-GND breakdown voltage (across D1)	Drain-to-GND curren	t = 250 μA	100			V
V _{DS(on)}	Drain-to-source on-state voltage	I _D = 0.75 A, See Notes 2 and 3	$V_{GS} = 5 V$,		0.45	0.53	V
VF	Forward on-state voltage, GND-to-drain	I _D = 0.75 A, See Notes 2 and 3			1.8		V
V _F (SD)	Forward on-state voltage, source-to-drain	Is = 0.75 A, See Notes 2 and 3 a	VGS = 0, nd Figure 12		0.85	1	V
l=	Zoro goto voltogo drain aurrent	V _{DS} = 48 V,	T _C = 25°C		0.05	1	
IDSS	Zero-gate-voltage drain current	$V_{GS} = 0$	T _C = 125°C		0.5	10	μΑ
IGSSF	Forward gate current, drain short circuited to source	V _{GS} = 16 V,	V _{DS} = 0		10	100	nA
I _{GSSR}	Reverse gate current, drain short circuited to source	V _{SG} = 16 V,	$V_{DS} = 0$		10	100	nA
l	Leakage current, drain-to-GND	\/p a \ \ p = 49 \/	T _C = 25°C		0.05	1	μΑ
l _{lkg}	Leakage current, drain-to-GND	V _{DGND} = 48 V	T _C = 125°C		0.5	10	μΑ
rno()	Static drain-to-source on-state resistance	$V_{GS} = 5 \text{ V},$ $I_{D} = 0.75 \text{ A},$	T _C = 25°C		0.6	0.7	Ω
rDS(on)	Static drain-to-source on-state resistance	See Notes 2 and 3 and Figures 6 and 7	T _C = 125°C		0.94	1	32
9fs	Forward transconductance	V _{DS} = 10 V, See Notes 2 and 3 a	I _D = 0.5 A, nd Figure 9	0.75	0.9		S
C _{iss}	Short-circuit input capacitance, common source				115	145	
C _{oss}	Short-circuit output capacitance, common source	V _{DS} = 25 V,	$V_{GS} = 0$,		60	75	рF
C _{rss}	Short-circuit reverse transfer capacitance, common source	f = 1 MHz,	See Figure 11		30	40	Pi

NOTES: 2. Technique should limit $T_J - T_C$ to $10^{\circ}C$ maximum.

source-to-drain and GND-to-drain diode characteristics, $T_{\mbox{\scriptsize C}}$ = 25 $^{\circ}\mbox{\scriptsize C}$

	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
	Payoroa rosayory timo			Z1, Z2, Z3		30		
trr(SD)	Reverse-recovery time	$l_S = 0.375 \text{ A},$ $di/dt = 100 \text{ A}/\mu \text{s},$	$V_{GS} = 0,$ $V_{DS} = 48 \text{ V},$	D1		85		ns
055	Total diada abarga	See Figures 1 and 14	VDS = 40 V,	Z1, Z2, Z3		0.03		
Q _{RR}	Total diode charge			D1		0.19		μC

^{3.} These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

resistive-load switching characteristics, T_C = 25°C

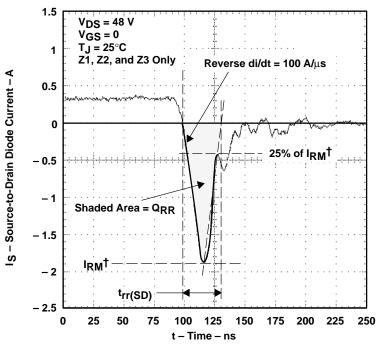
	PARAMETER	1	TEST CONDITIO	NS	MIN	TYP	MAX	UNIT																		
t _d (on)	Turn-on delay time					8	16																			
td(off)	Turn-off delay time	V _{DD} = 25 V,	$R_L = 67 \Omega$,	$t_{r1} = 10 \text{ ns},$		12	24	20																		
t _{r2}	Rise time	$t_{f1} = 10 \text{ ns},$	See Figure 2			14	28	ns																		
t _{f2}	Fall time]				13	26																			
Qg	Total gate charge					1.8	2.3																			
Q _{gs(th)}	Threshold gate-to-source charge	$V_{DS} = 48 \text{ V},$				V _{DS} = 48 V, See Figure 3															$I_D = 0.375 A,$	$V_{GS} = 5 V$		0.4	0.5	nC
Q _{gd}	Gate-to-drain charge	gui o o				1.1	1.4																			
L _D	Internal drain inductance					5		11																		
LS	Internal source inductance					5		nH																		
Rg	Internal gate resistance					0.25		Ω																		

thermal resistance

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance, See Note 4	All outputs with equal power		130		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			44	, and the second	

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink.

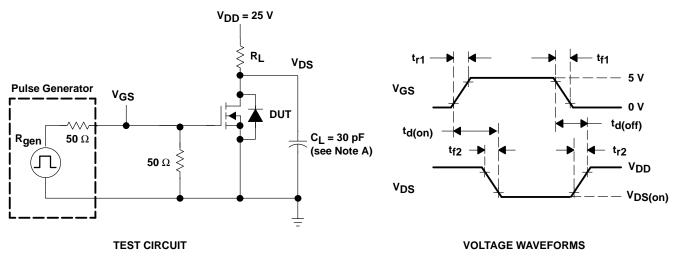
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current NOTE A. The above waveform represents D1 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode





NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

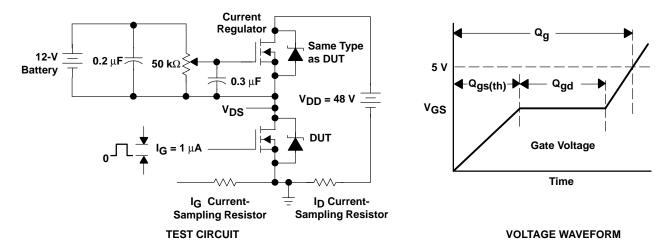
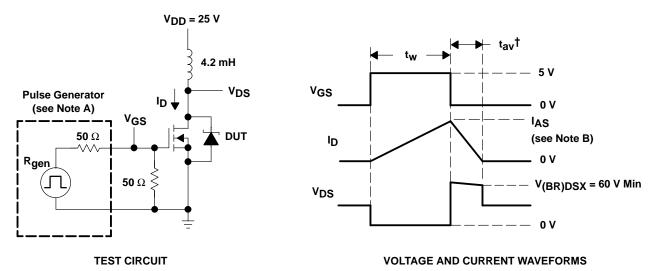


Figure 3. Gate-Charge Test Circuit and Voltage Waveform



† Non-JEDEC symbol for avalanche time

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $z_0 = 50 \Omega$.

B. Input pulse duration (t_W) is increased until peak current IAS = 2.25 A.

Figure 5

Energy test level is defined as
$$E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 19 \text{ mJ}$$
, where $t_{av} = \text{avalanche time}$.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE **JUNCTION TEMPERATURE JUNCTION TEMPERATURE** 2.5 1.5 VGS (th) - Gate-to-Source Threshold Voltage - V $I_D = 0.75 A$ $V_{DS} = V_{GS}$ DS(on) - Static Drain-to-Source On-State 2 1.2 $I_D = 1 mA$ Resistance - Ω 1.5 0.9 $I_D = 100 \, \mu A$ VGS = 4.5 V $V_{GS} = 5 V$ 0.6 0.5 0.3 20 40 60 80 100 120 140 160 40 60 80 100 120 140 160 -40 - 20-40 - 2020 T_J - Junction Temperature - °C T_J - Junction Temperature - °C

Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE

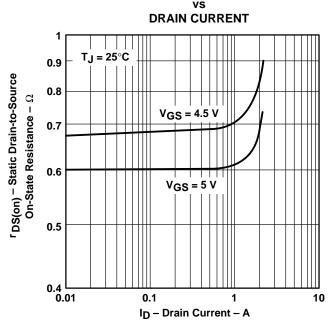


Figure 7

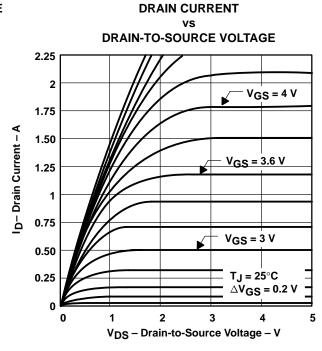


Figure 8

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

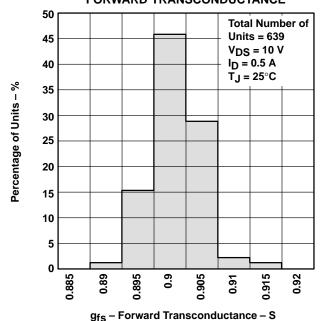


Figure 9

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

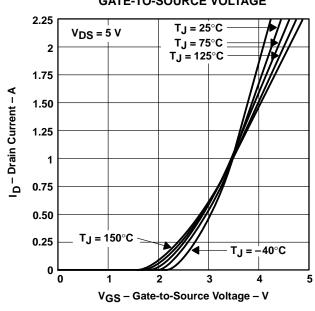


Figure 10



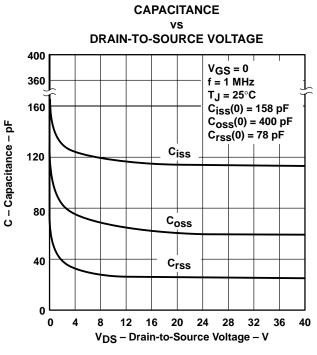


Figure 11

DRAIN-TO-SOURCE AND GATE-TO-SOURCE VOLTAGE

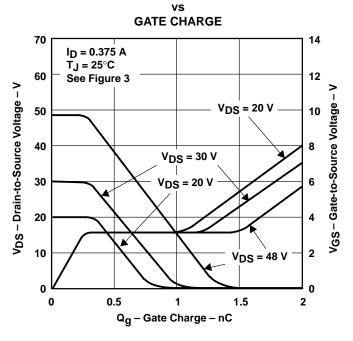


Figure 13

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

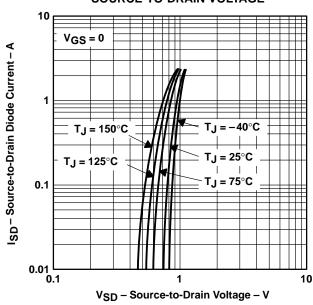


Figure 12

REVERSE-RECOVERY TIME

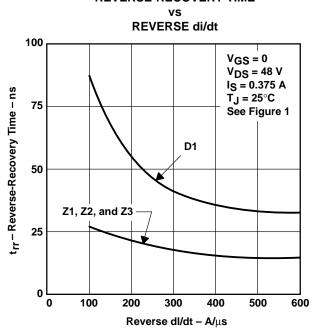


Figure 14

THERMAL INFORMATION

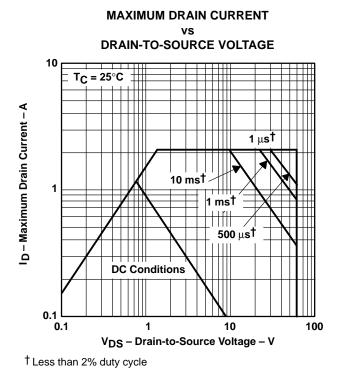


Figure 15

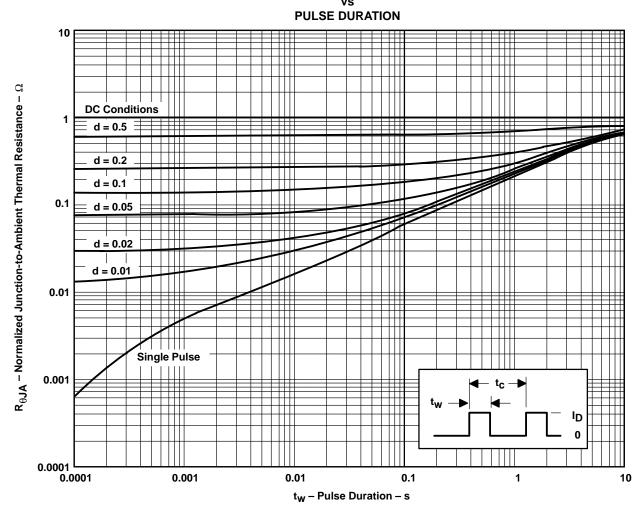
MAXIMUM PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE 4 See Figure 4 TC = 125°C TC = 125°C Tay - Time Duration of Avalanche - ms

Figure 16

TEXAS
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THERMAL INFORMATION

NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE



† Device mounted on FR4 printed-circuit board with no heat sink.

NOTE A: $Z_{\theta A}(t) = r(t) R_{\theta JA}$ $t_W = \text{pulse duration}$ $t_C = \text{cycle time}$ $d = \text{duty cycle} = t_W/t_C$

Figure 17

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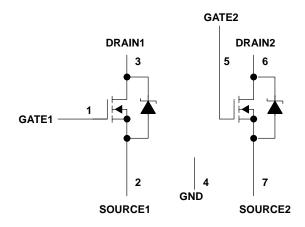
SLIS020 - SEPTEMBER 1992

- Two 7.5-A Independent Output Channels, Continuous Current Per Channel
- Low r_{DS(on)} . . . 0.09 Ω Typical
- Output Voltage . . . 60 V
- Pulsed Current . . . 15 A Per Channel
- Avalanche Energy . . . 120 mJ

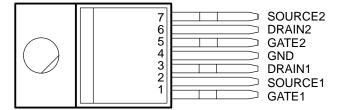
description

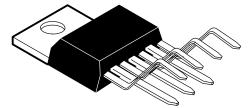
The TPIC5201 is a power monolithic DMOS array that consists of dual independent N-channel enhancement-mode DMOS transistors.

schematic



KV PACKAGE (TOP VIEW)





To ensure correct device operation, the source and the drain of the same transistor cannot simultaneously be taken below GND.

The tab is electrically connected to GND.

absolute maximum ratings over operating case temperature range (unless otherwise noted)

Drain-source voltage, V _{DS}	60 V
Source-GND voltage	60 V
Drain-GND voltage	60 V
Gate-source voltage, V _{GS}	±20 V
Continuous source-drain diode current	7.5 A
Pulsed drain current, each output, all outputs on, I _D (see Note 1)	15 A
Continuous drain current, each output, all outputs on	7.5 A
Single-pulse avalanche energy, E _{AS} (see Figure 4)	120 mJ
Continuous power dissipation at (or below) T _A = 25°C (see Note 2)	2 W
Continuous power dissipation at (or below) T _C = 75°C, all outputs on (see Note 2)	31 W
Operating virtual junction temperature range, T _J	-40°C to 150°C
Operating case temperature range, T _C	-40°C to 125°C
Storage temperature range, T _{stq}	-40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

NOTES: 1. Pulse duration = 10 ms, duty cycle = 6%

2. For operation above 25°C free-air temperature, derate linearly at the rate of 16 mW/°C. For operation above 75°C case temperature, and with all outputs conducting, derate linearly at the rate of 0.42 W/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded.



SLIS020 - SEPTEMBER 1992

electrical characteristics, $T_C = 25^{\circ}C$ (unless otherwise noted)

	PARAMETER		TEST CON	DITIONS		MIN	TYP	MAX	UNIT
V _{(BR)DS}	Drain-source breakdown voltage	$I_D = 1 \mu A$,	V _{GS} = 0			60			V
VTGS	Gate-source threshold voltage	$I_D = 1 \text{ mA},$	V _{DS} = V _{GS}			1.2	1.75	2.4	V
V _{DS(on)}	Drain-source on-state voltage	$I_D = 7.5 A,$	V _{GS} = 15 V,	See Notes	3 and 4		0.68	0.94	V
\/p.o.o	Zero-gate-voltage drain current	V _{DS} = 48 V,	V _{DS} = 0		$T_C = 25^{\circ}C$		0.07	1	μΑ
VDSS	Zero-gate-voltage drain current	VDS = 46 V,	VDS = 0		T _C = 125°C		1.3	10	μΑ
IGSSF	Forward gate current, drain short circuited to source	V _{GS} = 20 V,	V _{DS} = 0				10	100	nA
IGSSR	Reverse gate current, drain short circuited to source	$V_{GS} = -20 \text{ V},$	V _{DS} = 0				10	100	nA
	Static drain-source on-state	$V_{GS} = 15 \text{ V},$	I _D = 7.5 A,		T _C = 25°C		0.09	0.125	Ω
^r DS(on)	resistance	See Notes 3 ar		es 5 and 6	T _C = 125°C		0.15	0.21	12
9fs	Forward transconductance	$V_{DS} = 15 V$,	I _D = 5 A,	See Notes	3 and 4	2.5	4.7		S
C _{iss}	Short-circuit input capacitance, common source						490		
C _{oss}	Short-circuit output capacitance, common source	V _{DS} = 25 V,	$V_{GS} = 0$,	f = 300 kHz	<u>'</u>		285		pF
C _{rss}	Short-circuit reverse transfer capacitance, common source						90		

NOTES: 3. Technique should limit $T_J - T_C$ to 10°C maximum.

source-drain diode characteristics, $T_C = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{SD}	Forward on voltage	$I_S = 7.5 \text{ A}, V_{GS} = 0,$		0.8	1.3	V
t _{rr}	Reverse-recovery time	$di/dt = 100 \text{ A/}\mu\text{s}, \text{V}_{DS} = 48 \text{ V},$		200		ns
Q _{RR}	Total source-drain diode charge	See Figure 1		1.5		μС

resistive-load switching characteristics, $\rm T_{\hbox{\scriptsize C}}$ = 25 $^{\circ} \hbox{\scriptsize C}$

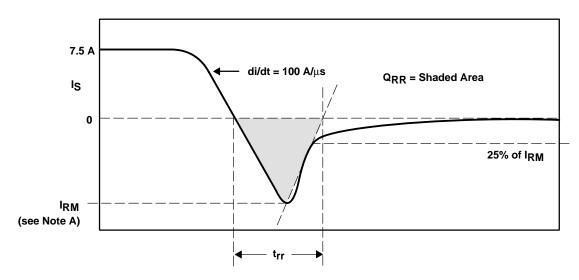
	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT															
td(on)	Turn-on delay time					12																	
t _r	Rise time	$V_{DD} = 25 \text{ V}, R_{L} = 6.7$	$R_L = 6.7 \Omega$,	$t_{en} = 10 \text{ ns},$		43		ns															
td(off)	Turn-off delay time	$t_{dis} = 10 \text{ ns},$				100		115															
tf	Fall time]				5																	
Qg	Total gate charge					13.6	18																
Qgs	Gate-source charge	V _{DD} = 48 V, See Figure 3																$I_D = 2.5 A,$	$V_{GS} = 15,$		8.3	11	nC
Q _{gd}	Gate-drain charge		500 1 igui 0 0			5.3	7																
L _D	Internal drain inductance					7		nH															
LS	Internal source inductance	_				7		ıп															

thermal resistance

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power			62.5	°C/W
Pa to	Junction-to-case thermal resistance	All outputs with equal power			2.4	°C/W
R ₀ JC	Junction-to-case thermal resistance	One output dissipating power			3.3	°C/W



^{4.} These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.



NOTE A: I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveforms of Source-Drain Diode

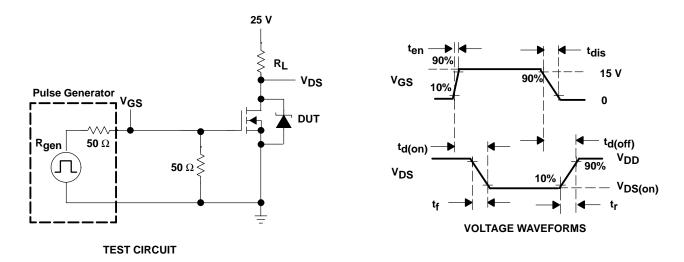


Figure 2. Resistive Switching

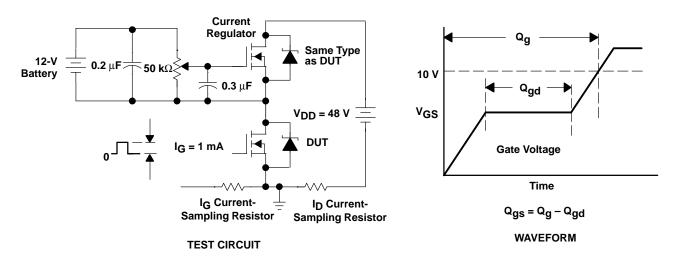
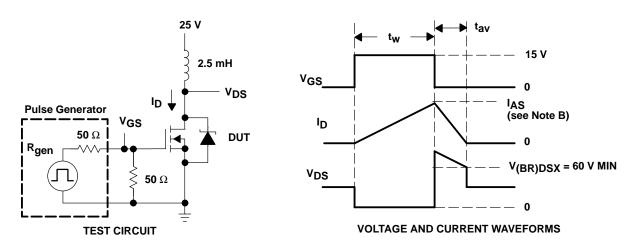


Figure 3. Gate Charge Test Circuit and Waveform



NOTES: A. The pulse generator has the following characteristics: $t_{\Gamma} \le 10$ ns, $t_{f} \le 10$ ns, $t_{O} = 50$ Ω .

B. Input pulse duration (t_W) is increased until peak current $I_{AS} = 7.5 \text{ A}$.

Energy test level is defined as
$$E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 120 \text{ mJ min.}$$

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

STATIC DRAIN-SOURCE ON-STATE RESISTANCE

CASE TEMPERATURE 0.3 $I_D = 7.5 A$ 0.25 ^rDS(on) - Static Drain-Source V_{GS} = 5 V On-State Resistance – Ω 0.2 VGS = 10 V 0.15 0.1 V_{GS} = 15 V V_{GS} = 20 V 0.05 0

STATIC DRAIN-SOURCE ON-STATE RESISTANCE

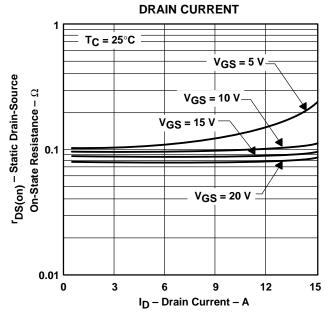


Figure 5

25

T_C - Case Temperature - °C

50

75

100

125

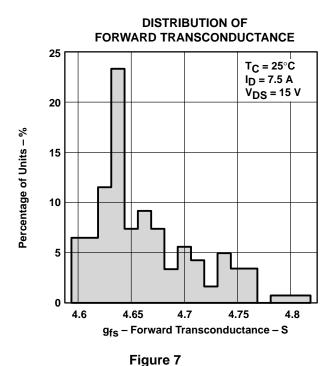
0

- 50

- 25



Figure 6



DRAIN CURRENT

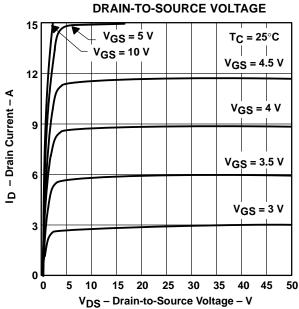


Figure 8

GATE-SOURCE THRESHOLD VOLTAGE CASE TEMPERATURE V_{TGS} - Gate-Source Threshold Voltage - V $I_D = 1 \text{ mA}$ 1.8 1.6 1.4 1.2 1 8.0 0.6 0.4 0.2 - 50 - 25 25 50 75 100 125 T_C – Case Temperature – $^{\circ}C$



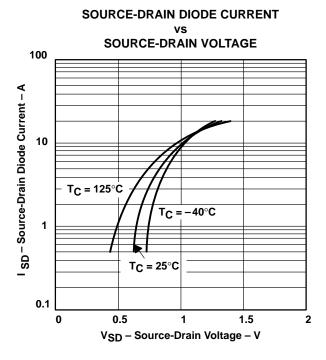
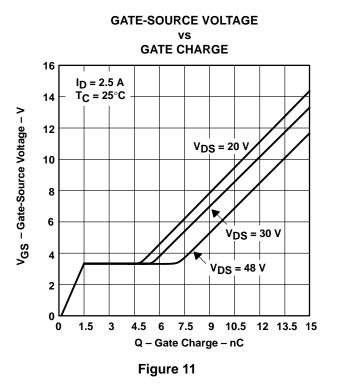


Figure 10



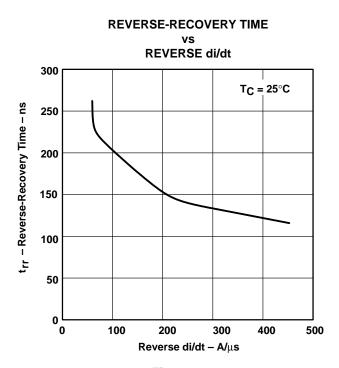


Figure 12

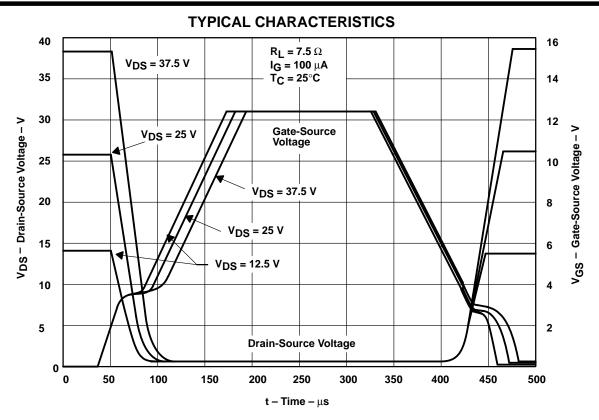
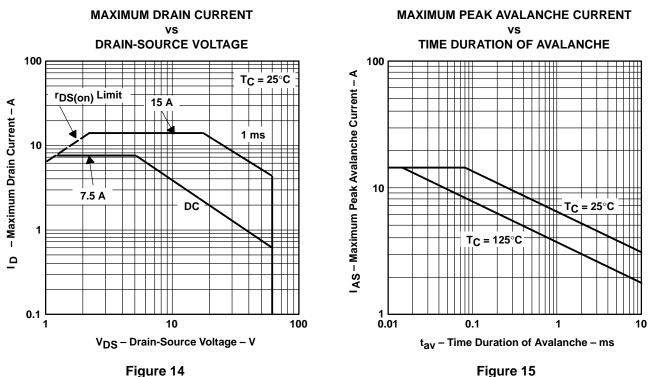


Figure 13. Resistive Switching Waveforms

THERMAL INFORMATION



iguic i 4

NORMALIZED TRANSIENT THERMAL IMPEDANCE **SQUARE-WAVE PULSE DURATION** 0.8 0.6 r(t) - Normalized Transient Resistance 0.4 0.5 0.2 0.2 0.1 0.08 0.06 0.05 0.04 Single Pulse 0.02 0.02 0.01 0.01 0.1 100 1000 10000 0.01 10 t_W - Pulse Duration - ms NOTES: $Z_{\theta JC}(t) = r(t) R_{\theta JC}$ t_W = pulse duration

Figure 16

= period

 $d = duty cycle = t_W/t_C$



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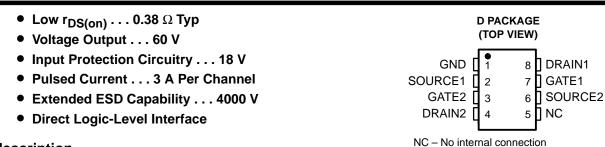
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TPIC5223L 2-CHANNEL INDEPENDENT GATE-PROTECTED LOGIC-LEVEL POWER DMOS ARRAY

SLIS043A - NOVEMBER 1994 - REVISED SEPTEMBER 1995

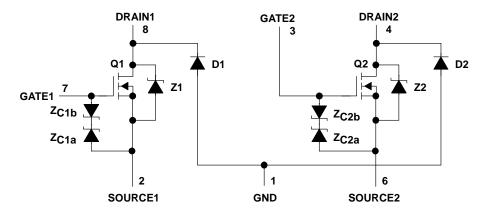


description

The TPIC5223L is a monolithic gate-protected logic-level power DMOS array that consists of two electrically isolated independent N-channel enhancement-mode DMOS transistors. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-k Ω resistor.

The TPIC5223L is offered in a standard eight-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature of -40° C to 125° C.

schematic



NOTE A: For correct operation, no terminal may be taken below GND.

TPIC5223L 2-CHANNEL INDEPENDENT GATE-PROTECTED LOGIC-LEVEL POWER DMOS ARRAY

SLIS043A - NOVEMBER 1994 - REVISED SEPTEMBER 1995

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V _{DS}	60 V
Source-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage range, V _{GS}	\dots -9 V to 18 V
Continuous drain current, each output, T _C = 25°C	1 A
Continuous source-to-drain diode current, T _C = 25°C	
Pulsed drain current, each output, I _{max} , T _C = 25°C (see Note 1 and Figure 15)	3 A
Continuous gate-to-source zener diode current, T _C = 25°C	$\dots \dots \pm 50 \text{ mA}$
Pulsed gate-to-source zener-diode current, T _C = 25°C	±500 mA
Single-pulse avalanche energy, E _{AS} , T _C = 25°C (see Figures 4 and 16)	108 mJ
Continuous total power dissipation, T _C = 25°C (see Figure 15)	0.95 W
Operating virtual junction temperature range, T _J	40°C to 150°C
Operating case temperature range, T _C	40°C to 125°C
Storage temperature range, T _{stq}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%



TPIC5223L 2-CHANNEL INDEPENDENT GATE-PROTECTED LOGIC-LEVEL POWER DMOS ARRAY SLIS043A – NOVEMBER 1994 – REVISED SEPTEMBER 1995

electrical characteristics, $T_C = 25^{\circ}C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V(BR)DSX	Drain-to-source breakdown voltage	I _D = 250 μA,	V _{GS} = 0	60			V
VGS(th)	Gate-to-source threshold voltage	I _D = 1 mA, See Figure 5	$V_{DS} = V_{GS}$	1.5	2.05	2.2	V
V _(BR) GS	Gate-to-source breakdown voltage	I _{GS} = 250 μA		18			V
V _(BR) SG	Source-to-gate breakdown voltage	I _{SG} = 250 μA		9			V
V _(BR)	Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND current = 250 μA		100			V
V _{DS(on)}	Drain-to-source on-state voltage	I _D = 1 A, See Notes 2 and 3	V _{GS} = 5 V,		0.375	0.425	V
V _{F(SD)}	Forward on-state voltage, source-to-drain	I _S = 1 A, V _{GS} = 0 (Z1, Z2), See Notes 2 and 3 and Figure 12			0.85	1.2	V
VF	Forward on-state voltage, GND-to-drain	I _D = 1 A (D1, D2), See Notes 2 and 3			3		V
l	Zero-gate-voltage drain current	V _{DS} = 48 V,	T _C = 25°C		0.05	1	μΑ
IDSS	Zero-gate-voltage drain current	VGS = 0	T _C = 125°C		0.5	10	μΛ
IGSSF	Forward-gate current, drain short circuited to source	V _{GS} = 15 V,	V _{DS} = 0		20	200	nA
I _{GSSR}	Reverse-gate current, drain short circuited to source	V _{SG} = 5 V,	V _{DS} = 0		10	100	nA
l	Leakage current, drain-to-GND	V _{DGND} = 48 V	T _C = 25°C		0.05	1	μA
llkg	Leakage current, diam-to-GND		T _C = 125°C		0.5	10	μΑ
rDS(on)	Static drain-to-source on-state resistance	V _{GS} = 5 V, I _D = 1 A,	T _C = 25°C		0.38	0.43	Ω
	Citatio diaminito socioco cin state resistante	See Notes 2 and 3 and Figures 6 and 7	T _C = 125°C		0.61	0.65	32
9fs	Forward transconductance	V_{DS} = 15 V, I_{D} = 500 mA, See Notes 2 and 3 and Figure 9		1.2	1.49		S
C _{iss}	Short-circuit input capacitance, common source		V _{GS} = 0, See Figure 11		150	190	
C _{oss}	Short-circuit output capacitance, common source	$V_{DS} = 25 V$,			100	125	pF
C _{rss}	Short-circuit reverse transfer capacitance, common source	f = 1 MHz,			40	50	P'

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.

source-to-drain and GND-to-drain diode characteristics, $T_C = 25^{\circ}C$

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t _{rr}	Payersa receivery time			Z1 and Z2		50		20
	Reverse-recovery time	Is = 500 mA,	$V_{DS} = 48 \text{ V},$	D1 and D2		210		ns
Q _{RR}	Total diada abarga	VGS = 0, See Figures 1 and 14	di/dt = 100 A/μs,	Z1 and Z2		50		nC
	Total diode charge			D1 and D2		800		IIC



^{3.} These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

TPIC5223L 2-CHANNEL INDEPENDENT GATE-PROTECTED LOGIC-LEVEL POWER DMOS ARRAY

SLIS043A - NOVEMBER 1994 - REVISED SEPTEMBER 1995

resistive-load switching characteristics, T_C = 25°C

	PARAMETER TEST CONDITIONS		MIN	TYP	MAX	UNIT
td(on)	Turn-on delay time			34	70	
td(off)	Turn-off delay time	$V_{DD} = 25 \text{ V}, R_L = 50 \Omega, t_{r1} = 10 \text{ ns},$		20	40	ns
t _{r1}	Rise time	t _{f1} = 10 ns, See Figure 2		28	55	
t _{f2}	Fall time			15	30	
Qg	Total gate charge			3.1	3.8	
Q _{gs(th)}	Threshold gate-to-source charge	$V_{DS} = 48 \text{ V}, I_{D} = 500 \text{ mA}, V_{GS} = 5 \text{ V},$ See Figure 3		0.5	0.6	nC
Q _{gd}	Gate-to-drain charge	- 000 r iguio 0		1.9	2.3	
L _D	Internal drain inductance			5		-11
LS	Internal source inductance			5		nΗ
Rg	Internal gate resistance			0.25		Ω

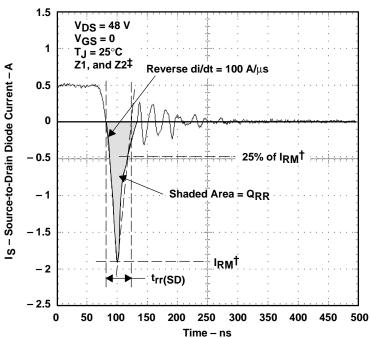
thermal resistance

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	See Notes 4 and 7		130		
$R_{\theta JB}$	Junction-to-board thermal resistance	See Notes 5 and 7		78.6		°C/W
$R_{\theta JP}$	Junction-to-pin thermal resistance	See Notes 6 and 7		34		

NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink.

- 5. Package mounted on a 24 in², 4-layer FR4 printed-circuit board.
- 6. Package mounted in intimate contact with infinite heatsink.
- 7. All outputs with equal power

PARAMETER MEASUREMENT INFORMATION

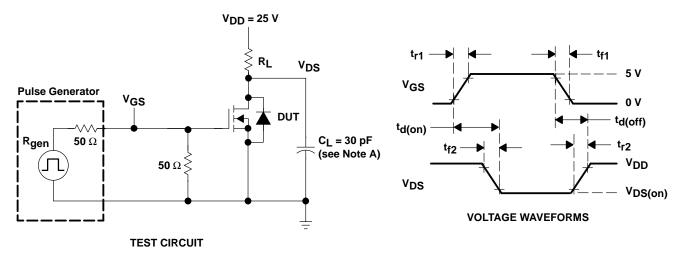


[†]I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode



[‡] The above waveform is representative of D1 and D2 in shape only.



NOTE A: C_I includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

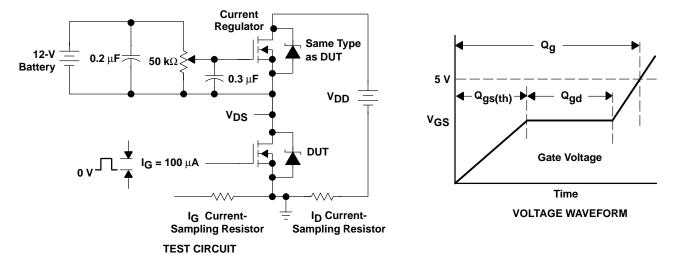
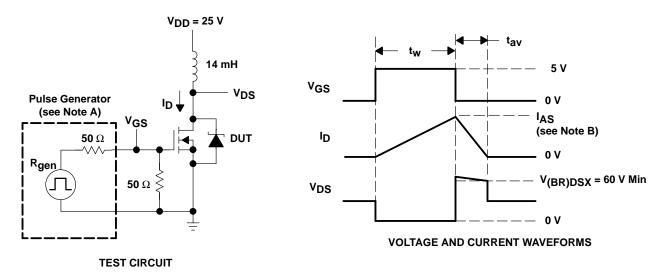


Figure 3. Gate-Charge Test Circuit and Voltage Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_O = 50 \Omega$.

B. Input pulse duration (t_W) is increased until peak current $I_{AS} = 3$ A.

Energy test level is defined as $E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 108 \text{ mJ}$, where $t_{av} = \text{avalanche time}$.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

Figure 5

JUNCTION TEMPERATURE $I_D = 1 A$ DS(on) - Static Drain-to-Source 0.8 On-State Resistance – Ω 0.6 V_{GS} = 4.5 V 0.4 $V_{GS} = 5 V$ 0.2 -40 -20 0 40 60 80 100 120 140 160 T_J – Junction Temperature – °C

Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE

TEXAS INSTRUMENTS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE

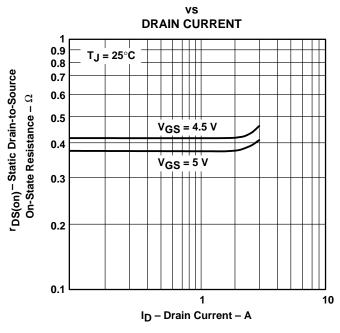


Figure 7

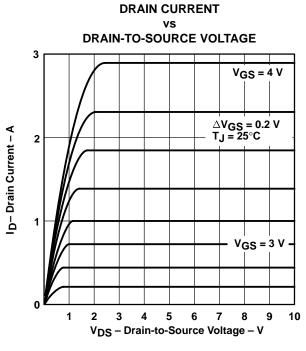


Figure 8

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

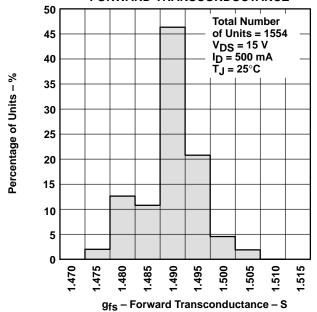


Figure 9

DRAIN CURRENT vs

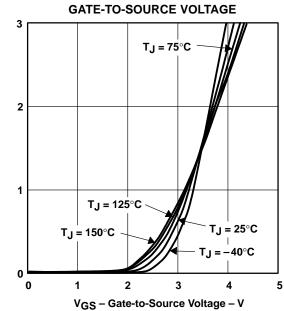


Figure 10

ID - Drain Current - A

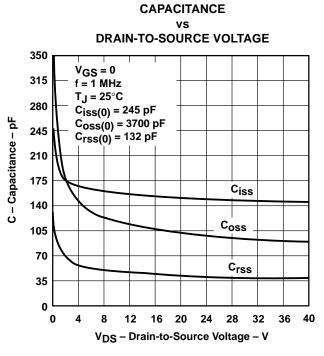


Figure 11

DRAIN-TO-SOURCE VOLTAGE AND GATE-TO-SOURCE VOLTAGE

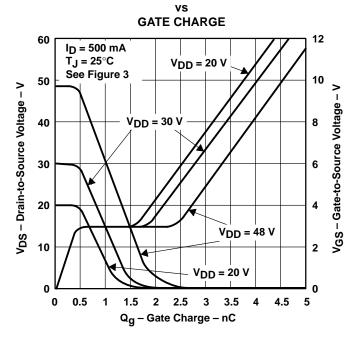


Figure 13

SOURCE-TO-DRAIN DIODE CURRENT SOURCE-TO-DRAIN VOLTAGE

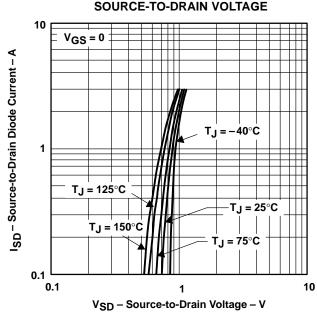


Figure 12

REVERSE-RECOVERY TIME

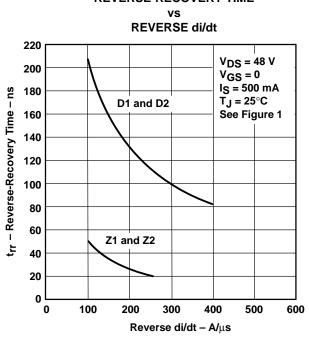
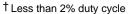


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT DRAIN-TO-SOURCE VOLTAGE 10 p T_C = 25°C ID - Maximum Drain Current - A 10 ms† **500** μs† θJP‡ **DC Conditions** 0.1 0.1 10 100 V_{DS} - Drain-to-Source Voltage - V



- ‡ Device mounted in intimate contact with infinite heatsink.
- § Device mounted on FR4 printed-circuit board with no heatsink.

Figure 15

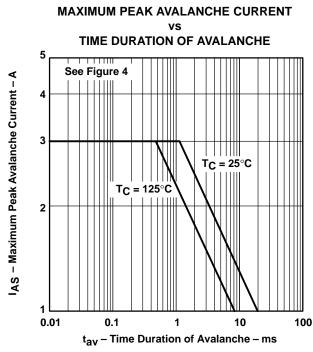
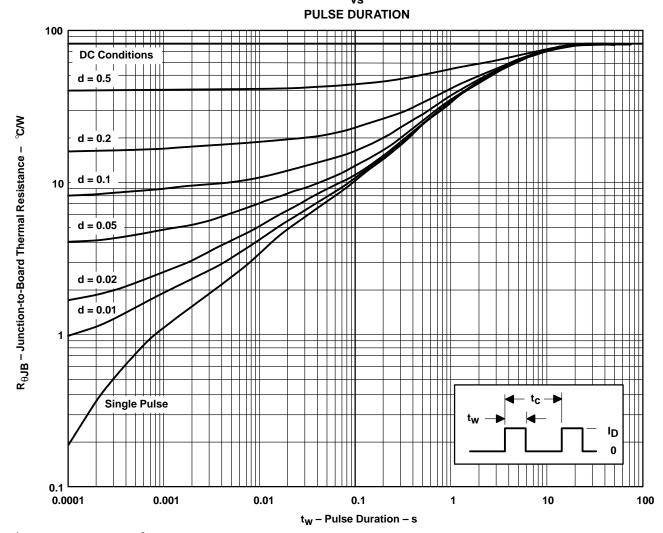


Figure 16

D PACKAGE[†] JUNCTION-TO-BOARD THERMAL RESISTANCE vs



[†] Device mounted on 24 in², 4-layer FR4 printed-circuit board with no heatsink.

NOTE A: $Z_{\theta B}(t) = r(t) R_{\theta JB}$ $t_W = \text{pulse duration}$ $t_C = \text{cycle time}$ $d = \text{duty cycle} = t_W/t_C$

Figure 17



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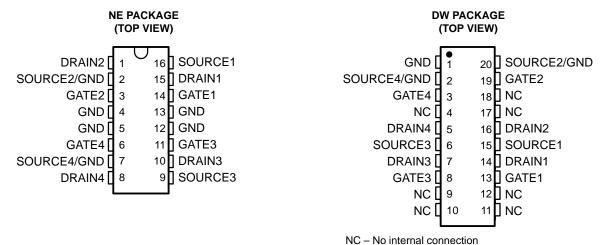
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- Low r_{DS(on)} . . . 0.3 Ω Typ
- High Voltage Output . . . 60 V
- Extended ESD Capability . . . 4000 V
- Pulsed Current . . . 10 A Per Channel
- Fast Commutation Speed

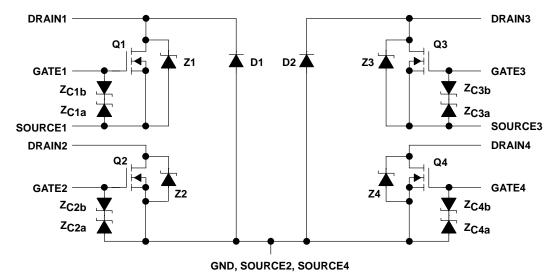
description

The TPIC5401 is a monolithic gate-protected power DMOS array that consists of four N-channel enhancement-mode DMOS transistors, two of which are configured with a common source. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-k Ω resistor.

The TPIC5401 is offered in a 16-pin thermally enhanced dual-in-line (NE) package and a 20-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature range of –40°C to 125°C.



schematic



NOTE: For correct operation, no terminal pin may be taken below GND.



TPIC5401 H-BRIDGE GATE-PROTECTED POWER DMOS ARRAY

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absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V _{DS}	60 V
Source-to-GND voltage (Q1, Q3)	
Drain-to-GND voltage (Q1, Q3)	
Drain-to-GND voltage (Q2, Q4)	60 V
Gate-to-source voltage range, V _{GS}	–9 V to 18 V
Continuous drain current, each output, T _C = 25°C: DW package	1.7 A
NE package	
Continuous source-to-drain diode current, T _C = 25°C	
Pulsed drain current, each output, I _{max} , T _C = 25°C (see Note 1 and Figure 15	s) 10 A
Continuous gate-to-source zener-diode current, T _C = 25°C	±50 mA
Pulsed gate-to-source zener-diode current, T _C = 25°C	±500 mA
Single-pulse avalanche energy, E _{AS} , T _C = 25°C (see Figures 4, 15, and 16)	21 mJ
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T _J	40°C to 150°C
Operating case temperature range, T _C	–40°C to 125°C
Storage temperature range	65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25^{\circ}C$ POWER RATING	DERATING FACTOR ABOVE T _C = 25°C	T _C = 125°C POWER RATING
DW	1389 mW	11.1 mW/°C	279 mW
NF	2075 mW	16.6 mW/°C	415 mW



electrical characteristics, $T_C = 25^{\circ}C$ (unless otherwise noted)

	PARAMETER	TEST COND	ITIONS	MIN	TYP	MAX	UNIT
V(BR)DSX	Drain-to-source breakdown voltage	I _D = 250 μA,	V _{GS} = 0	60			V
V _{GS(th)}	Gate-to-source threshold voltage	I _D = 1 mA, See Figure 5	V _{DS} = V _{GS} ,	1.5	1.85	2.2	V
V _(BR) GS	Gate-to-source breakdown voltage	I _{GS} = 250 μA		18			V
V _(BR) SG	Source-to-gate breakdown voltage	I _{SG} = 250 μA		9			V
V _(BR)	Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND curren	t = 250 μA	100			V
V _{DS(on)}	Drain-to-source on-state voltage	I _D = 2 A, See Notes 2 and 3	V _{GS} = 10 V,		0.6	0.7	V
V _F (SD)	Forward on-state voltage, source-to-drain	I _S = 2 A, V _{GS} = 0 (Z1, Z2, Z3, See Notes 2 and 3 and			1	1.2	V
VF	Forward on-state voltage, GND-to-drain	I _D = 2 A (D1, D2), See Notes 2 and 3			7.5		V
Inco	Zero-gate-voltage drain current	V _{DS} = 48 V,	T _C = 25°C		0.05	1	μΑ
IDSS	Zero-gate-voltage drain current	$V_{GS} = 0$	T _C = 125°C		0.5	10	μΛ
I _{GSSF}	Forward-gate current, drain short circuited to source	V _{GS} = 15 V,	V _{DS} = 0		20	200	nA
I _{GSSR}	Reverse-gate current, drain short circuited to source	V _{SG} = 5 V,	V _{DS} = 0		10	100	nA
1	Lookaga current drain to CND	V= = - 49 V	T _C = 25°C		0.05	1	
^I lkg	Leakage current, drain-to-GND	V _{DGND} = 48 V	T _C = 125°C		0.5	10	μΑ
[DC(***)	Static drain-to-source on-state resistance	V _{GS} = 10 V, I _D = 2 A,	T _C = 25°C		0.3	0.35	Ω
^r DS(on)	Static drain-to-source off-state resistance	See Notes 2 and 3 and Figures 6 and 7	T _C = 125°C		0.47	0.5	22
9fs	Forward transconductance	V _{DS} = 15 V, See Notes 2 and 3 ar	I _D = 1 A, nd Figure 9	1.6	1.9		S
C _{iss}	Short-circuit input capacitance, common source				220	275	
C _{oss}	Short-circuit output capacitance, common source	V _{DS} = 25 V,	$V_{GS} = 0$,		120	150	рF
C _{rss}	Short-circuit reverse-transfer capacitance, common source	f = 1 MHz,	See Figure 11		100	125	r'

NOTES: 2. Technique should limit T_J – T_C to 10°C maximum.

source-to-drain and GND-to-drain diode characteristics, $T_C = 25^{\circ}C$

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
	$I_S = 1 A$			Z1 and Z3		120		
t _{rr}			Z2 and Z4		280		ns	
		Is = 1 A,	V _{DS} = 48 V, di/dt = 100 A/μs,	D1 and D2		260		
	$V_{GS} = 0$, See Figures 1 and 14 Q_{RR} Total diode charge	$ai/at = 100 A/\mu s$,	Z1 and Z3		0.12			
Q_{RR}		J		Z2 and Z4		0.9		μC
				D1 and D2		2.2		



^{3.} These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

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resistive-load switching characteristics, T_C = 25°C

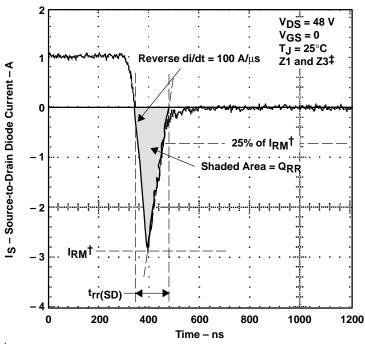
	PARAMETER	1	MIN	TYP	MAX	UNIT		
t _{d(on)}	Turn-on delay time					32	65	
td(off)	Turn-off delay time	V _{DD} = 25 V,	$V_{DD} = 25 \text{ V},$ $R_L = 25 \Omega,$ $t_{dis} = 10 \text{ ns},$ See Figure 2	$t_{en} = 10 \text{ ns},$		40	80	20
t _r	Rise time	$t_{dis} = 10 \text{ ns},$				15	30	ns
tf	Fall time					25	50	
Qg	Total gate charge					6.6	8	
Q _{gs(th)}	Threshold gate-to-source charge	V _{DS} = 48 V, See Figure 3	$I_D = 1 A$,	$V_{GS} = 10 V$,		0.8	1	nC
Q _{gd}	Gate-to-drain charge]				2.6	3.2	
L _d	Internal drain inductance					5		all
L _S	Internal source inductance					5		nΗ
Rg	Internal gate resistance					0.25		Ω

thermal resistances

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
$R_{\theta JA}$	Junction-to-ambient thermal resistance (see Note 4)				90			
					60			
$R_{\theta JB}$	Junction-to-board thermal resistance	DW	All outputs with equal power		53		°C/W	
$R_{\theta JC}$	Junction-to-case thermal resistance	DW			30			
$R_{\theta JP}$	Junction-to-pin thermal resistance	NE	25					

NOTE 4: Package mounted on an FR4 printed-circuit board with no heatsink.

PARAMETER MEASUREMENT INFORMATION

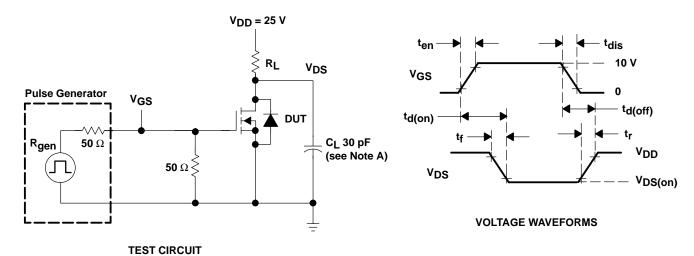


[†]I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode



[‡] The above waveform is representative of Z2, Z4, D1, and D2 in shape only.



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

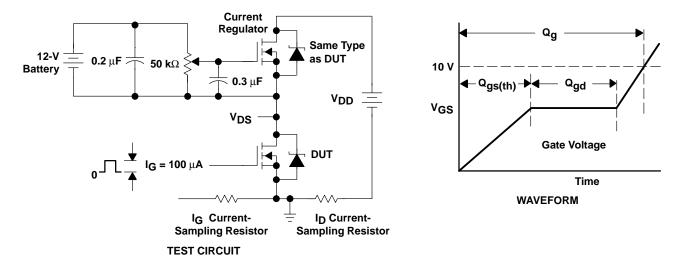
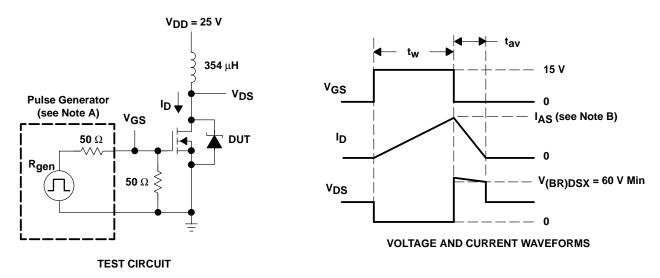


Figure 3. Gate-Charge Test Circuit and Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $z_0 = 50 \ \Omega$.

B. Input pulse duration (t_W) is increased until peak current $I_{AS} = 10 \text{ A}$.

Energy test level is defined as E_{AS} = $\frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2}$ = 21 mJ.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE VS JUNCTION TEMPERATURE $\begin{array}{c} 2.5 \\ \hline V_{DS} = V_{GS} \\ \hline \end{array}$

Figure 5

JUNCTION TEMPERATURE 0.5 ID = 2 A Voc = 10 V

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE

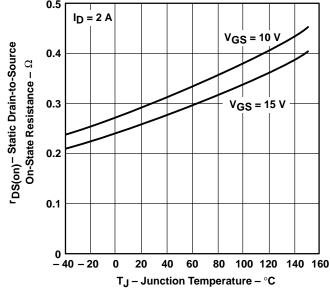


Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE

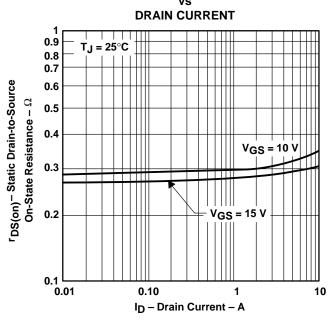


Figure 7

I_D- Drain Current - A

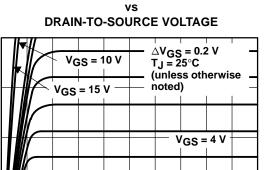
3

2

0

2

4 6



 $V_{GS} = 3 V$

18

20

DRAIN CURRENT

Figure 8

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

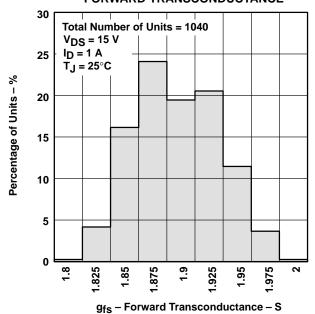


Figure 9

DRAIN CURRENT

10 12

V_{DS} - Drain-to-Source Voltage - V

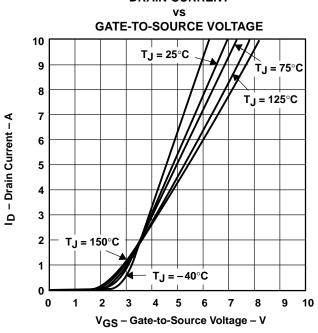
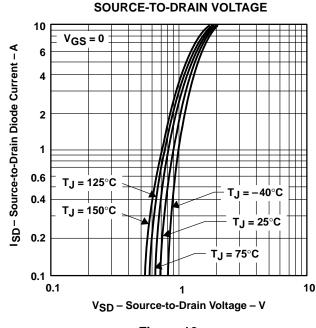


Figure 10



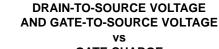
CAPACITANCE vs **DRAIN-TO-SOURCE VOLTAGE** 500 f = 1 MHz 450 $V_{GS} = 0$ T_J = 25°C 400 350 Capacitance - pF 300 Ciss 250 200 $\mathsf{C}_{\mathsf{oss}}$ 150 100 Crss 50 0 0 20 40 V_{DS} - Drain-to-Source Voltage - V

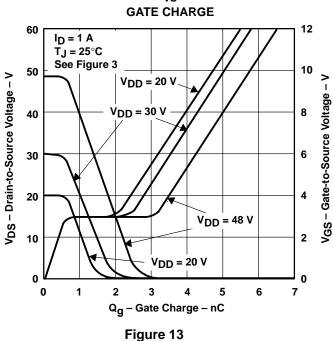
Figure 11



SOURCE-TO-DRAIN DIODE CURRENT

Figure 12





REVERSE-RECOVERY TIME

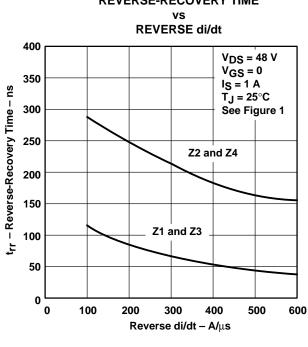


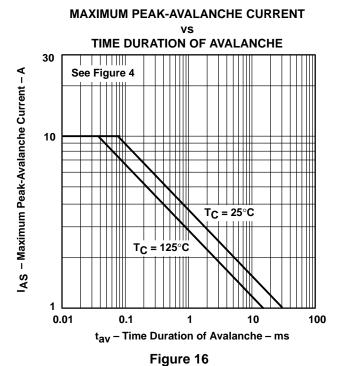
Figure 14



MAXIMUM DRAIN CURRENT DRAIN-TO-SOURCE VOLTAGE 100 $T_C = 25^{\circ}C$ ID - Maximum Drain Current - A 1 μs† 10 10 ms† 1 + 1 + 11 ms† **500** μs† DW Pkg **NE Pkg DC Conditions** 0.1 0.1 1 10 100 V_{DS} - Drain-to-Source Voltage - V

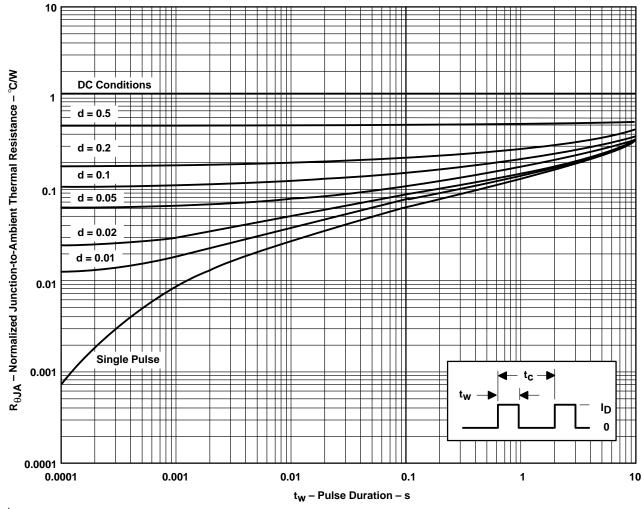
†Less than 2% duty cycle

Figure 15



NE PACKAGE† NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE

PULSE DURATION



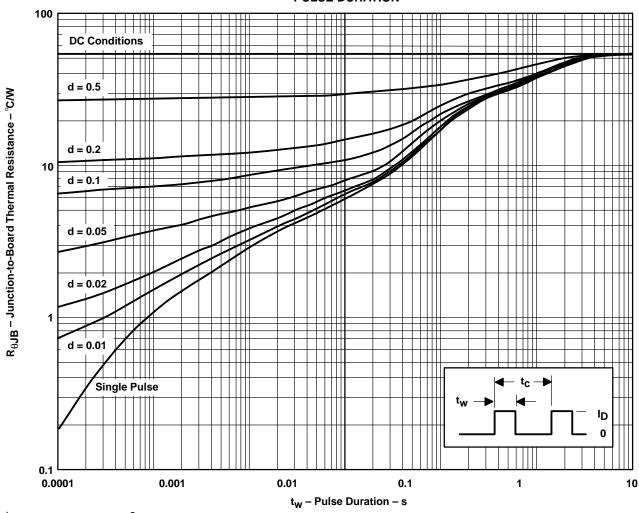
† Device mounted on FR4 printed-circuit board with no heatsink.

NOTE A: $Z_{\theta}J_{A}(t) = r(t) R_{\theta}J_{A}$ $t_{W} = \text{pulse duration}$ t_C = cycle time $d = duty cycle = t_W/t_C$

Figure 17



DW PACKAGE† JUNCTION-TO-BOARD THERMAL RESISTANCE vs **PULSE DURATION**



† Device mounted on 24 in², 4-layer FR4 printed-circuit board with no heatsink.

NOTE A: $Z_{\theta JB}(t) = r(t) R_{\theta JB}$ t_W = pulse duration t_C = cycle time $d = duty cycle = t_W/t_C$

Figure 18



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DW PACKAGE

- Low r_{DS(on)} . . . 0.4 Ω Typ
- Voltage Output . . . 60 V
- Input Protection Circuitry . . . 18 V
- Pulsed Current . . . 3 A Per Channel
- Extended ESD Capability . . . 4000 V
- Direct Logic-Level Interface

description

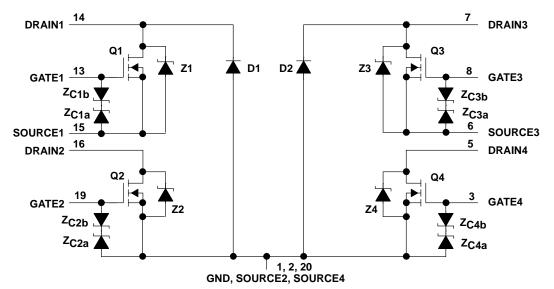
The TPIC5421L is a monolithic gate-protected logic-level power DMOS array that consists of four electrically isolated N-channel enhancement-mode DMOS transistors, two of which are configured with common source. Each transistor features integrated high-current zener diodes ($Z_{\rm CXa}$ and $Z_{\rm CXb}$) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-k Ω resistor.

The TPIC5421L is offered in a 20-pin wide-body surface-mount (DW) package and a 16-pin thermally-enhanced dual-in-line (NE) package and is characterized for operation over the case temperature of -40° C to 125° C.

(TOP VIEW) 20 SOURCE2/GND GND SOURCE4/GND [19 GATE2 18 NC GATE4 □ NC [17 NC 16 DRAIN2 DRAIN4 SOURCE3 15 SOURCE1 DRAIN3 [14 DRAIN1 13 GATE1 GATE3 ∏ 8 NC [9 12 NC NC [11 ∏ NC **NE PACKAGE** (TOP VIEW) 16 SOURCE1 DRAIN2 15 DRAIN1 SOURCE2/GND [GATE2 ∏ 3 14 GATE1 GND [13 GND GND [5 12 | GND GATE4 ∏ 6 11 | GATE3 10 DRAIN3 SOURCE4/GND [9 SOURCE3 DRAIN4

NC - No internal connection

schematic



NOTE A: For correct operation, no terminal may be taken below GND. Pin numbers shown are for the DW package.

TPIC5421L H-BRIDGE GATE-PROTECTED LOGIC-LEVEL POWER DMOS ARRAY

SLIS027A - OCTOBER 1994 - REVISED OCTOBER 1995

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V _{DS}	60 V
Source-to-GND voltage (Q1, Q3)	
Drain-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q2, Q4)	60 V
Gate-to-source voltage range, V _{GS}	–9 V to 18 V
Continuous drain current, each output, T _C = 25°C: NE package	1.5 A
	1 A
Continuous source-to-drain diode current, T _C = 25°C	1 A
Pulsed drain current, each output, I _{max} , T _C = 25°C (see Note 1 and Figure 15)	3 A
Continuous gate-to-source zener-diode current, T _C = 25°C	±50 mA
Pulsed gate-to-source zener-diode current, T _C = 25°C	±500 mA
Single-pulse avalanche energy, E _{AS} , T _C = 25°C (see Figures 4 and 16)	180 mJ
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T _J	40°C to 150°C
Operating case temperature range, T _C	40°C to 125°C
Storage temperature range, T _{stq}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

DISSIPATION RATING TABLE

PACKAGE	T _C ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _C = 25°C	T _C = 125°C POWER RATING
DW	1125 mW	9.0 mW/°C	225 mW
NE	2075 mW	16.6 mW/°C	415 mW



electrical characteristics, $T_C = 25^{\circ}C$ (unless otherwise noted)

	PARAMETER	TEST COND	MIN	TYP	MAX	UNIT	
V(BR)DSX	Drain-to-source breakdown voltage	I _D = 250 μA,	V _{GS} = 0	60			V
V _{GS(th)}	Gate-to-source threshold voltage	I _D = 1 mA, See Figure 5	$V_{DS} = V_{GS}$	1.5	1.85	2.2	٧
V _(BR) GS	Gate-to-source breakdown voltage	I _{GS} = 250 μA		18			V
V _(BR) SG	Source-to-gate breakdown voltage	I _{SG} = 250 μA		9			V
V _(BR)	Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND curren	t = 250 μA	100			V
V _{DS(on)}	Drain-to-source on-state voltage	I _D = 1 A, See Notes 2 and 3	V _{GS} = 5 V,		0.4	0.475	٧
V _{F(SD)}	Forward on-state voltage, source-to-drain	I _S = 1 A, V _{GS} = 0 (Z1, Z2, Z3, See Notes 2 and 3 ar			0.9	1.1	>
VF	Forward on-state voltage, GND-to-drain	I _D = 1 A (D1, D2), See Notes 2 and 3			4.6		٧
Inco	Zoro goto voltago drain gurrent	V _{DS} = 48 V,	T _C = 25°C		0.05	1	
IDSS	Zero-gate-voltage drain current	V _{GS} = 0	T _C = 125°C		0.5	10	μΑ
IGSSF	Forward-gate current, drain short circuited to source	V _{GS} = 15 V,	$V_{DS} = 0$		20	200	nA
IGSSR	Reverse-gate current, drain short circuited to source	$V_{SG} = 5 V$	$V_{DS} = 0$		10	100	nA
lu	Leakage current, drain-to-GND	VDGND = 48 V	T _C = 25°C		0.05	1	μΑ
llkg	Leakage current, drain-to-OND	VDGND = 40 V	T _C = 125°C		0.5	10	μΛ
IDC(on)	Static drain-to-source on-state resistance	V _{GS} = 5 V, I _D = 1 A,	T _C = 25°C		0.4	0.475	Ω
rDS(on)	State drain to source on state resistance	See Notes 2 and 3 and Figures 6 and 7	T _C = 125°C		0.65	0.68	22
9fs	Forward transconductance	V _{DS} = 15 V, See Notes 2 and 3 ar	I _D = 0.5 A, nd Figure 9	1.25	1.4		S
C _{iss}	Short-circuit input capacitance, common source				220	275	
Coss	Short-circuit output capacitance, common source	V _{DS} = 25 V,	$V_{GS} = 0$,		120	150	pF
C _{rss}	Short-circuit reverse-transfer capacitance, common source	f = 1 MHz,	See Figure 11		100	125	Pi.

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.

3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, $T_C = 25^{\circ}C$

	PARAMETER	TES	T CONDITIONS		MIN	TYP	MAX	UNIT	
	$I_{S} = 0.5 \text{ A},$ $V_{GS} = 0,$ See Figures 1 and 1			Z1 and Z3		55			
t _{rr}				Z2 and Z4		150		ns	
		Is = 0.5 A,	$I_S = 0.5 \text{ A},$ $V_{DS} = 48 \text{ V},$	$V_{DS} = 48 \text{ V},$ di/dt = 100 A/µs,	D1 and D2		200		
		See Figures 1 and 14		Z1 and Z3		0.06			
Q_{RR}		J		Z2 and Z4		0.3		μС	
				D1 and D2		0.7			



TPIC5421L H-BRIDGE GATE-PROTECTED LOGIC-LEVEL POWER DMOS ARRAY SLIS027A – OCTOBER 1994 – REVISED OCTOBER 1995

resistive-load switching characteristics, $T_C = 25^{\circ}C$

	PARAMETER	1	MIN	TYP	MAX	UNIT														
td(on)	Turn-on delay time					25	50													
td(off)	Turn-off delay time	$V_{DD} = 25 \text{ V},$	$R_L = 25 \Omega$,	$t_{r1} = 10 \text{ ns},$		20	40	no												
t _{r2}	Rise time	$t_{f1} = 10 \text{ ns},$	t _{f1} = 10 ns, See Figure 2			21	42	ns												
t _{f2}	Fall time	1				9	18													
Qg	Total gate charge			., -,,		3.9	5													
Q _{gs(th)}	Threshold gate-to-source charge	V _{DS} = 48 V, See Figure 3		VDS = 48 V, See Figure 3											$I_D = 0.5 A,$	$V_{GS} = 5 V$,		0.55	0.8	nC
Q _{gd}	Gate-to-drain charge	1				2.5	3.6													
L _D	Internal drain inductance					5		-11												
LS	Internal source inductance					5		nH												
Rg	Internal gate resistance					0.25		Ω												

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Park	RAIA Junction-to-ambient thermal resistance -	DW package	See Notes 4 and 6				
ΓθJA		NE package	See Notes 4 and 6	60			
$R_{\theta JB}$	Junction-to-board thermal resistance	DW package	See Notes 4 and 6		53		°C/W
Bo 15	Junction-to-pin thermal resistance	DW package	Con Notes Found C		30		
$R_{\theta JP}$	Junction-to-pin thermal resistance	NE package	See Notes 5 and 6		25		

NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink.

5. Package mounted in intimate contact with infinite heatsink.

6. All outputs with equal power

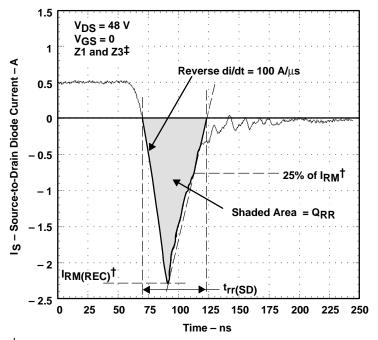
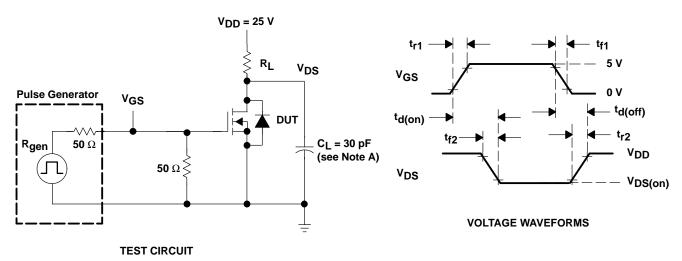


Figure 1. Reverse-Recovery-Current Waveforms of Source-to-Drain Diode



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms



 $^{^\}dagger$ IRM(REC) = maximum recovery current ‡ The above waveform is representative of Z2, Z4, D1, and D2 in shape only.

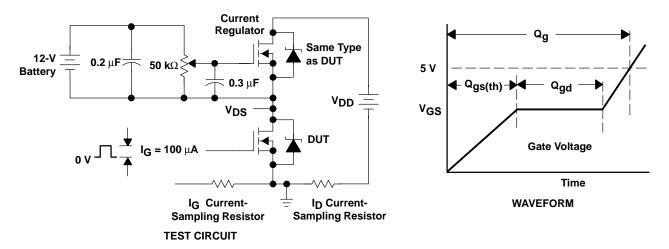
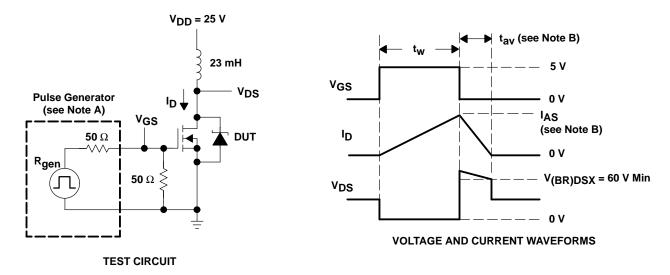


Figure 3. Gate-Charge Test Circuit and Waveform



- NOTES: A. The pulse generator has the following characteristics: $t_f \le 10$ ns, $t_f \le 10$ ns, $t_O = 50 \Omega$.
 - B. Input pulse duration (t_W) is increased until peak current $I_{AS} = 3$ A.

Energy test level is defined as E_{AS} =
$$\frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2}$$
 = 180 mJ, where t_{av} = avalanche time

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms



GATE-TO-SOURCE THRESHOLD VOLTAGE

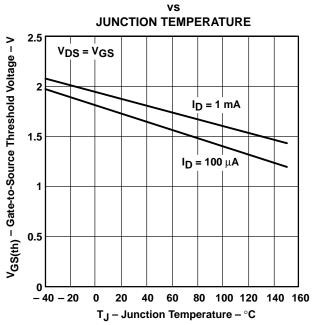


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE

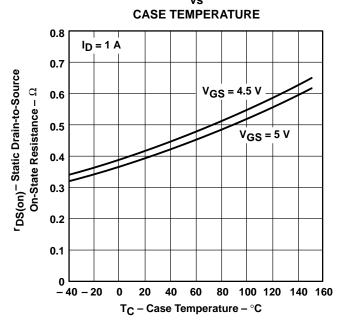


Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE

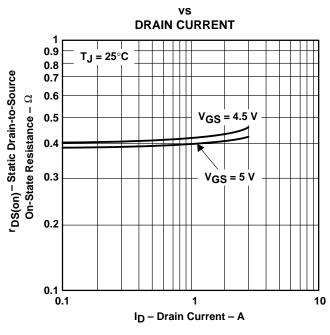


Figure 7

DRAIN CURRENT ٧S **DRAIN-TO-SOURCE VOLTAGE**

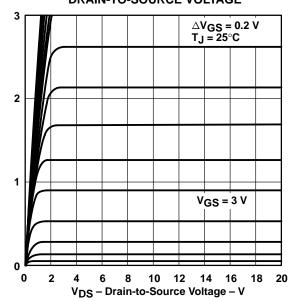


Figure 8

D- Drain Current - A

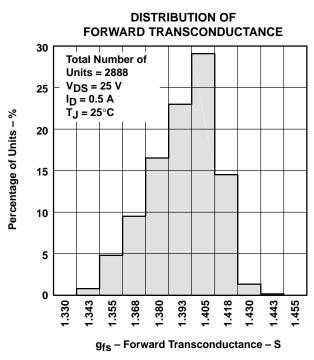
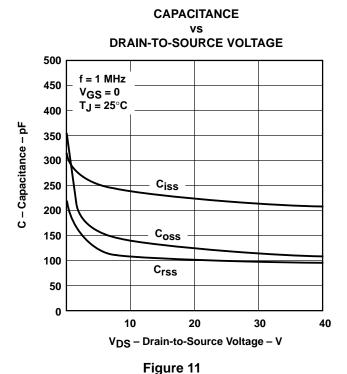


Figure 9



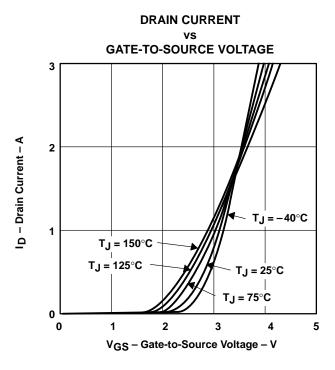
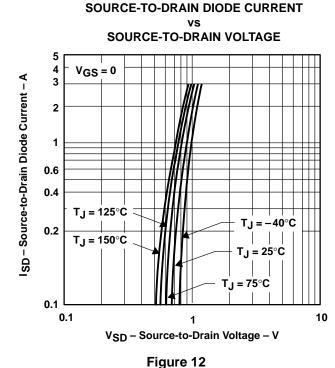


Figure 10





DRAIN-TO-SOURCE VOLTAGE AND GATE-TO-SOURCE VOLTAGE

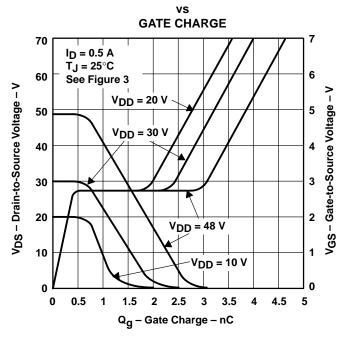


Figure 13

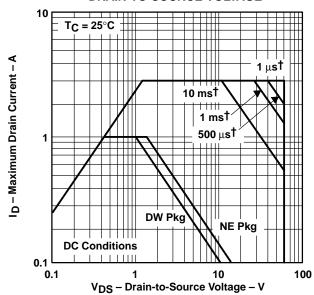
REVERSE-RECOVERY TIME

REVERSE di/dt 200 $V_{DS} = 48 V$ $V_{GS} = 0$ 175 I_S = 0.5 A T_J = 25°C t_{rr} - Reverse-Recovery Time - ns 150 See Figure 1 125 100 Z2 and Z4 75 50 Z1 and Z3 25 0 700 100 200 300 400 500 600 Reverse di/dt – A/ μ s

Figure 14



MAXIMUM DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



†Less than 2% duty cycle

Figure 15

MAXIMUM PEAK AVALANCHE CURRENT vs

TIME DURATION OF AVALANCHE

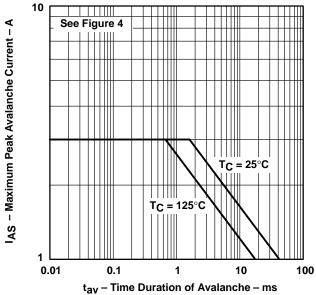
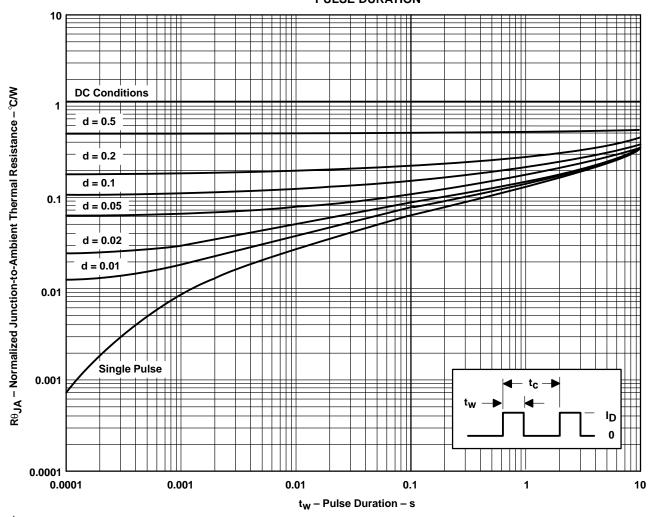


Figure 16



NE PACKAGE† NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE **PULSE DURATION**



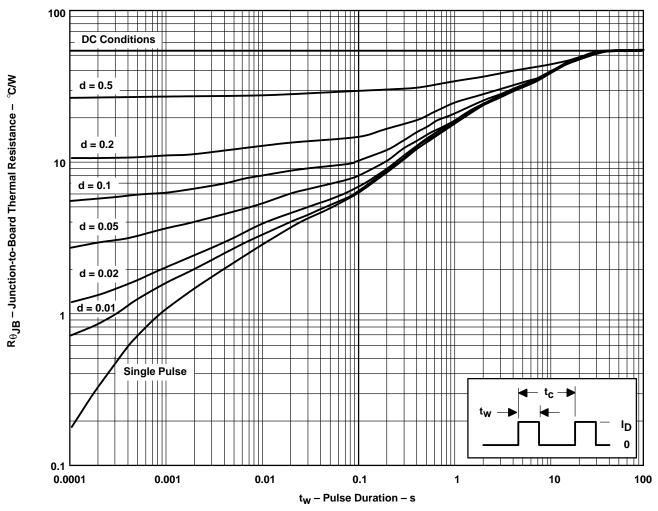
† Device mounted on FR4 printed-circuit board with no heatsink.

NOTES A: $Z_{\theta JA}(t) = r(t) R_{\theta JA}$ t_W = pulse duration t_{C} = cycle time $d = duty cycle = t_W/t_C$

Figure 17



DW PACKAGE† JUNCTION-TO-BOARD THERMAL RESISTANCE ٧S **PULSE DURATION**



[†] Device mounted on a 24 in², 4-layer FR4 printed-circuit board with no heatsink.

NOTES A: $Z_{\theta JB}(t) = r(t) R_{\theta JB}$ t_W = pulse duration t_C = cycle time d = duty cycle = t_W/t_C

Figure 18



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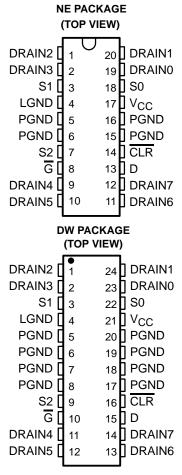
- Low r_{DS(on)} . . . 1 Ω Typ
- Output Short-Circuit Protection
- Avalanche Energy . . . 75 mJ
- Eight 350-mA DMOS Outputs
- 50-V Switching Capability
- Four Distinct Function Modes
- Low Power Consumption

description

This power logic 8-bit addressable latch controls open-drain DMOS-transistor outputs and is designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and decoders or demultiplexers. This is a multifunctional device capable of operating as eight addressable latches or an 8-line demultiplexer with active-low DMOS outputs. Each open-drain DMOS transistor features an independent chopping current-limiting circuit to prevent damage in the case of a short circuit.

Four distinct modes of operation are selectable by controlling the clear (\overline{CLR}) and enable (\overline{G}) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in (D) terminal is written into the addressed latch. The addressed DMOS-transistor output inverts the data input with all unaddressed DMOS-transistor outputs remaining in their previous states. In the memory mode, all DMOS-transistor outputs remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latch, enable G should be held high (inactive) while the address lines are changing. In the 8-line demultiplexing mode, the addressed output is inverted with respect to the D input and all other outputs are high. In the clear mode, all outputs are high and unaffected by the address and data inputs.

Separate power ground (PGND) and logic ground (LGND) terminals are provided to facilitate maximum system flexibility. All PGND terminals are internally connected, and each PGND terminal must be externally connected to the power system ground in order to minimize parasitic impedance. A single-point connection between LGND and PGND must be made externally in a manner that reduces crosstalk between the logic and load circuits.



FUNCTION TABLE

INPUTS		s	OUTPUT OF ADDRESSED	EACH OTHER	FUNCTION		
CLR	G	D	DRAIN	DRAIN	TONOTION		
Н	H L H		L	Q _{io}	Addressable		
Н	L	L	Н	Q _{io} Q _{io}	Latch		
Н	Н	Χ	Q _{io}	Q _{io}	Memory		
L	L	Н	L	Н	8-Line		
L	L	L	Н	Н	Demultiplexer		
L	Н	Χ	Н	Н	Clear		

LATCH SELECTION TABLE

SELE	CT IN	DRAIN					
S2	S1	S0	ADDRESSED				
L	L	L	0				
L	L	Н	1				
L	Н	L	2				
L	Н	Н	3				
Н	L	L	4				
Н	L	Н	5				
Н	Н	L	6				
Н	Н	Н	7				

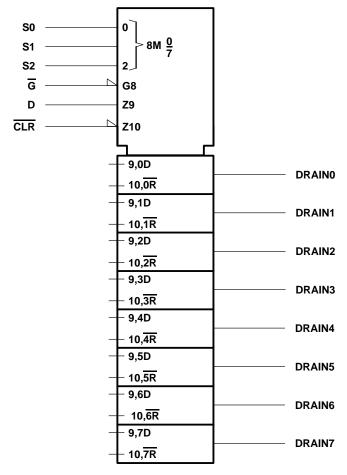
TEXAS INSTRUMENTS

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description (continued)

The TPIC6A259 is offered in a thermally-enhanced dual-in-line (NE) package and a wide-body, surface-mount (DW) package. The TPIC6A259 is characterized for operation over the operating case temperature range of -40° C to 125° C.

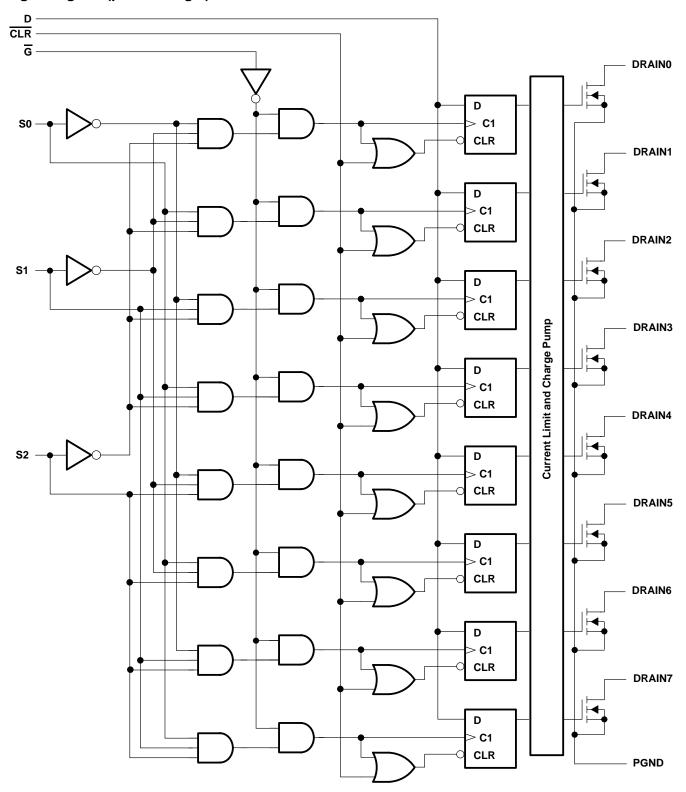
logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



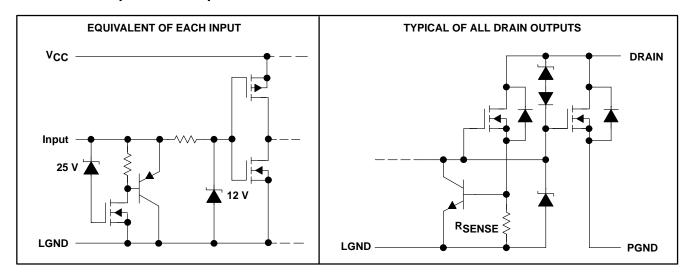
logic diagram (positive logic)





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schematic of inputs and outputs



absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V _{CC} (see Note 1)	
Power DMOS drain-to-source voltage, V _{DS} (see Note 2)	
Continuous source-to-drain diode anode current	
Pulsed source-to-drain diode anode current (see Note 3)	
Pulsed drain current, each output, all outputs on, I _D , T _C = 25°C (see Note 3)	
Continuous drain current, each output, all outputs on, I _{D.} T _C = 25°C	
Peak drain current single output, T _C = 25°C (see Note 3)	
Single-pulse avalanche energy, EAS (see Figure 6)	
Avalanche current, I _{AS} (see Note 4)	
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T _J	–40°C to 150°C
Operating case temperature range, T _C	40°C to 125°C
Storage temperature range, T _{stq}	65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to LGND and PGND.
 - 2. Each power DMOS source is internally connected to PGND.
 - 3. Pulse duration \leq 100 μ s, and duty cycle \leq 2%.
 - 4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 210 mH, and I_{AS} = 600 mA (see Figure 6).

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25^{\circ}C$ POWER RATING	DERATING FACTOR ABOVE T _C = 25°C	T _C = 125°C POWER RATING
DW	1750 mW	14 mW/°C	350 mW
NE	2500 mW	20 mW/°C	500 mW



recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V _{CC}	4.5	5.5	V
High-level input voltage, VIH	0.85 V _{CC}	VCC	V
Low-level input voltage, V _{IL}	0	0.15 V _{CC}	V
Pulsed drain output current, T _C = 25°C, V _{CC} = 5 V (see Notes 3 and 5)	-1.8	0.6	Α
Setup time, D high before G↑,t _{SU} (see Figure 2)	10		ns
Hold time, D high before G↑, th (see Figure 2)	5		ns
Pulse duration, t _W (see Figure 2)	15		ns
Operating case temperature, T _C	-40	125	°C

electrical characteristics, V_{CC} = 5 V, T_{C} = 25°C (unless otherwise noted)

PARAMETER		-	TEST CONDIT	TIONS	MIN	TYP	MAX	UNIT
V(BR)DSX	Drain-to-source breakdown voltage	I _D = 1 mA			50			V
V _{SD}	Source-to-drain diode forward voltage	IF = 350 mA,	See Note 3			0.8	1.1	V
lн	High-level input current	$V_I = V_{CC}$					1	μΑ
I _I L	Low-level input current	V _I = 0					-1	μΑ
Icc	Logic supply current	I _O = 0,	$V_I = V_{CC}$ or ()		0.5	5	mA
lok	Output current at which chopping starts	T _C = 25°C,	See Note 5 a	nd Figures 3 and 4	0.6	0.8	1.1	Α
I _(nom)	(nom) Nominal current $ \begin{array}{c} V_{DS(on)} = 0.5 \text{ V}, \ I_{(nom)} = I_D, T_C = 85^{\circ}C, \\ V_{CC} = 5 \text{ V}, \qquad \text{See Notes 5, 6, and 7} \end{array} $		T _C = 85°C, 6, and 7		350		mA	
1-	Off-state drain current	$V_{DS} = 40 \text{ V},$	T _C = 25°C			0.1	1	^
ΙD	On-state drain current	V _{DS} = 40 V,	T _C = 125°C			0.2	5	μΑ
	Static drain-to-source on-state	I _D = 350 mA,	T _C = 25°C	See Notes 5 and 6		1	1.5	0
rDS(on)	resistance	$I_D = 350 \text{ mA},$	T _C = 125°C	and Figures 9 and 10		1.7	2.5	Ω

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_{C} = 25^{\circ}\text{C}$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPHL	Propagation delay time, high- to low-level output from D			30		ns
tPLH	Propagation delay time, low- to high-level output from D $C_L = 30 \text{ pF}$, $I_D = 350 \text{ mA}$,			125		ns
t _r	Rise time, drain output	See Figures 1, 2, and 11		60		ns
t _f	Fall time, drain output			30		ns
ta	Reverse-recovery-current rise time	$I_F = 350 \text{ mA}, di/dt = 20 \text{ A/}\mu\text{s},$		100		ns
t _{rr}	Reverse-recovery time	See Notes 5 and 6 and Figure 5		300		ns

NOTES: 3. Pulse duration \leq 100 μ s and duty cycle \leq 2%.

- 5. Technique should limit $T_J T_C$ to 10°C maximum.
- 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
- Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

thermal resistance

PARAMETER			TEST CONDITIONS			UNIT
Po 10	Thermal resistance, junction-to-case		All eight outputs with agual power		10	°C/W
R ₀ JC	Thermal resistance, junction-to-case	NE	All eight outputs with equal power		10	C/VV
Po ta	Thermal registeres junction to embient	DW	All eight outputs with equal newer		50	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient		All eight outputs with equal power		50	C/VV



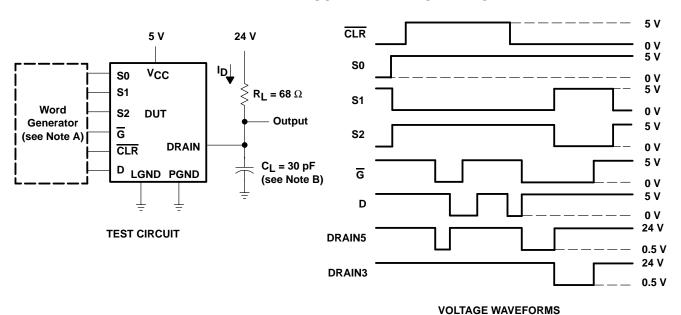


Figure 1. Typical Operation Mode

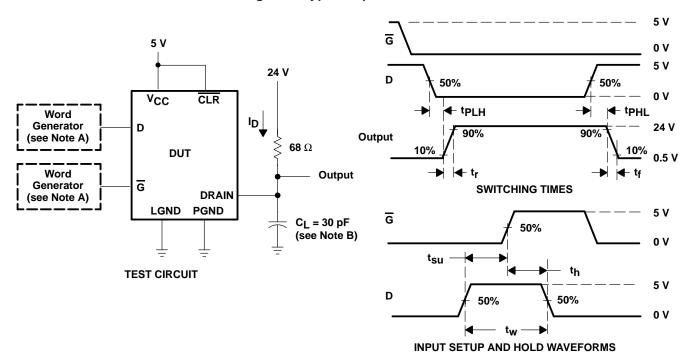


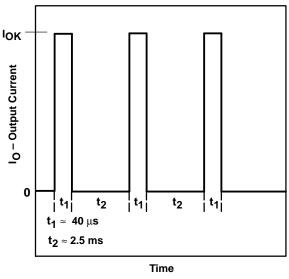
Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

- NOTES: A. The word generator has the following characteristics: $t_{\Gamma} \le 10$ ns, $t_{W} = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_{O} = 50 \ \Omega$.
 - B. CL includes probe and jig capacitance.



TIME FOR INCREASING LOAD RESISTANCE 1.5 1.25 1.25 0.75 0.25 Region 1 Region 2

REGION 1 CURRENT WAVEFORM



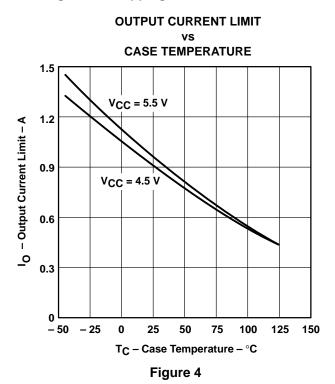
First output current pulses after turn-on in chopping mode with resistive load.

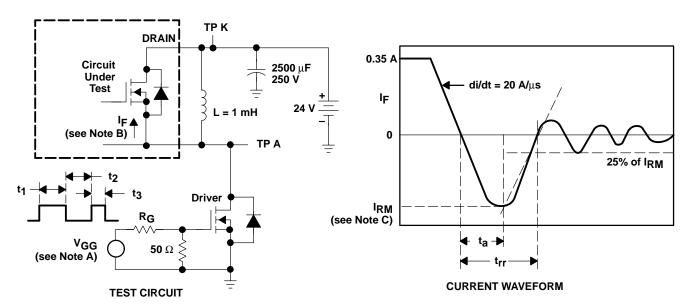
NOTES: A. Figure 3 illustrates the output current characteristics of the device energizing a load having initially low, increasing resistance, e.g., an incandescent lamp. In region 1, chopping occurs and the peak current is limited to I_{OK}. In region 2, output current is continuous. The same characteristics occur in reverse order when the device energizes a load having an initially high, decreasing resistance.

B. Region 1 duty cycle is approximately 2%.

Time

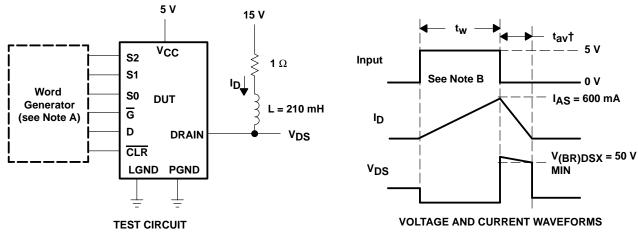
Figure 3. Chopping-Mode Characteristics





- NOTES: A. The V_{GG} amplitude and R_{G} are adjusted for di/dt = 20 A/ μ s. A V_{GG} double-pulse train is used to set I_{F} = 0.35 A, where t_{1} = 10 μ s, $t_2 = 7 \mu s$, and $t_3 = 3 \mu s$.
 - B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
 - C. IRM = maximum recovery current

Figure 5. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



† Non-JEDEC symbol for avalanche time.

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns,

B. Input pulse duration, t_W , is increased until peak current $I_{AS} = 600 \text{ mA}$. Energy test level is defined as $E_{AS} = (I_{AS} \times V_{(BR)DSX} \times t_{aV})/2 = 75 \text{ mJ}.$

Figure 6. Single-Pulse Avalanche Energy Test Circuit and Waveforms



MAXIMUM CONTINUOUS DRAIN CURRENT OF EACH OUTPUT

NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

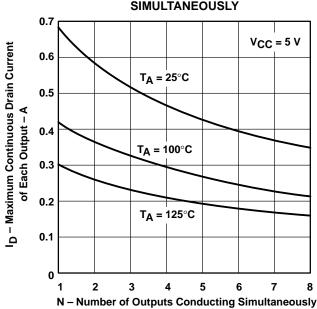


Figure 7

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT vs

NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

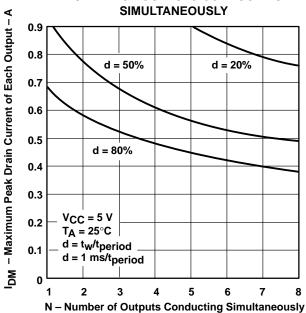
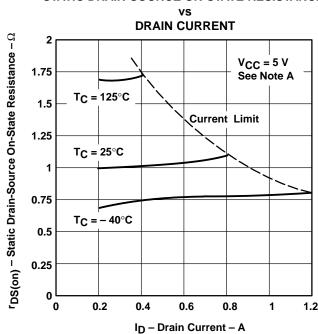


Figure 8

STATIC DRAIN-SOURCE ON-STATE RESISTANCE



NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 9

STATIC DRAIN-SOURCE ON-STATE RESISTANCE

vs LOGIC SUPPLY VOLTAGE

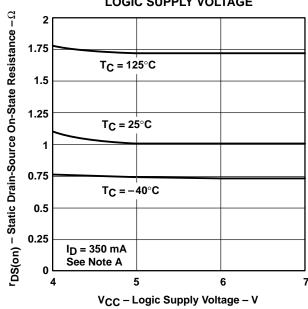


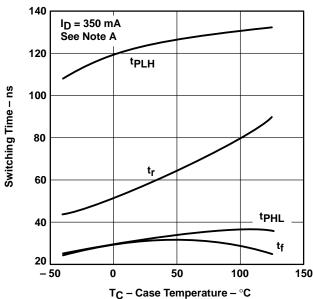
Figure 10



TYPICAL CHARACTERISTICS

SWITCHING TIME VS



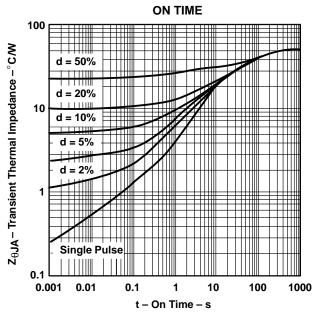


NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 11

THERMAL INFORMATION

NE PACKAGE TRANSIENT THERMAL IMPEDANCE vs



The single-pulse curve represents measured data. The curves for various pulse durations are based on the following equation:

$$\begin{split} Z_{\theta JA} &= \left| \begin{array}{c} \frac{t_w}{t_c} \right| R_{\theta JA} + \left| \begin{array}{c} 1 - \frac{t_w}{t_c} \right| Z_{\theta}(t_w + t_c) \\ \\ &+ Z_{\theta}(t_w) - Z_{\theta}(t_c) \end{split}$$

Where:

$$Z_{\theta}(t_{W})$$
 = the single-pulse thermal impedance for t = t_{W} seconds

$$\mathbf{Z}_{\theta}(t_{c}) \ = \ \text{the single-pulse thermal impedance} \\ \text{for } \mathbf{t} = \ t_{c} \ \text{seconds}$$

$$Z_{\theta}(t_W + t_C) = \text{the single-pulse thermal impedance}$$
 for $t = t_W + t_C \text{ seconds}$

$$d = t_W/t_C$$

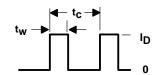


Figure 12



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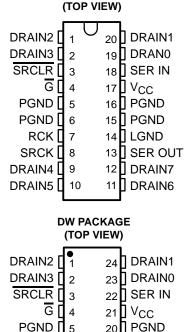
NE PACKAGE

- Low r_{DS(on)} . . . 1 Ω Typ
- Output Short-Circuit Protection
- Avalanche Energy . . . 75 mJ
- Eight 350-mA DMOS Outputs
- 50-V Switching Capability
- Devices Are Cascadable
- Low Power Consumption

description

The TPIC6A595 is a monolithic, high-voltage, high-current power logic 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads. Each open-drain DMOS transistor features an independent chopping current-limiting circuit to prevent damage in the case of a short circuit.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit, D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear (SRCLR) is high. When SRCLR is low, the input shift register is cleared. When output



19 PGND

18 PGND

17 PGND

16∏ LGND

15 SER OUT

14 DRAIN7

13 DRAIN6

PGND [

PGND **∏** 7

PGND ¶8

RCK [] 9

SRCK **1** 10

DRAIN4 1 11

DRAIN5

enable (\overline{G}) is held high, all data in the output buffers is held low and all drain outputs are off. When \overline{G} is held low, data from the storage register is transparent to the output buffers. The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices.

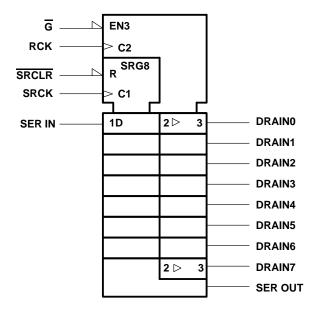
Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and a 350-mA continuous sink current capability. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink current capability.

Separate power ground (PGND) and logic ground (LGND) terminals are provided to facilitate maximum system flexibility. All PGND terminals are internally connected, and each PGND terminal must be externally connected to the power system ground in order to minimize parasitic impedance. A single-point connection between LGND and PGND must be made externally in a manner that reduces crosstalk between the logic and load circuits.

The TPIC6A595 is offered in a thermally-enhanced dual-in-line (NE) package and a wide-body surface-mount (DW) package. The TPIC6A595 is characterized for operation over the operating case temperature range of -40° C to 125°C.

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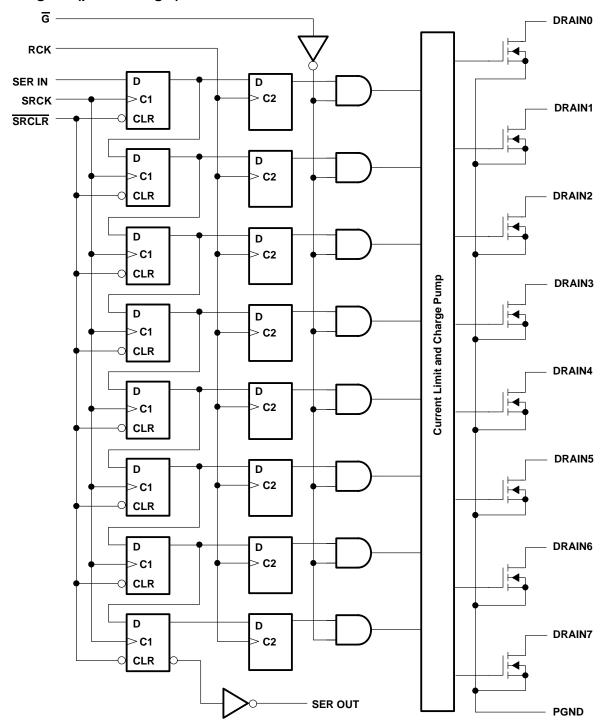
logic symbol†



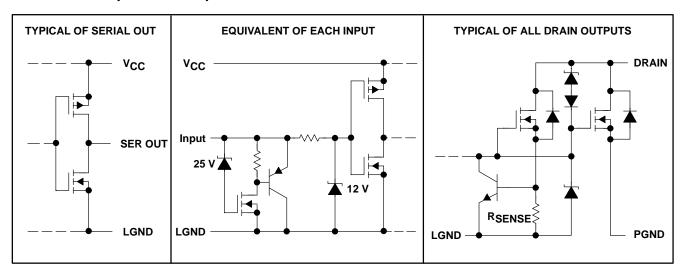
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted) $\!\!\!\!\!^{\dagger}$

Logic supply voltage, V _{CC} (see Note 1)	7 V
Logic input voltage range, V _I	0.3 V to 7 V
Power DMOS drain-to-source voltage, V _{DS} (see Note 2)	50 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current (see Note 3)	2 A
Pulsed drain current, each output, all outputs on, I_{Dn} , $T_A = 25^{\circ}C$ (see Note 3)	1.1 A
Continuous drain current, each output, all outputs on, I _{Dn} , T _A = 25°C	
Peak drain current, single output, T _A = 25°C (see Note 3)	1.1 A
Single-pulse avalanche energy, EAS (see Figure 6)	75 mJ
Avalanche current, I _{AS} (see Note 4)	600 mA
Continuous total dissipation	ee Dissipation Rating Table
Operating case temperature range, T _C	–40°C to 125°C
Operating virtual junction temperature range, T _{.j.}	–40°C to 150°C
Storage temperature range, T _{stq}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to LGND and PGND.
 - 2. Each power DMOS source is internally connected to PGND.
 - 3. Pulse duration \leq 100 μ s and duty cycle \leq 2 %.
 - 4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 210 mH, I_{AS} = 600 mA (see Figure 6).

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25^{\circ}C$ POWER RATING	DERATING FACTOR ABOVE T _C = 25°C	T _C = 125°C POWER RATING
DW	1750 mW	14 mW/°C	350 mW
NE	2500 mW	20 mW/°C	500 mW



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recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V _{CC}	4.5	5.5	V
High-level input voltage, V _{IH}	0.85 V _{CC}	VCC	V
Low-level input voltage, V _{IL}	0	0.15 V _{CC}	V
Pulsed drain output current, T _C = 25°C, V _{CC} = 5 V (see Notes 3 and 5)	-1.8	0.6	Α
Setup time, SER IN high before SRCK↑, t _{SU} (see Figure 2)	10		ns
Hold time, SER IN high after SRCK↑, th (see Figure 2)	10		ns
Pulse duration, t _W (see Figure 2)	20		ns
Operating case temperature, T _C	-40	125	°C

electrical characteristics, V_{CC} = 5 V, T_{C} = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{(BR)DSX}	Drain-to-source breakdown voltage	I _D = 1 mA	50			V
V _{SD}	Source-to-drain diode forward voltage	I _F = 350 mA, See Note 3		0.8	1.1	V
Vou	High-level output voltage,	$I_{OH} = -20 \mu\text{A}$	V _{CC} -0.1	Vcc		V
VOH	SER OUT	$I_{OH} = -4 \text{ mA}$	V _{CC} -0.5	V _{CC} -0.2		V
V0:	Low-level output voltage,	$I_{OL} = 20 \mu\text{A}$		0	0.1	V
VOL	SER OUT	I _{OL} = 4 mA		0.2	0.5	V
lн	High-level input current	VI = VCC			1	μΑ
I _{IL}	Low-level input current	V _I = 0			-1	μΑ
I _{O(chop)}	Output current at which chopping starts	T _C = 25°C, See Note 5 and Figures 3 and 4	0.6	0.8	1.1	Α
ICC	Logic supply current	$I_O = 0$, $V_I = V_{CC}$ or 0		0.5	5	mA
ICC(FRQ)	Logic supply current at frequency	$ \begin{array}{llllllllllllllllllllllllllllllllllll$		1.3		mA
I _(nom)	Nominal current	$V_{DS(on)} = 0.5 \text{ V},$ $I_{(nom)} = I_D, T_C = 85^{\circ}C,$ $V_{CC} = 5 \text{ V},$ See Notes 5, 6, and 7		350		mA
	Drain ourrent off state	$V_{DS} = 40 \text{ V}, T_{C} = 25^{\circ}\text{C}$		0.1	1	^
ID	Drain current, off-state	$V_{DS} = 40 \text{ V}, T_{C} = 125^{\circ}\text{C}$		0.2	5	μΑ
	Otatia duain assumas an atata	$I_D = 350 \text{ mA}, T_C = 25^{\circ}\text{C}$		1	1.5	
rDS(on)	Static drain-source on-state resistance	$I_D = 350 \text{ mA}$, $I_C = 125^{\circ}C$ See Notes 5 and 6 and Figures 10 and 11		1.7	2.5	Ω
·		$I_D = 350 \text{ mA}, T_C = 40^{\circ}\text{C}$				

NOTES: 3. Pulse duration $\leq 100~\mu s$ and duty cycle $\leq 2\%$

- 5. Technique should limit $T_J T_C$ to $10^{\circ}C$ maximum.
- 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
- 7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.



TPIC6A595 **POWER LOGIC 8-BIT SHIFT REGISTER**

SLIS005A – APRIL 1993 – REVISED JANUARY 1995

switching characteristics, V_{CC} = 5 V, T_{C} = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
^t PHL	Propagation delay time, high-to-low-level output from \overline{G}			30		ns
^t PLH	Propagation delay time, low-to-high-level output from \overline{G}	$C_L = 30 \text{ pF}, \qquad I_D = 350 \text{ mA},$		125		ns
t _r	Rise time, drain output	See Figures 1, 2, and 12		60		ns
t _f	Fall time, drain output			30		ns
ta	Reverse-recovery-current rise time	$I_F = 350 \text{ mA}, \text{di/dt} = 20 \text{ A/}\mu\text{s},$		100		ns
t _{rr}	Reverse-recovery time	See Notes 5 and 6 and Figure 5		300		ns

thermal resistance

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT		
D . Thermal resistance investigates to		DW	All eight outputs with equal power		10	°C/W	
$R_{\theta JC}$ Thermal resistance, junction-to-case	Thermal resistance, junction-to-case	NE	All eight outputs with equal power		10	C/VV	
D	R _{θJA} Thermal resistance, junction-to-ambient		All eight outputs with equal power		50	°C/W	
NθJA			All eight outputs with equal power		50	C/VV	



NOTES: 5. Technique should limit T_J – T_C to 10°C maximum.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

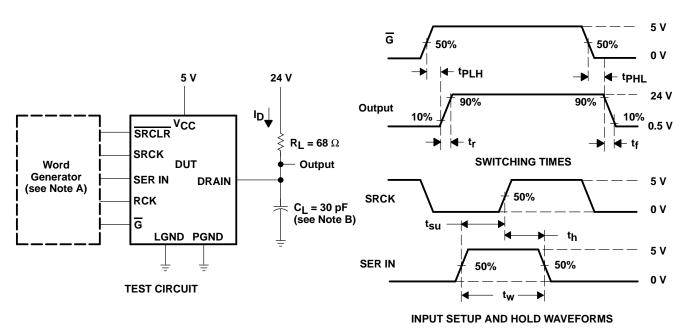
VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION 5 V 24 V **SRCK** 0 V ۷сс 5 V SRCLR G $R_L = 68 \Omega$ 0 V SRCK 5 V Output **SER IN** Word 0 V **DRAIN** Generator **SER IN** 5 V (see Note A) **RCK** $C_L = 30 pF$ **RCK** (see Note B) G SRCLR 0 V LGND PGND 24 V **DRAIN 0, 1, 4, 5** 0.5 V 24 V **TEST CIRCUIT DRAIN 2, 3, 6, 7**

NOTES: A. The word generator has the following characteristics: $t_{\Gamma} \le 10$ ns, $t_{W} = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_{O} = 50 \ \Omega$.

B. CL includes probe and jig capacitance.

Figure 1. Resistive Load Operation



NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_Q = 50 \ \Omega$.

B. C_I includes probe and jig capacitance.

Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

TIME FOR INCREASING LOAD RESISTANCE 1.5 1.25 O Region 1 Region 2

REGION 1 CURRENT WAVEFORM TOK t_1 t_1 t_1 t_2 t_1

First output current pulses after turn-on in chopping mode with resistive load.

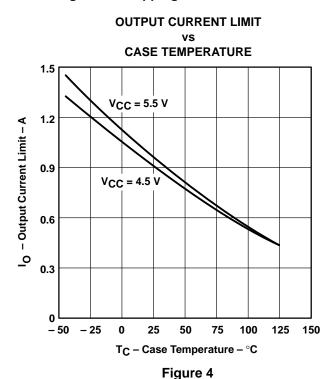
Time

NOTES: A. Figure 3 illustrates the output current characteristics of the device energizing a load having initially low, increasing resistance, e.g., an incandescent lamp. In region 1, chopping occurs and the peak current is limited to I_{OK}. In region 2, output current is continuous. The same characteristics occur in reverse order when the device energizes a load having an initially high, decreasing resistance.

B. Region 1 duty cycle is approximately 2%.

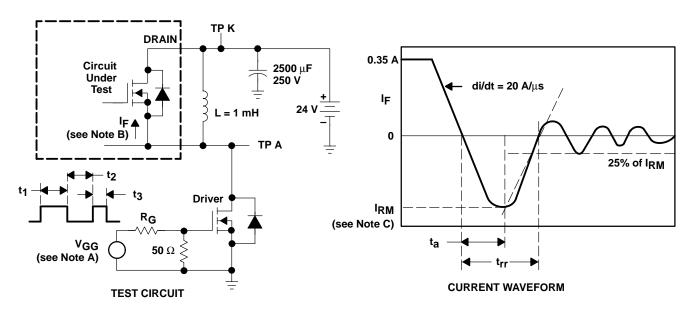
Time

Figure 3. Chopping-Mode Characteristics



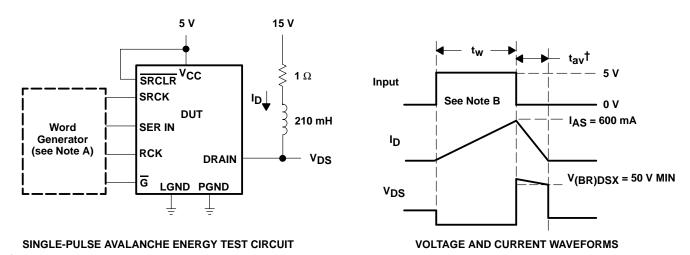


PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/ μ s. A V_{GG} double-pulse train is used to set I_F = 0.35 A, where t₁ = 10 μ s, t₂ = 7 μ s, and t₃ = 3 μ s.
 - B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
 - C. I_{RM} = maximum recovery current

Figure 5. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



[†] Non JEDEC symbol for avalanche time.

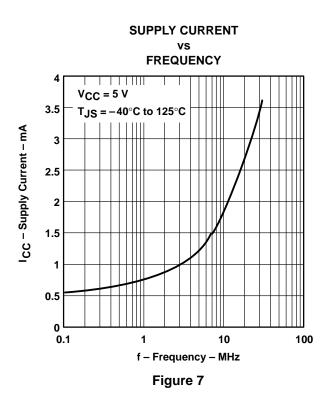
NOTES: A. The word generator has the following characteristics: $t_f \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50 \ \Omega$.

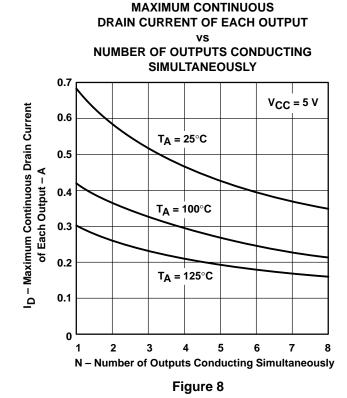
B. Input pulse duration, t_W , is increased until peak current $I_{AS} = 600$ mA. Energy test level is defined as $E_{AS} = (I_{AS} \times V_{(BR)DSX} \times t_{aV})/2 = 75$ mJ.

Figure 6. Single-Pulse Avalanche Energy Test Circuit and Waveforms



TYPICAL CHARACTERISTICS





MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT

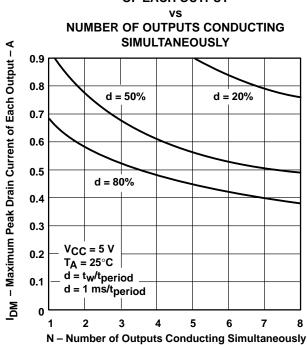
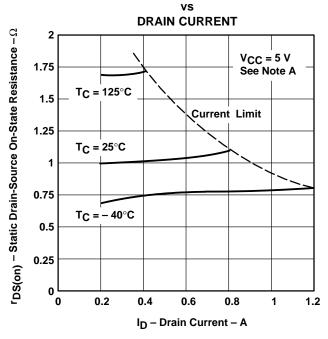


Figure 9

STATIC DRAIN-SOURCE ON-STATE RESISTANCE



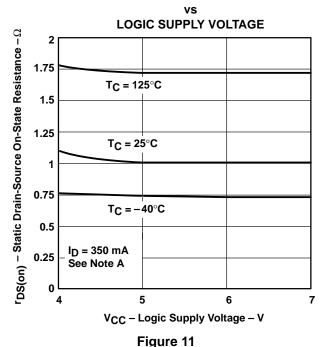
NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 10



TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE



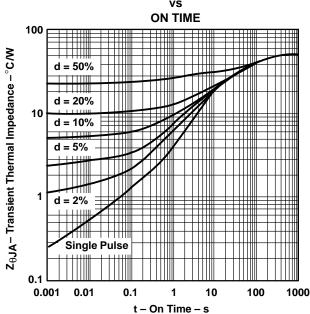
SWITCHING TIME CASE TEMPERATURE 140 I_D = 350 mA See Note A 120 ^tPLH Switching Time - ns 100 80 60 ^tPHL 40 tf 20 150 - 50 50 100 T_C - Case Temperature - °C

Figure 12

NOTE A: Technique should limit T_J – T_C to 10°C maximum.

THERMAL INFORMATION

NE PACKAGE TRANSIENT THERMAL IMPEDANCE VS



The single-pulse curve represents measured data. The curves for various pulse durations are based on the following equation:

$$Z_{\theta \mathsf{J}\mathsf{A}} \; = \; \left| \; \frac{t_{\mathsf{w}}}{t_{\mathsf{c}}} \; \right| \; \mathsf{R}_{\theta \mathsf{J}\mathsf{A}} \; + \; \left| \; 1 \; - \frac{t_{\mathsf{w}}}{t_{\mathsf{c}}} \; \right| \; Z_{\theta}(t_{\mathsf{w}} + t_{\mathsf{c}})$$

 $+ Z_{\theta}(t_{w}) - Z_{\theta}(t_{c})$

Where:

 $\mathbf{Z}_{\theta}(\mathbf{t_W}) \ = \ \text{the single-pulse thermal impedance} \\ \text{for } \mathbf{t} = \ \mathbf{t_W} \ \text{seconds}$

 $Z_{\theta}(t_{c}) \ = \ \text{the single-pulse thermal impedance} \\ \text{for } t = \ t_{c} \ \text{seconds}$

 $Z_{\theta}(t_W + t_C)$ = the single-pulse thermal impedance for t = $t_W + t_C$ seconds

$$d = t_W/t_C$$

$$t_W \longrightarrow \begin{bmatrix} t_C & & & \\ & & & \\ & & & \end{bmatrix}$$

Figure 13



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- Low r_{DS(on)} . . . 5 Ω Typical
- Avalanche Energy . . . 30 mJ
- **Eight Power DMOS-Transistor Outputs of 150-mA Continuous Current**
- 500-mA Typical Current-Limiting Capability
- Output Clamp Voltage . . . 50 V
- Four Distinct Function Modes
- Low Power Consumption

description

This power logic 8-bit addressable latch controls open-drain DMOS-transistor outputs and is general-purpose designed storage applications in digital systems. Specific uses include working registers, serial-holding registers, and decoders or demultiplexers. This is a multifunctional device capable of storing single-line data in eight addressable latches and 3-to-8 decoder or demultiplexer with active-low DMOS outputs.

Four distinct modes of operation are selectable by controlling the clear (\overline{CLR}) and enable (\overline{G}) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in (D) terminal is written into the addressed latch. The addressed DMOS-transistor output inverts the data input with all unaddressed DMOS-transistor outputs remaining in their previous states. In the memory mode, all DMOS-transistor outputs remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latch, enable G should be held high (inactive) while the address lines are changing. In the 3-to-8 decoding or demultiplexing mode, the addressed output is inverted with respect to the D input and all other

(TOP VIEW) 20 [] NC NC [19 CLR V_{CC} [] 2 18 D S0 [] 3 DRAIN0 **1** 4 17 DRAIN7 DRAIN1 1 5 16 DRAIN6 DRAIN2 [] 6 15 DRAIN5 14 DRAIN4 DRAIN3 **∏** 7 S1 [] 8 13 ∏ G

DW OR N PACKAGE

10 NC - No internal connection

GND [] 9

GND [

FUNCTION TABLE

12 S2

11 GND

INPUTS		S	OUTPUT OF	EACH	FUNCTION
CLR	G	D	ADDRESSED DRAIN	OTHER DRAIN	FUNCTION
H	L L	H L	L H	Q _{io} Q _{io}	Addressable Latch
Н	Н	Χ	Q_{i0}	Q _{io}	Memory
L L	L L	H L	L H	H H	8-Line Demultiplexer
L	Н	Х	Н	Н	Clear

LATCH SELECTION TABLE

SELE	CT IN	DRAIN	
S2	S1	S0	ADDRESSED
L	L	L	0
L	L	Н	1
L	Н	L	2
L	Н	Н	3
Н	L	L	4
Н	L	Н	5
Н	Н	L	6
Н	Н	Н	7

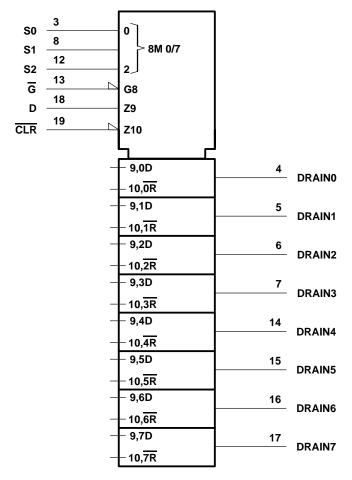
H = high level, L = low level

outputs are off. In the clear mode, all outputs are off and unaffected by the address and data inputs. When data is low for a given output, the DMOS-transistor output is off. When data is high, the DMOS-transistor output has sink-current capability.

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink-current capability. Each output provides a 500-mA typical current limit at T_C = 25°C. The current limit decreases as the junction temperature increases for additional device protection.

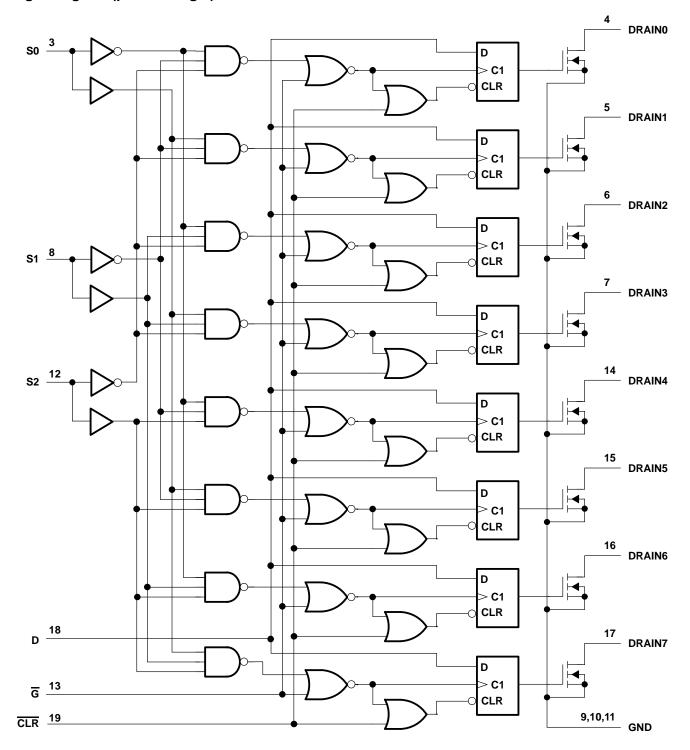
The TPIC6B259 is characterized for operation over the operating case temperature range of -40° C to 125°C.

logic symbol†



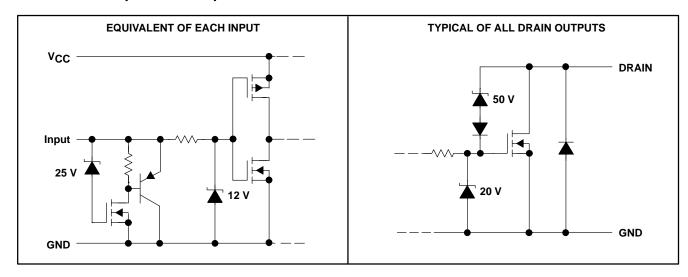
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





schematic of inputs and outputs



absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V _{CC} (see Note 1)	
Power DMOS drain-to-source voltage, V _{DS} (see Note 2)	
Continuous source-to-drain diode anode current	
Pulsed source-to-drain diode anode current (see Note 3)	
Pulsed drain current, each output, all outputs on, I _D , T _C = 25°C (see Note 3)	500 mA
Continuous drain current, each output, all outputs on, I_D , $T_C = 25^{\circ}C$	150 mA
Peak drain current single output, I _{DM} , T _C = 25°C (see Note 3)	500 mA
Single-pulse avalanche energy, E _{AS} (see Figure 4)	30 mJ
Avalanche current, I _{AS} (see Note 4)	500 mA
Continuous total dissipation	See Dissipating Rating Table
Operating virtual junction temperature range, T _J	40°C to 150°C
Operating case temperature range, T _C	–40°C to 125°C
Storage temperature range	65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to GND.
 - 2. Each power DMOS source is internally connected to GND.
 - 3. Pulse duration \leq 100 μ s and duty cycle \leq 2%.
 - 4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 200 mH, I_{AS} = 0.5 A (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25^{\circ}C$ POWER RATING	DERATING FACTOR ABOVE T _C = 25°C	T _C = 125°C POWER RATING
DW	1389 mW	11.1 mW/°C	278 mW
N	1050 mW	10.5 mW/°C	263 mW



recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V _{CC}	4.5	5.5	V
High-level input voltage, VIH	0.85 V _C C		V
Low-level input voltage, V _{IL}		0.15 V _{CC}	V
Pulsed drain output current, T _C = 25°C, V _{CC} = 5 V (see Notes 3 and 5)	-500	500	mA
Setup time, D high before $\overline{G} \uparrow$, t_{SU} (see Figure 2)	20		ns
Hold time, D high after $\overline{G}\uparrow$, th (see Figure 2)	20		ns
Pulse duration, t _W (see Figure 2)	40		ns
Operating case temperature, T _C	-40	125	°C

electrical characteristics, $V_{CC} = 5 \text{ V}$, $T_{C} = 25^{\circ}\text{C}$ (unless otherwise noted)

	PARAMETER		TEST CONDITIONS			TYP	MAX	UNIT
V _{(BR)DSX}	Drain-to-source breakdown voltage	I _D = 1 mA			50			V
V _{SD}	Source-to-drain diode forward voltage	IF = 100 mA				0.85	1	V
ΙΗ	High-level input current	$V_{CC} = 5.5 \text{ V},$	$V_I = V_{CC}$				1	μΑ
I _{IL}	Low-level input current	$V_{CC} = 5.5 \text{ V},$	V _I = 0				-1	μΑ
laa	Logic cumply current	V _{CC} = 5.5 V	All outputs off			20	100	^
lcc	Logic supply current	ACC = 2.2 A	All outputs on			150	300	μΑ
IN	Nominal current	V _{DS(on)} = 0.5 V, See Notes 5, 6, a		$T_C = 85^{\circ}C$,		90		mA
1	Off state design surrent	$V_{DS} = 40 \text{ V},$	V _{CC} = 5.5 V			0.1	5	^
DSX	Off-state drain current	V _{DS} = 40 V,	V _{CC} = 5.5 V,	T _C = 125°C		0.15	8	μΑ
		I _D = 100 mA,	V _{CC} = 4.5 V			4.2	5.7	
rDS(on)	Static drain-to-source on-state resistance	$I_D = 100 \text{ mA},$ $T_C = 125^{\circ}\text{C}$	V _{CC} = 4.5 V,	See Notes 5 and 6 and Figures 6 and 7		6.8	9.5	Ω
		$I_D = 350 \text{ mA},$	V _{CC} = 4.5 V			5.5	8	

switching characteristics, V_{CC} = 5 V, T_{C} = 25°C

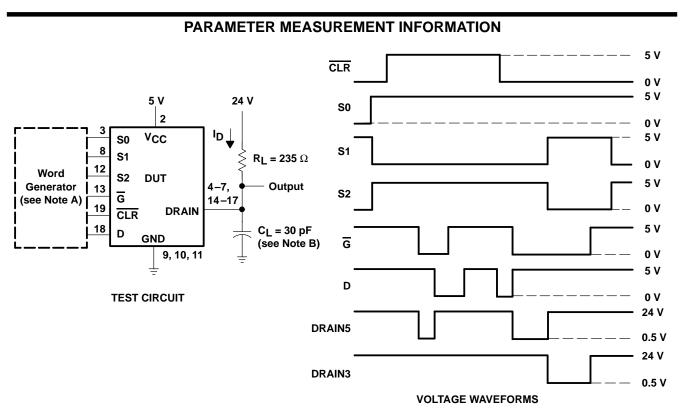
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	Propagation delay time, low-to-high-level output from D			150		ns
tPHL	Propagation delay time, high-to-low-level output from D	$C_L = 30 \text{ pF}, \qquad I_D = 100 \text{ mA},$		90		ns
t _r	Rise time, drain output	See Figures 1, 2, and 8		200		ns
t _f	Fall time, drain output			200		ns
ta	Reverse-recovery-current rise time	I _F = 100 mA, di/dt = 20 A/μs,		100		200
t _{rr}	Reverse-recovery time	See Notes 5 and 6 and Figure 3		300		ns

- NOTES: 3. Pulse duration \leq 100 μ s and duty cycle \leq 2%.
 - 5. Technique should limit $T_J T_C$ to 10°C maximum.
 - 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
 - Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.



thermal resistance

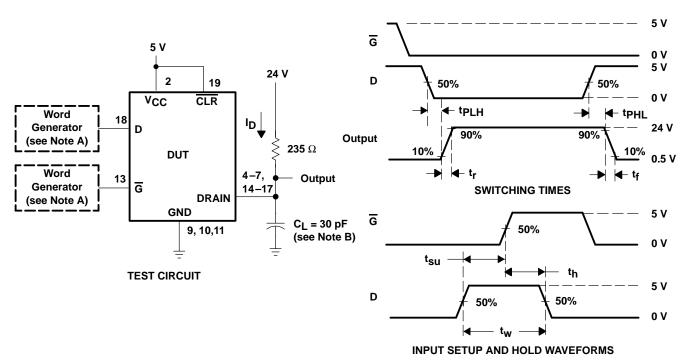
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT	
$R_{\theta JA}$	Thermal resistance junction-to-ambient	DW package	All 8 outputs with equal power	90		°C/W
	mermai resistance junction-to-ambient	N package			95	C/VV



- NOTES: A. The word generator has the following characteristics: $t_f \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50 \ \Omega$.
 - B. C_L includes probe and jig capacitance.

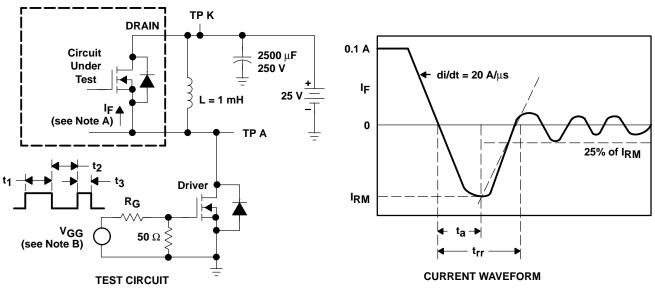
Figure 1. Resistive-Load Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The word generator has the following characteristics: $t_{\Gamma} \le 10$ ns, $t_{W} = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_{O} = 50 \ \Omega$.
 - B. CL includes probe and jig capacitance.

Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

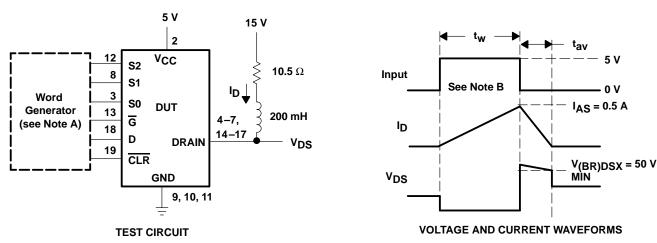


- NOTES: A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
 - B. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/ μ s. A V_{GG} double-pulse train is used to set I_F = 0.1 A, where t₁ = 10 μ s, t₂ = 7 μ s, and t₃ = 3 μ s.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode



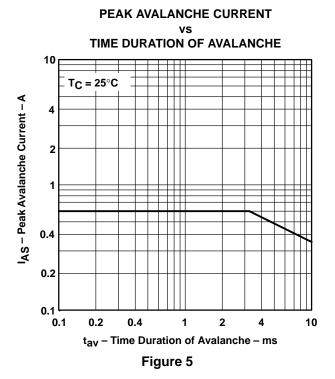
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The word generator has the following characteristics: $t_f \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50 \ \Omega$.
 - B. Input pulse duration, t_W , is increased until peak current $I_{AS} = 0.5$ A. Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 30$ mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS



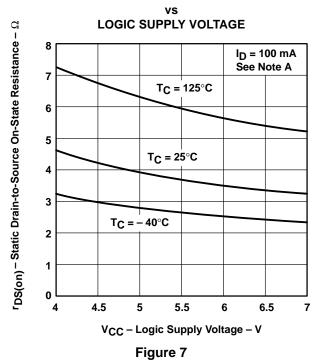
DRAIN-TO-SOURCE ON-STATE RESISTANCE vs **DRAIN CURRENT** $^{ m LDS(on)}$ – Drain-to-Source On-State Resistance – $^{ m CO}$ $V_{CC} = 5 V$ See Note A 16 14 T_C = 125°C 12 10 8 6 T_C = 25°C $T_C = -40^{\circ}C$ 2 0 0 100 200 300 400 500 600 700 ID - Drain Current - mA

NOTE C. Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE



NOTE D. Technique should limit $T_J - T_C$ to 10°C maximum.

SWITCHING TIME vs CASE TEMPERATURE

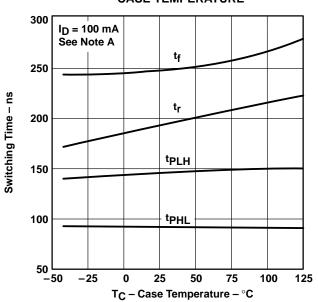
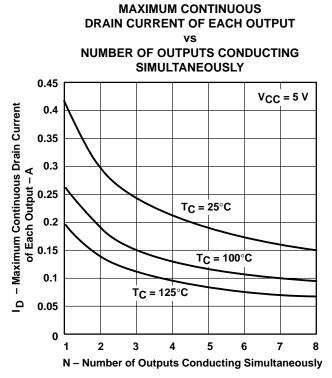


Figure 8

THERMAL INFORMATION



MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT NUMBER OF OUTPUTS CONDUCTING **SIMULTANEOUSLY** - Maximum Peak Drain Current of Each Output - A 0.5 d = 10% 0.45 d = 20%0.4 0.35 d = 50%0.3 0.25 d = 80%0.2 0.15 $V_{CC} = 5 V$ $T_C = 25$ °C 0.1 $d = t_W/t_{period}$ 0.05 = 1 ms/tperiod 0 ٥ 4 5 8 N - Number of Outputs Conducting Simultaneously

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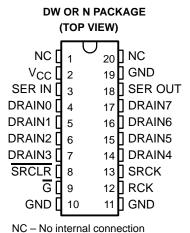
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- Low r_{DS(on)} . . . 5 Ω Typical
- Avalanche Energy . . . 30 mJ
- Eight Power DMOS-Transistor Outputs of 150-mA Continuous Current
- 500-mA Typical Current-Limiting Capability
- Output Clamp Voltage . . . 50 V
- Devices Are Cascadable
- Low Power Consumption

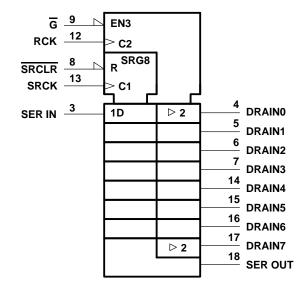
description

The TPIC6B595 is a monolithic, high-voltage, medium-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shiftregister clear (SRCLR) is high. When SRCLR is low, the input shift register is cleared. When output enable (\overline{G}) is held high, all data in the output buffers is held low and all drain outputs are off. When \overline{G} is held low, data from the storage register is transparent to the output buffers. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOStransistor outputs have sink-current capability. The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices.



logic symbol†

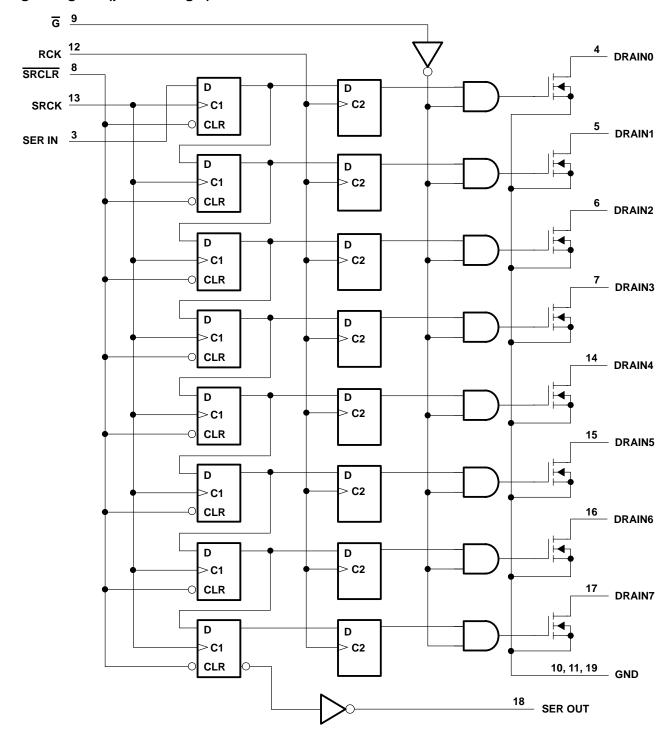


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink-current capability. Each output provides a 500-mA typical current limit at $T_C = 25^{\circ}C$. The current limit decreases as the junction temperature increases for additional device protection.

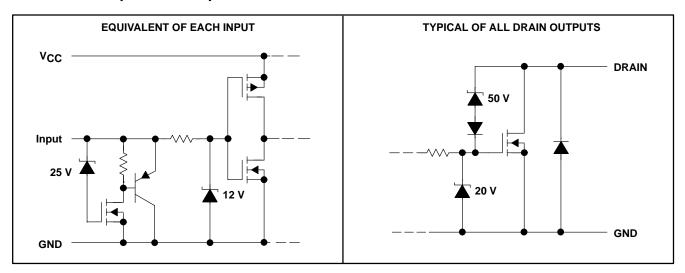
The TPIC6B595 is characterized for operation over the operating case temperature range of -40°C to 125°C.

logic diagram (positive logic)





schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted) †

Logic supply voltage, V _{CC} (see Note 1)	7 V
Logic input voltage range, V _I	0.3 V to 7 V
Power DMOS drain-to-source voltage, V _{DS} (see Note 2)	
Continuous source-to-drain diode anode current	500 mA
Pulsed source-to-drain diode anode current (see Note 3)	1 A
Pulsed drain current, each output, all outputs on, I _D , T _C = 25°C (see Note 3)	500 mA
Continuous drain current, each output, all outputs on, I _D , T _C = 25°C	150 mA
Peak drain current single output, I _{DM} ,T _C = 25°C (see Note 3)	500 mA
Single-pulse avalanche energy, E _{AS} (see Figure 4)	30 mJ
Avalanche current, I _{AS} (see Note 4)	500 mA
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T _J	40°C to 150°C
Operating case temperature range, T _C	40°C to 125°C
Storage temperature range	65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to GND.
 - 2. Each power DMOS source is internally connected to GND.
 - 3. Pulse duration \leq 100 μs and duty cycle \leq 2%.
 - 4. DRAIN supply voltage = 15 V, starting junction temperature (TJS) = 25°C, L = 200 mH, IAS = 0.5 A (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25^{\circ}C$ POWER RATING	DERATING FACTOR ABOVE T _C = 25°C	T _C = 125°C POWER RATING
DW	1389 mW	11.1 mW/°C	278 mW
N	1050 mW	10.5 mW/°C	263 mW



TPIC6B595 POWER LOGIC 8-BIT SHIFT REGISTER

SLIS032 - APRIL 1994 - REVISED JULY 1995

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V _{CC}	4.5	5.5	V
High-level input voltage, VIH	0.85 V _{CC}		V
Low-level input voltage, V _{IL}		0.15 V _{CC}	V
Pulsed drain output current, T _C = 25°C, V _{CC} = 5 V (see Notes 3 and 5)	-500	500	mA
Setup time, SER IN high before SRCK↑, t _{SU} (see Figure 2)	20		ns
Hold time, SER IN high after SRCK↑, th (see Figure 2)	20		ns
Pulse duration, t _W (see Figure 2)	40		ns
Operating case temperature, T _C	-40	125	°C

electrical characteristics, $V_{CC} = 5 \text{ V}$, $T_{C} = 25^{\circ}\text{C}$ (unless otherwise noted)

	PARAMETER	TEST COND	DITIONS	MIN	TYP	MAX	UNIT
V(BR)DSX	Drain-to-source breakdown voltage	I _D = 1 mA		50			V
V _{SD}	Source-to-drain diode forward voltage	I _F = 100 mA			0.85	1	٧
\/o	High-level output voltage,	$I_{OH} = -20 \mu A, V_{CC} = 4.5 V$		4.4	4.49		V
VOH	SER OUT	$I_{OH} = -4 \text{ mA}, V_{CC} = 4.5 \text{ V}$		4	4.2		٧
Vai	Low-level output voltage,	$I_{OL} = 20 \mu A$, $V_{CC} = 4.5 V$			0.005	0.1	V
VOL	SER OUT	$I_{OL} = 4 \text{ mA}, V_{CC} = 4.5 \text{ V}$			0.3	0.5	٧
lіН	High-level input current	$V_{CC} = 5.5 \text{ V}, V_I = V_{CC}$				1	μΑ
I _I L	Low-level input current	$V_{CC} = 5.5 \text{ V}, V_{I} = 0$				-1	μΑ
la a	Logio oupply ourrent	V 5.5.V	All outputs off		20	100	^
lcc	Logic supply current	V _{CC} = 5.5 V	All outputs on		150	300	μΑ
ICC(FRQ)	Logic supply current at frequency	fSRCK = 5 MHzCL = 30 pF, All outputs off,	See Figures 2 and 6		0.4	5	mA
I _N	Nominal current	$V_{DS(on)} = 0.5 \text{ V},$ $I_{N} = I_{D}, T_{C} = 85^{\circ}C$	See Notes 5, 6, and 7		90		mA
la ov	Off-state drain current	$V_{DS} = 40 \text{ V}, V_{CC} = 5.5 \text{ V}$			0.1	5	
IDSX	On-State drain current	$V_{DS} = 40 \text{ V}, V_{CC} = 5.5 \text{ V}$, T _C = 125°C		0.15	8	μΑ
		$I_D = 100 \text{ mA}, V_{CC} = 4.5 \text{ V}$			4.2	5.7	
rDS(on)	Static drain-source on-state resistance	$I_D = 100 \text{ mA}, T_C = 125^{\circ}\text{C}, \\ V_{CC} = 4.5 \text{ V}$	See Notes 5 and 6 and Figures 7 and 8		6.8	9.5	Ω
		$I_D = 350 \text{ mA}, V_{CC} = 4.5 \text{ V}$			5.5	8	

NOTES: 3. Pulse duration \leq 100 μ s and duty cycle \leq 2%.

- 5. Technique should limit T_J T_C to 10°C maximum.
- 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
- 7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at $T_C = 85^{\circ}C$.



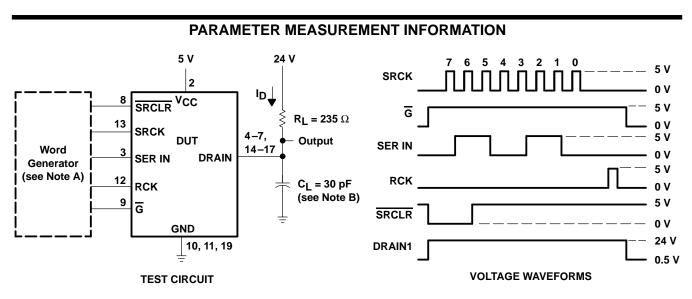
switching characteristics, $V_{CC} = 5 \text{ V}$, $T_{C} = 25^{\circ}\text{C}$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
^t PLH	Propagation delay time, low-to-high-level output from G			150		ns
tPHL	Propagation delay time, high-to-low-level output from \overline{G}	TEST CONDITIONS $C_L = 30 \text{ pF}, \qquad I_D = 100 \text{ mA},$ See Figures 1, 2, and 9 $I_F = 100 \text{ mA}, \qquad \text{di/dt} = 20 \text{ A/}\mu\text{s},$ See Notes 5 and 6 and Figure 3		90		ns
t _r	Rise time, drain output			200		ns
tf	Fall time, drain output			200		ns
ta	Reverse-recovery-current rise time			100		no
t _{rr}	Reverse-recovery time	See Figures 1, 2, and 9 I _F = 100 mA, di/dt = 20 A/μs,		300		ns

NOTES: 5. Technique should limit T_J – T_C to 10°C maximum.

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT	
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW package	All 9 outputs with agual power	90		°C/W
	memai resistance, junction-to-ambient	N package	All 8 outputs with equal power		95	C/VV



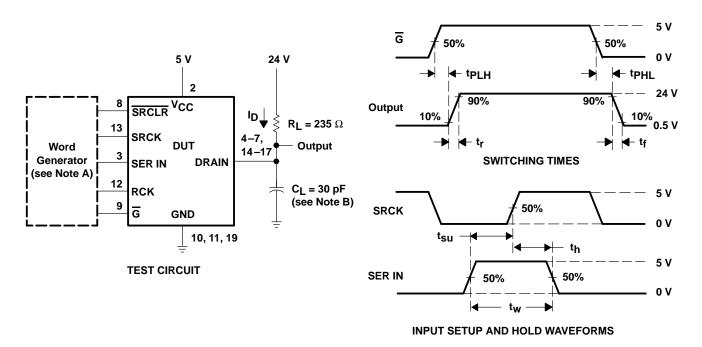
NOTES: A. The word generator has the following characteristics: $t_{\Gamma} \le 10$ ns, $t_{W} = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_{Q} = 50 \ \Omega$.

B. C_L includes probe and jig capacitance.

Figure 1. Resistive-Load Test Circuit and Voltage Waveforms

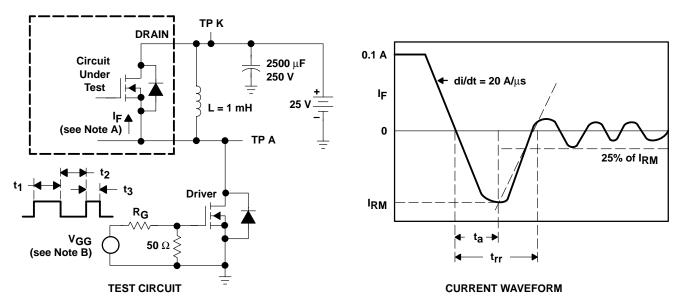
^{6.} These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The word generator has the following characteristics: $t_f \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50 \Omega$.
 - B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

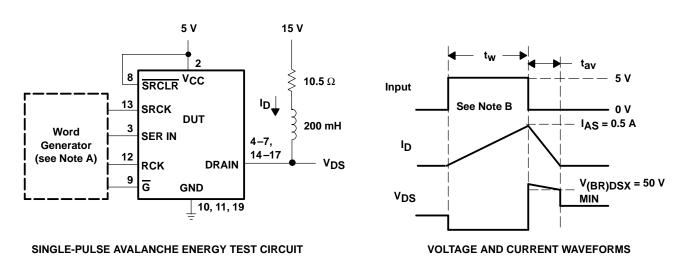


- NOTES: A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
 - B. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/ μ s. A V_{GG} double-pulse train is used to set I_F = 0.1 A, where t₁ = 10 μ s, t₂ = 7 μ s, and t₃ = 3 μ s.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode



PARAMETER MEASUREMENT INFORMATION

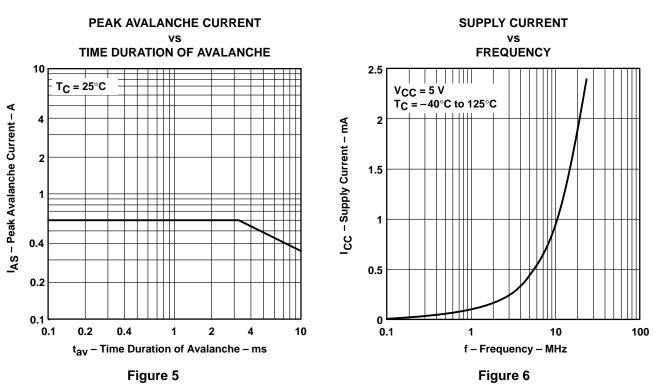


NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_{O} = 50 \Omega$.

B. Input pulse duration, t_W , is increased until peak current $I_{AS} = 0.5$ A. Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 30$ mJ.

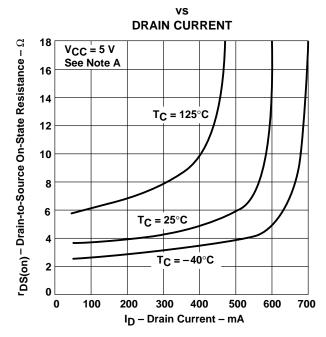
Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

DRAIN-TO-SOURCE ON-STATE RESISTANCE



STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE

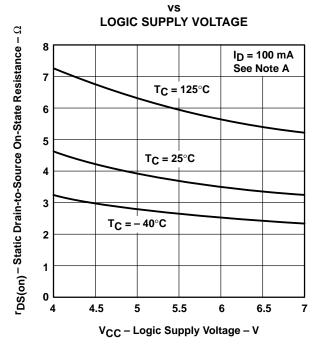
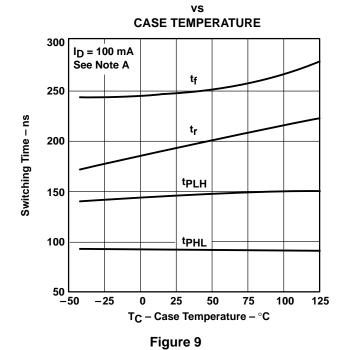


Figure 7 Figure 8

SWITCHING TIME



NOTE C. Technique should limit $T_J - T_C$ to 10°C maximum.



THERMAL INFORMATION

MAXIMUM CONTINUOUS DRAIN CURRENT OF EACH OUTPUT NUMBER OF OUTPUTS CONDUCTING **SIMULTANEOUSLY** 0.45 $V_{CC} = 5 V$ Maximum Continuous Drain Current of Each Output – A 0.4 0.35 0.3 0.25 T_C = 25°C 0.2 0.15 $T_C = 100^{\circ}C$ 0.1 T_C = 125°C ۵ 0.05 0 2 3 5 6 7 8

Figure 10

N - Number of Outputs Conducting Simultaneously

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT NUMBER OF OUTPUTS CONDUCTING **SIMULTANEOUSLY** $_{ m I_D}$ – Maximum Peak Drain Current of Each Output – A 0.5 d = 10%0.45 d = 20%0.4 0.35 d = 50% 0.3 0.25 d = 80% 0.2 0.15 $V_{CC} = 5 V$ $T_C = 25$ °C 0.1 $d = t_W/t_{period}$ 0.05 = 1 ms/tperiod 2 3 8 N - Number of Outputs Conducting Simultaneously

Figure 11

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