

SINGLE-CHIP HDMI TRANSMITTER PORT PROTECTION AND INTERFACE DEVICE

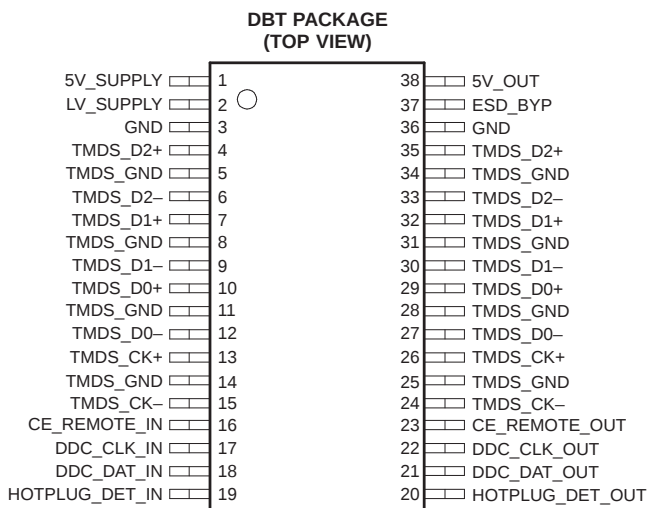
Check for Samples: [TPD12S521](#)

FEATURES

- Single-Chip ESD Solution for High-Definition Multimedia Interface (HDMI) Driver
- Supports HDMI 1.3 and HDMI 1.4 Data Rates (–3 dB Frequency > 3 GHz)
- 0.8-pF Capacitance for High-Speed Transition Minimized Differential Signaling (TMDS) Lines
- 0.05-pF Matching Capacitance Between the Differential Signal Pair
- Integrated Level Shifting for the Control Lines
- ±8-kV Contact ESD Protection on External Lines
- 38-Pin Thin Shrink Small-Outline Package (TSSOP) Provides Seamless Layout Option With HDMI Connector
- Backdrive Protection
 - TMDS_D[2:0]+/–
 - TMDS_CK+/–
 - CE_REMOTE_OUT
 - DDC_DAT_OUT
 - DDC_CLK_OUT
 - HOTPLUG_DET_OUT
- Lead-Free Package
- On-Chip Current Regulator With 55-mA Current Output

APPLICATIONS

- PCs
- Consumer Electronics
- Set-Top Boxes
- DVDRW Players



DESCRIPTION

The TPD12S521 is a single-chip ESD solution for the high-definition multimedia interface (HDMI) transmitter port. In many cases, the core ICs, such as the scalar chipset, may not have robust ESD cells to sustain system-level ESD strikes. In these cases, the TPD12S521 provides the desired system-level ESD protection, such as the IEC61000-4-2 (Level 4) ESD, by absorbing the energy associated with the ESD strike.

While providing the ESD protection, the TPD12S521 adds little or no additional glitch in the high-speed differential signals (see [Figure 6](#) and [Figure 7](#)). The high-speed transition minimized differential signaling (TMDS) lines add only 0.9-pF capacitance to the lines. In addition, the monolithic integrated circuit technology ensures that there is excellent matching between the two-signal pair of the differential line. This is a direct advantage over discrete ESD clamp solutions where variations between two different ESD clamps may significantly degrade the differential signal quality.

The low-speed control lines offer voltage-level shifting to eliminate the need for an external voltage level-shifter IC. The control line ESD clamps add 3.5-pF capacitance to the control lines. The 38-pin DBT package offers seamless layout routing option to eliminate the routing glitch for the differential signal pair.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION CONTINUED

The TPD12S521 provides an on-chip regulator with current output ratings of 55 mA at pin 38. This current enables HDMI receiver detection even when the receiver device is powered off. DBT package pitch (0.5 mm) matches with HDMI connector pitch. In addition, pin mapping follows the same order as the HDMI connector pin mapping. This HDMI receiver port protection and interface device is specifically designed for next-generation HDMI transmitter protection.

ORDERING INFORMATION

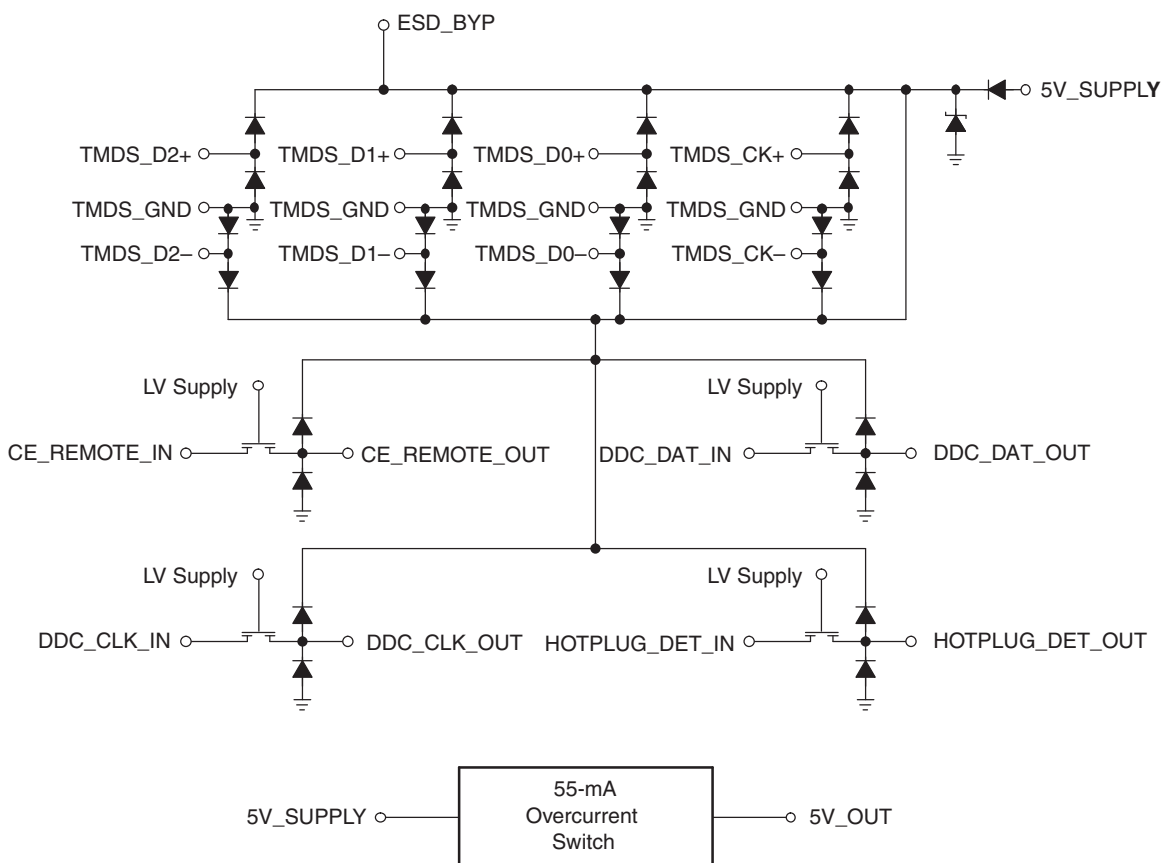
T _A	PACKAGE ⁽¹⁾ (2)	ORDERABLE PART NUMBER ⁽³⁾	TOP-SIDE MARKING
–40°C to 85°C	TSSOP-38 – DBT	TPD12S521DBTR	PN521

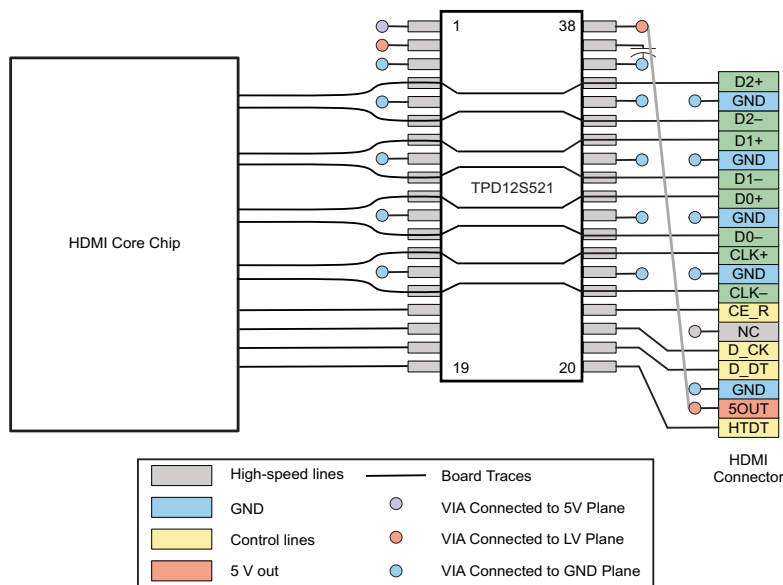
(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(3) Parts are shipped in tape-and-reel form, unless otherwise specified.

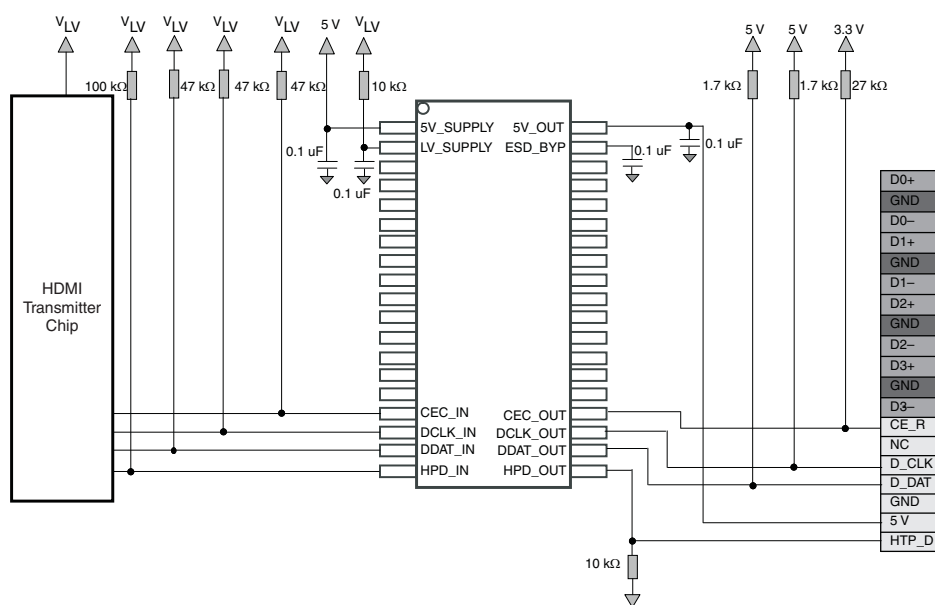
Figure 1. ELECTRICAL SCHEMATIC





A. External bypass capacitors and resistor components not included

Figure 2. Board Layout for HDMI Transmitter Using TPD12S521DBTR



A. V_{LV} = supply voltage of the core scalar chip

Figure 3. Application Schematic Showing Pins Requiring External Components: HDMI Transmitter Side

PIN DESCRIPTION

NAME	PIN NO.	ESD LEVEL	DESCRIPTION
5V_SUPPLY	1	2 kV ⁽¹⁾	Current source for 5V_OUT
LV_SUPPLY	2	2 kV ⁽¹⁾	Bias for CE/DDC/HOTPLUG level shifters
GND, TMDS_GND	3, 5, 8, 11, 14, 25, 28, 31, 34, 36	NA	TMDS ESD and parasitic GND return ⁽²⁾
TMDS_D2+	4, 35	8 kV ⁽³⁾	TMDS 0.8-pF ESD protection ⁽⁴⁾
TMDS_D2–	6, 33	8 kV ⁽³⁾	TMDS 0.8-pF ESD protection ⁽⁴⁾
TMDS_D1+	7, 32	8 kV ⁽³⁾	TMDS 0.8-pF ESD protection ⁽⁴⁾
TMDS_D1–	9, 30	8 kV ⁽³⁾	TMDS 0.8-pF ESD protection ⁽⁴⁾
TMDS_D0+	10, 29	8 kV ⁽³⁾	TMDS 0.8-pF ESD protection ⁽⁴⁾
TMDS_D0–	12, 27	8 kV ⁽³⁾	TMDS 0.8-pF ESD protection ⁽⁴⁾
TMDS_CK+	13, 26	8 kV ⁽³⁾	TMDS 0.8-pF ESD protection ⁽⁴⁾
TMDS_CK–	15, 24	8 kV ⁽³⁾	TMDS 0.8-pF ESD protection ⁽⁴⁾
CE_REMOTE_IN	16	2 kV ⁽¹⁾	LV_SUPPLY referenced logic level into ASIC
DDC_CLK_IN	17	2 kV ⁽¹⁾	LV_SUPPLY referenced logic level into ASIC
DDC_DAT_IN	18	2 kV ⁽¹⁾	LV_SUPPLY referenced logic level into ASIC
HOTPLUG_DET_IN	19	2 kV ⁽¹⁾	LV_SUPPLY referenced logic level into ASIC
HOTPLUG_DET_OUT	20	8 kV ⁽³⁾	5 V_SUPPLY referenced logic level out, plus 3.5-pF ESD ⁽⁵⁾ to connector
DDC_DAT_OUT	21	8 kV ⁽³⁾	5 V_SUPPLY referenced logic level out, plus 3.5-pF ESD to connector
DDC_CLK_OUT	22	8 kV ⁽³⁾	5 V_SUPPLY referenced logic level out, plus 3.5-pF ESD to connector
CE_REMOTE_OUT	23	8 kV ⁽³⁾	5 V_SUPPLY referenced logic level out, plus 3.5-pF ESD to connector
ESD_BYP	37	2 kV ⁽¹⁾	ESD bypass. This pin must be connected to a 0.1-μF ceramic capacitor.
5V_OUT	38	2 kV ⁽¹⁾	5-V regulator output

- (1) Human-Body Model (HBM) per MIL-STD-883C, Method 3015, $C_{DISCHARGE} = 100 \text{ pF}$, $R_{DISCHARGE} = 1.5 \text{ k}\Omega$, 5V_SUPPLY and LV_SUPPLY within recommended operating conditions, GND = 0 V, and ESD_BYP (pin 37) and HOTPLUG_DET_OUT (pin 20) each bypassed with a 0.1-μF ceramic capacitor connected to GND.
- (2) These pins should be routed directly to the associated GND pins on the HDMI connector, with single-point ground vias at the connector.
- (3) Standard IEC 61000-4-2, $C_{DISCHARGE} = 150 \text{ pF}$, $R_{DISCHARGE} = 330 \Omega$, 5V_SUPPLY and LV_SUPPLY within recommended operating conditions, GND = 0 V, and ESD_BYP (pin 37) and HOTPLUG_DET_OUT (pin 20) each bypassed with a 0.1-μF ceramic capacitor connected to GND.
- (4) These two pins must be connected together inline on the PCB.
- (5) This output can be connected to an external 0.1-μF ceramic capacitor, resulting in an increased ESD withstand voltage rating.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{5V_SUPPLY} V _{LV_SUPPLY}	Supply voltage		6	V
V _{I/O}	DC voltage at any channel input	GND – 0.5	6	V
T _{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Operating supply voltage	5V_SUPPLY		5	5.5	V
Bias supply voltage	LV_SUPPLY	1	3.3	5.5	V
Operating temperature		–40		85	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC5}	Operating supply current	5V_SUPPLY = 5 V			110	130	μ A
I_{CC3}	Bias supply current	LV_SUPPLY = 3.3 V			1	5	μ A
V_{DROP}	5V_OUT overcurrent output drop	5V_SUPPLY = 5 V, $I_{OUT} = 55$ mA			150	200	mV
I_{SC}	5V_OUT short-circuit current limit	5V_SUPPLY = 5 V, 5V_OUT = GND		90	135	175	mA
I_{OFF}	OFF-state leakage current, level-shifting NFET	LV_SUPPLY = 0 V			0.1	5	μ A
$I_{BACKDRIVE}$	Current conducted from output pins to V_SUPPLY rails when powered down	5V_SUPPLY < V_{CH_OUT}	TMDS_D[2:0]+/-, TMDS_CK+/-, CE_REMOTE_OUT, DDC_DAT_OUT, DDC_CLK_OUT, HOTPLUG_DET_OUT		0.1	5	μ A
V_{ON}	Voltage drop across level-shifting NFET when ON	LV_SUPPLY = 2.5 V, $V_S =$ GND, $I_{DS} = 3$ mA		75	95	140	mV
V_F	Diode forward voltage	$I_F = 8$ mA, $T_A = 25^\circ\text{C}^{(1)}$	Top diode		0.85		V
			Bottom diode		0.85		
V_{ESD}	ESD withstand voltage	Pins 4, 7, 10, 13, 20–24, 27, 30, 33 ^{(1) (2)}	IEC	± 8			kV
		Pins 1, 2, 16–19, 37, 38 ^{(1) (3)}	HBM	± 2			
V_{CL}	Channel clamp voltage at ± 8 -kV HBM ESD	$T_A = 25^\circ\text{C}^{(1) (3)}$	Positive transients		9		V
			Negative transients		–9		
R_{DYN}	Dynamic resistance	$I = 1$ A, $T_A = 25^\circ\text{C}^{(4)}$	Positive transients		3		Ω
			Negative transients		1.5		
I_{LEAK}	TMDS channel leakage current	$T_A = 25^\circ\text{C}^{(1)}$			0.01	1	μ A
$C_{IN, TMDS}$	TMDS channel input capacitance	5V_SUPPLY = 5 V, Measured at 1 MHz, $V_{BIAS} = 2.5$ V ⁽¹⁾			0.8	1.0	pF
$\Delta C_{IN, TMDS}$	TMDS channel input capacitance matching	5V_SUPPLY = 5 V, Measured at 1 MHz, $V_{BIAS} = 2.5$ V ^{(1) (5)}			0.05		pF
C_{MUTUAL}	Mutual capacitance between signal pin and adjacent signal pin	5V_SUPPLY = 0 V, Measured at 1 MHz, $V_{BIAS} = 2.5$ V ⁽¹⁾			0.07		pF
C_{IN}	Level-shifting input capacitance, capacitance to GND	5V_SUPPLY = 0 V, Measured at 100 KHz, $V_{BIAS} = 2.5$ V ⁽¹⁾	DDC		3.5	4	pF
			CEC		3.5	4	
			HP		3.5	4	

(1) This parameter is specified by design and verified by device characterization.

(2) Standard IEC 61000-4-2, $C_{DISCHARGE} = 150$ pF, $R_{DISCHARGE} = 330$ Ω

(3) Human-Body Model (HBM) per MIL-STD-883, Method 3015, $C_{DISCHARGE} = 100$ pF, $R_{DISCHARGE} = 1.5$ k Ω

(4) These measurements performed with no external capacitor on ESD_BYP.

(5) Intrapair matching, each TMDS pair (i.e., D+, D–)

TYPICAL PERFORMANCE

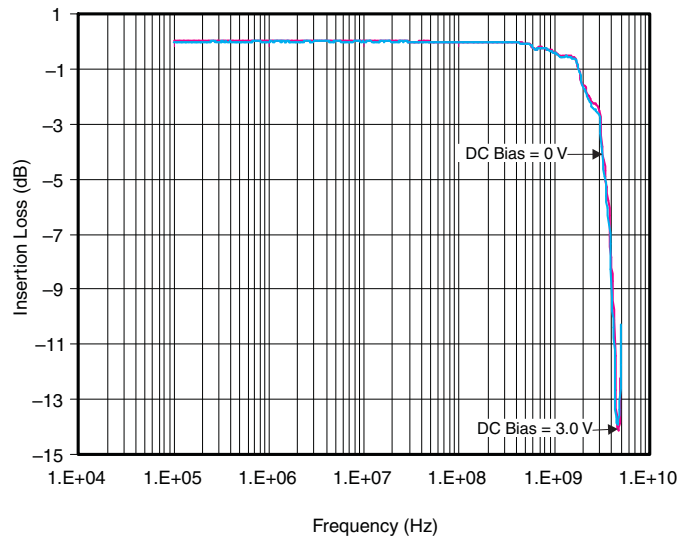


Figure 4. Insertion Loss Performance Across Frequency

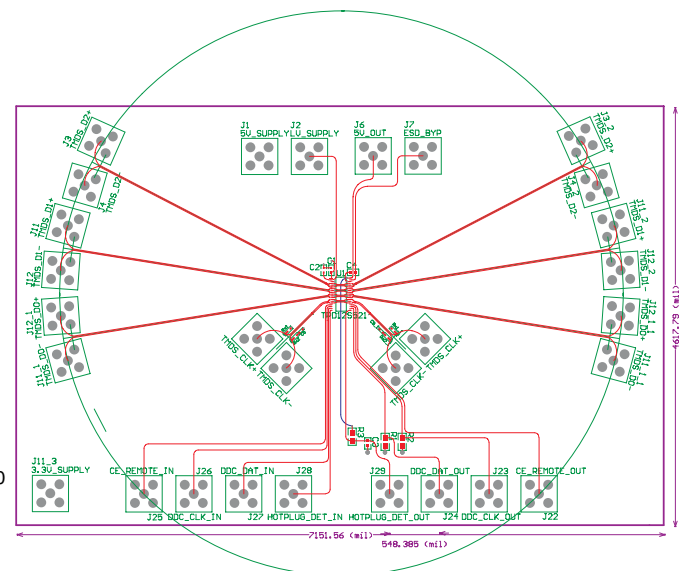


Figure 5. Test Board to Measure Eye Diagram for the TPD12S521 (Refer to Eye Diagram Plot)

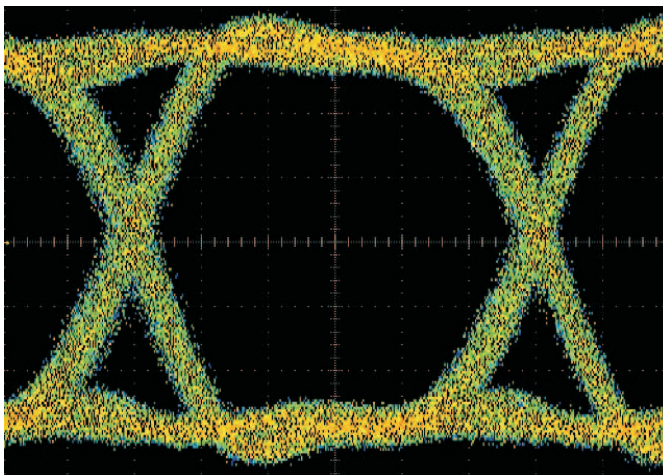


Figure 6. HDMI 1.65Gbps Eye Diagram With TPD12S521 on a Test Board

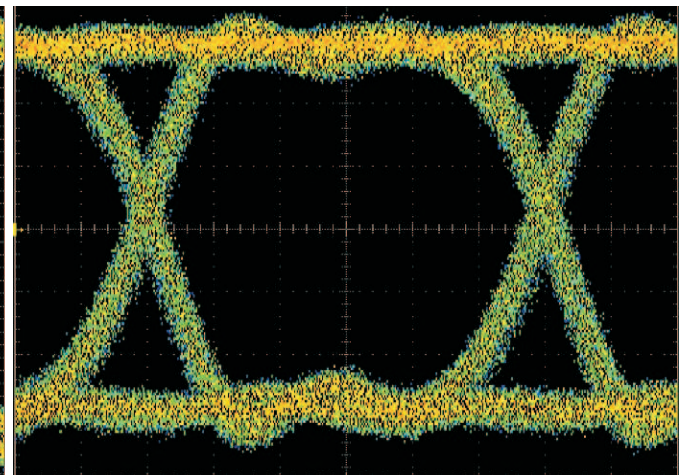


Figure 7. HDMI 1.65Gbps Eye Diagram Without TPD12S521 in the Socket in the Test Board

REVISION HISTORY

Changes from Revision B (April 2009) to Revision C	Page
• Added specific pins to Backdrive description in FEATURES	1
• Added HDMI 1.4 Data Rate support to FEATURES	1

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TPD12S521DBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPD12S521DBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS

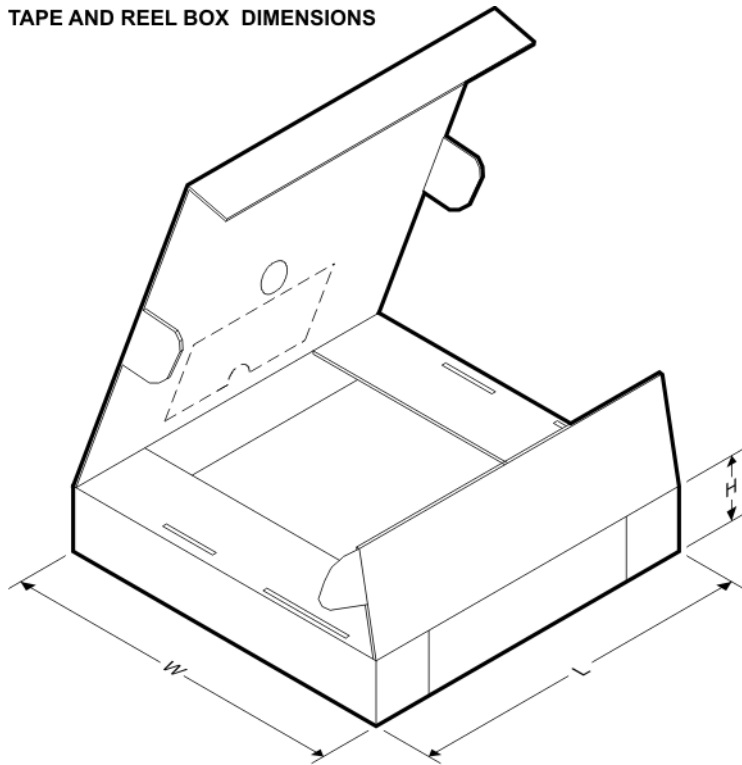

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD12S521DBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

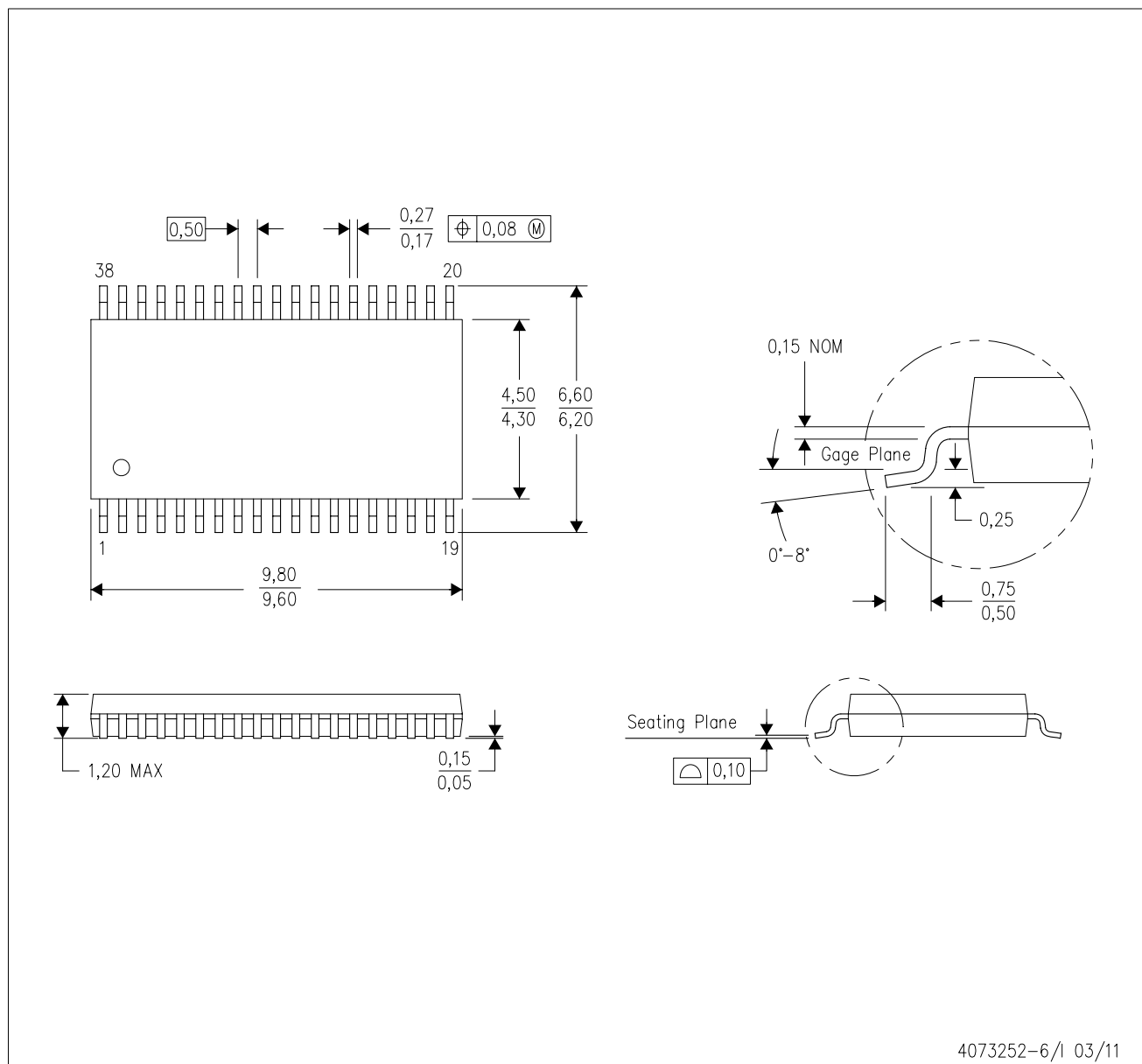


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD12S521DBTR	TSSOP	DBT	38	2000	367.0	367.0	38.0

DBT (R-PDSO-G38)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-153.

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