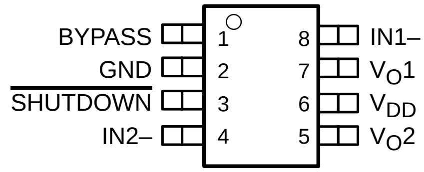
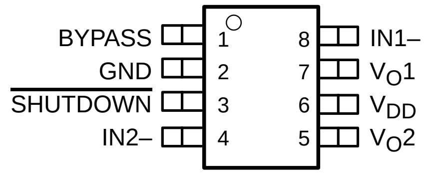
- **50-mW Stereo Output**
- **Low Supply Current . . . 0.75 mA**
- **Low Shutdown Current . . . 50 nA**
- **Pin Compatible With LM4881 and TPA102†**
- **Pop Reduction Circuitry**
- **Internal Mid-Rail Generation**
- **Thermal and Short-Circuit Protection**
- **Surface-Mount Packaging**
  - **MSOP**
  - **SOIC**
- **1.6-V to 3.6-V Supply Voltage Range**

† The polarity of the SHUTDOWN pin is reversed.

D PACKAGE (TOP VIEW)



DGK PACKAGE (TOP VIEW)



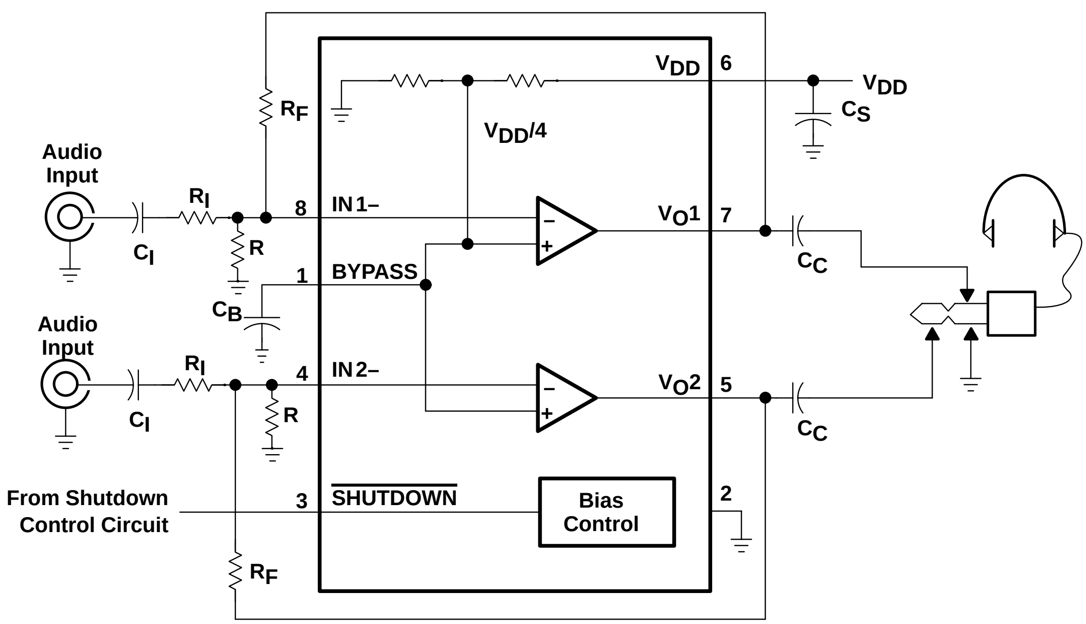
description

The TPA6100A2 is a stereo audio power amplifier packaged in either an 8-pin SOIC package or an 8-pin MSOP package capable of delivering 50 mW of continuous RMS power per channel into 16-Ω loads. Amplifier gain is externally configured by a means of three resistors per input channel and does not require external compensation for settings of 1 to 10.

The TPA6100A2 is optimized for battery applications because of its low supply current, shutdown current, and THD+N. To obtain the low-supply voltage range, the TPA6100A2 biases BYPASS to $V_{DD}/4$. A resistor with a resistance equal to R_F must be added from the inputs to ground to allow the output to be biased at $V_{DD}/2$.

When driving a 16-Ω load with 45-mW output power from 3.3 V, THD+N is 0.04% at 1 kHz, and less than 0.2% across the audio band of 20 Hz to 20 kHz. For 28 mW into 32-Ω loads, the THD+N is reduced to less than 0.03% at 1 kHz, and is less than 0.2% across the audio band of 20 Hz to 20 kHz.

typical application circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE		MSOP SYMBOLIZATION
	SMALL OUTLINE (D)	MSOP (DGK)	
–40°C to 85°C	TPA6100A2D	TPA6100A2DGK	AJL

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	1	I	Tap to voltage divider for internal mid-supply bias supply. BYPASS is set at V_{DD}/4. Connect to a 0.1-µF to 1-µF low-ESR capacitor for best performance.
GND	2	I	GND is the ground connection.
IN1–	8	I	IN1– is the inverting input for channel 1.
IN2–	4	I	IN2– is the inverting input for channel 2.
$\overline{\text{SHUTDOWN}}$	3	I	Active-low input. When held low, the device is placed in a low supply current mode.
V_{DD}	6	I	V_{DD} is the supply voltage terminal.
V_O1	7	O	V_O1 is the audio output for channel 1.
V_O2	5	O	V_O2 is the audio output for channel 2.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} . . . . 4 V
Input voltage, V_I . . . . –0.3 V to V_{DD} + 0.3 V
Continuous total power dissipation . . . . Internally Limited
Operating junction temperature range, T_J . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	710 mW	5.68 mW/°C	454 mW	369 mW
DGK	469 mW	3.75 mW/°C	300 mW	244 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1.6	3.6	V
Operating free-air temperature, T_A	–40	85	°C

dc electrical characteristics at T_A = 25°C, V_{DD} = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Power supply rejection ratio	V_{DD} = 3.0 V to 3.6 V		72		dB
I_{DD}	Supply current			0.75	1.2	mA
$I_{DD(SD)}$	Supply current in $\overline{\text{SHUTDOWN}}$ mode			50	250	nA
$\|I_{IH}\|$	High-level input current ($\overline{\text{SHUTDOWN}}$)	V_{DD} = 3.3 V, V_I= V_{DD}			1	µA
$\|I_{IL}\|$	Low-level input current ($\overline{\text{SHUTDOWN}}$)	V_{DD} = 3.3 V, V_I= 0 V			1	µA
Z_I	Input impedance (IN1–, IN2–)			>1		MΩ

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 16 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%, f = 1 kHz		50		mW
THD+N	Total harmonic distortion + noise	P_O = 45 mW, 20–20 kHz		0.2%		
B_{OM}	Maximum output power BW	G = 1, THD < 0.5%		> 20		kHz
k_{SVR}	Supply ripple rejection	f = 1 kHz		52		dB
SNR	Signal-to-noise ratio	P_O = 50 mW		90		dB
V_n	Noise output voltage (no noise weighting filter)			28		µV(rms)

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%, f = 1 kHz		35		mW
THD+N	Total harmonic distortion + noise	P_O = 30 mW, 20–20 kHz		0.2%		
B_{OM}	Maximum output power BW	G = 1, THD < 0.2%		>20		kHz
k_{SVR}	Supply ripple rejection	f = 1 kHz		52		dB
SNR	Signal-to-noise ratio	P_O = 35 mW		91		dB
V_n	Noise output voltage (no noise weighting filter)			28		µV(rms)

dc electrical characteristics at T_A = 25°C, V_{DD} = 1.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Power supply rejection ratio	V_{DD} = 1.5 V to 1.7 V		80		dB
I_{DD}	Supply current			1.2		mA
$I_{DD(SD)}$	Supply current in $\overline{\text{SHUTDOWN}}$ mode			50	250	nA
$\lvert I_{IH}\rvert$	High-level input current ($\overline{\text{SHUTDOWN}}$)	V_{DD} = 1.6 V, V_I = V_{DD}			1	µA
$\lvert I_{IL}\rvert$	Low-level input current ($\overline{\text{SHUTDOWN}}$)	V_{DD} = 1.6 V, V_I = 0 V			1	µA
Z_I	Input impedance (IN1–, IN2–)			>1		MΩ

ac operating characteristics, V_{DD} = 1.6 V, T_A = 25°C, R_L = 16 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%, f = 1 kHz		9.5		mW
THD+N	Total harmonic distortion + noise	P_O = 9.5 mW, 20–20 kHz		0.4%		
B_{OM}	Maximum output power BW	G = 0 dB, THD < 0.4%		> 20		kHz
k_{SVR}	Supply ripple rejection	f = 1 kHz		53		dB
SNR	Signal-to-noise ratio	P_O = 9.5 mW		86		dB
V_n	Noise output voltage (no noise weighting filter)			18		µV(rms)

ac operating characteristics, V_{DD} = 1.6 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%, f = 1 kHz		7.1		mW
THD+N	Total harmonic distortion + noise	P_O = 6.5 mW, 20–20 kHz		0.3%		
B_{OM}	Maximum output power BW	G = 0 dB, THD < 0.3%		>20		kHz
k_{SVR}	Supply ripple rejection	f = 1 kHz		53		dB
SNR	Signal-to-noise ratio	P_O = 7.1 mW		88		dB
V_n	Noise output voltage (no noise weighting filter)			18		µV(rms)

APPLICATION INFORMATION

gain setting resistors, R_F, R_I, and R

The voltage gain for the TPA6100A2 is set by resistors R_F and R_I according to equation 1.

$$\text{Gain} = -\left(\frac{R_F}{R_I}\right) \text{ or Gain (dB)} = 20 \log \left(\frac{R_F}{R_I}\right) \quad (1)$$

Given that the TPA6100A2 is a MOS amplifier, the input impedance is very high. Consequently input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper start-up operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 2.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \quad (2)$$

As an example, consider an input resistance of 20 kΩ and a feedback resistor of 20 kΩ. The gain of the amplifier would be –1 and the effective impedance at the inverting terminal would be 10 kΩ, which is within the recommended range.

For high performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ, the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F. This, in effect, creates a low-pass filter network with the cutoff frequency defined in equation 3.

$$f_c = \frac{1}{2\pi R_F C_F} \quad (3)$$

For example, if R_F is 100 kΩ and C_F is 5 pF then f_c is 318 kHz, which is well outside the audio range.

For maximum signal swing and output power at low supply voltages like 1.6 V to 3.3 V, BYPASS is biased to $V_{DD}/4$. However, to allow the output to be biased at $V_{DD}/2$, a resistor, R, equal to R_F must be placed from the negative input to ground.

input capacitor, C_I

In the typical application, an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 4.

$$f_c = \frac{1}{2\pi R_I C_I} \quad (4)$$

The value of C_I is important to consider, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 20 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 4 is reconfigured as equation 5.

$$C_I = \frac{1}{2\pi R_I f_c} \quad (5)$$

APPLICATION INFORMATION

input capacitor, C_I (continued)

In this example, C_I is 0.40 µF, so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (>10). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/4$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA6100A2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the power amplifier is recommended.

midrail bypass capacitor, C_B

The midrail bypass capacitor (C_B) serves several important functions. During startup, C_B determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so low it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 55-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 6 should be maintained.

$$\frac{1}{\left(C_B \times 55\ \text{k}\Omega\right)} \le \frac{1}{\left(C_I R_I\right)} \qquad (6)$$

As an example, consider a circuit where C_B is 1 µF, C_I is 1 µF, and R_I is 20 kΩ. Inserting these values into the equation 6 results in: 18.18 ≤ 50 which satisfies the rule. Bypass capacitor (C_B) values of 0.47-µF to 1-µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

output coupling capacitor, C_C

In the typical single-supply single-ended (SE) configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 7.

$$f_c = \frac{1}{2\pi R_L C_C} \qquad (7)$$

The main disadvantage, from a performance standpoint, is that the typically small load impedances drive the low-frequency corner higher. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 68 µF is chosen and loads vary from 32 Ω to 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

APPLICATION INFORMATION

Table 1. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
32 Ω	68 µF	73 Hz
10,000 Ω	68 µF	0.23 Hz
47,000 Ω	68 µF	0.05 Hz

As Table 1 indicates, headphone response is adequate and drive into line level inputs (a home stereo for example) is very good.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

$$\frac{1}{\left(C_B \times 55\ \text{k}\Omega\right)} \leq \frac{1}{\left(C_I R_I\right)} \ll \frac{1}{R_L C_C} \qquad (8)$$

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this application. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

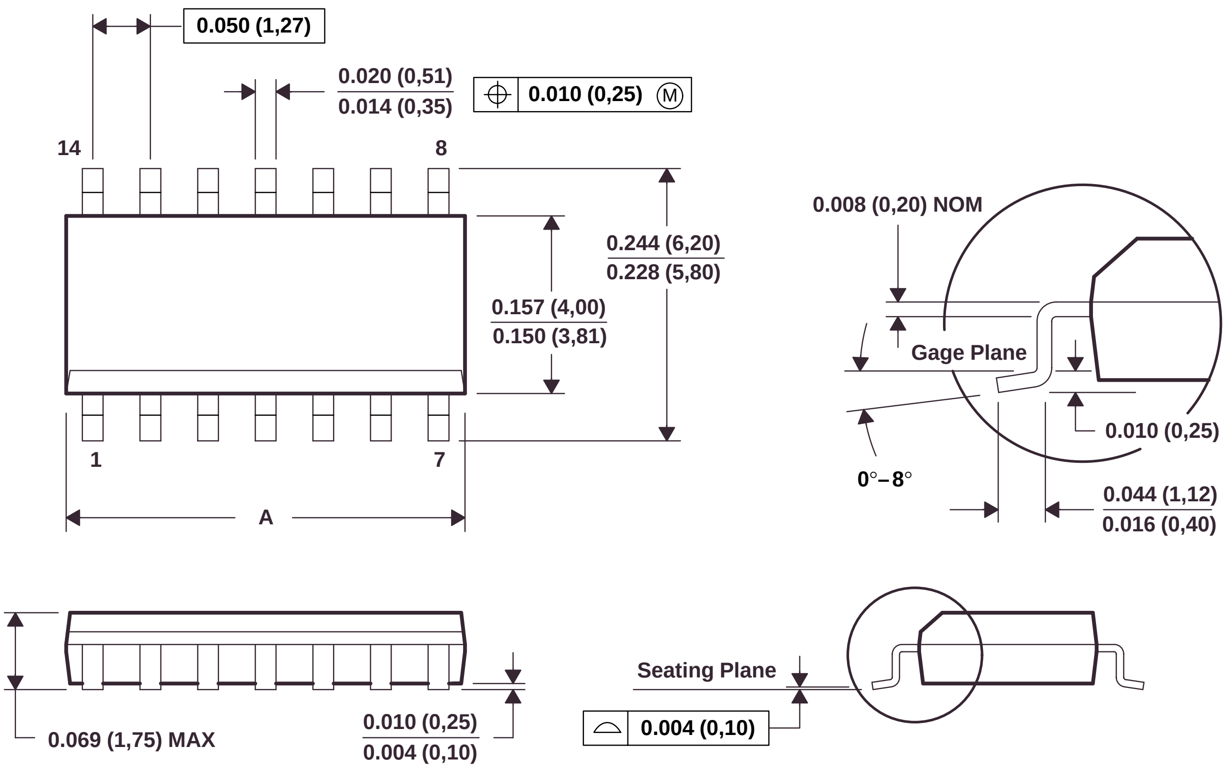
3.3-V versus 1.6-V operation

The TPA6100A2 was designed for operation over a supply range of 1.6 V to 3.6 V. There are no special considerations for 1.6-V versus 3.3-V operation as far as supply bypassing, gain setting, or stability. Supply current is slightly reduced from 0.75 mA (typical) to 0.65 mA (typical). The most important consideration is that of output power. Each amplifier can produce a maxium output voltage swing within a few hundred millivolts of the rails with a 10-kΩ load. However, this voltage swing decreases as the load resistance decreases and the $r_{DS(on)}$ as the output stage transistors becomes more significant. For example, for a 32-Ω load, the maximum peak output voltage with V_{DD} = 1.6 V is approximately 0.7 V with no clipping distortion. This reduced voltage swing effectively reduces the maximum undistorted output power.

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



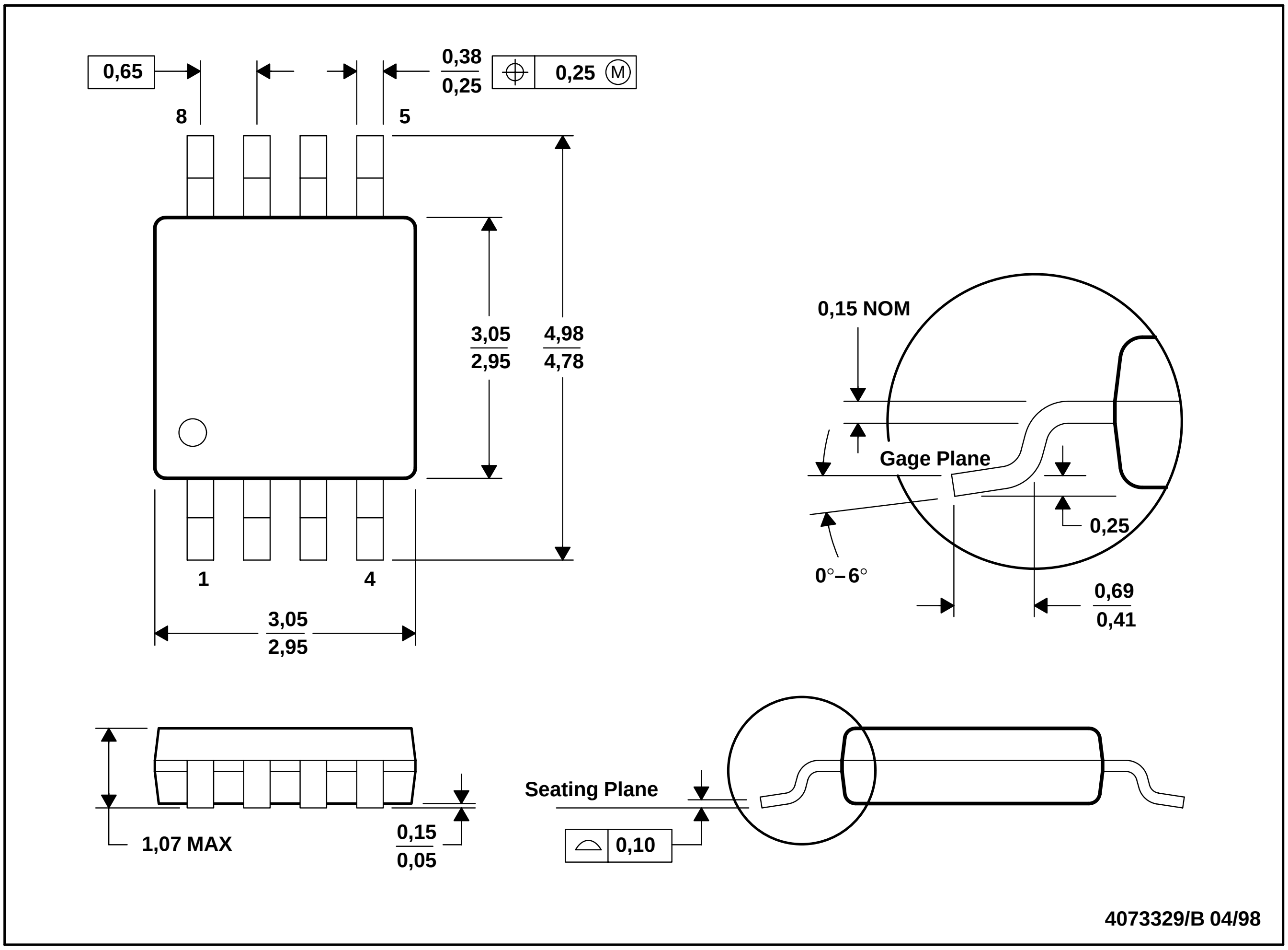
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

MECHANICAL INFORMATION

DGK (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, license, warranty or endorsement thereof.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations and notices. Representation or reproduction of this information with alteration voids all warranties provided for an associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Resale of TI's products or services with *statements different from or beyond the parameters* stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Also see: Standard Terms and Conditions of Sale for Semiconductor Products. www.ti.com/sc/docs/stdterms.htm

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265