National Semiconductor

TP5116A, TP5116A-1, TP5156A, TP5156A-1 Monolithic CODECs

General Description

The TP5116A and TP5156A are monolithic PCM CODECs implemented with double-poly CMOS technology. The TP5116A is intended for μ-law applications and the TP5156A is for A-law applications.

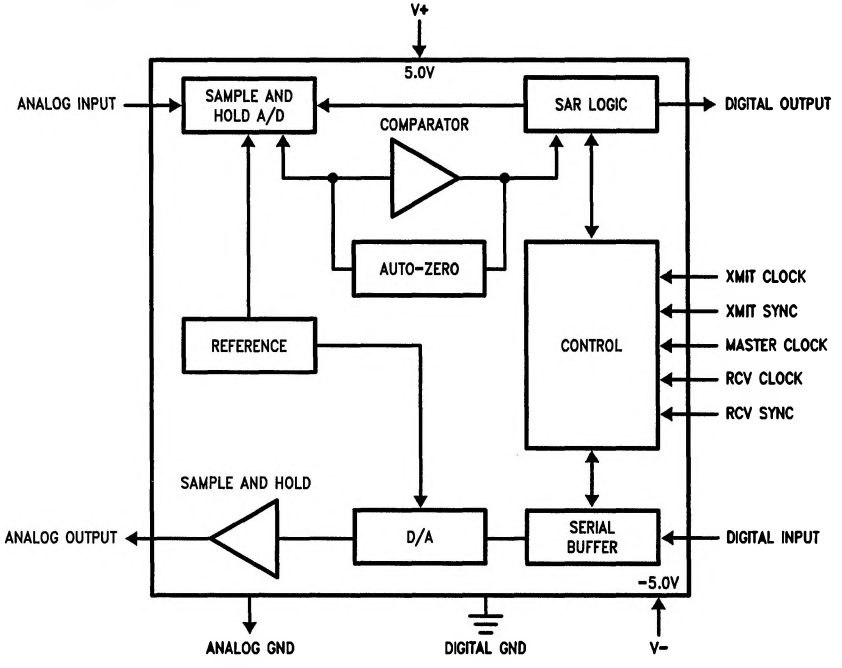
Each device contains separate D/A and A/D circuitry, all necessary sample and hold capacitors, and internal auto-zero circuits. Each device also contains a precision internal voltage reference, eliminating the need for an external reference. There are no internal connections to pins 15 or 16, making them directly interchangeable with CODECs using external reference components.

All devices are intended to be used with the TP3040 monolithic PCM filter which provides the input anti-aliasing function for the encoder, smooths the output of the decoder and corrects for the sin x/x distortion introduced by the decoder sample and hold output.

Features

- TP5116A—μ-law coding (sign plus magnitude format)
- TP5156A—A-law coding
- Synchronous or asynchronous operation
- Precision voltage reference on-chip
- Internal sample-and-hold capacitors
- Internal auto-zero circuit
- Low operation power—40 mW typical
- ±5V operation
- TTL compatible digital interface

Simplified Block Diagram



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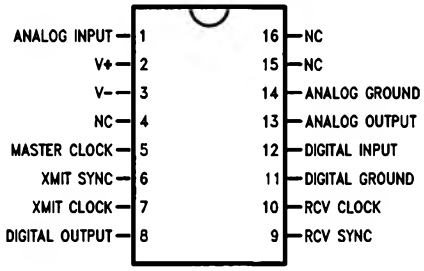
Connection Diagram

Dual-In-Line Package



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Top View

Order Number TP5116AJ or TP5156AJ
See NS Package Number J16A

Description of Pin Functions

Symbol	Function
ANALOG INPUT	ANALOG INPUT to the encoder. This signal will be sampled at the beginning of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
V^+	5V(±5%) Power Supply.
V^-	−5V(±5%) Power Supply.
NC	Unused.
MASTER CLOCK	MASTER CLOCK input used to operate the internal encode and decode sequencers. Should be 1.536 MHz, 1.544 MHz or 2.048 MHz.
XMIT SYNC	Encoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally eight XMIT CLOCK cycles wide.
XMIT CLOCK	Transmit bit clock input used to shift out the PCM data on DIGITAL OUTPUT. May operate from 64 kHz to 2.048 MHz. May be asynchronous with RCV CLOCK.
DIGITAL OUTPUT	Serial PCM TRI-STATE output from encoder. During the encoder time slot, the PCM code for the previous sample of ANALOG INPUT is shifted out, most significant bit first, on the rising edge of XMIT CLOCK.
RCV SYNC	Decoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally eight RCV CLOCK cycles wide.
RCV CLOCK	Receive bit clock input used to shift in the PCM data on DIGITAL INPUT. May operate from 64 kHz to 2.048 MHz. May be asynchronous with XMIT CLOCK.
DIGITAL GROUND	All digital levels referenced to the DIGITAL GROUND pin.
DIGITAL INPUT	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into DIGITAL INPUT, most significant bit first, on the rising edge of RCV CLOCK.
ANALOG OUTPUT	ANALOG OUTPUT from the decoder. The decoder sample and hold amplifier is updated approximately 15 μs after the end of the decode time slot.
ANALOG GROUND	All analog signals are referenced to the ANALOG GROUND pin.

ENCODING FORMAT AT DIGITAL OUTPUT

	TP5116A Sign + Magnitude								TP5156A A-Law (Includes Even Bit Inversion)							
V_{IN} = +Full-Scale	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0
V_{IN} = 0V	1	0	0	0	0	0	0	0	1	1	0	1	0	1	0	1
	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1
V_{IN} = −Full-Scale	0	1	1	1	1	1	1	1	0	0	1	0	1	0	1	0

Functional Description

Approximately 4 μs after the rising edge of the XMIT SYNC pulse, the voltage present on the ANALOG INPUT is sampled and the process of encoding that sample into a PCM code is begun. Simultaneously, the 8-bit PCM code corresponding to the previous sample is shifted out of the DIGITAL OUTPUT, MSB first, on the rising edge of the next eight cycles of the XMIT CLOCK. When XMIT SYNC (which is normally eight XMIT CLOCK cycles long) goes low, the TRI-STATE DIGITAL OUTPUT is returned to the high impedance state. On the TP5116A, the PCM code is in a μ-law sign plus magnitude format. The TP5156A uses the standard A-law coding.

An 8-bit PCM code is shifted into DIGITAL INPUT on the rising edge of the first eight RCV CLOCK pulses after RCV SYNC goes high. RCV SYNC is nominally eight RCV CLOCK cycles wide. Approximately 15 μs after RCV SYNC goes low, the ANALOG OUTPUT is updated to the voltage corresponding to the PCM input code.

All encoding and decoding operations are run from the MASTER CLOCK. MASTER CLOCK should be in the range of 1.536 MHz to 2.048 MHz and must be synchronous with XMIT CLOCK. The XMIT and RCV CLOCK may vary from 64 kHz to 2.048 MHz.

ENCODING DELAY

The encoding process begins immediately at the beginning of the encode time slot and is concluded no later than 18 time slots later. In normal applications, the PCM data is not shifted out until the next time slot 125 μs later, resulting in an encoding delay of 125 μs. In some applications it is possible to operate the CODEC at a higher frame rate to reduce this delay. With a 2.048 MHz MASTER CLOCK, the FS rate could be increased to 15 kHz, reducing the delay from 125 μs to 67 μs.

DECODING DELAY

The decoding process begins immediately after the end of the decoder time slot. The output of the decoder sample and hold amplifier is updated 28 MASTER CLOCK cycles later. The decoding delay is therefore approximately 28 clock cycles plus one half of a frame time or, 81 μs for a 1.544 MHz system with an 8 kHz frame rate or, 76 μs for a 2.048 MHz system with an 8 kHz frame rate. Again, for some applications the frame rate could be increased to reduce this delay.

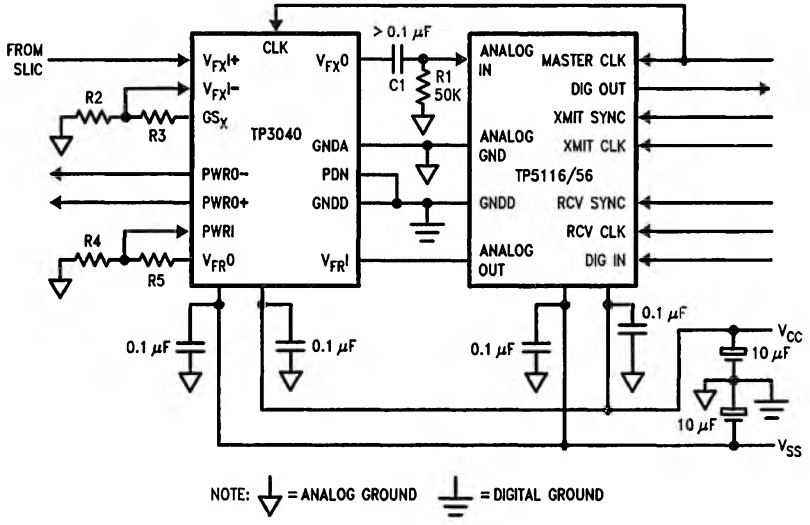
Typical Application

A typical application of these CODECs used in conjunction with the TP3040 PCM filter is shown below. The values of resistor R1 and DC blocking capacitor C1, are non-critical. The capacitor value should exceed 0.1 μF, R1 should be less than 50 kΩ, and the product R1×C1 should exceed 4 ms.

$$\text{XMIT GAIN} = 20 \times \log\left(\frac{R3 + R2}{R2}\right) + 3\ \text{dB}$$

$$\text{RCV GAIN} = 20 \times \log\left(\frac{R4}{R4 + R5}\right)$$

The power supply decoupling capacitors should be 0.1 μF. In order to take advantage of the excellent noise performance of these CODECs, care must be taken in board layout to prevent coupling of digital noise into the sensitive analog lines. For card insertion into a hot connector, care should be taken to insure that GNDA and GNDD are contacted prior to V_{CC} and V_{BB}.



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Operating Temperature	−25°C to +125°C
Storage Temperature	−65°C to +150°C
V^+ with Respect to DIGITAL GROUND	7V
V^- with Respect to DIGITAL GROUND	−7V
Voltage at Any Analog Input or Output	V^- −0.3V to V^+ +0.3V
Voltage at Any Digital Input or Output	GNDD−0.3V to V^+ + 0.3V
Lead Temperature (Solderdip 10 sec.)	300°C
ESD rating to be determined.	

DC Electrical Characteristics

Unless otherwise noted T_A = 0°C to 70°C, V^+ = 5.0V ±5%, V^- = −5.0V ±5%. Typical characteristics are specified at V^+ = 5.0V,V^- = −5.0V and T_A = 25°C. All digital signals are referenced to DIGITAL GROUND. All analog signals are referenced to ANALOG GROUND. Limits printed in bold characters are guaranteed for V^+ = 5.0V ±5%, V^- = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
I_I	Input Current	$0V < V_{IN} < V^+$	**−10**		**10**	μA
V_{IL}	Input Low Voltage				**0.6**	V
V_{IH}	Input High Voltage		**2.2**			V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 6 mA	2.4			V
ANALOG INTERFACE						
Z_I	Analog Input Impedance when Sampling	Resistance in Series with Approximately 70 pF	2			kΩ
Z_O	Output Impedance at Analog Output			10	20	Ω
I_{IN}	Analog Input Bias Current	V_{IN} = 0V	−0.1		0.1	μA
R1 × C1	DC Blocking Time Constant		4.0			ms
C1	DC Blocking Capacitor		0.1			μF
R1	Input Bias Resistor				50	kΩ
POWER DISSIPATION						
I_{CC1}	Operating Current, V_{CC}			3.5	**8.0**	mA
I_{BB1}	Operating Current, V_{BB}			3.5	**8.0**	mA

AC Electrical Characteristics

Unless otherwise noted, T_A = 25°C, V^+ =5.0V,V^- = −5.0V. The analog input is a 0 dBm0, 1.02 kHz sine wave. The DIGITAL INPUT is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected, limits printed in bold characters are guaranteed for V^+ = 5.0V ±5%, V^- = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Absolute Level	The nominal 0 dBm0 levels for the TP5116A is 1.227 Vrms and 1.231 Vrms for the TP5156A. The resulting nominal overload level is 2.5V peak for all devices. All gain measurements for the encode and decode portions of the devices are based on these nominal levels after the necessary sin x/x corrections are made.				
G_{RA}	Receive Gain, Absolute	T_A = 25°C, V^+ = 5V, V^- = −5V TP5116A, TP5156A TP5116A-1, TP5156A-1	 **−0.125** **−0.175**		 **0.125** **0.175**	 dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	T_A = 0°C to 70°C	−0.05		0.05	dB

AC Electrical Characteristics (Continued)

Unless otherwise noted, T_A = 25°C, V^+ = 5.0V, V^- = −5.0V. The analog input is a 0 dBm0, 1.02 kHz sine wave. The DIGITAL INPUT is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected. Limits printed in bold characters are guaranteed for V^+ = 5.0V ±5%, V^- = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	V^+ = 5V ±5%, V^- = −5V±5%	−0.07		0.07	dB
G_{XA}	Transmit Gain, Absolute	T_A = 25°C, V^+ = 5V, V^- = −5V TP5116A, TP5156A TP5116A-1, TP5156A-1	**−0.125** **−0.175**		**0.125** **0.175**	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	T_A = 0°C to 70°C	−0.05		0.05	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	V^+ = 5V ±5%, V^- = −5V ±5%	−0.07		0.07	dB
G_{RAL}	Absolute Receive Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0 0 dBm0 to 3 dBm0 −40 dBm0 to 0 dBm0 −50 dBm0 to −40 dBm0 −55 dBm0 to −50 dBm0	 **−0.3** **−0.2** **−0.4** **−1.0**		 **0.3** **0.2** **0.4** **1.0**	 dB dB dB dB
G_{XAL}	Absolute Transmit Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0 0 dBm0 to 3 dBm0 −40 dBm0 to 0 dBm0 −50 dBm0 to −40 dBm0 TP5116A, TP5156A TP5116A-1, TP5156A-1 −55 dBm0 to −50 dBm0	 **−0.3** **−0.2** **−0.4** **−0.475** **−1.0**		 **0.3** **0.2** **0.4** **0.475** **1.0**	 dB dB dB dB dB
STD_R	Receive Signal to Distortion Ratio	Sinusoidal Test Method Input Level −30 dBm0 to 0 dBm0 −40 dBm0 −45 dBm0	 **35** **29** **25**			 dBC dBC dBC
STD_X	Transmit Signal to Distortion Ratio	Sinusoidal Test Method Input Level −30 dBm0 to 0 dBm0 −40 dBm0 −45 dBm0	 **35** **29** **25**			 dBC dBC dBC
N_R	Receive Idle Channel Noise	D_R = Idle Code			**8**	dBrnC0
N_X	Transmit Idle Channel Noise	TP5116A, VF_X = 0V TP5156A, VF_x = 0V			**13** **−66**	dBrnC0 dBm0p
$PPSR_X$	Positive Power Supply Rejection, Transmit	Input Level = 0V, V_{CC} = 5.0 V_{DC} +300 mVrms, f = 1.02 kHz	**50**			dB
$PPSR_R$	Positive Power Supply Rejection, Receive	D_R = Idle Code V_{CC} = 5.0 V_{DC} + 300 mVrms, f = 1.02 kHz	**40**			dB
$NPSR_X$	Negative Power Supply Rejection, Transmit	Input Level = 0V, V_{BB} = −5.0 V_{DC} +300 mVrms, f = 1.02 kHz	**50**			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	D_R = Steady PCM Code, V_{BB} = −5.0 V_{DC} + 300 mVrms, f = 1.02 kHz	**45**			dB
CT_{XR}	Transmit to Receive Crosstalk	D_R = Steady PCM Code			**−75**	dB
CT_{RX}	Receive to Transmit Crosswalk	Transmit Input Level = 0V TP5116A TP5156A			 **−70** **−65** (Note 2)	 dB dB

Note 1: Measured by extrapolation from the distortion test result at −50 dBm0 level.

Note 2: Theoretical worst-case for a perfectly zeroed encoder with alternating sign bit, due to the decoding law.

Timing Specifications

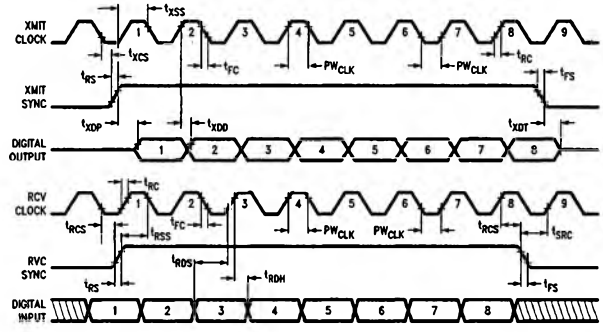
Unless otherwise noted, T_A = 0°C to 70°C, V^+ = +5V±5%, V^- = −5V ± 5%. All digital signals are referenced to DIGITAL GROUND and are measured at V_{IH} and V_{IL} as indicated in the Timing Waveforms. Limits printed in bold characters are guaranteed for V^+ = 5.0V ±5%, V^- = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All timing specifications measured at V_{OH} = 2.0V and V_{OL} = 0.7V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_M	MASTER CLOCK Frequency		1.5	2.048	2.1	MHz
F_X, F_R	XMIT, RCV CLOCK Frequency		0.064	2.048	2.1	MHz
PW_{CLK}	Clock Pulse Width	MASTER, XMIT, RCV CLOCKS	150			ns
t_{RC}, t_{FC}	Clock Rise and Fall Time	MASTER, XMIT, RCV CLOCKS			50	ns
t_{RS}, t_{FS}	Sync Pulse Rise and Fall Time	RCV, XMIT, SYNC			50	ns
t_{RCS}, t_{XCS}	Clock to Sync Delay	RCV, XMIT	0			ns
t_{XSS}	XMIT SYNC Set-Up Time		150			ns
t_{XDD}	XMIT Data Delay	Load = 100 pF + 2 LSTTL Loads			200	ns
t_{XDP}	XMIT Data Present	Load = 100 pF + 2 LSTTL Loads			200	ns
t_{XDT}	XMIT Data TRI-STATE®				150	ns
t_{SRC}	RCV CLOCK to RCV SYNC Delay		0			ns
t_{RDS}	RCV Data Set-Up Time		0			ns
t_{RSS}	RCV SYNC Set-Up Time		150			ns
t_{RDH}	RCV Data Hold Time		100			ns
t_{XSL}	XMIT SYNC Low Time	64 kHz Operation	300			ns
t_{RSL}	RCV SYNC Low Time	64 kHz Operation	17			(Note 3)

Note 3: RCV SYNC must remain low for at least 17 cycles of MASTER CLOCK, each frame.

Timing Waveforms

72 kHz or Greater Operation



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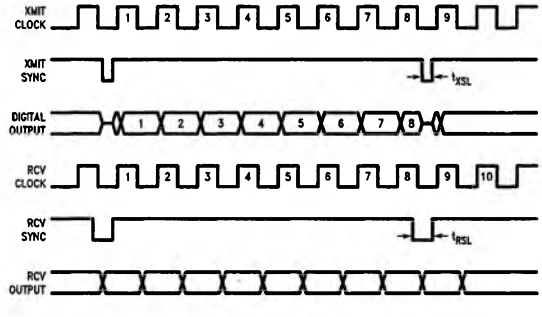
64 kHz Operation



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