National Semiconductor

PRELIMINARY

TP3460 ISDN R Interface USART

General Description

The TP3460 is a USART which, when connected to a control processor (running the appropriate software) with access to an ISDN B-channel, enables a standards compliant implementation of the CCITT V.110 (ECMA-102) and V.120 Terminal Adaption specifications for serial interface terminals. Conventional UART's and USART's do not comply with many of the requirements of these two standards.

Data rates up to 19.2 kbaud async and 64 kbaud sync are supported.

In asynchronous V.110 mode the TP3460 will compensate the input and output data bandwidths by inserting/deleting stop bits as required, thereby allowing the transmitting terminal to operate at up to 1% overspeed.

In other asynchronous protocols, e.g. V.120, the operation is similar to that of a normal UART where start/stop bits are removed and parity checked.

In synchronous V.110/V.120 modes where the terminal is not synchronous to the ISDN the TP3460, in conjunction with the V.110 software, provides a full implementation of Network Independent Clocking (NIC) to compensate for instantaneous phase differences between the two networks.

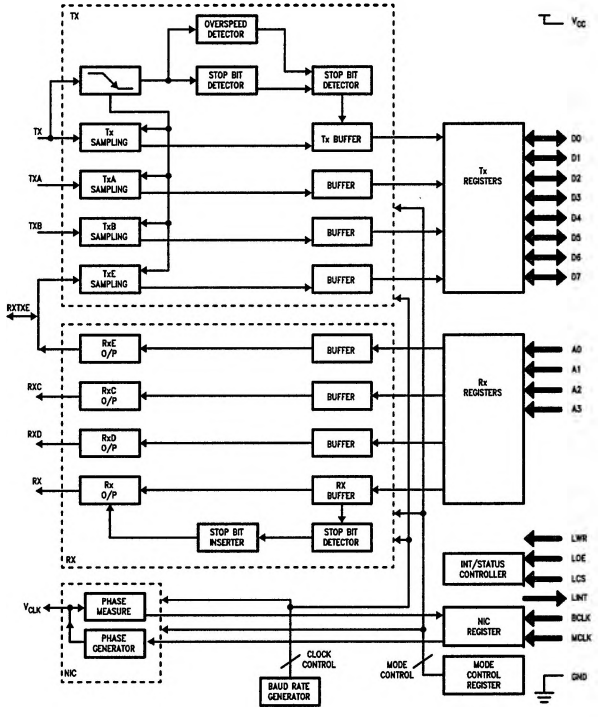
Features

- Full asynchronous and synchronous functions
- Correct V.110 (ECMA-102) start/stop bit processing
- V.110 Co-ordination of S and D bits
- V.120 compatibility
- Network independent clocking
- Asynchronous and synchronous speeds up to 19.2 kbaud
- Synchronous speeds of 48k, 56k and 64k supported
- Synchronous clock master or slave
- Demultiplexed microprocessor bus

Applications

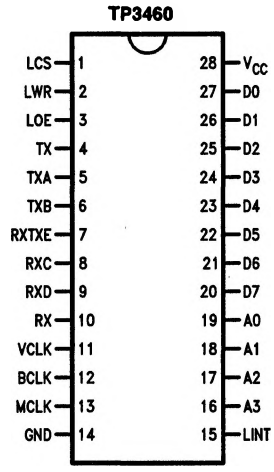
- Multi standard terminal adapters
- Integrated voice/data terminal
- Interworking units between ISDN and non-ISDN
- Host computer connection via Primary Rate Interface

Block Diagram



TL/H/10729–1

Pin Descriptions



TL/H/10729–2

Name	Description
GND	Negative power supply pin, normally 0V (ground). All signals are referenced to this pin.
V_{CC}	Positive power supply input, which must be 5V ± 5%.
D(7:0)	8-bit processor data input/output bus.
A(3:0)	4 address pins for the internal read/write registers.
LWR	This pin controls the direction of the transfer of data between the device and the data bus. When LWR and LCS are both low, the contents are written into the addressed register. When LWR is high and LCS is low a read operation has been selected, control of the data bus is then passed to LOE.
LCS	The chip is selected for a read/write operation when LCS (chip select) is low.
LOE	The output on D(7:0) is enabled when LOE is low.
LINT	Interrupt output, a latched output signal which is normally high-impedance, and goes low when the device requires the processor to service it. LINT will return to a high-impedance state on completion of a status register read.
MCLK	The Master clock input which is programmable to accept either 15–36 MHz or 7.68 MHz.
BCLK	This is the input for the ISDN clock and enables the internally generated baud clock to be synchronized to the ISDN. This clock must be a multiple of 256 kHz and be in the range 256 kHz to 4096 kHz.
Tx	Transmit data for the ISDN B channel via the control processor (receive data from the R-interface terminal). Has internal pull-up resistor to V_{CC}.
Rx	Receive data from the ISDN B channel via the control processor (transmit data to the R-interface terminal).
TxA	Input interchange circuit which is sampled at the same instant as Tx. Has internal pull-up resistor to V_{CC}.
TxB	Input interchange circuit which is sampled at the same instant as Tx. Has internal pull-up resistor to V_{CC}.
RxC	Output interchange circuit which is changed at the same instant as Rx.
RxD	Output interchange circuit which is changed at the same instant as Rx.
RxTxE	Interchange circuit which is selectable either as an output or an input. In both cases the sampling/change instant is identical to the other interchange circuits. Has internal pull-up resistor to V_{CC}.
VCLK	Clock input or output controlling the sampling/change instant for the synchronous applications. If VCLK is programmed as an output then it is synchronous with the BCLK input. Has internal pull-up resistor to V_{CC}.

Functional Description

ASYNCHRONOUS SERIAL INTERFACE

Asynchronous V.110

In V.110 mode (selected via the Mode A Register) the TP3460 functions as the RA0 block. The asynchronous transmitter sets up a virtually transparent path between the Serial Interface and the processor, with the transmitter continually sampling Tx data at the baud rate. The samples (stop and start bits are treated as normal data) are loaded serially into an eight bit buffer.

The sample instant is set to be at the 50% point of a bit. On the start bit edge of each character, the sample point is reset (to ensure accurate sampling).

When the incoming data is running at up to 1% overspeed the TP3460 will delete stop bits (as required), up to a maximum of one out of eight, thus keeping the data rate to the processor at the nominal baud rate.

The receiver reverses the process and monitors the incoming Rx data from the processor to look for missing stop bits. If a missing stop bit is detected then the receiver inserts a stop bit of width $^7/_8$ and reduces the next seven stop bits by $^1/_8$, thereby equalizing the input/output bandwidth.

There is no requirement for parity bits to be checked in V.110, however if a parity bit is present then it must be indicated in the Mode A Register so the device can calculate the correct character length.

Asynchronous Non-V.110 Mode

When the TP3460 is used for rate adaption with protocols other than V.110, e.g., V.120, the TP3460 performs as a standard UART. The Asynchronous transmitter strips off the start/stop bits and, for eight bit data, parity can be checked. The character and any parity error are then made available to the processor. The receiver adds on the start/stop bits and regenerates the parity or parity error as required. For seven bit data with parity the parity is not checked but is passed on with the seven data bits in data register.

BREAK DETECTION/GENERATION

V.110 Break Detection

In V.110 the data received on the Tx pin is checked for the presence of a break signal. A break signal is defined as a string of zeroes of length ≥ M where M is the number of bits in the character. The break signal is then conditioned so that the minimum length of break which is passed to the ISDN (V.110 frame) is 2M + 3 zeroes. If the break signal on the TX pin is of length greater than 2M + 3 bits then the whole length of the break signal is passed to the ISDN. The receiver TA should in theory take no action on the break signal, and pass the 2M + 3 zeroes unchanged. However the possibility exists where the receiver TA believes the beginning of the break is a null character with its stop bit deleted. The TA will then insert a stop, creating a null character and shortening the break signal to ≥ M + 4; the break signal however is still greater than the minimum break signal and will be recognized by the receiving terminal.

V.120 Break Detection/Generation

In V.120 the data received on the Tx pin is checked for the presence of a break signal. A break signal is defined as a string of zeroes of length ≥ M where M is the number of bits in the character. The detection of the break generates an interrupt with a Status Register bit signaling the detection (txbrk). The μP should set the Break bit in the frame sent to the ISDN so that the receiver can be instructed to regenerated the break. The TP3460 receiver can be made to generate a break by setting the rxbrk bit in the Par_data Register, upon which the receiver generates a break of 27 zeroes followed by 27 one's. The rxbrk bit is reset automatically by the device.

Interchange Lines

V.110 Interchange Lines

The register structure of the interchange lines is similar to that of the Rx/Tx Data Register. This allows bit-for-bit mapping of transitions on the interchange lines with the data lines, as called for in V.110. However, apart from sampling/clocking at the same time intervals as the Rx/Tx Data Registers, no further manipulation is carried out.

V.120 Interchange Lines

In V.120 mode the interchange circuits behave similarly to those of a UART. Any transition on the Tx Interchange circuits will generate an interrupt. The state of the Tx Interchange lines can be read at any time by reading the Tx_intch Register, and the state of the Rx Interchange lines can be changed at any time by writing to the Rx_intch Register.

SYNCHRONOUS SERIAL INTERFACE

Synchronous V.110/V.120

The operation of the synchronous mode is identical to the asynchronous mode in the way that data is interfaced to the processor. The main difference is that the data I/O is clocked in/out on the clock edges of VCLK. In the synchronous mode, data is transmitted towards the V.24/X.21 interface on the falling edge of VCLK and received on the rising edge of VCLK. In terms of how the data is handled there is no difference between V.110 and V.120, these modes only differ in how the data is presented to the μP. Start bit alignment, stop bit deletion and parity checker do not operate in the synchronous mode.

Master/Slave Clocking

The TP3460 can operate as the receiver or the generator of the data clock. In V.110 mode Network Independent Clocking (NIC) is available to synchronize near and far end clocks. In V.120 the NIC circuit is also available to provide a means of data rate equalization (method not fully defined in V.120).

Network Independent Clocking (NIC)

NIC In V.110

NIC is used when synchronous data signals are received which are not synchronized to the ISDN. In order that both near and far end signals can operate (but asynchronously with the ISDN) the following method is used to allow the passing of relative phase information to allow both near and far end clocks to synchronize themselves dynamically.

(i) The transmitting TA terminal clock (VCLK input) is compared to the ISDN clock, the relative phase is measured, the result is coded into 5% segments and passed to the control processor in PHASE (4:0) bits in the Nic_data Register.

(ii) The processor encodes these 5% segments into 20% increments and inserts them into the 80-bit frame (negative/positive compensation).

(iii) The far end receiving TA decodes the phase shift back to 5% segments and writes this to the TP3460 in PHASE (4:0) bits of the Nic_data Register. The TP3460 then regenerates the output VCLK by comparing it to the ISDN clock and producing the required phase shifted output.

NIC In V.120

The method of clock synchronization in V.120 synchronous modes is not fully defined but is based on monitoring the level to which the receive buffers (μP) are filled and comparing that to the transmit buffers. If both are synchronized then the buffers should fill to precisely the same level, any difference will provide an indication of how much the clock rate should be adjusted. This adjustment can be accomplished by making repeated small adjustments in the phase of the clock (which is derived from the ISDN clock) by using the NIC circuitry.

BAUD RATES

The TP3460 expects the MCLK input to be 15.36 MHz or 7.68 MHz as programmed in the Mode C register, from which it derives the standard baud rates. The appropriate baud rate is selected via Mode B Register from the selection in Table I.

TABLE I. Baud Rates

Baud Rate	Asynchronous	Synchronous	NIC
75	Yes	No	No
150	Yes	No	No
300	Yes	No	No
600	Yes	Yes	Yes
1.2k	Yes	Yes	Yes
2.4k	Yes	Yes	Yes
4.8k	Yes	Yes	Yes
9.6k	Yes	Yes	Yes
12k	Yes	No	No
19.2k	Yes	Yes	Yes
48k	No	Yes	No
56k	No	Yes	No
64k	No	Yes	No

PROCESSOR PARALLEL INTERFACE

The processor interface consists of eight TRI-STATE® bidirectional data lines (D0–D7), four address lines (A0–A3), a read/write control line (LWR), an output enable (LOE), a chip select (LCS) and an interrupt output (LINT). Control of the data lines is defined in Table II.

TABLE II. Processor Control Pins

Mode	LWR	LCS	LOE	I/O
Write	0	0	0	D_{IN}
Write	0	0	1	D_{IN}
—	0	1	0	Hi-Z
—	0	1	1	Hi-Z
Read	1	0	0	D_{OUT}
—	1	0	1	Hi-Z
—	1	1	0	Hi-Z
—	1	1	1	Hi-Z

INTERRUPT GENERATOR

The TP3460 provides a means of signaling to the μP (via LINT and the status register) that its buffers are full/empty and requires service from the μP.

The LINT pin is an open-drain output which goes low when the device requires service. The open-drain output means that several devices can be wired-or and use the same interrupt port, the processor must read the Status Register for confirmation that it was the TP3460 that had generated the interrupt.

If the μP fails to start or complete its service routine for the TP3460 then one or all of the data registers will have been over/under written. There are two flags in the Status Register (txovw, rxunw) to indicate that this has happened.

Depending on the mode of operation, the read of the Status Register (following an interrupt) will signal different actions. In all modes, reading of the Status Register will cause the cancellation of the interrupt.

V.110 Interrupts

In V.110 mode, on reading the Status Register, the **devrdy** flag (device ready) will be set. The status flags of the device can also be read at this point. When the device is ready, the μP can write/read to all data, interchange and NIC registers (or a subset). The μP has up to eight sampled data bits (R-Interface) of time to service the interrupt before the registers will be updated/emptied again.

V.110 Idle Mode

Due to the constant interrupt rate generated in V.110 mode, regardless of the useful data content that is being handled, an idle mode has been included. Idle mode is entered by the device when data on the Tx lines is unchanging and the μP has stopped writing to the Rx Registers (because of unchanging nature of the data being received). The device first flags that it is going to enter idle mode through the Status Register, and if conditions remain unchanged will then cease to generate interrupts. Idle mode is exited by any change on the Tx data lines or a write to any Rx Register. Idle mode operates in V.110 asynchronous mode only. Idle mode can be inhibited via the Mode C register.

V.120 Mode

Unlike V.110, which has only one source of interrupts, V.120 has four. In this manner V.120 behaves very much like a normal UART. The four interrupts are:

(i) **txrdy** A Tx character has been received and is ready to be read.

(ii) **rxrdy** The Rx buffer is empty and ready for another character.

(iii) **intrdy** A Tx interchange circuit has changed state.

(iv) **txbrk** A break signal is present on Tx.

All these interrupts are independent and can occur in any combination. If, however, an interrupt becomes pending while another is being serviced then it is held off until the status register is read and the LINT pin returns to the high impedance state.

REGISTERS

The register organization of the TP3460 is divided into two separate areas, namely the data and control/status. Depending on whether **V.110** or **V.120** mode has been selected, the registers have **dual** meanings.

V.110 Registers

Hex Address	Register	Read/Write
0	Tx_data	Read
1	Rx_data	Read/Write
2	Tx_A	Read
3	Tx_B	Read
4	Rx_C	Read/Write
5	Rx_D	Read/Write
6	Rxtx_E	Read/Write
7	Nic_data	Read/Write
8	Mode_A	Read/Write
9	Mode_B	Read/Write
A	Mode_C	Read/Write
B	Status	Read
F	Mode_D	Read/Write

Tx_data

tx7	tx6	tx5	tx4	tx3	tx2	tx1	tx0

Rx_data

rx7	rx6	rx5	rx4	rx3	rx2	rx1	rx0

Tx_A

txa7	txa6	txa5	txa4	txa3	txa2	txa1	txa0

Tx_B

txb7	txb6	txb5	txb4	txb3	txb2	txb1	txb0

Rx_C

vxc7	vxc6	vxc5	vxc4	vxc3	vxc2	vxc1	vxc0

Rx_D

vxd7	vxd6	vxd5	vxd4	vxd3	vxd2	vxd1	vxd0

Rxtx_e

rxtxe7	rxtxe6	rxtxe5	rxtxe4	rxtxe3	rxtxe2	rxtxe1	rxtxe0

Nic_data

0	0	0	phse4	phse3	phse2	phse1	phse0

Mode_A

lv110	lasync	vmode	data1	data0	parity	polarity	stop

Mode_B

div3	div2	div1	div0	baud3	baud2	baud1	baud0

Mode_C

int	iidle	edir	isbd	isbi	iiovw	iiunw	msel

Mode_D

den	reset	0	0	0	0	loop2	loop1

Status

devrdy	intp	0	txbrk	txica	rxica	txovw	rxunw

V.120 Registers

Hex Address	Register	Read/Write
0	Tx_data	Read
1	Rx_data	Read/Write
2	Tx_intch	Read
3	—	—
4	Rx_intch	Read/Write
5	—	—
6	—	—
7	Par_data	Read/Write
8	Mode_A	Read/Write
9	Mode_B	Read/Write
A	Mode_C	Read/Write
B	Status	Read
F	Mode_D	Read/Write

Tx_data

tx7	tx6	tx5	tx4	tx3	tx2	tx1	tx0

Rx_data

rx7	rx6	rx5	rx4	rx3	rx2	rx1	rx0

Tx_intch

1	1	1	1	1	rxtxe	txb	txa

Rx_intch

0	0	0	0	0	rxtxe	rxd	rxc

Par_data

rxparem	rxbrk	0	phse4	phse3	phse2	phse1	phse0

Mode_A

lv110	lasync	vmode	data1	data0	parity	polarity	stop

Mode_B

div3	div2	div1	div0	baud3	baud2	baud1	baud0

Mode_C

int	0	edir	0	0	0	0	msel

Mode_D

den	reset	0	0	0	0	loop2	loop1

Status

txrdy	rxrdy	intrdy	txbrk	txica	0	txovw	txparerr

Control and Status Registers

Mode_A

msb							lsb
lv110	lasync	vmode	data1	data0	parity	polarity	stop

lv110 Sets the device into either V.110 or V.120 mode.

lv110	Mode
0	V.110
1	V.120

lasync Sets the device into either asynchronous or synchronous mode.

lasync	Mode
0	Asynchronous
1	Synchronous

vmode Defines whether the VCLK pin is a slave of timing (input) or a master of timing (output).

vmode	Mode
0	Input VCLK
1	Output VCLK

data (1:0) Sets the number of data bits in an asynchronous character.

data1	data0	Number of Data Bits
0	0	7
0	1	8
1	0	9*
1	1	—

*Option only valid for V.110 Mode

parity For parity to be selected, the parity bit must be set high.

parity	Mode
0	No Parity
1	Parity

For V.110 mode, the parity bit is only used to determine the number of bits in an asynchronous character.

In the V.120 mode, the Tx circuitry will carry out a parity check and flag any parity error in the Status Register. In the Rx circuitry, a parity bit will be generated which can be transformed to a parity error by setting the rxparerr bit in the Par_data Register. Parity is checked/generated only when there are eight data bits. In the seven data bit case the parity bit is passed to the μP in the Tx_data Register.

polarity Sets the polarity of the parity bit for V.120 mode. (The polarity is not required for the V.110 mode).

polarity	
0	Odd
1	Even

stop Defines the number of stop bits in an asynchronous character.

stop	Number of Stop Bits
0	1
1	2

Mode_B

msb							lsb
div3	div2	div1	div0	baud3	baud2	baud1	baud0

div (3:0) In the synchronous mode, the internal circuitry needs a 256 kHz reference clock. This reference is taken from a divided down BCLK. Div(3:0) sets the divisor of BCLK to generate the 256 kHz reference clock, e.g., if BCLK is 1024 kHz then div(3:0) should be set for a divisor of 4.

div3	div2	div1	div0	divisor
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

baud(3:0) The R-interface baud rate is set by baud(3:0).

baud3	baud2	baud1	baud0	rate
0	0	0	0	75*
0	0	0	1	150*
0	0	1	0	300*
0	0	1	1	12k*
0	1	0	0	600~
0	1	0	1	1.2k~
0	1	1	0	2.4k~
0	1	1	1	4.8k~
1	0	0	0	9.6k~
1	0	0	1	19.2k~
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	48k^
1	1	1	0	56k^
1	1	1	1	64k^

*Asynchronous mode only
^ Synchronous mode only
~Synchronous and asynchronous modes

Mode_C

msb							lsb
int	iidle	edir	isbd	isbi	iiovw	iiunw	msel

int If int is set, then the TP3460 can be a source of interrupts. It int is low then the interrupt control effectively passes to the iidle bit in the Mode_C Register.

iidle The iidle bit will select the idle mode when low. The idle mode will inhibit interrupts when all the data registers are quiet i.e., the Tx input lines have not changed state for 24 user bits (3 successive interrupts) and the μP has stopped updating the Rx Registers. The iintp (Status Register) bit will then be set indicating that the conditions for idle have been met. If no action is taken by the μP before the point when the next interrupt is due, then the interrupt (and all subsequent interrupts) are turned off. However if at any time data starts changing on the Tx lines or the μP writes to one of the Rx registers then the device will automatically come out of idle mode and start to generate interrupts.

The idle mode does not operate in V.120. Consequently, iidle has no function and the int bit then determines if interrupts are generated.

int	iidle	State
0	0	Turn off interrupts but if data active turn on
0	1	Turn off interrupts
1	0	Interrupts enabled
1	1	Interrupts enabled

edir edir controls whether the interchange pin RxTxE acts as an output or an input.

edir	State
0	Input
1	Output

isbd When this bit is set, the stop bit deletion mechanism (asynchronous mode, Tx direction) is inhibited. If overspeed occurs in the Tx data then a stop bit is deleted immediately without ensuring that it meets the criteria set down in V.110. Isbd operates in V.110 mode only.

isbi When this bit is set, the stop bit insertion (asynchronous mode, Rx direction) is inhibited. Isbi operates in V.110 mode only.

iiovw Inhibit interchange overwrite, iiovw, controls whether an overwrite of the Tx interchange registers will cause the txovw flag in the Status Register to be set, e.g., if the Tx_A Register contains 8 bits which have not been read by the control processor and is overwritten by the transmitter then txovw will be set. Iiovw operates in V.110 mode only.

iiunw Inhibit interchange underwrite, iiunw, controls whether an underwrite of the Tx interchange registers will cause the rxunw flag in the Status Register to be set, e.g., if the device loads the Rxd driver from the Rx_D Register and there has been no control processor write since the previous Rx load then the rxunw bit will be set. Iiunw operates in V.110 mode only.

msel When this bit is set test modes are enabled but not activated.

Mode_D

By setting the den bit in the Mode_D Register, additional control bits become accessible to the μP.

Mode_D behaves like a normal register and can be seen as an extension of the mode registers, its function is to provide additional monitoring functions.

When the den bit is reset all Mode_D functions are automatically terminated.

msb							lsb
den	reset	0	0	0	0	loop2	loop1

den When this bit is set, the other bits in the Mode_D register are enabled.

reset If set, the device will be reset to the power up state, including all μP registers and will force exit from all test modes.

loop2 If set, RX is looped back to TX at R-interface.

loop1 If set, TX is looped back to RX at R-interface.

Status Register in V.110 Mode

msb							lsb
devrdy	iintp	0	txbrk	txica	rxica	txovw	rxunw

devrdy When set, the TP3460 is ready to have its Tx Registers read and its Rx Registers written to. When this flag is set an interrupt is generated. Reading the Status Register will clear the device ready flag and return LINT to the high impedance state.

iintp An inhibit of interrupts is pending. Unless a Tx data change or an Rx Register write operation is carried out before the next interrupt is due, interrupts will be inhibited and the device will go into idle mode.

txbrk Transmitter break of ≥ M bits has been detected. The break detector is only active in asynchronous mode. M = number of bits in a character.

txica The Tx circuitry has lost character alignment due to receiving an incorrectly framed character, i.e., after synchronizing to a start bit edge the start bit failed to validate at the 50% sampling point or the stop bit was not validated (or both). Txica operates in asynchronous mode only.

rxica The Rx circuitry has lost character alignment due to receiving an incorrectly framed character, i.e., a stop bit is missing which does not conform to the criteria defined in V.110 (1 of 8). Rxica operates in asynchronous mode only.

txovw One of the transmit registers has been overwritten.

rxunw An underwrite has occurred in one of the Rx registers.

Status Register in V.120 Mode

msb							lsb
txrdy	rxrdy	intrdy	txbrk	txica	0	txovw	txparerr

txrdy The transmitter has a character ready to be read by the processor.

rxrdy The receiver is ready to send another character.

intrdy One of the Tx interchange circuits has changed state.

txbrk A break signal has been received by the transmitter.

txica The Tx circuitry has lost character alignment due to receiving an incorrectly framed character, i.e., after synchronizing to a start bit edge the start bit failed to validate at the 50% sampling point or the stop bit was not validated (or both). Txica operates in asynchronous mode only.

txovw One of the transmit registers has been overwritten.

txparerr Input transmit character has a parity error.

V.110 Data Registers

Tx_Data

msb							lsb
tx7	tx6	tx5	tx4	tx3	tx2	tx1	tx0

tx(7:0) Contains the last 8 samples from the Tx input pin.

Rx_Data

msb							lsb
rx7	rx6	rx5	rx4	rx3	rx2	rx1	rx0

rx(7:0) Contains the next 8 samples to be output Rx pin.

Tx_A

msb							lsb
txa7	txa6	txa5	txa4	txa3	txa2	txa1	txa0

txa(7:0) Contains the last 8 samples from the interchange input pin TxA. (Sampled at the same instant as Tx.)

Tx_B

msb							lsb
txb7	txb6	txb5	txb4	txb3	txb2	txb1	txb0

txb(7:0) Contains the last 8 samples from the interchange input pin TxB. (Sampled at the same instant as Tx.)

Rx_C

msb							lsb
rxc7	rxc6	rxc5	rxc4	rxc3	rxc2	rxc1	rxc0

rxc(7:0) Contains the next eight bits to be output on the RxC interchange pin. (Output at same instant as Rx.)

Rx_D

msb							lsb
rxd7	rxd6	rxd5	rxd4	rxd3	rxd2	rxd1	rxd0

rxd(7:0) Contains the next eight bits to be output on the RxD interchange pin. (Output at same instant as Rx.)

RxTx_E

msb							lsb
rxtxe7	rxtxe6	rxtxe5	rxtxe4	rxtxe3	rxtxe2	rxtxe1	rxtxe0

rxtxe(7:0) Depending on whether the RxTxE pin has been selected as an input or an output, it contains input data that has been received or is to be transmitted on the RxTxE pin.

Nic_data

msb							lsb
0	0	0	phse4	phse3	phse2	phse1	phse0

phse(4:0) If VCLK is configured as an acceptor of timing (input) then phse(4:0) contains the absolute phase measured between the reference (derived from BCLK) and VCLK in 5% increments. The range of output 0–19 gives a 0% to 95% phase measurement range.

If VCLK is configured as a generator of timing (output) then phse(4:0) must contain the required absolute phase shift in 5% increments. The range of the output 0–19 gives a 0% to 95% phase adjustment. If the input value of phse (4:0) exceeds 19 then the device will generate a phase shift of 95%. The maximum phase jump which can be handled by the NIC circuitry is 25%.

V.120 Data Registers

Tx_data

msb							lsb
tx7	tx6	tx5	tx4	tx3	tx2	tx1	tx0

tx(7:0) Contains the data bits of the last character received on Tx pin.

Rx_data

msb							lsb
rx7	rx6	rx5	rx4	rx3	rx2	rx1	rx0

rx(7:0) Contains the data bits of the next character to be output on the Rx pin.

Tx_intch

msb							lsb
1	1	1	1	1	rxtxe	txb	txa

rxtxe Status of interchange circuit RxTxE.

txb Status of interchange circuit pin TxB.

txa Status of interchange circuit pin TxA.

Rx_intch

msb							lsb
0	0	0	0	0	rxtxe	rxd	rxc

rxtxe The output value of the RxTxE pin. This is only valid when RxTxE is in the output mode, if it is in input mode then the value of RxTxE is ignored.

rxd The output value of the interchange RxD pin.

rxc The output value of the interchange RxC pin.

Par_data

msb							lsb
rxparerr	rxbrk	0	phse4	phse3	phse2	phse1	phse0

rxparerr When active, a parity error is forced in the next Rx character. This bit is reset after each character has been output.

rxbrk When high, the Rx pin is forced to a low for 27 bits after which Rx is forced high for 27 bits. This bit is then reset after the break signal has been output.

phse(4:0) If VCLK is configured as a slave of timing (input) then phse(4:0) contains the absolute phase measured between the reference (derived from BCLK and VCLK) in 5% increments. The range of output 0–19 gives a 0% to 95% phase measurement range.

If VCLK is configured as a master of timing (output) then phse (4:0) in the range 0–19 causes a phase adjustment from 0% to 95% in 5% increments. If the input value of phse(4:0) exceeds 19 then the device will generate a phase shift of 95%. The maximum phase jump which can be handled by the NIC circuitry in a single adjustment is 25%.

POWER ON RESET

The TP3460 has an on-chip Power On Reset (POR) circuit. The POR ensures that all the registers and counters power up correctly into a valid known state. To ensure the POR circuit operates correctly the rise time of the Power Supply (V_{CC}) with respect to GND should not be greater than 10 ms.

The POR states of the μP Registers are:

Address	Register	POR State
0	Tx_data	FF (Hex)
1	Rx_data	FF
2	Tx_a	FF
3	Tx_b	FF
4	Rx_c	FF
5	Rx_d	FF
6	RxTx_e	FF
7	Nic_data	00
8	Mode_a	00
9	Mode_c	00
A	Mode_c	00
B	Status	00
F	Mode_D	00

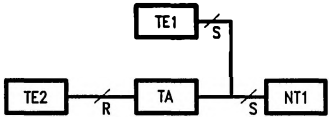
SUMMARY OF V.110/V.120 DIFFERENCES

Parameter	V.110	V.120
Interrupt Sources	devrdy	txrdy rxrdy intrdy txbrk
Stop Bits (async)	Tx: Delete single bit when overspeed Rx: If missing, insert 7/8 Stop Bit and reduce next 7 Stop Bits to 7/8	Tx: Always delete Rx: Always insert
Start Bit (Async)	No alteration	Tx: Always delete Rx: Always insert
Parity (async)	Only required to calculate number of bits in character	Tx: Check Parity, flag if error Rx: Calculate Parity, Forcing Parity Error if required
Data Bits (async)	Only required to calculate number of bits in character	Only required to calculate number of bits in character
Break (async)	Tx: Detect ≥ M Start Bits and force 2M + 3 Start Bits Rx: No alteration (may shorten by inserting Stop Bit)	Tx: Signal Break if Receive ≥ M 0's Rx: Transmit (to Terminal) 27 0's followed by 27 1's
Clocking (sync)	No change	No change

Applications Information

ISDN TERMINAL ADAPTER OVERVIEW

The CCITT reference model, *Figure 1*, illustrates the basic function of a terminal adapter i.e. to connect a non-ISDN terminal (a TE type 2) to the ISDN. V.110 and V.120 are the two CCITT recommended methods for Terminal Adaption.



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TE2: Non ISDN Terminal, i.e., V.24, X.21.

TA: Terminal Adapter

FIGURE 1. ISDN Reference Model

R-INTERFACE CONNECTIONS

DCE Mode

In the normal configuration, the terminal adapter is a DCE (Data Communicating Equipment). In this mode the TP3460 should be configured such that the RxTxE pin is an output. The recommended connection of the DCE interchange circuits is shown in *Figure 2*.

DTE Mode

In the case where the terminal adapter is connected to a modem (interworking), then the TP3460 should be configured as a DTE (Data Terminal Equipment) with the RxTxE pin as an input. The recommended connection of the DTE interchange circuits is shown in *Figure 3*.

V.110/ECMA-102 TERMINAL ADAPTION

The V.110 method interfaces a TE2 (V.24 or X.21) terminal to the ISDN by means of an 80-bit frame. The frame is connected into the B-channel octets in 4, 2 or 1-bit nibbles depending on the R interface rate. Both synchronous and asynchronous protocols are catered for by using the three stage rate adaption technique, *Figure 4*.

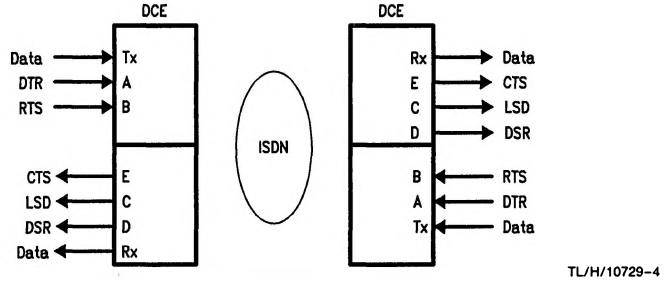

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FIGURE 2. DCE Interchange Connections

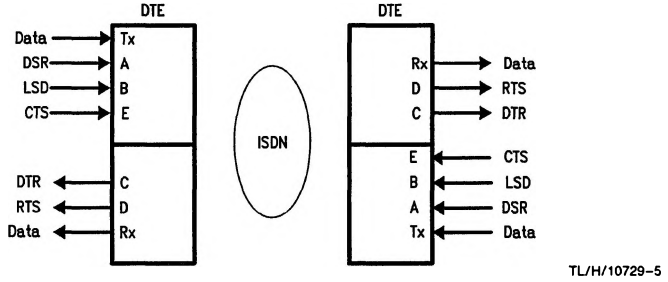

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FIGURE 3. DTE Interchange Connections

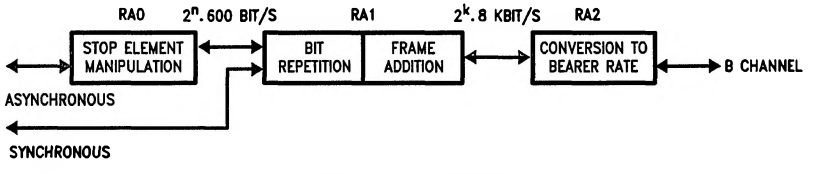

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FIGURE 4. V.110 Method

RA0

The RA0 function is only required for V.series interfaces and converts asynchronous user data into a synchronous rate of 2^n x 600 bit/s. The format of V.series asynchronous data is a START bit followed by a number of data bits and finally a STOP bit. Unlike a normal UART, RA0 treats START and STOP bits exactly the same as data except for the case of overspeed.

When the terminal is transmitting into the TA at up to 1% overspeed, the input buffers would eventually overflow because the input rate exceeds the output bandwidth. The RA0 detects this scenario and deletes up to one stop bit in every eight characters to equalize the bandwidths.

In the path towards the terminal, the RA0 must detect any valid missing stop bits and re-insert them. When a stop bit has been reinserted, RA0 has more data for the terminal than the user rate will allow. To balance the I/O rates, RA0 shortens the length of the stop bit by 1/8th of a bit for eight characters, thus eliminating the effect of the stop bit insertion. Apart from the overspeed case, RA0 makes no adjustment of the incoming/outgoing data.

RA1

RA1 takes synchronous user data from either the synchronous user interface or the RA0 output and loads it into the 80-bit frame as D-bits. In each 80-bit frame 48 bits are assigned to data and, depending on the user rate, repetition of data can occur. The remaining 32 bits of the frame contain:

(i) Frame alignment information

(ii) Clock speed and relative phasing information

(iii) Interchange circuit and flow control information

RA1 controls the sampling of the interchange circuits and ensures that the data and interchange circuit data retain their relative phase from the local R-Interface (terminal) to the remote R-Interface.

The output/input of RA1 is connected to RA2 and can be at 8k, 16k, or 32 kbits.

RA2

RA2 takes data from RA1 and loads it into the B-channel octet filling either 4, 2 or 1 per octet.

Intermediate Rate kbit/s	No. of Bits Occupied
8	1
16	2
32	4

Therefore, RA2 can multiplex up to 8 different TE's into one B-channel (at the 8 kbit/s intermediate rate).

V.120 TERMINAL ADAPTION

The V.120 method is to take the R-Interface data and convert it into modified LAPD frames using an HDLC protocol.

The Terminal Adaption method is divided into two general categories, protocol sensitive operation for character or message encapsulation and bit transparent operation.

Protocol Sensitive Operation (Asynchronous Mode)

In the direction towards the network, the start and stop bits are removed and parity may be checked. The stripped characters are buffered and transported in modified LAPD frames on a bearer channel. In the direction towards the Terminal, data is reformed into characters by the addition of start and stop bits.

Bit Transparent Operation (Synchronous Mode)

In Bit Transparent Operation the TA encapsulates the bits from the interface at the R-Interface point into V.120 frames as they are received, without modification. These frames are forwarded to a bearer channel. The peer TA removes the bits from the frames and sends them onto the R reference point. No processing or modification of the bits is performed and there is no checking for bit stream errors on the interface at the R reference point.

TERMINAL ADAPTER ARCHITECTURE

The Terminal Adapter utilizes existing TE1 architectures and consists of an ISDN USART (TP3460), a control processor with B-channel access (HPC16400) and an S Interface Device (TP3420). The overall system is shown in *Figure 5*.

A typical application circuit could be configured as shown in *Figure 6*.

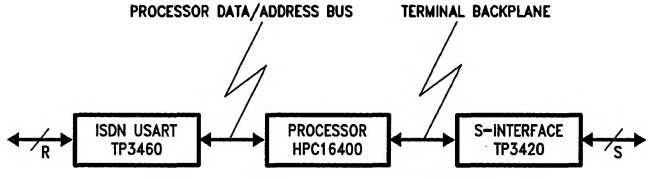

FIGURE 5. Terminal Adapter Architecture

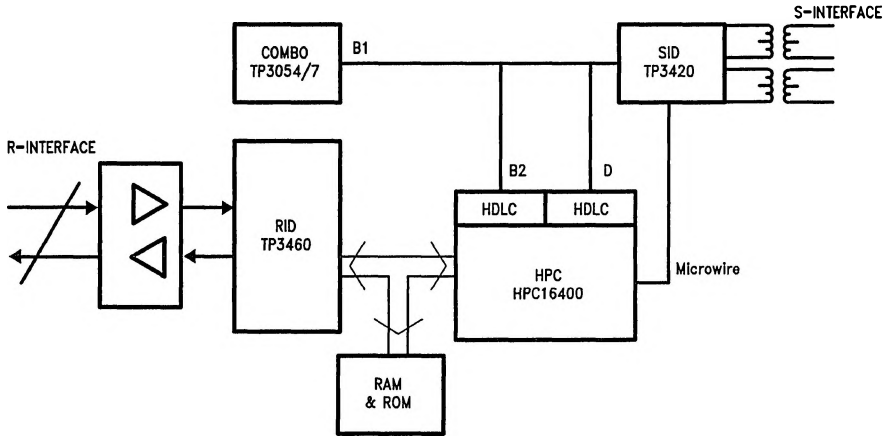

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FIGURE 6. Typical Application Circuit

V.110 Terminal Adapter

The V.110 TA operation is partitioned between the TP3460 and the control processor. The TP3460 functions are shown below with the remaining functions being assigned to the processor.

(i) RA0 including stop bit deletion/insertion
(ii) Tx and Rx sampling
(iii) Interchange circuit sampling with retention of relative phasing with data
(iv) Synchronous clock I/O
(v) Network Independent Clocking

V.120 Terminal Adapter

The V.120 TA operation is partitioned between the TP3460 and the control processor. The TP3460 functions are shown below with the remaining functions being assigned to the processor.

(i) Start/Stop bit removal
(ii) Tx and Rx sampling
(iii) Parity check/generation
(iv) Interchange circuit sampling
(v) Synchronous clock I/O
(vi) Use of NIC circuit to equalize data I/O rates (optional)

Device Electrical Specifications

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GND	7V
Input Voltage	$-0.3V$ to $V_{CC} + 0.3V$
Storage Temperature Range	$-65°C$ to $+150°C$
Lead Temperature (Soldering, 10 Sec.)	300°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, limits printed in **BOLD** characters are electrical testing limits at $V_{CC} = 5.0V$ and $T_A = 25°$. All other limits are design goals for $V_{CC} = 5.0V \pm 5\%$ and $T_A = 0$ to 70°C. This data sheet is still preliminary and parameter limits are not indicative of characterization data with respect to power supply or temperature variations. Please contact your National Semiconductor Sales Office for the most current product information.

Symbol	Parameter	Conditions	Limits		Units
			Min	Max	
V_{IL}	Input Low Voltage	All Inputs		0.8	V
V_{IH}	Input High Voltage	All Inputs	2.0		V
V_{OL}	Output Low Voltage	Rx, RxC, RxD, RxTxE, VCLK: $I_{OL} = 1$ mA, D(7:0), LINT: $I_{OL} = 2$ mA		0.4	V
V_{OH}	Output High Voltage	Rx, RxC, RxD, RxTxE VCLK: $I_{OH} = 1$ mA, D(7:0): $I_{OH} = 2$ mA	3.7		V
I_{IH}	High Level Input Current	All Inputs		10	μA
I_{IL}	Low Level Input Current	All except Tx, TxA, TxB, RxTxE, VCLK Tx, TxA, TxB, RxTxE, VCLK		−10 −150	μA μA
I_{OZ}	Output Curent in Hi-Z	D(7:0), LINT		±10	μA
I_{CC}	Dynamic Supply Current			7	mA

TIMING CHARACTERISTICS

Symbol	Parameter	Conditions	Typ	Limits		Units
				Min	Max	
f_{MCLK}	Master Clock Frequency	msel = 0	15.36			MHz
		msel = 1	7.68			
f_{BCLK}	Bit Clock Frequency	n x 256 where n = 1 to 16 as defined by div(3:0)		256	4096	kHz
t_{STR}	μP Strobe Width	When MCLK is 15.36 MHz		70		ns
		When MCLK is 7.68 MHz		140		
t_{SAS}	Address Setup Time			10		ns
t_{HSA}	Address Hold Time			10		ns
t_{SDS}	Data Setup Time			40		ns
t_{HDS}	Data Hold Time			10		ns
t_{DV}	Data Valid Delay				70	ns
t_{DZ}	Data TRI-STATE Delay				20	ns
t_{RV}	Rx Output Delay	Synchronous Mode Only			100	ns
t_{STV}	Tx Setup Time	Synchronous Mode Only		50		ns
t_{HTV}	Tx Hold Time	Synchronous Mode Only		50		ns

TIMING DIAGRAMS

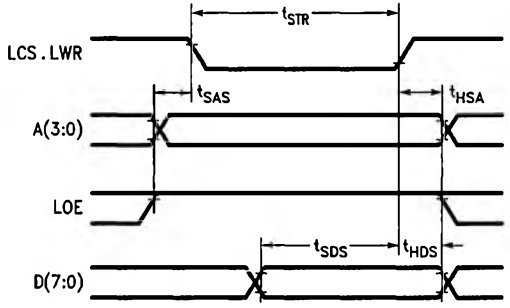

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FIGURE 7. μP Write Operation

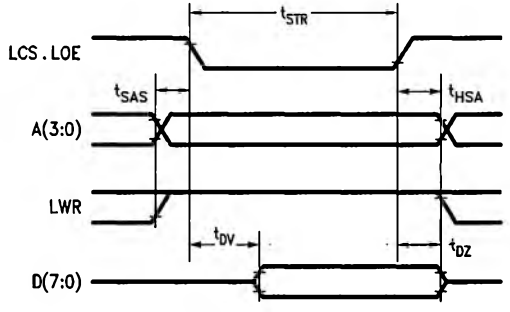

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FIGURE 8. μP Read Operation

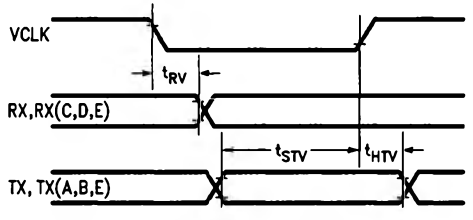

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FIGURE 9. Serial Interface