TMS320F2803x Piccolo Local Interconnect Network (LIN) Module

User's Guide

Literature Number: SPRUGE2B
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Read This First

This document describes the Local Interconnect Network (LIN) Module.

About This Manual

The TMS320C2000™ is part of the TMS320™ family.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h or with a leading 0x. For example, the following number is 40 hexadecimal (decimal 64): 40h or 0x40.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation

The following books describe the TMS320x28x and related support tools that are available on the TI website:

SPRS584 — TMS320F28032, TMS320F28033, TMS320F28034, TMS320F28035 Piccolo Microcontrollers Data Manual contains the pinout, signal descriptions, as well as electrical and timing specifications for the 2803x devices.

SPRZ295 — TMS320F28032, TMS320F28033, TMS320F28034, TMS320F28035 Piccolo MCU Silicon Errata describes known advisories on silicon and provides workarounds.

CPU User's Guides—

SPRU430 — TMS320C28x CPU and Instruction Set Reference Guide describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). It also describes emulation features available on these DSPs.

Peripheral Guides—

SPRUGL8 — TMS320x2803x Piccolo System Control and Interrupts Reference Guide describes the various interrupts and system control features of the 2803x microcontrollers (MCUs).

SPRU566 — TMS320x28xx, 28xxx DSP Peripheral Reference Guide describes the peripheral reference guides of the 28x digital signal processors (DSPs).

SPRUGO0 — TMS320x2803x Piccolo Boot ROM Reference Guide describes the purpose and features of the boot loader (factory-programmed boot-loading software) and provides examples of code. It also describes other contents of the device on-chip boot ROM and identifies where all of the information is located within that memory.

SPRUGE6 — TMS320x2803x Piccolo Control Law Accelerator (CLA) Reference Guide describes the operation of the Control Law Accelerator (CLA).

SPRUGE2 — TMS320x2803x Piccolo Local Interconnect Network (LIN) Module Reference Guide describes the operation of the Local Interconnect Network (LIN) Module.

SPRUFK8 — TMS320x2803x Piccolo Enhanced Quadrature Encoder Pulse (eQEP) Reference Guide describes the operation of the Enhanced Quadrature Encoder Pulse (eQEP) .

SPRUGL7 — TMS320x2803x Piccolo Enhanced Controller Area Network (eCAN) Reference Guide describes the operation of the Enhanced Controller Area Network (eCAN).

SPRUGE5 — TMS320x2802x, 2803x Piccolo Analog-to-Digital Converter (ADC) and Comparator Reference Guide describes how to configure and use the on-chip ADC module, which is a 12-bit pipelined ADC.

SPRUGE9 — TMS320x2802x, 2803x Piccolo Enhanced Pulse Width Modulator (ePWM) Module Reference Guide describes the main areas of the enhanced pulse width modulator that include digital motor control, switch mode power supply control, UPS (uninterruptible power supplies), and other forms of power conversion.

SPRUGE8 — TMS320x2802x, 2803x Piccolo High-Resolution Pulse Width Modulator (HRPWM) describes the operation of the high-resolution extension to the pulse width modulator (HRPWM).

SPRUGH1 — TMS320x2802x, 2803x Piccolo Serial Communications Interface (SCI) Reference Guide describes how to use the SCI.

SPRUFZ8 — TMS320x2802x, 2803x Piccolo Enhanced Capture (eCAP) Module Reference Guide describes the enhanced capture module. It includes the module description and registers.

SPRUG71 — TMS320x2802x, 2803x Piccolo Serial Peripheral Interface (SPI) Reference Guide describes the SPI - a high-speed synchronous serial input/output (I/O) port - that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmed bit-transfer rate.

SPRUFZ9 — TMS320x2802x, 2803x Piccolo Inter-Integrated Circuit (I2C) Reference Guide describes the features and operation of the inter-integrated circuit (I2C) module.

Tools Guides—

SPRU513 — TMS320C28x Assembly Language Tools v5.0.0 User's Guide describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

SPRU514 — TMS320C28x Optimizing C/C++ Compiler v5.0.0 User's Guide describes the TMS320C28x™ C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

SPRU608 — TMS320C28x Instruction Set Simulator Technical Overview describes the simulator, available within the Code Composer Studio for TMS320C2000 IDE, that simulates the instruction set of the C28x™ core.

Local Interconnect Network (LIN) Module

This document describes the buffered local interconnect network (BLIN) module. Since this module can also operate like a conventional serial communications interface (SCI) port, it is referred to as the SCI/BLIN module in this document. In the SCI (UART) mode, it is functionally compatible to the standalone SCI module in the TMS320x2803x device. However, since the SCI/BLIN module uses a different register/bit structure, code written for this module cannot be directly ported to the standalone SCI module and vice versa.

1 Introduction and Features

The SCI/BLIN is compliant to the LIN 2.0 protocol specified in the LIN Specification Package. This module uses the SCI as its core and augments the SCI's hardware features for LIN compatibility. This module can be configured to operate in either LIN mode or the SCI (UART) mode. The SCI mode is also referred to as *compatibility mode* in this document.

1.1 Purpose

The SCI/BLIN provides a communications structure at the hardware and software level. It provides a low-cost solution where the bandwidth and fault tolerance of a controller area network (CAN) are not required.

1.2 Features

The following are the features of the SCI/BLIN module:

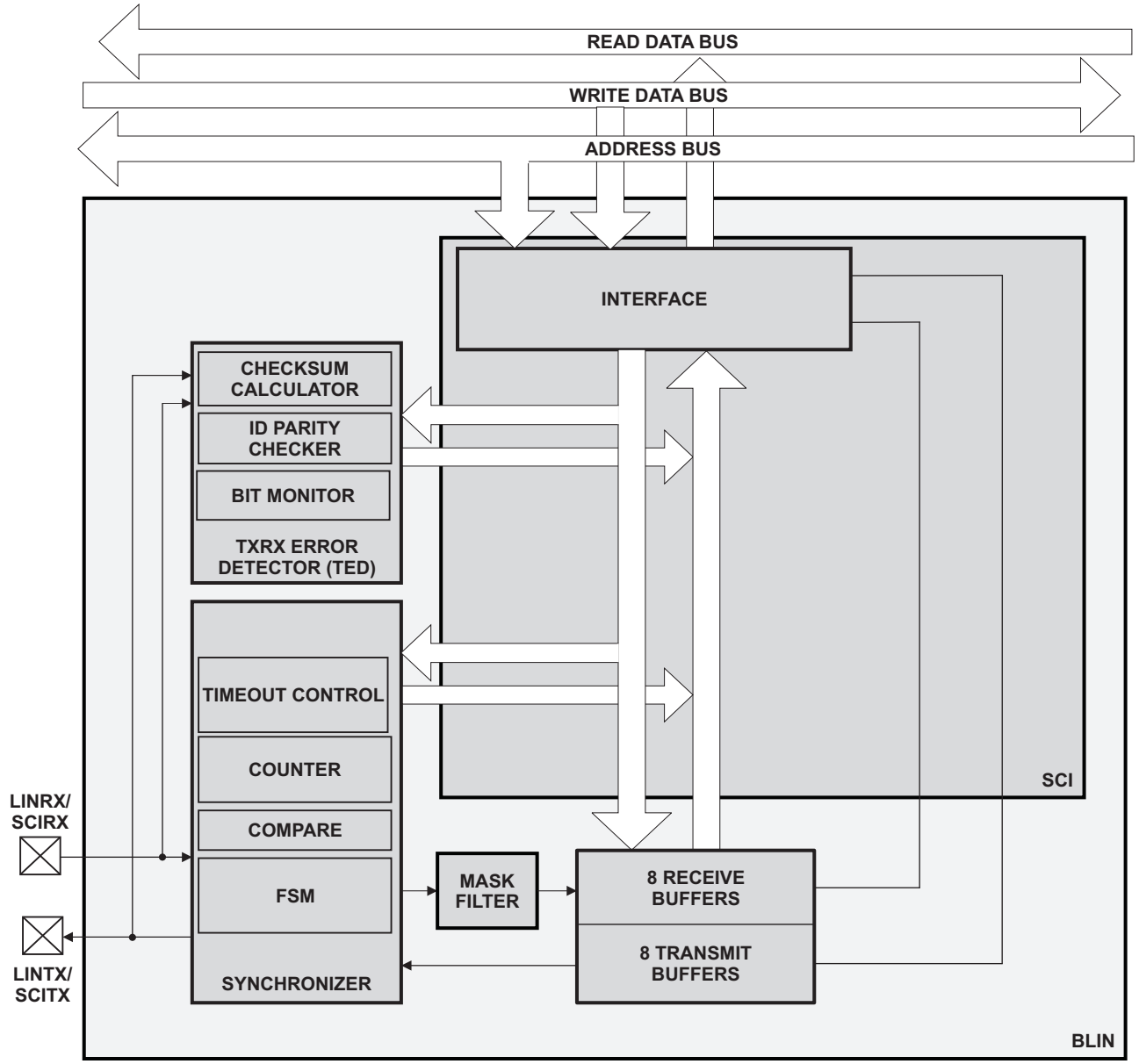
- Compatibility with LIN 1.3 or 2.0 protocols (LIN Specification Package 2002)
- Two external pins: LINRX and LINTX
- Functionally compatible with the standalone SCI of C2000 devices
- Multi-buffered receive and transmit units
- Identification masks for message filtering
- Automatic master header generation
  - Programmable synchronization break field
  - Synchronization field
  - Identifier field
- Slave automatic synchronization
  - Synchronization break detection
  - Optional baud rate update
  - Synchronization validation
- 2^{28} programmable transmission rates
- Wakeup on LINRX dominant level from transceiver
- Automatic wakeup support
  - Wakeup signal generation
  - Expiration times on wakeup signals
- Automatic bus idle detection
- Error detection
  - Bit error

  - Bus error
  - No-response error
  - Checksum error
  - Synchronization field error
  - Parity error
- 2 Interrupt lines with priority encoding for:
  - Receive
  - Transmit
  - ID, error, and status
- Support for LIN 2.0 checksum
- Enhanced synchronizer finite state machine (FSM) support for frame processing
- Enhanced handling of extended frames
- Enhanced baud rate generator

1.3 Block Diagram

The SCI/BLIN module is based on the SCI with the addition of an error detector (parity calculator, checksum calculator, and bit monitor), a mask filter, a synchronizer, and a multibuffered receiver and transmitter. The SCI interface and the baud generator are modified as part of the hardware enhancements for LIN compatibility. Figure 1 shows the SCI/BLIN block diagram.

Figure 1. SCI/BLIN Block Diagram



1.4 Standards

The LIN standard is based on the SCI (UART) serial data link format. The communication concept is single-master/multiple-slave with a message identification for multi-cast transmission between any network nodes.

For compatibility with LIN2.0 standard, the following additional features are implemented over LIN1.3:

(i) Support for LIN 2.0 checksum

(ii) Enhanced synchronizer FSM support for frame processing

(iii) Enhanced handling of extended frames

(iv) Enhanced baudrate generator

(v) Update wakeup/go to sleep

The SCI/BLIN module covers the CPU performance-consuming features, defined in the *LIN Specification Package* Revision 1.3 and 2.0 by hardware.

2 Operation

The SCI/BLIN module can be used in LIN mode or SCI (UART) mode. The enhancements for baud generation and additional receive/transmit buffers necessary for LIN mode operation are part of the enhanced buffered SCI/BLIN module.

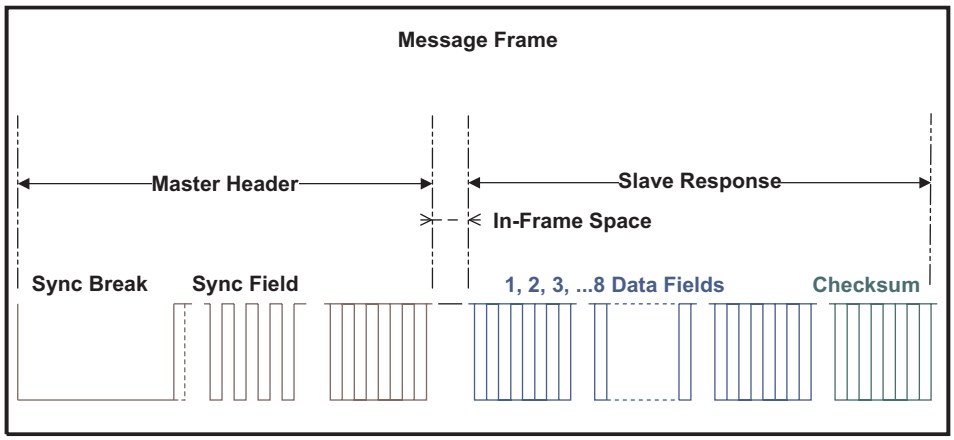
NOTE: To make a determination of the bit value, 16 samples for each bit are taken with majority vote on samples 8, 9, and 10.

For a detailed description of SCI/BLIN registers, see Section 6.

2.1 Message Frame

The LIN protocol defines a message frame format, illustrated in Figure 2. Each frame includes one master header, one response, one in-frame response space, and inter-byte spaces. In-frame-response and interbyte spaces may be 0.

Figure 2. LIN Protocol Message Frame Format: Master Header and Slave Response



There is no arbitration in the definition of the LIN protocol; therefore, multiple slave nodes responding to a header might be detected as an error.

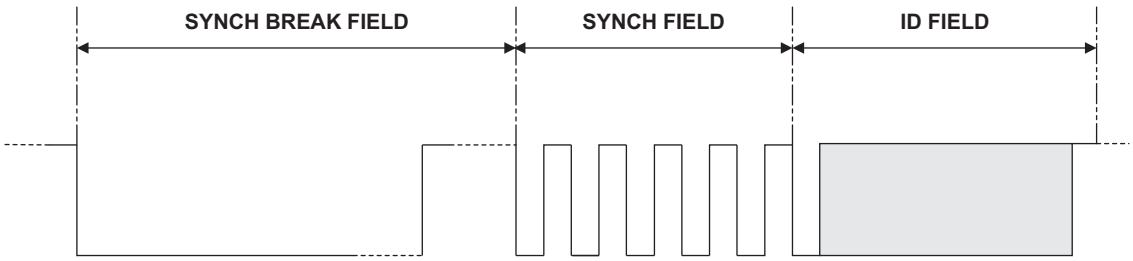
The LIN bus is a single channel wired-AND. The bus has a binary level: either dominant for a value of 0, or recessive for a value of 1.

2.1.1 Message Header

The header of a message is initiated by a master (see Figure 3) and consists of a three field-sequence:

- The synch break field signaling the beginning of a message
- The synch field conveying bit rate information of the LIN bus
- The ID field denoting the content of a message

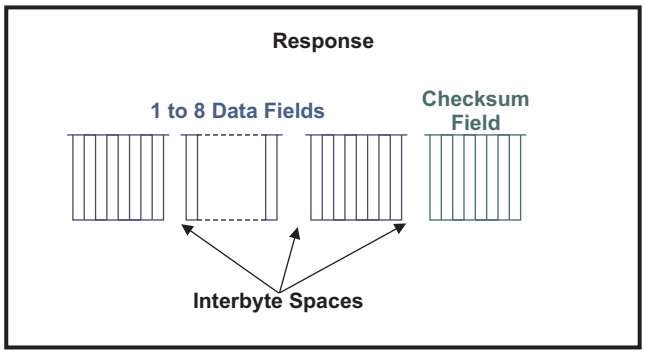
Figure 3. Header Fields: Synch Break, Synch, and ID



2.1.2 Response

The format of the response is as illustrated in Figure 4. There are two types of fields in a response: data and checksum. The data field consists of exactly one data byte, one start bit, and one stop bit, for a total of 10 bits. The LSB is transmitted first. The checksum field consists of one checksum byte, one start bit and one stop bit. The checksum byte is the inverted modulo-256 sum over all data bytes in the data fields of the response.

Figure 4. Response Format of LIN Message Frame



The format of the response is a stream of "N" data fields and one checksum field. Typically N is from 1 to 8, with the exception of the extended command frames. The length N of the response is indicated with the optional length control bits of the identifier, or by the SCIFORMAT(18–16) register (Section 6.11); see Table 1. The SCI/BLIN module supports response lengths from 1 to 8 bytes in compliance with LIN 2.0.

Table 1. Response Length with SCIFORMAT(18–16) Programming

SCIFORMAT (18–16)	No. of Bytes
000	1
001	2
010	3
011	4
100	5
101	6
110	7
111	8

2.2 Synchronizer

The synchronizer has three major functions in the messaging between master and slave nodes. It generates the master header data stream, it synchronizes to the LIN bus for responding, and it locally detects timeouts. A bit rate is programmed using the prescalers in the BRS register as indicated by the LIN_speed value in the LIN description file (LDF).

The SCI/BLIN synchronizer will perform the following functions: master header signal generation, slave detection and synchronization to message header with optional baud rate adjusting, response transmission timing and timeout control.

The SCI/BLIN synchronizer should be capable of detecting an incoming break and initialize communication at all times.

2.3 Baud Rate

The LIN module is clocked at a frequency of one-half the CPU clock (SYSCLKOUT). i.e. LIN Module input clock (LM_CLK) = SYSCLKOUT/2. For a 60 MHz device, LM_CLK = 30 MHz.

The transmission baud rate of any node is configured by the CPU in the beginning; this defines the bit time T_{bit}. The bit time is derived from the fields P and M in the baud rate selection register (BRSR; Section 6.12).

The ranges for the prescaler values in the BRSR are:

P = 0, 1, 2, 3, . . . , 2^{24} - 1

M = 0, 1, 2, . . . , 15

The BRSR with P and M values are user programmable. These divider values are automatically obtained in LIN mode (during header reception) when the synchronization field is measured, if the ADAPT bit is set. Otherwise, the P and M dividers could be used for both SCI mode and LIN mode to select a baud rate.

The LIN protocol defines baud rate boundaries as follows:

$$1kHz \leq F_{LINCLK} \leq 20kHZ$$

All transmitted bits are shifted in and out at T_{bit} periods.

2.3.1 Fractional Divider

The M field of the BRSR register (Section 6.12) modifies the integer prescaler P for finer tuning of the baud rate. The M value adds in increments of 1/16 of the P value.

Therefore, the LINCLK frequency is given by

$$\text{For all P other than 0, and all M, } T_{bit} = 16\left[P + 1 + \frac{M}{16}\right]T_{LM\_CLK}$$

$$\text{For } P = 0 : T_{bit} = 32T_{LM\_CLK}$$

Therefore, the LINCLK frequency is given by:

$$F_{LINCLK} = \frac{LM\_CLK}{16\left[P + 1 + \frac{M}{16}\right]}, \text{for all P other than zero}$$

$$F_{LINCLK} = \frac{LM\_CLK}{32}, \text{for } P = 0$$

NOTE: LM_CLK = 30 MHz, T_{LM_CLK} = 33.3 ns for a 60 MHz device.

2.4 Header Generation

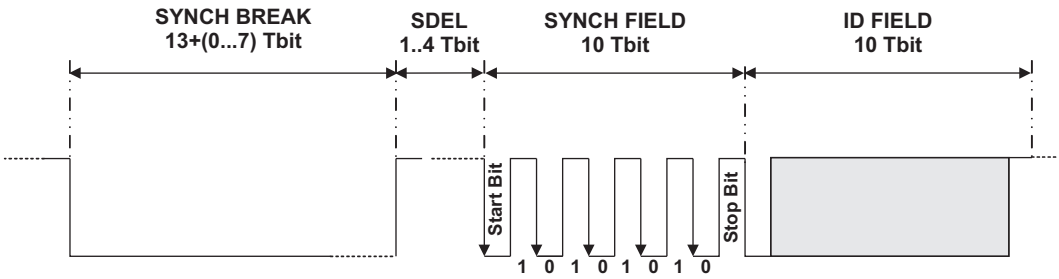
Automatic generation of the LIN protocol header data stream is supported without CPU interaction. The CPU will trigger a message header generation and the SCI/BLIN state machine will handle the generation itself. The header is always sent by the master to initiate a LIN communication and consists of three fields: synchronization break field, synchronization field, and identification field, as seen in Figure 5.

- The synchronization break field consists of two components.
  - The synchronization break (SYNCH BREAK) consists of a minimum of 13 (dominant) low bits to a maximum of 20 dominant bits. The synch break length may be extended from the minimum with the 3- bit SBREAK value in the LINCOMP register.
  - The synchronization break delimiter (SDEL) consists of a minimum of 1 (recessive) high bit to a maximum of 4 recessive bits. The delimiter marks the end of the synchronization break field. The synch break delimiter length depends on the 2-bit SDEL value in the LINCOMP register.
- The synchronization field (SYNCH FIELD) consists of one start bit, byte 0x55, and a stop bit. It is used to convey T_{bit} information and resynchronize LIN bus nodes.

- The identifier field's ID byte may use six bits as an identifier (optional length control within it), and two optional bits as parity of the identifier. The identifier parity is used and checked if the (SCIGCR1.2) PARITY enable bit is set. If length control bits are not used, then there can be a total of 64 identifiers plus parity. If neither length control or parity are used there can be up to 256 identifiers. See Figure 6 for an illustration of the ID field.

NOTE: The LIN protocol uses the parity bits in the identifier. The control length bits are optional to the LIN protocol.

Figure 5. Message Header in Terms of T_{bit}



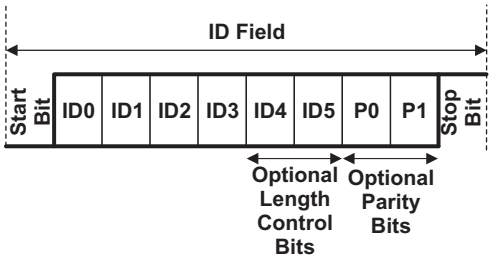
A master node initiates header generation on CPU writes to the IDBYTE in the LINID register (Section 6.19).

NOTE: IDBYTE [LINID(5–4); Section 6.19] conveys response length information if compliant to standards earlier than LIN 1.3.

ID5	ID4	Number of Data bytes
0	0	2
0	1	2
1	0	4
1	1	8

The SCIFORMAT register (Section 6.11) stores the length of the response for later versions of the LIN protocol.

Figure 6. ID Field



2.4.1 Event Triggered Frame Handling

The LIN 2.0 protocol uses event-triggered frames that may occasionally cause collisions. Event-triggered frames have to be handled in software.

If no slave answers to an event triggered frame header, the master node will set the NRE flag and a NRE interrupt will occur if enabled. If a collision occurs, a frame error and checksum error may arise before the NRE error. Those errors are flagged and the appropriate interrupts will occur, if enabled.

Frame errors and checksum errors depend on the behavior and synchronization of the responding slaves. If the slaves are totally synchronized and stop transmission once the collision occurred, it is possible that only the NRE error is flagged despite the occurrence of a collision. To detect if there has been a reception of one byte before the NRE error is flagged use the bus busy flag (SCIFLR.3) as an indicator.

The bus busy flag is set on the reception of the first bit of the header and remains set until the header reception is complete, and again is set on the reception of the first bit of the response. In the case of a collision, the flag is cleared in the same cycle as the NRE flag is set.

Software could implement the following sequence:

- Once the reception of the header is done (poll for RXID flag), wait for the bus busy flag to get set or NRE flag to get set.
- If bus busy flag is not set before NRE flag, then it is a true no response case (no data has been transmitted onto the bus).
- If bus busy flag gets set, then wait for NRE flag to get set or for successful reception. If NRE flag is set, then in this case a collision has occurred on the bus.

Even in the case of a collision, the received (corrupted) data is accessible in the RX buffers; registers LINRD0 and LINRD1.

2.4.2 Header Reception and Adaptive Baud Rate

A slave node baud rate might be adjusted to the detected bit rate as an option in the SCI/BLIN module. The adaptive baud rate option is enabled by setting the ADAPT bit in SCIGCR1 (Section 6.2). During header reception, a slave measures the baud rate during detection of the synch field. If SCIGCR1[10] (the ADAPT bit) is set, then the measured baud rate is compared to the slave node's programmed baud rate and adjusted to the LIN bus baud rate if necessary.

The SCI/BLIN synchronizer determines two measurements: BRK_count and BAUD_count (Figure 7). These values are always calculated during the Header reception for synch field validation (Figure 8).

NOTE: When an inconsistent synch field (ISF) error occurs, suggested action for the application is
- Reset the SWnRST bit.
- Set the SWnRST bit to make sure that the internal FSMs are back to their normal states

Figure 7. Measurements for Synchronization

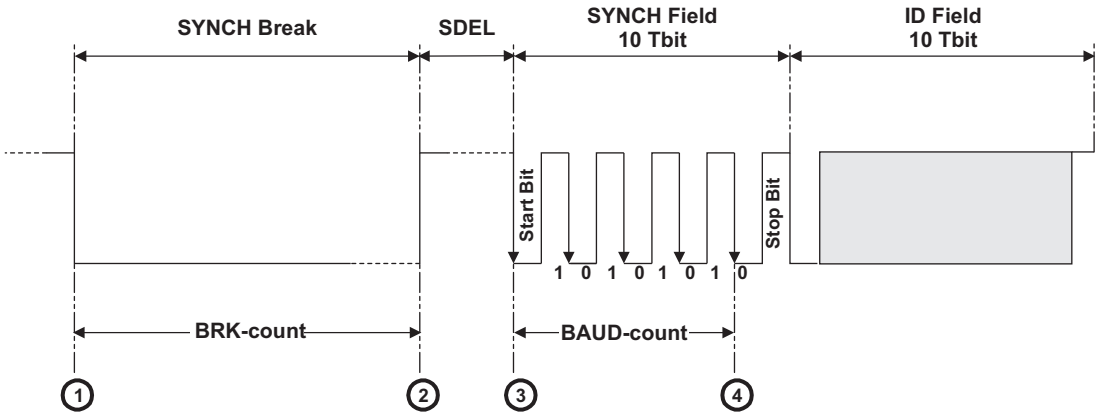
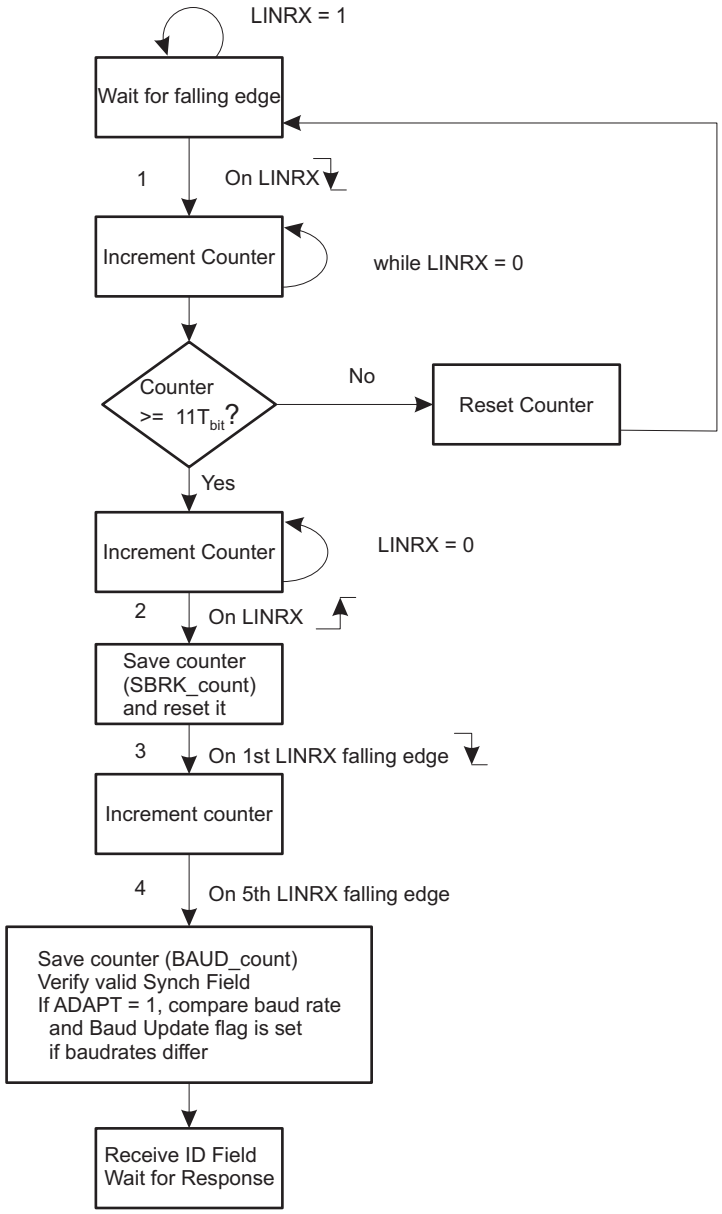


Figure 8. Synchronization Validation Process and Baud Rate Adjustment



By measuring the values BRK_count and BAUD_count, a valid synch break sequence can be detected as described in Figure 8. The four numbered events in Figure 7 signal the start/stop of the synchronizer counter. The synchronizer counter uses LM_CLK as the time base.

The synchronizer counter is used to measure the synch break relative to the detecting node T_{bit}. For a slave node receiving the synch break, a threshold of 11 T_{bit} is used as required by the LIN protocol. For detection of the dominant data stream of the synch break, the synchronizer counter is started on a falling edge and stopped on a rising edge of the LINRX. On detection of the synch break delimiter, the synchronizer counter value is saved and then reset.

On detection of five consecutive falling edges, the BAUD_count is measured. Bit timing calculation and consistency to required accuracy is implemented following the recommendations of LIN revision 2.0. A slave node can calculate a single T_{bit} time by division of BAUD_count by 8. In addition, for consistency between the detected edges the following is evaluated:

$$\mathrm{BAUD\_count} + \mathrm{BAUD\_count} \gg 2 + \mathrm{BAUD\_count} \gg 3 \leq \mathrm{BRK\_count}$$

The BAUD_count value is shifted 3 times to the right and rounded using the first insignificant bit to obtain a T_{bit} unit. If the ADPAT bit is set then, the detected baud rate is compared to the programmed baud rate.

During the header reception processing as illustrated in Figure 8, if the measured BRK_count value is less than 11 T_{bit} the synch break is not valid according to the protocol for a fixed rate. If the ADAPT bit is set, then the MBRS (Section 6.22) is used for measuring BRK_count and BAUD_count values and automatically adjusts to any allowed LIN bus rate (refer to LIN Specification Package 2.0).

NOTE: The MBRS divider should be set so that the rate is 20 kHz.

NOTE: The synch-break-threshold relative to the slave node is 11 T_{bit}. The synch break is 13 T_{bit} as specified in LIN version 1.3.

If the synch field is not detected within the given tolerances, the inconsistent-synch-field-error (ISFE) flag will be set. An ISFE interrupt will be generated, if enabled by its respective bit in the SCISETINT register (Section 6.6). The ID byte should be received after the synch field validation was successful. Any time a valid synch break (larger than 11 T_{bit}) is detected, the receiver's state machine should reset to reception of this new frame. This reset condition is only valid during response state, it should not occur if an additional synch break occurs during header reception.

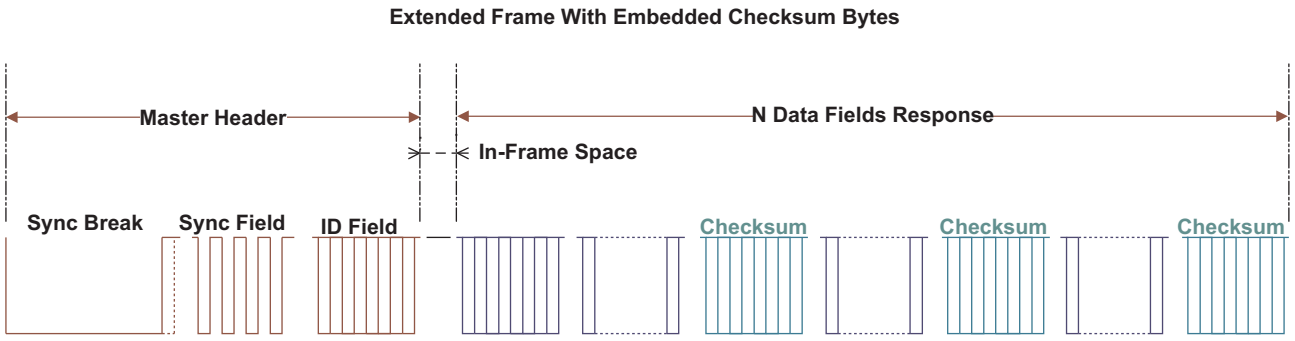
2.5 Extended Frames Handling

The LIN protocol includes two extended frames with identifiers 62 (user defined) and 63 (reserved extended). The length for these identifiers will be set during network configuration and are to be shared with the LIN bus nodes.

NOTE: Only identifier 62 (0x3E) applies to this special extended frame handling of unlimited response length.

Extended frame communication is triggered on reception of a header with identifier 0x3E; see Figure 9. Once the extended frame communication is triggered, unlike normal frames, this communication needs to be stopped before issuing another header. To stop the current extended frame communication, the SCIGCR1.13 bit must be set.

Figure 9. Optional Embedded Checksum in Response for Extended Frames



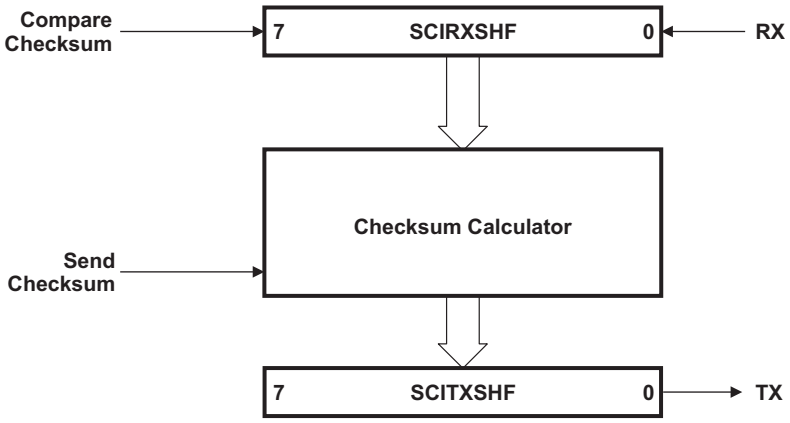
For the LIN 2.0 specification, the length of the user-defined frame is unlimited. Therefore, an ID interrupt will be generated (if enabled and there is a match) on reception of this identifier. This interrupt allows the CPU using a software counter to keep track of the bytes that are being sent out and decides when to calculate and insert a checksum byte (recommended at periodic rates). To handle this procedure, bit SCIGCR2[16] (Section 6.3) is used. A write to the SCIGCR2[16] bit will initiate an automatic send of the checkbyte. The last data field should be a checksum in compliance with the LIN protocol.

The periodicity of the checksum insertion, defined during network configuration, is used by the receiving node to evaluate the checksum of the ongoing message and has the benefit of enhanced reliability.

For the sending node, the automatic embedding of checksum should be possible when the SCIGCR2[16] bit is set. For the receiving node, a checksum comparison should be forced when the SCIGCR2[17] bit is set; see Figure 10.

NOTE: The LIN 2.0 enhanced checksum does not apply to the reserved identifiers. They will always use the classic checksum.

Figure 10. Checksum Compare and Send for Extended Frames



2.6 Timeout Control

Any SCI/BLIN node listening to the bus and expecting a response initiated from a master node could flag a no-response error timeout event. The LIN protocol defines four types of timeout events, which are all handled by the hardware of the SCI/BLIN module. The four LIN protocol events are:

- No-response timeout error
- Bus idle detection
- Timeout after wakeup signal
- Timeout after three wakeup signals

2.6.1 No-Response Error

The no-response error will occur when any node expecting a response waits for T_{FRAME_MAX} time and the message frame is not fully completed within the maximum length allowed, T_{FRAME_MAX}. After this time a no-response error (NRE) is flagged in the NRE bit of the SCIFLR register. An interrupt is triggered if enabled.

As specified in the LIN 1.3 standard, the minimum time to transmit a frame is:

$T_{FRAME\_MIN} = T_{HEADER\_MIN} + T_{DATA\_FIELD} + TC_{HECKSUM\_FIELD} = 44 + 10N$

where N = number of data fields.

And the maximum time frame is given by:

$T_{FRAME\_MAX} = (T_{FRAME\_MIN} + 1) \times 1.4$

The timeout value T_{FRAME_MAX} is derived from the N number of data fields value. The N value is either embedded in the header's ID field for messages or is part of the description file. In the latter case, the 3-bit CHAR value, SCIFORMAT(18–16) in Section 6.11, will indicate the value for N.

Table 2. Timeout Values in T_{bit} Units

N	T_{DATA_FIELD}	T_{FRAME_MIN}	T_{FRAME_MAX}
1	10	54	77
2	20	64	91
3	30	74	105

Table 2. Timeout Values in T_{bit} Units (continued)

N	T_{DATA_FIELD}	T_{FRAME_MIN}	T_{FRAME_MAX}
4	40	84	119
5	50	94	133
6	60	104	147
7	70	114	161
8	80	124	175

NOTE: The length coding of the ID field does not apply to two extended frame identifiers, with ID fields 0x3E (62) and 0x3F (63). In these cases, the ID field can be followed by an arbitrary number of data byte fields. The LIN 2.0 protocol specification mentions that ID field 0x3F (63) cannot be used. For these two cases, the NRE will not be handled by the SCI/BLIN controller hardware.

2.6.2 Bus Idle Detection

The second type of timeout can occur when a node detects an inactive LIN bus: no transitions between recessive and dominant values are detected on the bus. This should happen after a minimum of 4 s (this is 80,000 F_{LINCLK} cycles with the fastest bus rate of 20 kbps). If a node detects no activity in the bus as the TIMEOUT bit is set (Section 6.8), then it can be assumed that the LIN bus is in sleep mode.

2.6.3 Timeout after Wakeup Signal and Timeout after Three Wakeup Signals

The third and fourth types of timeout are related to the wakeup signal. A node initiating a wakeup should expect a header from the master within a defined amount of time: timeout after wakeup signal. See Section 4.3 for more details.

2.7 TXRX Error Detector (TED)

The following sources of error are detected by the TXRX error detector logic (TED). The TED logic consists of a bit monitor, an ID parity checker, and a checksum error. The following errors are detected:

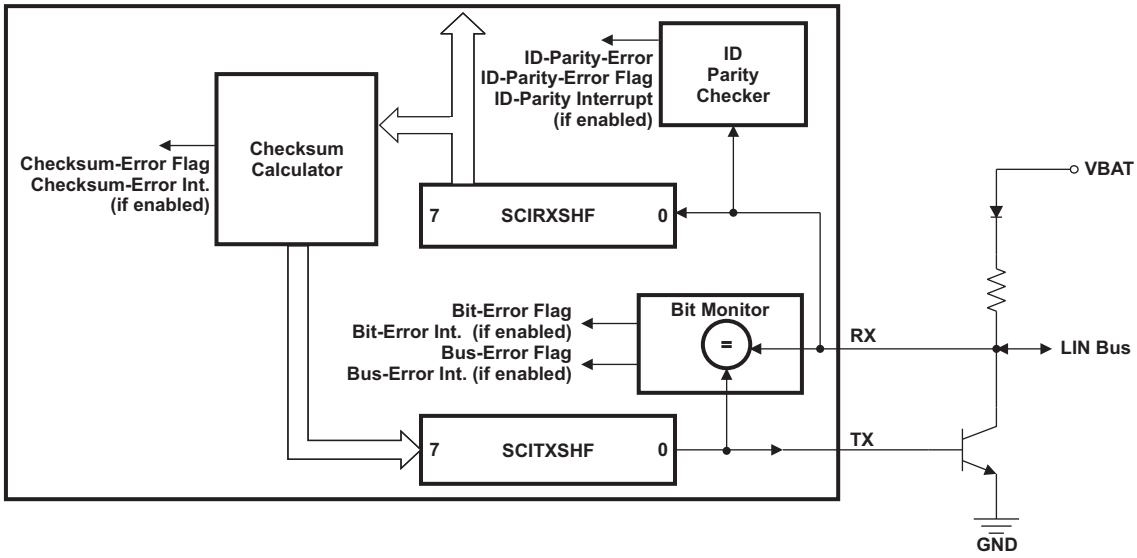
- Bit errors (BE)
- Physical bus errors (PBE)
- Identifier parity errors (PE)
- Checksum errors (CE)

All of these errors (BE, PBE, PE, CE) are flagged. An interrupt for the flagged errors will be generated if enabled. A message is valid for both the transmitter and the receiver if there is no error detected until the end of the frame.

2.7.1 Bit Errors

A BE has to be detected at that bit time when the bit value that is monitored is different from the bit value that is sent. A BE is indicated by the BE flag in SCIFLR (Section 6.8). After signaling a BE, the transmission has to be aborted no later than the next byte. The bit monitor ensures that the transmitted bit in LINTX is the correct value on the LIN bus by reading back on the LINRX pin as shown in Figure 11.

Figure 11. TXRX Error Detector



2.7.2 Physical Bus Errors

A PBE must be detected by a master if no valid message can be generated on the bus (i.e., the bus is shorted to GND or V_{BAT}). The bit monitor can detect a physical bus error during header generation as it compares the actual value on the bus with the expected value at each bit time.

2.7.3 ID Parity Errors

If parity is enabled, an ID parity error has to be detected, if any of the two parity bits of the sent ID byte are not equal to the calculated parity on the receiver node. The two parity bits are generated using the following mixed parity algorithm.

$$P0 = ID0 \oplus ID1 \oplus ID2 \oplus ID4 (\text{even parity})$$

$$P1 = \overline{ID1 \oplus ID3 \oplus ID4 \oplus ID5} (\text{odd parity})$$

An ID-parity error is flagged if detected and the received ID is not valid. See Section 2.7.4 for details.

2.7.4 Checksum Errors

A CE must be detected and flagged at the receiving end if the calculated modulo-256 sum over all received data bytes (including the ID byte if it is the enhanced checksum type) plus the checkbyte does not result in 0xFF. The modulo-256 sum is calculated over each byte by adding with carry, where the carry bit of each addition is added to the LSB of its resulting sum.

For the transmitting node, the checkbyte sent at the end of a message is the inverted sum of all the data bytes (see Figure 12) for classic implementation. The checkbyte is the inverted sum of the identifier byte and all the data bytes (see Figure 13) for the LIN 2.0 compliant implementation. The classic implementation should always be used for reserved identifiers 60 to 63; therefore, the CTYPE bit (SCIGCR1[12]; Section 6.2) will be overridden in this case. For signal-carrying-frame identifiers (0 to 59) the type of checksum used depends on the CTYPE bit (SCICGR1.12)

Figure 12. Classic Checkbyte Generation at Transmitting Node

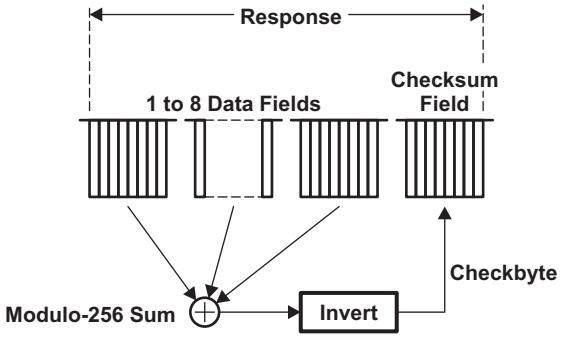
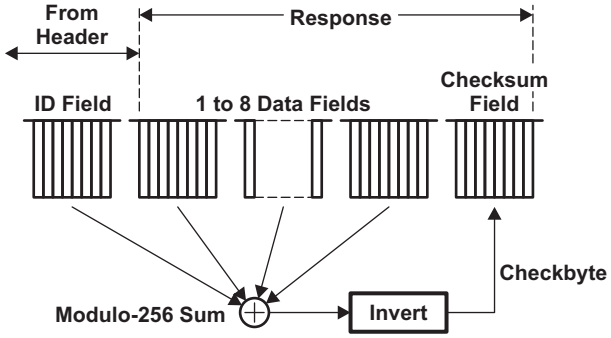


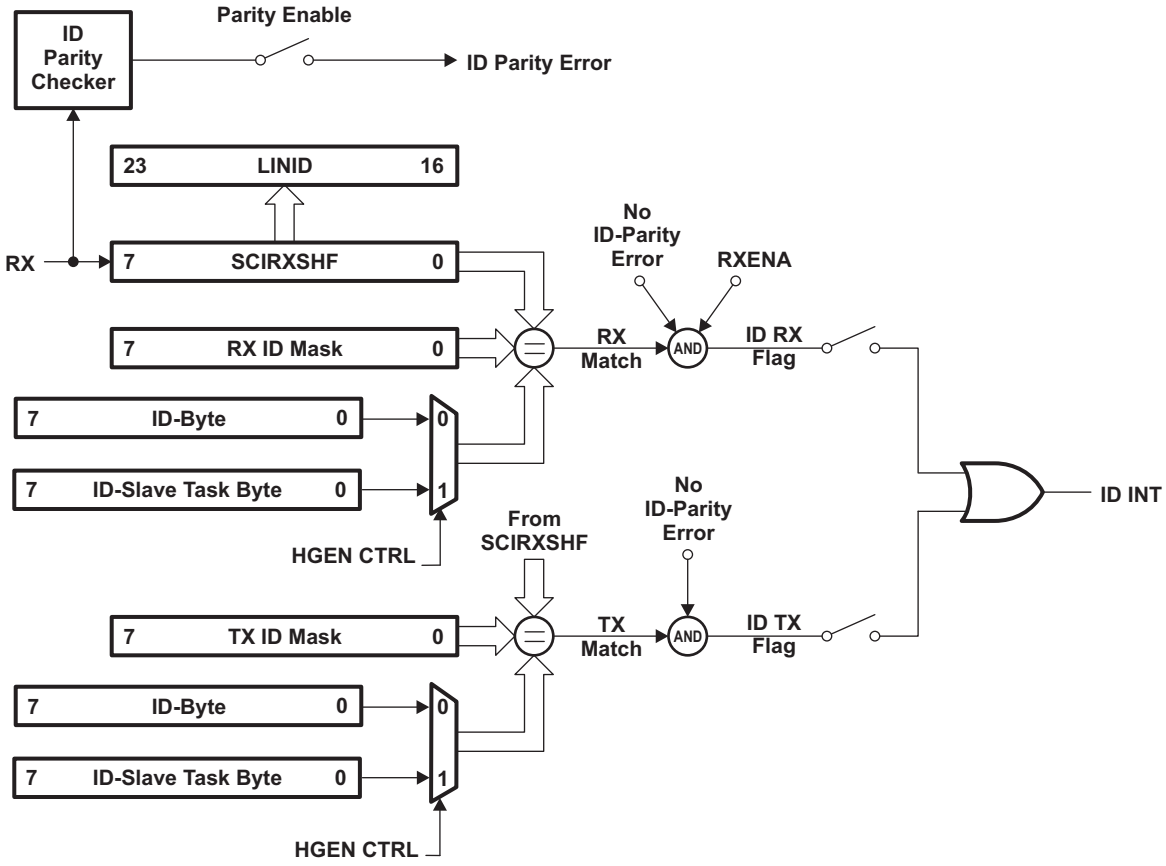
Figure 13. LIN 2.0-Compliant Checkbyte Generation at Transmitting Node



2.8 Message Filtering and Validation

Message filtering uses the entire identifier to determine which nodes will participate in a response, either receiving or transmitting a response. Therefore, two acceptance masks are used as shown in Figure 14.

Figure 14. ID Reception, Filtering and Validation



During header reception, all nodes filter the received ID-Field and decide whether they transmit or receive a response for the current message. There are two masks: one to receive a response; the other to initiate a transmission. All nodes compare the received ID to the identifier stored in the ID-SlaveTask BYTE field of the LINID register (Section 6.19) and use the RX-ID MASK and the TX-ID MASK fields in the LINMASK register (Section 6.18) to filter the bits of the identifier that should not be compared.

If there is an RX match with no parity error and the RXENA (SCIGCR1[24]; Section 6.2) bit is set, there will be an ID RX flag and an interrupt will be triggered if enabled. If there is a TX match with no parity error and the TXENA (SCIGCR1[25]; Section 6.2) bit is set, there will be an ID TX flag and an interrupt will be triggered if enabled in the SCISETINT register.

The masked bits become don't cares for the comparison. To build a mask for a set of identifiers, an XOR function could be used.

For example, to build a mask to accept IDs 0x26 and 0x25 using LINID(7–0) = 0x20; i.e., compare five most significant bits (MSBs) and filter three least significant bits (LSBs), the acceptance mask could be:

$$(0x26 + 0x25) \oplus 0x20 = 0x07$$

A mask of all zeros will compare all bits of the received identifier in the shift register with the ID-BYTE in LINID(7–0). If HGEN CTRL in SCIGCR1 (Section 6.2) is set to 1, a mask of 0xFF will always cause a match. A mask of all 1s will filter all bits of the received identifier, and thus there will be an ID match regardless of the content of the ID-SlaveTask BYTE field in the LINID register (Section 6.19).

NOTE: When the HGEN CTRL bit = 0, the LIN nodes compare the received ID to the ID-BYTE field in the LINID register, and uses the RX-ID MASK and the TX-ID MASK in the LINMASK register to filter the bits of the identifier that should not be compared.

If there is an RX match with no parity error and the RXENA (SCIGCR1[24]) bit is set, there will be an ID RX flag and an interrupt will be triggered if enabled. A mask of all 0s will compare all bits of the received identifier in the shift register with the ID-BYTE field in LINID(7–0). A mask of all 1s will filter all bits of the received identifier and there will be no match.

If HGEN CTRL = 1:
Received ID is compared with the ID-SlaveTask byte, using the RX-ID mask and the TX-ID mask.
A mask of all ones will always result in a match.
A mask of all zeroes means all the bits must be the same to result in a match.
If a mask has some bits which are ones, then those bits will not be used for the filtering criterion.

If HGEN CTRL = 0:
Received ID is compared with the ID-Byte, using the RX-ID mask and the TX-ID mask.
A mask of all ones will result in No-match.
A mask of all zeroes means all the bits must be the same to result in a match.
If a mask has some bits which are ones, then those bits will not be used for the filtering criterion.

During header reception, the received identifier is copied to the RECEIVED ID field [23:16] in the LINID register. If there is no parity error and there is either a TX match or an RX match, then the corresponding TX or RX ID flag is set (SCIFLR[13] or SCIFLR[14]; Section 6.8). If the ID interrupt is enabled (SCISETINT[13] = 1; Section 6.4), then an ID interrupt is generated.

After the ID interrupt is generated, the CPU may read the LINID (23–16) buffer and determine what response to load into the transmit buffers.

NOTE: When byte 0 is written to TDO (LINTDO(31–24), the response transmission is automatically generated.

In multibuffer mode, the TXRDY flag (Section 6.8) will be set when all the response data bytes and checkbyte are copied to the shift register SCITXSHF, which is a shadow register not accessible by the user.

In any other mode, the TXRDY flag is set each time a byte is copied to the SCITXSHF register and the last byte of the frame after the checkbyte is copied to the SCITXSHF register.

In multibuffer mode, the TXEMPTY flag is set when both the transmit buffer(s) TDy and the SCITXSHF shift register are emptied and after the checksum has been sent.

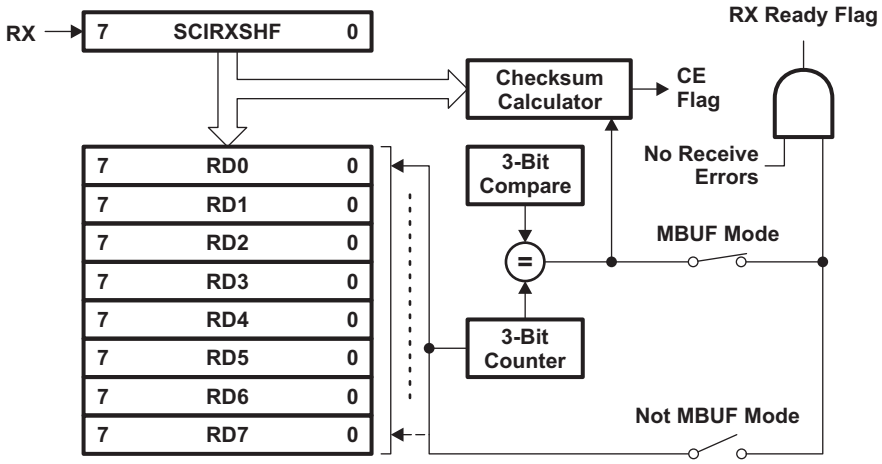
In any other mode, TXEMPTY is set each time TD0 and SCITXSHF are emptied except for the last byte of the frame where the checkbyte must also be transmitted. In multibuffer mode, TXEMPTY is set when the checkbyte has been transmitted.

If parity is enabled (bit SCIGCR1[3]), all slave receiving nodes will validate the identifier using all eight bits of the received ID byte. The SCI/BLIN will flag a corrupted identifier because of an IDparity error.

2.9 Receive Buffers

To reduce CPU load when receiving a LIN N-byte (with N = 1–8) response in interrupt mode, the SCI/BLIN module has eight receive buffers; see Figure 15 . These buffers can store an entire LIN response in the RDy receive buffers (SCIGCR1[11]; Section 6.2). Also, these receive buffers may be used in buffered SCI mode (the LIN MODE bit, SCIGCR1[6], = 0 and the MBUF MODE bit, SCIGCR1[10], = 1).

Figure 15. Receive Buffers



The checkbyte following the data bytes should be validated by the checksum calculator in the TED logic. The checksum error flag indicates a checksum error and a CE interrupt will be generated if enabled in the SCISETINT register.

The multibuffer 3-bit counter counts the data bytes transferred from the SCIRXSHF register to the RDy receive buffers (Section 6.16–Section 6.17) if multibuffer mode is enabled, or to RD0 if multibuffer mode is disabled. The 3-bit compare register contains the number of data bytes expected to be received. Therefore, it should be loaded with the length control field (bits 4 and 5) of the ID BYTE field received during the header reception. In cases where the ID BYTE field does not convey message length, the LENGTH value, SCIFORMAT(18–16) (Section 6.11), indicates the expected length and should be used to load the 3-bit compare register. Whether the length control field or the LENGTH value is used is selectable with the SCIGCR1[0] bit in communication mode.

A receive interrupt (RX interrupt; see the SCIINTVECT0/1 registers in Section 6.9/Section 6.10, and a receive ready RXRDY flag (SCIFLR[9]; Section 6.8) could occur after receiving a response if there are no response receive errors for the frame (checksum error, frame error, and overrun error). The checkbyte will be compared before acknowledging a reception.

2.10 Transmit Buffers

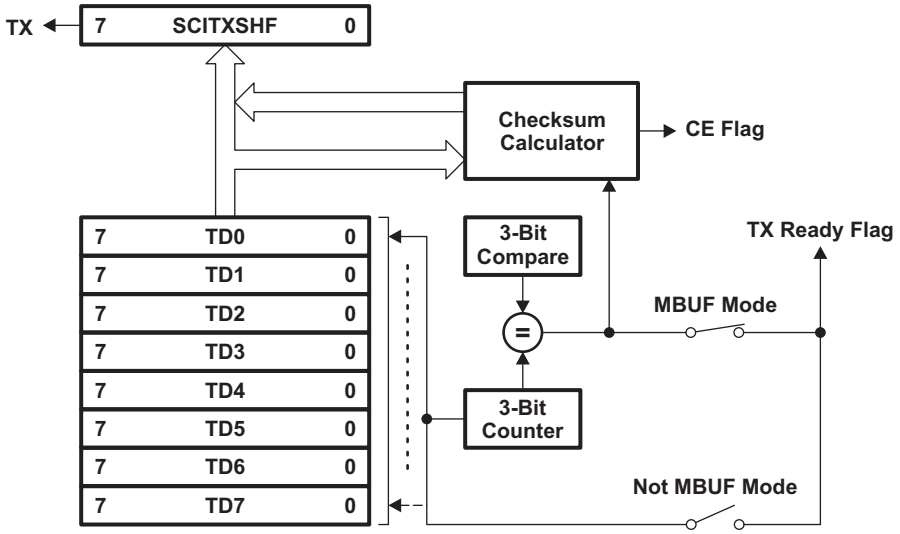
To reduce the CPU load when transmitting a LIN N-byte (with N = 1–8) response in interrupt mode, the SCI/BLIN module has eight transmit buffers, TD0–TD7 in LINTDO and LINTD1 (Section 6.20 and Section 6.21). With these buffers, it can preload an entire LIN response field in the TXy transmit buffers. Also, these transmit buffers may be used in buffered SCI mode (LIN MODE bit, SCIGCR1[6], = 0 and MBUF MODE bit, SCIGCR1[10], = 1).

The multibuffer 3-bit counter counts the data bytes transferred from the TDy transmit buffers register in multibuffer mode, or from TD0 to SCITXSHF if multibuffer mode is disabled. The 3-bit compare register contains the number of data bytes expected to be transmitted. Therefore it should be loaded with the length control field (bits 4 and 5) of the ID BYTE (Section 6.19) received during the header reception. If the ID field is not used to convey message length, the LENGTH value, SCIFORMAT(18–16), indicates the expected length and should be used instead to load the 3-bit compare register. Which bit field is used is selectable with the COMM MODE bit in LIN mode, SCIGCR1[0].

A transmit interrupt (TX interrupt) and a transmit ready flag (TX ready flag) could occur after transmitting a response.

Figure 16 illustrates the transmit buffers.

Figure 16. Transmit Buffers



The checkbyte will be generated by the checksum calculator and sent after the data-fields transmission is finished. The multibuffer 3-bit counter counts the data bytes transferred from the TDy buffers into the SCITXSHF register.

3 Interrupts

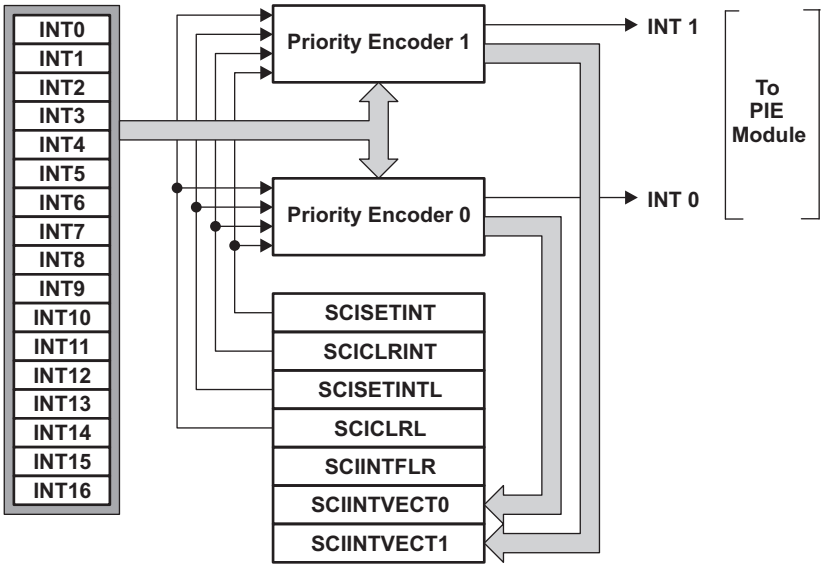
The SCI/BLIN module has two interrupt lines, level 0 and level 1, to the peripheral interrupt expansion (PIE) module (see Figure 17). Two offset registers (SCIINTVECT0 and SCIINTVECT1; and Section 6.10) determine which flag triggered the interrupt according to the respective priority encoders. Each interrupt has a bit to enable/disable the interrupt in the SCISETINT and SCICLRINT registers (Section 6.6 and Section 6.7), respectively.

Each interrupt has a bit to be set as interrupt level 0 or as interrupt level 1. By default, interrupts are in line level 0. SCISETINTLVL sets a given interrupt to line level1. SCICLEARINTLVL (Section 6.7) resets a given interrupt level to the default line level 0.

The interrupt vector registers SCIINTVECT0 and SCIINTVECT1 (and Section 6.10) return the vector of the pending interrupt line INT0 or INT1. If more than one interrupt is pending, the interrupt vector register holds the highest priority interrupt.

If multiple interrupts are pending, interrupts must be disabled and re-enabled after the first interrupt is serviced, in order for the other pending interrupts to be serviced.

Figure 17. General Interrupt Scheme



There are 16 interrupt sources in the SCI/BLIN module, with 9 being LIN mode only, as seen in Table 3.

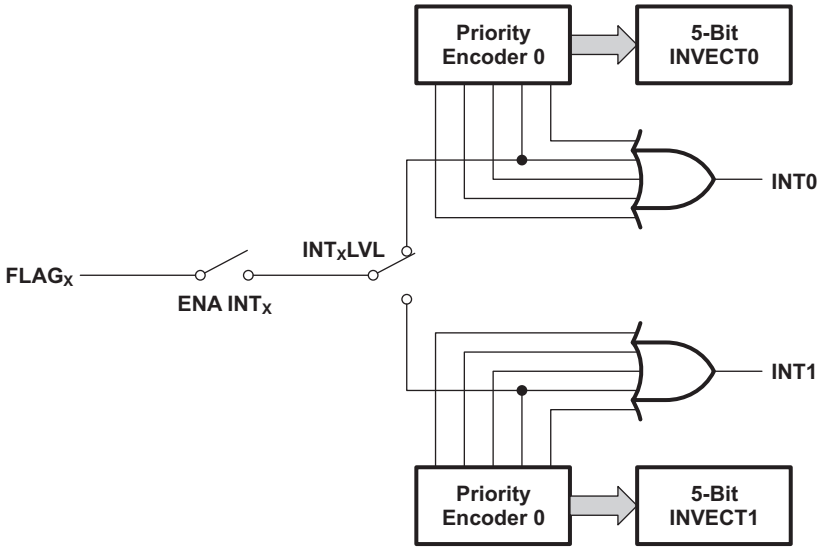
Table 3. SCI/BLIN Interrupts

Offset[1]	Interrupt	Comment
0	No interrupt	
1	Wakeup	SCI + LIN mode
2	Inconsistent-synch-field error	LIN mode only
3	Parity error	SCI + LIN mode
4	ID	LIN mode only
5	Physical bus error	LIN mode only
6	Frame error	SCI + LIN mode
7	Break detect	SCI mode only
8	Checksum error	LIN mode only
9	Overrun error	SCI + LIN mode
10	Bit error	LIN mode only
11	Receive	SCI + LIN mode
12	Transmit	SCI + LIN mode
13	No-response error	LIN mode only
14	Timeout after wakeup signal (150 ms)	LIN mode only
15	Timeout after three wakeup signals (1.5 s)	LIN mode only
16	Timeout (Bus Idle, 4s)	LIN mode only

(1) Offset 1 is the highest priority. Offset 16 is the lowest priority.

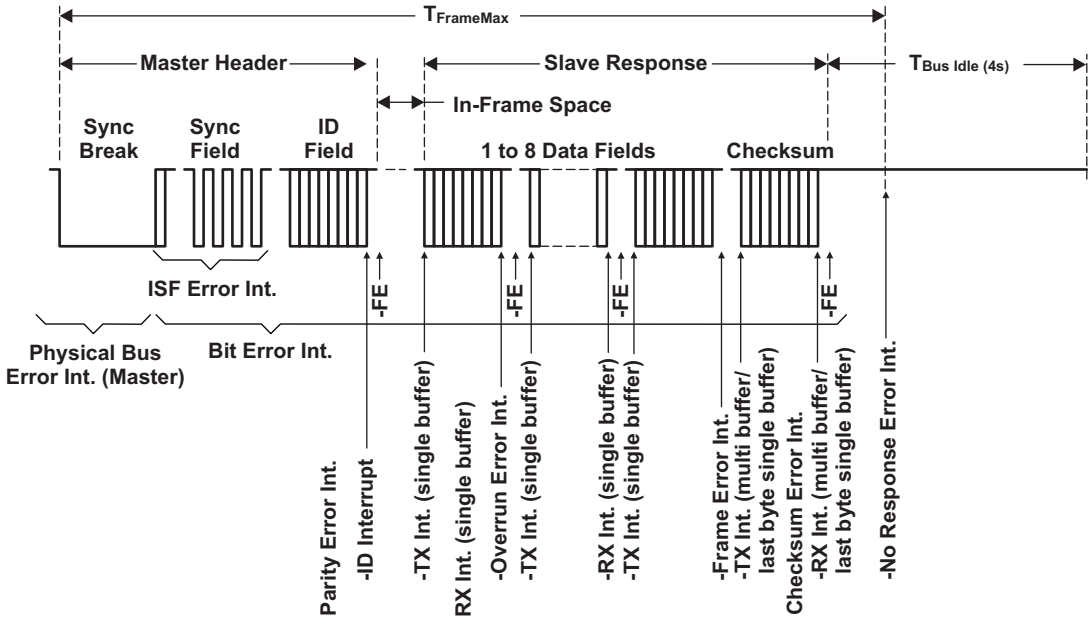
For each of the interrupt sources FLAGx, the SCISETINT and SCICLRINT register pair is used to enable/ disable the interrupt. For each source, the interrupt line can be chosen to be INT0 or INT1 with the SCISETINTLVL and SCICLRINTLVL register pair.

Figure 18. Interrupt Generation for Given Flags



A LIN message frame indicating the timing and sequence of the according LIN interrupts that could occur is shown in Figure 19 .

Figure 19. LIN Message Frame Showing LIN Interrupt Timing and Sequence”



4 Low-Power Mode

The SCI/BLIN module enters low-power mode when a sleep command frame is received. A wakeup signal will terminate the sleep mode of the LIN bus. On receipt of the sleep command, the POWERDOWN bit in SCIGCR2 (Section 6.3) must be set by the application software and the module enters local low-power mode.

NOTE: If the module needs to be able to wake up upon a wake-up request, the following sequence should be followed:

1. Enable wakeup interrupt in the SCISETINT register (Section 6.4).
2. Set the POWERDOWN bit.

The SCI/BLIN module can be put in either local or global low-power mode. Global low-power mode is asserted by the system and is not controlled by the SCI/BLIN module. During global low-power mode (HALT and STANDBY), all clocks to the SCI/BLIN are turned off so the module is completely inactive.

NOTE: Enabling Local Low-Power Mode During Receive and Transmit.
If the wakeup interrupt is enabled and low-power mode is requested while the receiver is receiving data, then the SCI/BLIN immediately generates a wake-up interrupt to clear the powerdown bit. Thus, the SCI/BLIN is prevented from entering low-power mode and completes the current reception. Otherwise, if the wakeup interrupt is disabled, the SCI/BLIN completes the current reception and then enters the lowpower mode.

4.1 Entering Sleep Mode

In LIN mode, a sleep command is used to broadcast the sleep mode to all nodes. The sleep command consists of a diagnostic master request frame with identifier 0x3C (60), with the first data field as 0x00. There should be no activity in the bus once all nodes receive the sleep command: the bus is in sleep mode.

Local low-power mode is asserted by setting the POWERDOWN (SCIGCR2[0]; Section 6.3) bit; setting this bit stops the clocks to the SCI/BLIN internal logic and registers. Clearing the POWERDOWN bit causes SCI/ BLIN to exit from local low-power mode. All the registers are accessible during local power-down mode. If a register is accessed in low-power mode, this access results in enabling the clock to the module for that particular access alone.

4.2 Wakeup

The wakeup interrupt is used to allow the SCI/BLIN module to automatically exit low-power mode. A SCI/BLIN wakeup is triggered when a low level is detected on the LINRX pin, and this clears the POWERDOWN bit.

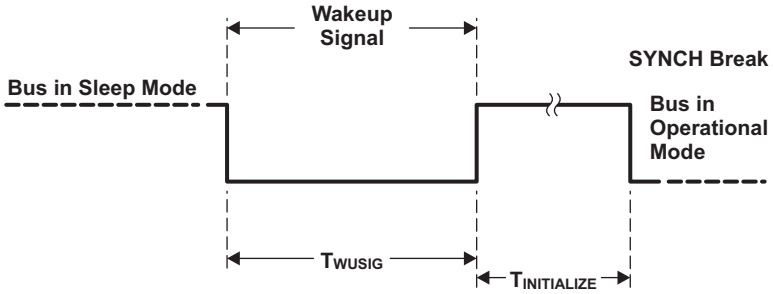
NOTE: A node which is not in power-down mode but is receiving a wake-up pulse will not trigger a wake-up interrupt. Wake-up interrupt can only be triggered if the module is in power-down mode.

NOTE: If the wakeup interrupt is disabled (WAKEUP INT in the SCISETINT register is cleared), then the SCI/BLIN enters low-power mode whenever it is requested to do so, but a low level on the receive RX pin does NOT cause the SCI/BLIN to exit low-power mode.

In LIN mode, any node can terminate sleep mode by sending a wakeup signal; see Figure 20 . A slave node that detects the bus in sleep mode, if a wakeup request is pending, will send a wakeup signal. The wakeup signal is generated with a dominant value on the LIN bus for T_{WUSIG}; this should be at least 5 T_{bits} for the LIN bus baud rates. The wakeup signal should be generated by sending an 0xF0 byte containing 5 dominant T_{bits} and 5 recessive T_{bits}.

$$0.25\ ms \leq T_{WUSIG} \leq 5ms$$

Figure 20. Wakeup Signal Generation



Assuming a perfect bus with no noise or loading effects, a write of 0xF0 to TD0 will load the transmitter to meet the wakeup signal timing requirement for TWUSIG. Then, setting the GENWU bit (SCIGCR2[8]; Section 6.3) will transmit the preloaded value in TD0 for a wakeup signal transmission. The ability of a node to transmit a wakeup is independent of the value of the TXENA (SCIGCR1.25) bit.

NOTE: The GENWU bit can be set/reset only when SWnRST is set to 1 and the node is in power down mode. The bit will be cleared on a valid synch break detection. A master sending a wakeup request, will exit power down mode upon reception of the wakeup pulse. The bit will be cleared on a SWnRST (SCIGCR1[7]; Section 6.2). This can be used to stop a master from sending further wakeup requests.

The TI TPIC1021 LIN transceiver, upon receiving a wakeup signal, will translate it to the microcontroller for wakeup with a dominant level on the LINRX pin, or a signal to the voltage regulator. While the POWERDOWN (SCIGCR2[0]; Section 6.3) bit is set, if the SCI/BLIN module detects a dominant level in the LINRX pin, it will generate a wakeup interrupt if enabled in the SCISETINT register (Section 6.4).

The TI TPIC1021 LIN transceiver will detect a dominant level on the bus longer than 150 ms as a wakeup request. The SCI/BLIN controller's slave should be ready to listen to the bus in less than 100 ms ($T_{INITIALIZE}$<100 ms) after a dominant-to-recessive edge (end-of-wakeup signal).

4.3 Wakeup Timeouts

The LIN protocol defines the following timeouts for a wakeup sequence. After a wakeup signal has been sent to the bus, all nodes wait for the master to send a header. If no synch field is detected before 150 ms (3,000 cycles at 20 kHz) after dominant wakeup signal's ending edge, a new wakeup is sent by the same node that requested the first wakeup. This sequence is not repeated more than three times. After three attempts to wake up the LIN bus, wakeup signal generation is suspended for a 1.5 s (30,000 cycles at 20 kHz) period.

NOTE: The SCI/BLIN controller handles the wakeup expiration times defined by the LIN protocol with a hardware implementation.

NOTE: The MBRS register (Section 6.22) must be set to assure that the LIN 2.0 (real-timebased) timings meet the LIN 1.3 bit time base. A node triggering the wakeup should set the MBRS register accordingly to meet the targeted time as 128 T_{bits} x programmed prescaler.

5 Emulation Mode

In emulation mode, the CONT bit of the SCIGCR1 (Section 6.2) determines how the SCI/BLIN operates when the program is suspended. The SCI/BLIN counters are affected by this bit during debug mode; when set, the counters are not stopped and when cleared, the counters are stopped.

Any reads in emulation mode to a SCI/BLIN register will not have any effect on the flags in the SCIFLR register (Section 6.8).

6 SCI/BLIN Control Registers

The SCI/BLIN module registers are based on the SCI registers, with added functionality registers enabled by the LIN MODE bit in the SCIGCR1 register.

These registers are accessible in 8-, 16-, and 32-bit reads or writes. The SCI/BLIN is controlled and accessed through the registers listed in Table 4. Among the features that can be programmed are the LIN protocol mode, communication and timing modes, baud rate value, frame format, and interrupt configuration.

Table 4. LIN Registers

Address	Register	Description	Section
0x6C00	SCIGCR0	Global Control Register 0	Section 6.1
0x6C02	SCIGCR1	Global Control Register 1	Section 6.2
0x6C04	SCIGCR2	Global Control Register 2	Section 6.3
0x6C06	SCISETINT	Interrupt Enable Register	Section 6.4
0x6C08	SCICLEARINT	Interrupt Disable Register	Section 6.5
0x6C0A	SCISETINTLVL	Set Interrupt Level Register	Section 6.6
0x6C0C	SCICLEARINTLVL	Clear Interrupt Level Register	Section 6.7
0x6C0E	SCIFLR	Flag Register	Section 6.8
0x6C10	SCIINTVECT0	Interrupt Vector Offset Register 0	Section 6.9
0x6C12	SCIINTVECT1	Interrupt Vector Offset Register 1	Section 6.10
0x6C14	SCIFORMAT	Length Control register	Section 6.11
0x6C16	BRSR	Baud Rate Selection Register	Section 6.12
0x6C18	SCIED	Emulation buffer register	Section 6.13.1
0x6C1A	SCIRD	Receiver data buffer register	Section 6.13.2
0x6C1C	SCITD	Transmit data buffer register	Section 6.13.3
0x6C22	SCIPIO2	Pin control register 2	Section 6.14
0x6C30	LINCOMP	Compare register	Section 6.15
0x6C32	LINRD0	Receive data register 0	Section 6.16
0x6C34	LINRD1	Receive data register 1	Section 6.17
0x6C36	LINMASK	Acceptance mask register	Section 6.18
0x6C38	LINID	Register containing ID- byte, ID-SlaveTask byte, and ID received fields.	Section 6.19
0x6C3A	LINTD0	Transmit Data Register 0	Section 6.20
0x6C3C	LINTD1	Transmit Data Register 1	Section 6.21
0x6C3E	MBRSR	Baud Rate Selection Register	Section 6.22
0x6C48	IODFTCTRL	IODFT for BLIN	Section 6.23

SCI Global Control Register 0 (SCIGCR0)

31	16
Reserved	
R-0	

15	1	0
Reserved		RESET
R-0		R/W-0

SCI Global Control Register (SCIGCR1)

31	26	25	24
Reserved		TXENA	RXENA
R-0		R/W-0	R/W-0

23	18	17	16
Reserved		CONT	LOOP BACK
R-0		R/W-0	R/W-0

15	14	13	12	11	10	9	8
Reserved		STOPEXT FRAME	HGEN CTRL	CTYPE	MBUF MODE	ADAPT	SLEEP
R-0		R/WL-0	R/WL-0	R/WL-0	R/W-0	R/WL-0	R/WC-0

7	6	5	4	3	2	1	0
SW nRST	LIN MODE	CLK_MASTER	STOP	PARITY	PARITY ENA	TIMING MODE	COMM MODE
R/W-0	R/W-0	R/W-0	R/WC-0	R/WC-0	R/W-0	R/W-0	R/W-0

SCI Global Control Register (SCIGCR2)

31	18	17	16
Reserved		CC	SC
R-0		R/W-L0	R/WL-0

15	9	8	7	1	0
Reserved		GENWU	Reserved		POWER DOWN
R-0		R/W-0	R-0		R/W-0

SCI Set Interrupt Register (SCISETINT)

31	30	29	28	27	26	25	24
SET BE INT	SET PBE INT	SET CE INT	SETISFE INT	SET NRE INT	SET FE INT	SET OE INT	SET PE INT
R/WL-0	R/WL-0	R/WL-0	R/WL-0	R/WL-0	R/W-0	R/W-0	R/W-0

23	16
Reserved	
R-0	

15	14	13	12	10	9	8
Reserved		SET ID INT	Reserved		SET RX INT	SET TX INT
R-0		R/WL-0	R-0		R/W-0	R/W-0

7	6	5	4	3	2	1	0
SET TOA3 WUS INT	SET TOA WUS INT	Reserved	SETTIMEOUT INT	Reserved		SET WAKE UP INT	SET BRKDT INT
R/WL-0	R/WL-0	R-0	R/WL-0	R-0		R/W-0	R/WC-0

SCI Clear Interrupt Register (SCICLEARINT)

31	30	29	28	27	26	25	24
CLR BE INT	SET PBE INT	CLR CE INT	CLRISFE INT	CLR RE INT	CLR FE INT	CLR OE INT	CLR PE INT
R/WL-0	R/WL-0	R/WL-0	R/WL-0	R/WL-0	R/W-0	R/W-0	R/W-0
23							16
Reserved							
R-0							
15	14	13	12		10	9	8
Reserved		CLR ID INT	Reserved			CLR RX INT	CLR TX INT
R-0		R/WL-0	R-0			R/W-0	R/W-0
7	6	5	4	3	2	1	0
CLR TOA3 WUS INT	CLR TOA WUS INT	Reserved	CLRTIMEOUT INT	Reserved		CLR WAKE UP INT	CLR BRKDT INT
R/WL-0	R/WL-0	R-0	R/WL-0	R-0		R/W-0	R/WC-0

SCI Set Interrupt Level Register (SCISETINTLVL)

31	30	29	28	27	26	25	24
SET BE INT LVL	SET PBE INT LVL	SET CE INT LVL	SET ISFE INT LVL	SET NRE INT LVL	SET FE INT LVL	SET OE INT LVL	SET PE INT LVL
23							16
Reserved							
R-0							
15	14	13	12	11	10	9	8
Reserved		SET ID INT LVL	Reserved			SET RX INT LVL	SET TX INT LVL
R-0			R-0				
7	6	5	4	3	2	1	0
SETTOA3WUS INT LVL	SETTOAWUS INT LVL	Reserved	SETTIMEOUT INT LVL	Reserved		SET WAKE UP INT LVL	SET BRKDT INT LVL
		R-0		R-0			

SCI Clear Interrupt Level Register (SCICLEARINTLVL)

31	30	29	28	27	26	25	24
CLR BE INT LVL	CLR PBE INT LVL	CLR CE INT LVL	CLR ISFE INT LVL	CLR NRE INT LVL	CLR FE INT LVL	CLR OE INT LVL	CLR PE INT LVL
R/WL-0	R/WL-0	R/WL-0	R/WL-0	R/WL-0	R/W-0	R/W-0	R/W-0
23							16
Reserved							
R-0							
15	14	13	12		10	9	8
Reserved		CLR ID INT LVL	Reserved			CLR RX INT LVL	CLR TX INT LVL
R-0		R/WL-0	R-0			R/W-0	R/W-0
7	6	5	4	3	2	1	0
CLRTOA3WUS INT LVL	CLRTOAWUS INT LVL	Reserved	CLRTIMEOUT INTLVL	Reserved		CLR WAKE UP INT LVL	CLR BRKDT INT LVL
R/WL-0	R/WL-0	R-0	R/WL-0	R-0		R/W-0	R/WC-0

SCI Flags Register (SCIFLR)

31	30	29	28	27	26	25	24
BE	PBE	CE	ISFE	NRE	FE	OE	PE
R/WL-0	R/WL-0	R/WL-0	R/WL-0	R/WL-0	R/W-0	R/W-0	R/W-0

23	16
Reserved	
R-0	

15	14	13	12	11	10	9	8
Reserved	RX ID	TX ID	RX WAKE	TX EMPTY	TX WAKE	RX RDY	TX RDY
R-0	R/WL-0	R/WL-0	R/WC-0	R/W-1	R/WC-0	R/W-0	R/W-1

7	6	5	4	3	2	1	0
TOA3 WUS	TOA WUS	Reserved	TIMEOUT	BUSY	IDLE	WAKE UP	BRKDT
R/WL-0	R/WL-0	R-0	R/WL-0	R/W-0	R/WC-0	R/WL-0	R/WC-0

SCI Interrupt Vector Offset 0 (SCIINTVECT0)

31	16
Reserved	
R-0	

15	5	4	0
Reserved		INTVECT0	
R-0		R-0	

SCI Interrupt Vector Offset 1 (SCIINTVECT1)

31	16
Reserved	
R-0	

15	5	4	0
Reserved		INTVECT1	
R-0		R-0	

SCI Format Control Register (SCIFORMAT)

31	19	18	16
Reserved		LENGTH	
R-0		R/W-0	

15	3	2	0
Reserved		CHAR	
R-0		R/WC-0	

Baud Rate Selection Register (BRSR)

31	28	27	24	23	16
Reserved		M		P	
R-0		R/W-0		R/W-0	

15	0
P	
R/W-0	

Receiver Emulation Data Buffer (SCIED)

31–16	15–8	7–0
Reserved	Reserved	ED
R-0	R-0	R-0

Receiver Data Buffer (SCIRD)

31–16	15–8	7–0
Reserved	Reserved	RD
R-0	R-0	R/WC-0

Transmit Data Buffer Register (SCITD)

31–16	15–8	7–0
Reserved	Reserved	TD
R-0	R-0	R/W-0

SCI Pin I/O Control Register 2 (SCIPIO2)

31–16	15–3	2	1	0
Reserved	Reserved	TX IN	RX IN	Reserved
R-0	R-0	R-x	R-x	R-0

LIN Compare Register (LINCOMPARE)

31–16	15–10	9–8	7–3	2–0
Reserved	Reserved	SDEL	Reserved	SBREAK
R-0	R-0	R/WL-0	R-0	R/WL-0

LIN Receive Buffer 0 Register (LINRD0)

31–24	23–16	15–8	7–0
RD0	RD1	RD2	RD3
R-0	R-0	R-0	R-0

LIN Receive Buffer 1 Register (LINRD1)

31–24	23–16
RD4	RD5
R-0	R-0
15–8	**7–0**
RD6	RD7
R-0	R-0

LIN Mask Register (LINMASK)

31–24	23–16
Reserved	RX ID MASK
R-0	R-0
15–8	**7–0**
Reserved	TX ID MASK
R-0	R-0

LIN Identification Register (LINID)

31–24	23–16
Reserved	RECEIVED ID
R-0	R-0
15–8	**7–0**
ID-SlaveTask BYTE	ID BYTE
R/WL-0	R/WL-0

LIN Transmit Buffer 0 Register (LINTD0)

31–24	23–16
TD0	TD1
R/W-0	R/W-0
15–8	**7–0**
TD2	TD3
R/W-0	R/W-0

LIN Transmit Buffer 1 Register (LINTD1)

31–24	23–16
TD4	TD5
R/W-0	R/W-0
15–8	**7–0**
TD6	TD7
R/W-0	R/W-0

Maximum Baud Rate Selection Register (MBRS)

31–16
Reserved
R-0

15–13	12–0
Reserved	MBR
R-0	R/WL-0

I/O Design For Test Control (IODFTCTRL) Register

31	30	29	28	27	26	25	24
Bit Error Enable	Physical Bus Error Enable	Checksum Error Enable	Inconsistent Synch Field Error Enable	Reserved	Frame Error Enable	Parity Error Enable	Break Detect Error Enable
R/W-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0

23	21	20	19	18	16
Reserved		PIN SAMPLE MASK		TX SHIFT	
R-0		R/W-0		R/W-0	

15	12	11	8
Reserved		IODFTENA	
R-0		R/W-0	

7	2	1	0
Reserved		LPBENA	RXPENA
R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

6.1 SCI Global Control Register 0 (SCIGCR0)

The SCI Global Control Register 0 (SCIGCR0) is shown in Figure 21 and described in Table 5.

Figure 21. SCI Global Control Register 0 (SCIGCR0)

31	16
Reserved	
R-0	

15	1	0
Reserved		RESET
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 5. SCI Global Control Register 0 (SCIGCR0) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved		Reads return zero and writes have no effect.
0	RESET		This bit resets the SCI/BLIN module. This bit is effective in SCI and LIN mode.
			EALLOW-protected Write mode:
		0	Reset module
		1	Pull module out of reset
			EALLOW-protected and normal mode Read:
		0	Module is under reset.
		1	Module is out of reset.

6.2 SCI Global Control Register (SCIGCR1)

The SCI Global Control Register 1 (SCIGCR1) is shown in Figure 22 and described in Table 6.

Figure 22. SCI Global Control Register (SCIGCR1)

31	26	25	24
Reserved		TXENA	RXENA
R-0		R/W-0	R/W-0

23	18	17	16
Reserved		CONT	LOOP BACK
R-0		R/W-0	R/W-0

15	14	13	12	11	10	9	8
Reserved		STOPEXT FRAME	HGEN CTRL	CTYPE	MBUF MODE	ADAPT	SLEEP
R-0		R/WL-0	R/WL-0	R/WL-0	R/W-0	R/WL-0	R/WC-0

7	6	5	4	3	2	1	0
SW nRST	LIN MODE	CLK_MASTER	STOP	PARITY	PARITY ENA	TIMING MODE	COMM MODE
R/W-0	R/W-0	R/W-0	R/WC-0	R/WC-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; WL = Write in LIN mode only; WC = Write in sci-compatible mode only; -*n* = value after reset

Table 6. SCI Global Control Register (SCIGCR1) Field Descriptions

Bit	Field	Value	Description
31-26	Reserved		Reads return zero and writes have no effect.

Table 6. SCI Global Control Register (SCIGCR1) Field Descriptions (continued)

Bit	Field	Value	Description
25	TXENA		Transmit enable. This bit is effective in LIN and SCI modes. Data is transferred from SCITD or the TDy (with y=0, 1,...7) buffers in LIN mode to the SCITXSHF shift out register only when the TXENA bit is set.
		0	Disable transfers from SCITD or TDy to SCITXSHF
		1	Enable transfers of data from SCITD or TDy to SCITXSHF
			Note: Data written to SCITD or the transmit multi-buffer before TXENA is set is not transmitted. If TXENA is cleared while transmission is ongoing, the data previously written to SCITD is sent (including the checkbyte in LIN mode).
24	RXENA		Receive enable. This bit is effective in LIN and SCI modes. RXENA allows or prevents the transfer of data from SCIRXSHF to SCIRD or the receive multibuffers.
		0	Prevents the receiver from transferring data from the shift buffer to the receive buffer or multi-buffers.
		1	Allows the receiver to transfer data from the shift buffer to the receive buffer or multi-buffers.
			Note: Clearing RXENA stops received characters from being transferred into the receive buffer or multi-buffers, prevents the RX status flags (see Table 7) from being updated by receive data, and inhibits both receive and error interrupts. However, the shift register continues to assemble data regardless of the state of RXENA.
			Note: If RXENA is cleared before the time the reception of a frame is complete, the data from the frame is not transferred into the receive buffer.
			Note: If RXENA is set before the time the reception of a frame is complete, the data from the frame is transferred into the receive buffer. If RXENA is set while SCIRXSHF is in the process of assembling a frame, the status flags are not guaranteed to be accurate for that frame. To ensure that the status flags correctly reflect what was detected on the bus during a particular frame, RXENA should be set before the detection of that frame
23-18	Reserved		Reads return zero and writes have no effect.
17	CONT		Continue on suspend. This bit has an effect only when a program is being debugged with an emulator, and it determines how the SCI/BLIN operates when the program is suspended. The BLIN counters are affected by this bit: when set the counters are not stopped, when clear the counters are stopped during debug mode.
		0	When debug mode is entered, the SCI/BLIN state machine is frozen. Transmissions and LIN counters are halted and resume when debug mode is exited.
		1	When debug mode is entered, the SCI/BLIN continues to operate until the current transmit and receive functions are complete.
16	LOOP BACK		Loopback bit. This bit is effective in LIN and SCI modes. The selfchecking option for the SCI/BLIN can be selected with this bit. If the LINTX and LINRX pins are configured with SCI/BLIN functionality, then the LINTX pin is internally connected to the LINRX pin. Externally, during loop back operation, the LINTX pin outputs a high value and the LINRX pin is in a high-impedance state. If this bit value is changed while the SCI/BLIN is transmitting or receiving data, errors may result.
		0	Loop back mode is disabled.
		1	Loop back mode is enabled.
15-14	Reserved		Reads return zero and writes have no effect.
13	STOP EXT FRAME		Stop extended frame communication. This bit is effective in LIN mode only. This bit can be written only during extended frame communication. When the extended frame communication is stopped, this bit is cleared automatically.
		0	No effect
		1	Extended frame communication will be stopped, once current frame transmission/reception is completed.

Table 6. SCI Global Control Register (SCIGCR1) Field Descriptions (continued)

Bit	Field	Value	Description
12	HGEN CTRL		LIN mode bit. This bit controls the type of Mask filtering comparison.
		0	ID filtering using ID-Byte. RECID and ID-BYTE fields in LINID register are used for detecting a match (using TX/RX MASK values). Mask of 0xFF in LINMASK register will result in NO match.
		1	ID filtering using ID-SlaveTask byte (Recommended). RECID and ID-Slave task byte are used for detecting a match (using TX/RX Mask values).Mask of 0xFF in LINMASK register will result in ALWAYS match.
11	CTYPE		Checksum type. This bit is effective in LIN mode only. This bit controls the type of checksum to be used: classic or enhanced.
		0	Classic checksum is used.
		1	Enhanced checksum is used.
10	MBUF MODE		Multibuffer mode. This bit is effective in LIN and SCI modes.This bit controls receive/transmit buffer usage, i.e., whether the RX/TX multibuffers are used or a single register, RD0/TD0, is used.
		0	The multi-buffer mode is disabled.
		1	The multi-buffer mode is enabled.
9	ADAPT		Adapt mode enable. This mode is effective in LIN mode only. This bit has an effect during the detection of the Synch Field. There are two LIN protocol bit rate modes that could be enabled with this bit according to the Node capability file definition: automatic or select. Software and network configuration will decide which of the previous two modes. When this bit is cleared, the LIN 2.0 protocol fixed bit rate should be used. If the ADAPT bit is set, a BLIN slave node detecting the baudrate will compare it to the prescalers in BRSR register and update it if they are different. The BRSR register will be updated with the new value. If this bit is not set there will be no adjustment to the BRSR register. EALLOW-protected and normal mode Read:
		0	Automatic baudrate adjustment is disabled
		1	Automatic baudrate adjustment is enabled
			EALLOW-protected and normal mode Write:
		0	Disable Automatic baudrate adjustment
		1	Enable Automatic baudrate adjustment
8	SLEEP		SCI sleep SCI compatibility mode only. In a multiprocessor configuration, this bit controls the receive sleep function. Clearing this bit brings the SCI out of sleep mode.
		0	Sleep mode is disabled.
		1	Sleep mode is enabled.
			The receiver still operates when the SLEEP bit is set; however, RXRDY is updated and SCIRD is loaded with new data only when an address frame is detected. The remaining receiver status flags (see Table 7) are updated and an error interrupt is requested if the corresponding interrupt enable bit is set, regardless of the value of the SLEEP bit. In this way, if an error is detected on the receive data line while the SCI is asleep, software can promptly deal with the error condition. The SLEEP bit is not automatically cleared when an address byte is detected.
7	SWnRESET		Software reset (active low). This bit is effective in LIN and SCI modes.
		0	The SCI/BLIN is in its reset state; no data will be transmitted or received. Writing a 0 to this bit initializes the SCI state machines and operating flags as defined in Table 7 and Table 8 . All affected logic is held in the reset state until a 1 is written to this bit.
		1	The SCI/BLIN is in its ready state; transmission and reception can be done. The configuration of the module should not change. Only the following configuration bits can be changed in runtime (i.e., while SW nRESET = 1): • STOP EXT Frame (SCIGCR1[13];) • CC bit (SCIGCR2[17];) • SC bit (SCIGCR2[16];) **Note**: The SCI/ BLIN should only be configured while SW nRESET = 0.

Table 6. SCI Global Control Register (SCIGCR1) Field Descriptions (continued)

Bit	Field	Value	Description
6	LIN MODE		LIN mode
			This bit controls the module mode of operation.
		0	LIN mode is disabled; SCI compatibility mode is enabled.
		1	LIN mode is enabled; SCI compatibility mode is disabled.
5	CLK_MASTER		SCI internal clock enable or LIN Master/Slave configuration.
			In the SCI mode, this bit enables the clock to the SCI module. In LIN mode, this bit determines whether a LIN node is a slave or master.
			SCI-compatible mode
		0	Reserved.
		1	Enable clock to the SCI module.
			LIN mode
		0	The node is in slave mode.
		1	The node is in master mode.
4	STOP		SCI number of stop bits. This bit specifies the number of stop bits transmitted.
			This bit is effective in SCI-compatible mode only.
		0	One stop bit is used.
		1	Two stop bits are used.
			Note: The receiver checks for only one stop bit. However in idle-line mode, the receiver waits until the end of the second stop bit (if STOP = 1) to begin checking for an idle period.
3	PARITY		SCI parity odd/even selection.
			SCI-Compatible mode only. If the PARITY ENA bit (SCIGCR1.2) is set, PARITY designates odd or even parity.
		0	Odd parity is used.
		1	Even parity is used.
			Note: The parity bit is calculated based on the data bits in each frame and the address bit (in address-bit mode). The start and stop fields in the frame are not included in the parity calculation.
			Note: For odd parity, the SCI transmits and expects to receive a value in the parity bit that makes odd the total number of bits in the frame with the value of 1.
			For even parity, the SCI transmits and expects to receive a value in the parity bit that makes even the total number of bits in the frame with the value of 1.
2	PARITY ENA		Parity enable.
			Enables or disables the parity function. Compatible or buffered SCI mode:
			SCI compatibility or buffered SCI mode
		0	Parity disabled; no parity bit is generated during transmission or is expected during reception
		1	Parity enabled. A parity bit is generated during transmission and is expected during reception
			LIN mode
		0	ID-parity verification is disabled.
		1	ID-parity verification is enabled.
1	TIMING MODE		SCI timing mode bit.
			This bit is effective in SCI-compatible mode only. It must be set to 1 when the SCI mode is used. It configures the SCI for asynchronous operation.
		0	Reserved.
		1	Must be set to 1 when module is configured for SCI operation

Table 6. SCI Global Control Register (SCIGCR1) Field Descriptions (continued)

Bit	Field	Value	Description
0	COMM MODE		SCI/BLIN communication mode bit.
			In compatibility mode, it selects the SCI communication mode. In LIN mode it selects length control option for ID-field bits ID4 and ID5.
			SCI-compatible mode:
		0	Idle-line mode is used.
		1	Address-bit mode is used.
			See the SCI document for more information on these communication modes.
			LIN mode
		0	ID4 and ID5 are not used for length control.
		1	ID4 and ID5 are used for length control.

Table 7. SCI Receiver Status Flags

SCI Flag	Register	Bit	Value After SW nRESET[1]
CE	SCIFLR	29	0
ISFE	SCIFLR	28	0
NRE	SCIFLR	27	0
FE	SCIFLR	26	0
OE	SCIFLR	25	0
PE	SCIFLR	24	0
RXWAKE	SCIFLR	12	0
RXRDY	SCIFLR	9	0
BUSY	SCIFLR	3	0
IDLE	SCIFLR	2	1
WAKE UP	SCIFLR	1	0
BRKDT	SCIFLR	0	0

(1) The flags are frozen with their reset value while SW nRESET = 0.

Table 8. SCI Transmitter Status Flags

SCI Flag	Register	Bit	Value After SW nRESET[1]
BE	SCIFLR	31	0
PBE	SCIFLR	30	0
TX WAKE	SCIFLR	10	0
TX EMPTY	SCIFLR	11	1
TXRDY	SCIFLR	8	1

(1) The flags are frozen with their reset value while SW nRESET = 0.

6.3 SCI Global Control Register (SCIGCR2)

The SCIGCR2 register is used to send or compare a checkbyte during extended frames, to generate a wakeup and for low-power mode control of the LIN module.

The SCI Global Control Register (SCIGCR2) is shown in Figure 23 and described in Table 9.

Figure 23. SCI Global Control Register (SCIGCR2)

31	18	17	16
Reserved		CC	SC
R-0		R/W-L0	R/WL-0

15	9	8	7	1	0
Reserved		GENWU	Reserved		POWER DOWN
R-0		R/W-0	R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 9. SCI Global Control Register (SCIGCR2) Field Descriptions

Bit	Field	Value	Description
31-18	Reserved		Reads return zero and writes have no effect.

Table 9. SCI Global Control Register (SCIGCR2) Field Descriptions (continued)

Bit	Field	Value	Description
17	CC		Compare Checksum. LIN mode only. This bit is used by the receiver for extended frames to trigger a checksum compare. The user will initiate this transaction by writing a one to this bit. In non multibuffer mode, once the CC bit is set, the checksum will be compared on the byte that is currently being received, expected to be the checkbyte. During MultiBuffer mode, following are the scenarios associated with the "CC" bit : • If "Compare Checksum" bit is set during the reception of the data, then the byte that is received after the reception of the programmed no. of data bytes indicated by SCIFORMAT[18:16], is treated as a checksum byte. • If "Compare Checksum" bit is set during the IDLE period (i.e. during inter-frame space), then the next immediate byte will be treated as a checksum byte. A CE will immediatly be flagged if there is a checksum error. This bit is automatically cleared once the checksum is successfully compared. See Section 2.5 for more details.
		0	No effect
		1	Compare checksum on expected checkbyte
16	SC		Send Checksum LIN mode only. This bit is used by the transmitter with extended frames to send a checkbyte. In non multibuffer mode the checkbyte will be sent after the current byte transmission. In multibuffer mode the checkbyte will be sent after the last byte count, indicated by the SCIFORMAT[18:16]). See Section 2.5 for more details. This bit will be cleared after the checkbyte has been transmitted.
		0	No checkbyte will be sent.
		1	A checkbyte will be sent.
15-9	Reserved		Reads return zero and writes have no effect.
8	GEN WU		Generate wakeup signal. This bit controls the generation of a wakeup signal, by transmitting the TDO buffer value. This bit is cleared on reception of a valid synch break. EALLOW-protected and normal mode Write:
		0	No effect
		1	Transmit TDO for wakeup The bit will be cleared on a SWnRST (SCIGCR1.7)
7-1	Reserved		Reads return zero and writes have no effect.
0	POWERDOWN		Power down. This bit is effective in LIN or SCI-compatible mode. When the powerdown bit is set, the SCI/BLIN module attempts to enter local low-power mode. If the POWERDOWN bit is set while the receiver is actively receiving data and the wakeup interrupt is disabled, then the SCI/BLIN will delay low-power mode from being entered until completion of reception. In LIN mode the user may set the POWERDOWN bit on Sleep Command reception or on idle bus detection (more than 4 seconds, i.e. 80,000 cycles at 20kHz). See Section 4 for more information on low-power mode. EALLOW-protected and normal mode Write:
		0	Normal operation
		1	Request local low-power mode

6.4 SCI Set Interrupt Register (SCISETINT)

This register is used to enable interrupts.

The SCI Set Interrupt Register (SCISETINT) is shown in Figure 24 and described in Table 10.

Figure 24. SCI Set Interrupt Register (SCISETINT)

31	30	29	28	27	26	25	24
SET BE INT	SET PBE INT	SET CE INT	SETISFE INT	SET NRE INT	SET FE INT	SET OE INT	SET PE INT
R/WL-0	R/WL-0	R/WL-0	R/WL-0	R/WL-0	R/W-0	R/W-0	R/W-0

23	16
Reserved	
R-0	

15	14	13	12	10	9	8
Reserved		SET ID INT	Reserved		SET RX INT	SET TX INT
R-0		R/WL-0	R-0		R/W-0	R/W-0

7	6	5	4	3	2	1	0
SET TOA3 WUS INT	SET TOA WUS INT	Reserved	SETTIMEOUT INT	Reserved		SET WAKE UP INT	SET BRKDT INT
R/WL-0	R/WL-0	R-0	R/WL-0	R-0		R/W-0	R/WC-0

LEGEND: R/W = Read/Write; R = Read only; WL = Write in LIN mode only; WC = Write in sci-compatible mode only; -*n* = value after reset

Table 10. SCI Set Interrupt Register (SCISETINT) Field Descriptions

Bit	Field	Value	Description
31	SET BE INT		Set bit error interrupt.
			This bit is effective in LIN mode only. Setting this bit enables the SCI/BLIN module to generate an interrupt when there is a bit error.
			Normal and EALLOW mode (read):
		0	Interrupt is disabled
		1	Interrupt is enabled
			Normal and EALLOW mode (write):
		0	leaves the corresponding bit unchanged
		1	enable interrupt
30	SET PBE INT		Set physical bus error interrupt.
			This bit is effective in LIN mode only. Setting this bit enables the SCI/BLIN module to generate an interrupt when a physical bus error occurs.
			Normal and EALLOW mode (read):
		0	Interrupt is disabled
		1	Interrupt is enabled
			Normal and EALLOW mode (write):
		0	leaves the corresponding bit unchanged
		1	enable interrupt
29	SET CE INT		Set checksum-error Interrupt.
			This bit is effective in LIN mode only. Setting this bit enables the SCI/BLIN module to generate an interrupt when there is a checksum error.
			Normal and EALLOW mode (read):
		0	Interrupt is disabled
		1	Interrupt is enabled
			Normal and EALLOW mode (write):
		0	leaves the corresponding bit unchanged
		1	enable interrupt

Table 10. SCI Set Interrupt Register (SCISETINT) Field Descriptions (continued)

Bit	Field	Value	Description
28	SET ISFE INT		Set inconsistent-synch-field-error interrupt.
			This bit is effective in LIN mode only. Setting this bit enables the SCI/BLIN module to generate an interrupt when there is an inconsistent synch field error.
			Normal and EALLOW mode (read):
		0	Interrupt is disabled
		1	Interrupt is enabled
			Normal and EALLOW mode (write):
		0	leaves the corresponding bit unchanged
		1	enable interrupt
27	SET NRE INT		Set no-response-error interrupt.
			This bit is effective in LIN mode only. Setting this bit enables the SCI/BLIN module to generate an interrupt when a no-response error occurs.
			Normal and EALLOW mode (read):
		0	Interrupt is disabled
		1	Interrupt is enabled
			Normal and EALLOW mode (write):
		0	leaves the corresponding bit unchanged
		1	enable interrupt
26	SET FE INT		Set framing-error interrupt.
			This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/BLIN module to generate an interrupt when a framing error occurs.
			Normal and EALLOW mode (read):
		0	Interrupt is disabled
		1	Interrupt is enabled
			Normal and EALLOW mode (write):
		0	leaves the corresponding bit unchanged
		1	enable interrupt
25	SET OE INT		Set overrun-error interrupt.
			This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/BLIN module to generate an interrupt when an overrun error occurs.
			Normal and EALLOW mode (read):
		0	Interrupt is disabled
		1	Interrupt is enabled
			Normal and EALLOW mode (write):
		0	leaves the corresponding bit unchanged
		1	enable interrupt
24	SET PE INT		Set parity interrupt.
			This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/BLIN module to generate an interrupt when a parity error occurs.
			Normal and EALLOW mode (read):
		0	Interrupt is disabled
		1	Interrupt is enabled
			Normal and EALLOW mode (write):
		0	leaves the corresponding bit unchanged
		1	enable interrupt
23-14	Reserved		These bits are always read as 0. Writes have no effect.

Table 10. SCI Set Interrupt Register (SCISETINT) Field Descriptions (continued)

Bit	Field	Value	Description
13	SET ID INT		LIN mode only. This bit is set to enable interrupt once a valid matching identifier is received see Section 2.8 for more details. Normal and EALLOW mode (read): 0 interrupt is disabled 1 interrupt is enabled Normal and EALLOW mode (write): 0 leaves the corresponding bit unchanged 1 enable interrupt
12-10	Reserved		These bits are always read as 0. Writes have no effect.
9	SET RX INT		Receiver interrupt enable. Setting this bit enables the SCI to generate a receive interrupt after a frame has been completely received and the data is being transferred from SCIRXSHF to SCIRD. Normal and EALLOW mode (read): 0 Interrupt is disabled 1 Interrupt is enabled Normal and EALLOW mode (write): 0 leaves the corresponding bit unchanged 1 enable interrupt
8	SET TX INT		Set Transmitter interrupt. Setting this bit enables the SCI/ BLIN to generate a transmit interrupt as data is being transferred from SCITD to SCITXSHF and the TXRDY bit is being set. Normal and EALLOW mode (read): 0 Interrupt is disabled 1 Interrupt is enabled Normal and EALLOW mode (write): 0 leaves the corresponding bit unchanged 1 enable interrupt
7	SET TOA3WUS INT		Set Timeout After 3 Wakeup Signals interrupt. LIN mode only. Setting this bit enables the BLIN to generate an interrupt when there is a timeout after 3 wakeup signals have been sent. Normal and EALLOW mode (read): 0 Interrupt is disabled 1 Interrupt is enabled Normal and EALLOW mode (write): 0 leaves the corresponding bit unchanged 1 enable interrupt
6	SET TOAWUS INT		Set Timeout After Wakeup Signal interrupt. LIN mode only. Setting this bit enables the BLIN to generate an interrupt when there is a timeout after one wakeup signal has been sent. Normal and EALLOW mode (read): 0 Interrupt is disabled 1 Interrupt is enabled Normal and EALLOW mode (write): 0 leaves the corresponding bit unchanged 1 enable interrupt
5	Reserved		These bits are always read as 0. Writes have no effect

Table 10. SCI Set Interrupt Register (SCISETINT) Field Descriptions (continued)

Bit	Field	Value	Description
4	SET TIMEOUT INT		Set timeout interrupt. This bit is effective in LIN mode only. Setting this bit enables the SCI/BLIN to generate an interrupt when no LIN bus activity occurs for at least four seconds. Normal and EALLOW mode (read): 0 Interrupt is disabled 1 Interrupt is enabled Normal and EALLOW mode (write): 0 leaves the corresponding bit unchanged 1 enable interrupt
3-2	Reserved		These bits are always read as 0. Writes have no effect
1	SET WAKEUP INT		Set wakeup interrupt. This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/BLIN to generate a wake-up interrupt and thereby exit low-power mode. The wakeup interrupt is asserted on falling edge of the wakeup pulse. If enabled, the wake-up interrupt is asserted when local low-power mode is requested while the receiver is busy or if a low level is detected on the LINRX pin during low-power mode. Wakeup interrupt is not asserted upon a wakeup pulse if the module is not in power down mode. Normal and EALLOW mode (read): 0 Interrupt is disabled 1 Interrupt is enabled Normal and EALLOW mode (write): 0 leaves the corresponding bit unchanged 1 enable interrupt
0	SET BRKDT INT		Set break-detect interrupt. This bit is effective in SCI-compatible mode only. Setting this bit enables the SCI/BLIN to generate an error interrupt if a break condition is detected on the LINRX pin. Normal and EALLOW mode (read): 0 Interrupt is disabled 1 Interrupt is enabled Normal and EALLOW mode (write): 0 leaves the corresponding bit unchanged 1 enable interrupt

6.5 SCI Clear Interrupt Register (SCICLEARINT)

This register is used to disable interrupts. The SCI Clear Interrupt Register (SCICLEARINT) is shown in Figure 25 and described in Table 11.

Caution should be exercised while modifying the SCICLEARINT register to avoid disabling interrupts inadvertently. This is because of the READ-MODIFY-WRITE performed by the OR instruction generated by the compiler. Specifically, individual bits of the SCICLEARINT register should not be written to. One should also not use the OR ("|") in C, while modifying the SCICLEARINT register.

The following example statements should not be used:

```
Case 1: LinaRegs.SCICLEARINT.bit.CLRFEINT = 1; Case 2: LinaRegs.SCICLEARINT.all |= 0x04000000;
```

The following example statements work fine:

```
Case 1: LinaRegs.SCICLEARINT.all = 0x04000000; Case 2: LinaRegs.SCICLEARINT.all &= 0x04000000;
Case 3: *(Uint32 *)0x6C08 = 0x04000000;
```

Figure 25. SCI Clear Interrupt Register (SCICLEARINT)

31	30	29	28	27	26	25	24
CLR BE INT	SET PBE INT	CLR CE INT	CLRISFE INT	CLR RE INT	CLR FE INT	CLR OE INT	CLR PE INT
R/WL-0	R/WL-0	R/WL-0	R/WL-0	R/WL-0	R/W-0	R/W-0	R/W-0

23	16
Reserved	
R-0	

15	14	13	12	10	9	8
Reserved		CLR ID INT	Reserved		CLR RX INT	CLR TX INT
R-0		R/WL-0	R-0		R/W-0	R/W-0
					R/W-0	R/W-0

7	6	5	4	3	2	1	0
CLR TOA3 WUS INT	CLR TOA WUS INT	Reserved	CLRTIMEOUT INT	Reserved		CLR WAKE UP INT	CLR BRKDT INT
R/WL-0	R/WL-0	R-0	R/WL-0	R-0		R/W-0	R/WC-0

LEGEND: R/W = Read/Write; R = Read only; WC = Write in sci-compatible mode only; WL = Write in LIN mode only; -*n* = value after reset

Table 11. SCI Clear Interrupt Register (SCICLEARINT) Field Descriptions

Bit	Field	Value	Description
31	CLR BE INT		Clear Bit Error Interrupt.
			LIN mode only. This bit disables the bit error interrupt when set.
			Normal and EALLOW mode (read):
		0	Interrupt is disabled
		1	Interrupt is enabled
			Normal and EALLOW mode (write):
		0	leaves the corresponding bit unchanged
		1	disable interrupt
30	CLR PBE INT		Clear Physical Bus Error Interrupt.
			LIN mode only. This bit disables the physical-bus error interrupt when set.
			Normal and EALLOW mode (read):
		0	Interrupt is disabled
		1	Interrupt is enabled
			Normal and EALLOW mode (write):
		0	leaves the corresponding bit unchanged
		1	disable interrupt
29	CLR CE INT		Clear checksum-error Interrupt.
			LIN mode only. This bit disables the checksum interrupt when set.
			Normal and EALLOW mode (read):
		0	Interrupt is disabled
		1	Interrupt is enabled
			Normal and EALLOW mode (write):
		0	leaves the corresponding bit unchanged
		1	disable interrupt

Table 11. SCI Clear Interrupt Register (SCICLEARINT) Field Descriptions (continued)

Bit	Field	Value	Description
28	CLR ISFE INT		Clear Inconsistent-Synch-Field-Error Interrupt.
			LIN mode only. This bit disables the ISFE interrupt when set.
			Normal and EALLOW mode (read):
		0	Interrupt is disabled
		1	Interrupt is enabled
			Normal and EALLOW mode (write):
		0	leaves the corresponding bit unchanged
		1	disable interrupt
27	CLR NRE INT		Clear No-Reponse-Error Interrupt.
			LIN mode only. Setting this bit disables the BLIN module to generate an interrupt when there is a No-Response error.
			Normal and EALLOW mode (read):
		0	Interrupt is disabled
		1	Interrupt is enabled
			Normal and EALLOW mode (write):
		0	leaves the corresponding bit unchanged
		1	disable interrupt
26	CLR FE INT		Clear Framing-Error Interrupt.
			Setting this bit disables the SCI/BLIN module to generate an interrupt when there is a Framing error.
			Normal and EALLOW mode (read):
		0	Interrupt is disabled
		1	Interrupt is enabled
			Normal and EALLOW mode (write):
		0	leaves the corresponding bit unchanged
		1	disable interrupt
25	CLR OE INT		Clear Overrun-Error Interrupt.
			This bit disables the SCI/ BLIN overrun interrupt when set.
			Normal and EALLOW mode (read):
		0	Interrupt is disabled
		1	Interrupt is enabled
			Normal and EALLOW mode (write):
		0	leaves the corresponding bit unchanged
		1	disable interrupt
24	CLR PE INT		Clear Parity Interrupt.
			Setting this bit disables the BLIN /SCI Parity error interrupt.
			Normal and EALLOW mode (read):
		0	Interrupt is disabled
		1	Interrupt is enabled
			Normal and EALLOW mode (write):
		0	leaves the corresponding bit unchanged
		1	disable interrupt
23-14	Reserved		These bits are always read as 0. Writes have no effect.

Table 11. SCI Clear Interrupt Register (SCICLEARINT) Field Descriptions (continued)

Bit	Field	Value	Description
13	CLR ID INT		LIN mode only.
			This bit disables the ID interrupt when set.
			Normal and EALLOW mode (read):
		0	interrupt is disabled
		1	interrupt is enabled
			Normal and EALLOW mode (write):
		0	leaves the corresponding bit unchanged
		1	disable interrupt
12-10	Reserved		These bits are always read as 0. Writes have no effect.
9	CLR RX INT		Clear Receiver interrupt.
			This bit disables the receiver interrupt when set.
			Normal and EALLOW mode (read):
		0	Interrupt is disabled
		1	Interrupt is enabled
			EALLOW mode (write):
		0	leaves the corresponding bit unchanged
		1	disable interrupt
8	CLR TX INT		Clear Transmitter interrupt.
			This bit disables the transmitter interrupt when set.
			Normal and EALLOW mode (read):
		0	Interrupt is disabled
		1	Interrupt is enabled
			Normal and EALLOW mode (write):
		0	leaves the corresponding bit unchanged
		1	disable interrupt
7	CLR TOA3WUS INT		Clear Timeout After 3 Wakeup Signals interrupt.
			LIN mode only. Setting this bit disables the timeout after 3 wakeup signals interrupt.
			Normal and EALLOW mode (read)
		0	Interrupt is disabled
		1	Interrupt is enabled
			Normal and EALLOW mode (write):
		0	leaves the corresponding bit unchanged
		1	disable interrupt
6	CLR TOAWUS INT		Clear Timeout After Wakeup Signal interrupt.
			LIN mode only. Setting this bit disables the timeout after one wakeup signal interrupt.
			Normal and EALLOW mode (read):
		0	Interrupt is disabled
		1	Interrupt is enabled
			Normal and EALLOW mode (write):
		0	leaves the corresponding bit unchanged
		1	disable interrupt
5	Reserved		These bits are always read as 0. Writes have no effect.

Table 11. SCI Clear Interrupt Register (SCICLEARINT) Field Descriptions (continued)

Bit	Field	Value	Description
4	CLR TIMEOUT INT		Clear Timeout interrupt. LIN mode only. Setting this bit disables the timeout (LIN bus idle) interrupt. Normal and EALLOW mode (read): 0 Interrupt is disabled 1 Interrupt is enabled Normal and EALLOW mode (write): 0 leaves the corresponding bit unchanged 1 disable interrupt
3-2	Reserved		These bits are always read as 0. Writes have no effect.
1	CLR WAKEUP INT		Clear Wake-up interrupt. This bit disables the wakeup interrupt when set. Normal and EALLOW mode (read): 0 Interrupt is disabled 1 Interrupt is enabled Normal and EALLOW mode (write): 0 leaves the corresponding bit unchanged 1 disable interrupt
0	CLR BRKDT INT		Clear Break-detect interrupt. Compatibility mode. This bit disables the Break-detect interrupt when set. Normal and EALLOW mode (read): 0 Interrupt is disabled 1 Interrupt is enabled Normal and EALLOW mode (write): 0 leaves the corresponding bit unchanged 1 disable interrupt

6.6 SCI Set Interrupt Level Register (SCISETINTLVL)

The SCI Set Interrupt Level Register (SCISETINTLVL) is shown in Figure 26 and described in Table 12.

Figure 26. SCI Set Interrupt Level Register (SCISETINTLVL)

31	30	29	28	27	26	25	24
SET BE INT LVL	SET PBE INT LVL	SET CE INT LVL	SET ISFE INT LVL	SET NRE INT LVL	SET FE INT LVL	SET OE INT LVL	SET PE INT LVL

23	16
Reserved	
R-0	

15	14	13	12	11	10	9	8
Reserved		SET ID INT LVL	Reserved			SET RX INT LVL	SET TX INT LVL
R-0			R-0				

7	6	5	4	3	2	1	0
SETTOA3WUS INT LVL	SETTOAWUS INT LVL	Reserved	SETTIMEOUT INT LVL	Reserved		SET WAKE UP INT LVL	SET BRKDT INT LVL
		R-0		R-0			

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 12. SCI Set Interrupt Level Register (SCISETINTLVL) Field Descriptions

Bit	Field	Value	Description
31	SET BE INT LV		Set Bit Error Interrupt Level.
			LIN mode only.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Set interrupt level to line INT1
30	SET PBE INT LVL		Set Physical Bus Error Interrupt Level.
			LIN mode only.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Set interrupt level to line INT1
29	SET CE INT LVL		Set checksum-error Interrupt Level.
			LIN mode only.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Set interrupt level to line INT1
28	SET ISFE INT LVL		Set Inconsistent-Synch-Field-Error Interrupt Level.
			LIN mode only.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Set interrupt level to line INT1
27	SET NRE INT LVL		Set No-Reponse-Error Interrupt Level.
			LIN mode only.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Set interrupt level to line INT1
26	SET FE INT LVL		Set Framing-Error Interrupt Level.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Set interrupt level to line INT1

Table 12. SCI Set Interrupt Level Register (SCISETINTLVL) Field Descriptions (continued)

Bit	Field	Value	Description
25	SET OE INT LVL		Set Overrun-Error Interrupt Level.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Set interrupt level to line INT1
24	SET PE INT LVL		Set Parity Error Interrupt Level.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Set interrupt level to line INT1
23-14	Reserved		These bits are always read as 0. Writes have no effect.
13	SET ID INT LVL		Set ID interrupt level.
			LIN mode only.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Set interrupt level to line INT1
12-10	Reserved		This bit is always read as 0. Writes have no effect.
9	SET RX INT LVL		Set Receiver interrupt Level.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Set interrupt level to line INT1
8	SET TX INT LVL		Set Transmitter interrupt Level.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Set interrupt level to line INT1
7	SET TOA3WUS INT LVL		Set Timeout After 3 Wakeup Signals interrupt Level.
			LIN mode only.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Set interrupt level to line INT1

Table 12. SCI Set Interrupt Level Register (SCISETINTLVL) Field Descriptions (continued)

Bit	Field	Value	Description
6	SET TOAWUS INT LVL		Set Timeout After Wakeup Signal interrupt Level.
			LIN mode only.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Set interrupt level to line INT1
5	Reserved		This bit is always read as 0. Writes have no effect.
4	SET TIMEOUT INT LVL		Set Timeout interrupt Level.
			LIN mode only
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Set interrupt level to line INT1
3-2	Reserved		These bits are always read as 0. Writes have no effect.
1	SET WAKEUP INT LVL		Set Wake-up interrupt Level
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Set interrupt level to line INT1
0	SET BRKDT INT		Set Break-detect interrupt Level.
			Compatible mode only.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Set interrupt level to line INT1

6.7 SCI Clear Interrupt Level Register (SCICLEARINTLVL)

The SCI Clear Interrupt Level Register (SCICLEARINTLVL) is shown in Figure 27 and described in Table 13.

Figure 27. SCI Clear Interrupt Level Register (SCICLEARINTLVL)

31	30	29	28	27	26	25	24
CLR BE INT LVL	CLR PBE INT LVL	CLR CE INT LVL	CLR ISFE INT LVL	CLR NRE INT LVL	CLR FE INT LVL	CLR OE INT LVL	CLR PE INT LVL
R/WL-0	R/WL-0	R/WL-0	R/WL-0	R/WL-0	R/W-0	R/W-0	R/W-0

23	16
Reserved	
R-0	

15	14	13	12	10	9	8
Reserved		CLR ID INT LVL	Reserved		CLR RX INT LVL	CLR TX INT LVL
R-0		R/WL-0	R-0		R/W-0	R/W-0

7	6	5	4	3	2	1	0
CLRTOA3WUS INT LVL	CLRTOAWUS INT LVL	Reserved	CLRTIMEOUT INTLVL	Reserved		CLR WAKE UP INT LVL	CLR BRKDT INT LVL
R/WL-0	R/WL-0	R-0	R/WL-0	R-0		R/W-0	R/WC-0

LEGEND: R/W = Read/Write; R = Read only; WC = Write in sci-compatible mode only; WL = Write in LIN mode only; -*n* = value after reset

Table 13. SCI Clear Interrupt Level Register (SCICLEARINTLVL) Field Descriptions

Bit	Field	Value	Description
31	CLR BE INT LVL		Clear Bit Error Interrupt Level.
			LIN mode only.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Reset interrupt level to line INT0
30	CLR PBE INT LVL		Clear Physical Bus Error Interrupt Level.
			LIN mode only.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Normal and EALLOW mode (write):
		1	Reset interrupt level to line INT0
29	CLR CE INT LVL		Clear checksum-error Interrupt Level. LIN mode only.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Reset interrupt level to line INT0

Table 13. SCI Clear Interrupt Level Register (SCICLEARINTLVL) Field Descriptions (continued)

Bit	Field	Value	Description
28	CLR ISFE INT LVL		Clear Inconsistent-Synch-Field-Error Interrupt Level.
			LIN mode only.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Reset interrupt level to line INT0
27	CLR NRE INT LVL		Clear No-Reponse-Error Interrupt Level.
			LIN mode only.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Reset interrupt level to line INT0
26	CLR FE INT LVL		Clear Framing-Error Interrupt Level.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Reset interrupt level to line INT0
25	CLR OE INT LVL		Clear Overrun-Error Interrupt Level.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Reset interrupt level to line INT0
24	CLR PE INT LVL		Clear Parity Error Interrupt Level.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Reset interrupt level to line INT0
23-14	Reserved		These bits are always read as 0. Writes have no effect.
13	CLR ID INT LVL		Clear ID interrupt level.
			LIN mode only.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Reset interrupt level to line INT0
12-10	Reserved		These bits are always read as 0. Writes have no effect.

Table 13. SCI Clear Interrupt Level Register (SCICLEARINTLVL) Field Descriptions (continued)

Bit	Field	Value	Description
9	CLR RX INT LVL		Clear Receiver interrupt Level.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Reset interrupt level to line INT0
8	CLR TX INT LVL		Clear Transmitter interrupt Level.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Reset interrupt level to line INT0
7	CLR TOA3WUS INT LVL		Clear Timeout After 3 Wakeup Signals interrupt Level. .
			LIN mode only
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Reset interrupt level to line INT0
6	CLR TOAWUS INT LVL		Clear Timeout After Wakeup Signal interrupt Level.
			LIN mode only.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Reset interrupt level to line INT0
5	Reserved		These bits are always read as 0. Writes have no effect.
4	CLR TIMEOUT INT LVL		Clear Timeout interrupt Level.
			LIN mode only
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Reset interrupt level to line INT0
3-2	Reserved		These bits are always read as 0. Writes have no effect.
1	CLR WAKEUP INT LVL		Clear Wake-up interrupt Level
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Reset interrupt level to line INT0

Table 13. SCI Clear Interrupt Level Register (SCICLEARINTLVL) Field Descriptions (continued)

Bit	Field	Value	Description
0	CLR BRKDT INT		Clear Break-detect interrupt Level.
			Compatible mode only.
			Normal and EALLOW mode (read):
		0	Interrupt level mapped to INT0 line
		1	Interrupt level mapped to INT1 line
			Normal and EALLOW mode (write):
		0	Leaves the corresponding bit unchanged
		1	Reset interrupt level to line INT0

6.8 SCI Flags Register (SCIFLR)

The SCI Flags Register (SCIFLR) is shown in Figure 28 and described in Table 14.

Figure 28. SCI Flags Register (SCIFLR)

31	30	29	28	27	26	25	24
BE	PBE	CE	ISFE	NRE	FE	OE	PE
R/WL-0	R/WL-0	R/WL-0	R/WL-0	R/WL-0	R/W-0	R/W-0	R/W-0
23							16
Reserved							
R-0							
15	14	13	12	11	10	9	8
Reserved	RX ID	TX ID	RX WAKE	TX EMPTY	TX WAKE	RX RDY	TX RDY
R-0	R/WL-0	R/WL-0	R/WC-0	R/W-1	R/WC-0	R/W-0	R/W-1
7	6	5	4	3	2	1	0
TOA3 WUS	TOA WUS	Reserved	TIMEOUT	BUSY	IDLE	WAKE UP	BRKDT
R/WL-0	R/WL-0	R-0	R/WL-0	R/W-0	R/WC-0	R/WL-0	R/WC-0

LEGEND: R/W = Read/Write; R = Read only; WC = Write in sci-compatible mode only; WL = Write in LIN mode only; -*n* = value after reset

Table 14. SCI Flags Register (SCIFLR) Field Descriptions

Bit	Field	Value	Description
31	BE		Bit Error Flag.
			This bit is set when there has been a bit error. This is detected by the bit monitor in TED. See Section 2.7 for more information. The Bit Error flag is cleared by reading the corresponding interrupt offset in the SCIINTVECT0/1 register, by the RESET bit, by the SW nRESET bit, by a system reset or by writing a 1 to this bit.
			Read:
		0	No bit error detected
		1	Bit error detected
			Write:
		0	No effect
		1	Clears this bit to 0

Table 14. SCI Flags Register (SCIFLR) Field Descriptions (continued)

Bit	Field	Value	Description
30	PBE		Physiscal Bus Error Flag. LIN mode only. This bit is set when there has been a physical bus error. This is detected by the bit monitor in TED. See Section 2.7 for more information. The Physical Bus Error flag is cleared by reading the corresponding interrupt offset in the SCIINTVECT0/1 register, by the RESET bit, by the SW nRESET bit, by a system reset or by writing a 1 to this bit. Read:
		0	No physiscal bus error detected
		1	Physical Bus error detected
			Write:
		0	No effect
		1	Clears this bit to 0
29	CE		Checksum Error Flag. LIN mode only. This bit is set when there is checksum error detected by a receiving node. This is detected by the TED logic. See Section 2.7 , for more information. The type of checksum to be used depends on the SCIGCR1.CTYPE bit. The Checksum Error flag is cleared by reading the corresponding interrupt offset in the SCIINTVECT0/1 register, by the RESET bit, by the SW nRESET bit, by a system reset or by writing a 1 to this bit. Read:
		0	No Checksum error detected
		1	Checksum error detected
			Write:
		0	No effect
		1	Clears this bit to 0
28	ISFE		Inconsistent Synch Field Error Flag. LIN mode only. This bit is set when there has been an inconsistent Synch Field error detected by the Synchronizer during Header reception. See section 1.5.2.3, "Header Reception and Adaptive Baudrate" , for more information. The Inconsistent Synch Field Error flag is cleared by reading the corresponding interrupt offset in the SCIINTVECT0/1 register, by the RESET bit, by the SW nRESET bit, by a system reset or by writing a 1 to this bit. Read:
		0	No Inconsistent Synch Field error detected
		1	Inconsistent Synch Field error detected
			Write:
		0	No effect
		1	Clears this bit to 0
27	NRE		No-Response Error Flag. LIN mode only. This bit is set when there is no response to a master's Header completed within T_{FRAME_MAX}. This timeout period is applied for message frames of known length (identifiers 0 to 61). This is detected by the Synchronizer. See Section 2.6 , for more information. The No-Response Error flag is cleared by reading the corresponding interrupt offset in the SCIINTVECT0/1 register, by the RESET bit, by the SW nRESET bit, by a system reset or by writing a 1 to this bit. Read:
		0	No No-Response error detected
		1	No-Repsonse error detected
			Write:
		0	No effect
		1	Clears this bit to 0

Table 14. SCI Flags Register (SCIFLR) Field Descriptions (continued)

Bit	Field	Value	Description
26	FE		Framing error flag. This bit is effective in LIN or SCI-compatible mode. This bit is set when an expected stop bit is not found. In SCI compatible mode, only the first stop bit is checked. The missing stop bit indicates that synchronization with the start bit has been lost and that the character is incorrectly framed. Detection of a framing error causes the SCI to generate an error interrupt if the RXERR INT ENA bit is set. The framing error flag is cleared by reading the corresponding interrupt offset in the SCIINTVECT0/1 register, by the RESET bit, by the SW nRESET bit, by a system reset or by writing a 1 to this bit. In multibuffer mode the frame is defined in the SCIFORMAT register. Read:
		0	No framing error detected
		1	Framing error detected
			Write:
		0	No effect
		1	Clears this bit to 0
25	OE		Overrun error flag. This bit is effective in LIN or SCI-compatible mode. This bit is set when the transfer of data from SCIRXSHF to SCIRD overwrites unread data already in SCIRD or the RDy buffers. Detection of an overrun error causes the LIN to generate an error interrupt if the SET OE INT bit is one. The OE flag is reset by reading the corresponding interrupt offset in the SCIINTVECT0/1 register, by the RESET bit, by an active SW nRESET, a system reset, or by writing a 1 to this bit. Read:
		0	No overrun error detected
		1	Overrun error detected
			Write:
		0	No effect
		1	Clears this bit to 0
24	PE		Parity error flag. This bit is effective in LIN or SCI-compatible mode. This bit is set when a parity error is detected in the received data. In address-bit mode, the parity is calculated on the data and address bit fields of the received frame. In idle-line mode, only the data is used to calculate parity. An error is generated when a character is received with a mismatch between the number of 1s and its parity bit. For more information on parity checking, see [1] Section 1.10.3, "SCI Global Control Register (SCIGCR1)". If the parity function is disabled (that is, SCIGCR1.2 = 0), the PE flag is disabled and read as 0. Detection of a parity error causes the LIN to generate an error interrupt if the SET PE INT bit =1. The PE bit is reset by reading the corresponding interrupt offset in the SCIINTVECT0/1 register, by the RESET bit, by an active SW nRESET, a system reset or by writing a 1 to this bit. Read:
		0	No parity error or parity disabled
		1	Parity error detected
			Write:
		0	No effect
		1	Clears this bit to 0
23-15	Reserved		These bits are always read as 0. Writes have no effect.

Table 14. SCI Flags Register (SCIFLR) Field Descriptions (continued)

Bit	Field	Value	Description
14	ID RX Flag		Identifier On Receive Flag. LIN mode only. This flag is set once an identifier is received with an RX match and no ID-parity error. See section 1.5.6, "Message Filtering and Validation" , for more details. When this flag is set it indicates that a new valid identifier has been received on an RX match. This bit is cleared by reading the corresponding interrupt offset in the SCIINTVECT0/1 register, by the RESET bit, by an active SW nRESET, a system reset, by reading the LINID register or by writing a 1 to this bit. Read
		0	No valid ID received
		1	Valid ID RX received in LINID[23:16] on RX match
			Write
		0	No effect
		1	Clears this bit to 0
13	ID TX Flag		Identifier On Transmit Flag. LIN mode only. This flag is set once an identifier is received with a TX match and no ID-parity error. See section 1.5.6, "Message Filtering and Validation", for more details. When this flag is set it indicates that a new valid identifier has been received on a TX match. This bit is cleared by reading the corresponding interrupt offset in the SCIINTVECT0/1 register, by the RESET bit, by an active SW nRESET, a system reset, by reading the LINID register or by writing a 1 to this bit. Read
		0	No valid ID received
		1	Valid ID received in LINID[23:16] on TX match
			Write
		0	No effect
		1	Clears this bit to 0
12	RXWAKE		Receiver wakeup detect flag. Compatible mode only. The SCI sets this bit to indicate that the data currently in SCIRD is an address. RXWAKE is cleared by the RESET bit, by an active SW nRESET, a system reset, or by the SCI upon receipt of a data frame.
		0	The data in SCIRD is not an address.
		1	The data in SCIRD is an address.
			See [1] Section 3.4.4, Sleep Mode for Multiprocessor Communication, on page 16 for more information on using the RXWAKE bit with sleep mode.
11	TX EMPTY		Transmitter Empty flag. The value of this flag indicates the contents of the transmitter's buffer register(s) (SCITD/TDy) and shift register (SCITXSHF). In multibuffer mode, this flag indicates the value of the TDx registers and shift register (SCITXSHF). In non multibuffer mode, this flag indicates the value of LINTDO (byte) and shift register (SCITXSHF). The RESET bit, an active SW nRESET (SCIGCR1.7) or a system reset sets this bit. This bit does not cause an interrupt request. Compatible mode or LIN with no multibuffer.
		0	Transmitter buffer or shift register (or both) are loaded with data.
		1	Transmitter buffer and shift registers are both empty.
			In LIN mode using multibuffer mode
		0	Multibuffer or shift register (or all) are loaded with data
		1	Multibuffer and shift registers are all empty.

Table 14. SCI Flags Register (SCIFLR) Field Descriptions (continued)

Bit	Field	Value	Description
10	TXWAKE		SCI transmitter wakeup method select. Compatibility mode only. The TXWAKE bit controls whether the data in SCITD should be sent as an address or data frame using multiprocessor communication format. This bit is set to 1 or 0 by software before a byte is written to SCITD and is cleared by the SCI when data is transferred from SCITD to SCITXSHF or by a system reset. TXWAKE is not cleared by the SW nRESET bit (SCIGCR1.7). Address-bit mode:
		0	Frame to be transmitted will be data (address bit = 0).
		1	Frame to be transmitted will be an address (address bit=1)
			Idle-line mode:
		0	Frame to be transmitted will be data
		1	Following frame to be transmitted will be an address (writing a 1 to this bit followed by writing dummy data to the SCITD will result in a idle period of 11 bit periods before the next frame is transmitted).
			See Section 3.4, SCI Multiprocessor Communication Modes, on page 12 for more information on using the TXWAKE bit in the available communication modes.
9	RXRDY		Receiver ready flag. In compatibility mode, the receiver sets this bit to indicate that the SCIRD contains new data and is ready to be read by the CPU. In LIN mode, RXRDY is set once a valid frame is received in multibuffer mode, a valid frame being a message frame received with no errors. In non multibuffer mode RXRDY is set for each received byte and will be set for the last byte of the frame if there are no errors. The SCI/BLIN generates a receive interrupt when RXRDY flag bit is set if the interrupt-enable bit is set (SCISETINT.9). RXRDY is cleared by the RESET bit, by an active SW nRESET, a system reset, writing a 1 to this bit, by reading SCIRD in compatibility mode, or by reading last data byte RDy of the response in LIN mode. **Note**: The RXRDY flag cannot be cleared by reading the corresponding interrupt offset in the SCIINTVECT0/1 register. Read:
		0	No new data in SCIRD/RDy
		1	New data ready to be read from SCIRD
			Write:
		0	No effect
		1	Clears this bit to 0
8	TXRDY		Transmitter buffer register ready flag. When set, this bit indicates that the transmit buffer(s) register (SCITD in compatibility mode and LINTDO, LINTD1 in MBUF mode) is/are ready to get another character from a CPU write. In compatibility mode writing data to SCITD automatically clears this bit. In LIN mode, this bit is cleared once byte 0 (TD0) is written to LINTD0. This bit is set after the data of the TX buffer are shifted into the SCITXSHF register. This event can trigger a transmit interrupt, if the interrupt enable bit is set. TXRDY is also set to 1 by the RESET bit, by enabling SW nRESET (SCIGCR1.7) or by a system reset. **Note**: The TXRDY flag cannot be cleared by reading the corresponding interrupt offset in the SCIINTVECT0/1 register. **Note**: The transmit interrupt request can be eliminated until the next series of data is written into the transmit buffers LINTD0 and LINTD1, by disabling the corresponding interrupt via the SCICLEARINT register or by disabling the transmitter via the TXENA bit (SCIGCR1.25=0). Compatible mode:
		0	SCITD is full.
		1	SCITD is ready to receive the next character
			LIN mode:
		0	The multibuffers are full.
		1	The multibuffers are ready to receive the next character(s).
			For more information on transmit interrupt handling, see Section 2.8 for LIN mode.

Table 14. SCI Flags Register (SCIFLR) Field Descriptions (continued)

Bit	Field	Value	Description
7	TOA3WUS		Timeout After 3 Wakeup Signals flag. LIN mode only. This flag is set if there is no Synch Break received after 3 wakeup signals and a period of 1.5 seconds have passed. Such expiration time is used before issuing another round of wakeup signals. This bit is cleared by reading the corresponding interrupt offset in the SCIINTVECT0/1 register, by the RESET bit, by the SW nRESET bit, by a system reset, or by writing a 1 to this bit. See Section 4.3 . Normal and EALLOW mode (read): 0 No timeout after 3 wakeup signals 1 Timeout after 3 wakeup signals and 1.5s time. Normal and EALLOW mode (write): 0 No effect 1 Clears this bit to zero
6	TOAWUS		Timeout After Wakeup Signal flag. LIN mode only. This bit is set if there is no Synch Break received after a wakeup signal has been sent. A minimum of 150ms expiration time is used before issuing another wakeup signal. This bit is cleared by reading the corresponding interrupt offset in the SCIINTVECT0/1 register, by the RESET bit, by the SWnRESET bit, by a system reset, or by writing a 1 to this bit. See Section 4.3 . Normal and EALLOW mode (read): 0 No timeout after one wakeup signal (150 ms) 1 Timeout after one wakeup signal Normal and EALLOW mode (write): 0 No effect 1 Clears this bit to zero
5	Reserved		This bit is always read as 0. Writes have no effect.
4	TIMEOUT		LIN Bus IDLE timeout flag. LIN mode only. This bit is set if there is no LIN bus activity for at least 4 seconds. LIN bus activity being a transition from recessive to dominant. This bit is cleared by reading the corresponding interrupt offset in the SCIINTVECT0/1 register, by the RESET bit, by the SWnRESET bit, by a system reset, or by writing a 1 to this bit. See Section 2.6 . Normal and EALLOW mode (read): 0 No bus idle detected 1 LIN bus idle detected Normal and EALLOW mode (write): 0 No effect 1 Clears this bit to zero
3	BUSY		Bus BUSY flag. This bit is effective in LIN mode and SCI-compatible mode. This bit indicates whether the receiver is in the process of receiving a frame. As soon as the receiver detects the beginning of a start bit, the BUSY bit is set to 1. When the reception of a frame is complete, the BUSY bit is cleared. If SET WAKEUP INT is set and power down is requested while this bit is set, the SCI/BLIN automatically prevents low-power mode from being entered and generates wakeup interrupt. The BUSY bit is controlled directly by the SCI receiver but is cleared by the RESET bit, by an active SWnRESET or by a system reset. 0 Receiver is not currently receiving a frame. 1 Receiver is currently receiving a frame

Table 14. SCI Flags Register (SCIFLR) Field Descriptions (continued)

Bit	Field	Value	Description
2	IDLE		SCI receiver in idle state. Compatible mode only. While this bit is set, the SCI looks for an idle period to resynchronize itself with the bit stream. The receiver does not receive any data while the bit is set. The bus must be idle for 11 bit periods to clear this bit. The SCI enters this state: • After a system reset • After a SCI software reset • After coming out of power down
		0	Idle period detected, the SCI is ready to receive.
		1	Idle period not detected, the SCI will not receive any data.
1	WAKEUP		Wake-up flag. This bit is set by the SCI/BLIN when receiver or transmitter activity has taken the module out of power-down mode. An interrupt is generated if the SET WAKEUP INT bit (SCISETINT.1) is set. It is cleared by the following: • Reading the corresponding interrupt offset in the SCIINTVECT0/1 register. • Setting the SWnRESET bit (SCIGCR1.7 • RESET bit (SCIGCR0.0) • System reset • By writing a 1 to this bit. For more information on low- power mode, see Section 4 Read:
		0	Do not wake up from power-down mode
		1	Wake up from power-down mode
			Write:
		0	No effect
		1	Clears this bit to zero
0	BRKDT		SCI break-detect flag. Compatible mode only This bit is set when the SCI detects a break condition on the LINRX pin. A break condition occurs when the LINRX pin remains continuously low for at least 10 bits after a missing first stop bit, that is, after a framing error. Detection of a break condition causes the SCI to generate an error interrupt if the BRKDT INT ENA bit is set. The BRKDT bit is cleared by the following: • Reading the corresponding interrupt offset in the SCIINTVECT0/1 register. • Setting the SWnRESET bit (SCIGCR1.7) • RESET bit (SCIGCR0.0) • System reset • By writing a 1 to this bit. Read:
		0	No break condition detected
		1	Break condition detected
			Write:
		0	No effect
		1	Clears this bit to 0

6.9 SCI Interrupt Vector Offset 0 (SCIINTVECT0)

The SCI Interrupt Vector Offset 0 (SCIINTVECT0) is shown in Figure 29 and described in Table 15.

Figure 29. SCI Interrupt Vector Offset 0 (SCIINTVECT0)

31	16
Reserved	
R-0	

15	5	4	0
Reserved		INTVECT0	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 15. SCI Interrupt Vector Offset 0 (SCIINTVECT0) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved		Reads return zero and writes have no effect.
4-0	INTVECT0	0–1Fh	Interrupt vector offset for INT0. This register indicates the offset for interrupt line INT0. A read to this register updates its value to the next highest priority pending interrupt in SCIFLR and clears the flag corresponding to the offset that was read. See Table 3 for list of interrupts. **Note**: The flags for the receive (SCIFLR.9) and the transmit (SCIFLR.8) interrupts cannot be cleared by reading the corresponding offset vector in this register (see detailed description in SCIFLR register).

6.10 SCI Interrupt Vector Offset 1 (SCIINTVECT1)

The SCI Interrupt Vector Offset 1 (SCIINTVECT1) is shown in Figure 30 and described in Table 16.

Figure 30. SCI Interrupt Vector Offset 1 (SCIINTVECT1)

31	16
Reserved	
R-0	

15	5	4	0
Reserved		INTVECT1	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 16. SCI Interrupt Vector Offset 1 (SCIINTVECT1) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved		Reads return zero and writes have no effect.
4-0	INTVECT1	0–1Fh	Interrupt vector offset for INT1. This register indicates the offset for interrupt line INT1. A read to this register updates its value to the next highest priority pending interrupt in SCIFLR and clears the flag corresponding to the offset that was read. See Table 3 for list of interrupts. **Note**: The flags for the receive (SCIFLR.9) and the transmit (SCIFLR.8) interrupts cannot be cleared by reading the corresponding offset vector in this register (see detailed description in SCIFLR register).

6.11 SCI Format Control Register (SCIFORMAT)

The SCI Format Control Register (SCIFORMAT) is shown in Figure 31 and described in Table 17.

Figure 31. SCI Format Control Register (SCIFORMAT)

31	19	18	16
Reserved		LENGTH	
R-0		R/W-0	

15	3	2	0
Reserved		CHAR	
R-0		R/WC-0	

LEGEND: R/W = Read/Write; R = Read only; WC = Write in SCI-compatible mode only; -*n* = value after reset

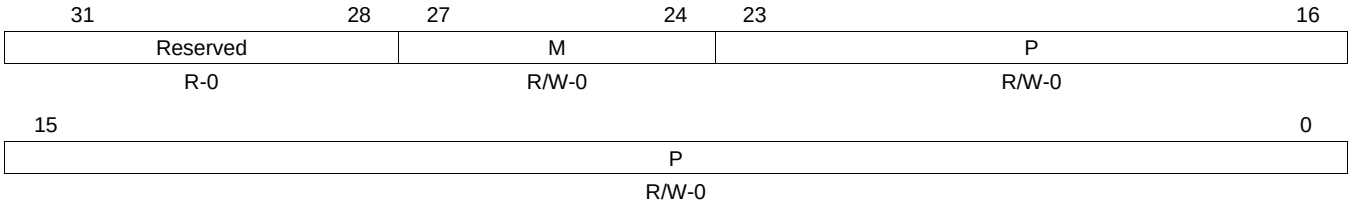
Table 17. SCI Format Control Register (SCIFORMAT) Field Descriptions

Bit	Field	Value	Description
31-19	Reserved		Reads return zero and writes have no effect.
18-16	LENGTH		Frame length control bits. In LIN mode, these bits indicate the number of bytes in the response field from 1 to 8 bytes. In buffered SCI mode, these bits indicate the number of characters. When these bits are used to indicate LIN response length (SCIGCR1[0] = 1), then when there is an ID RX match, this value should be updated with the expected length of the response. In buffered SCI mode, these bits indicate the number of characters with SCIFORMAT[2:0] bits per character. i.e. these bits indicate the transmitter/receiver format for the number of characters: 1 to 8. There can be up to eight characters with eight bits each.
		0h	The response field has 1 bytes/characters.
		1h	The response field has 2 bytes/characters.
		2h	The response field has 3 bytes/characters.
		3h	The response field has 4 bytes/characters.
		4h	The response field has 5 bytes/characters.
		5h	The response field has 6 bytes/characters.
		6h	The response field has 7 bytes/characters.
		7h	The response field has 8 bytes/characters.
15-3	Reserved		Reads return zero and writes have no effect.
2-0	CHAR		Character length control bits. These bits are effective in SCI compatible or buffered SCI modes only. These bits set the SCI character length from 1 to 8 bits. **Note**: In compatibility mode or buffered SCI mode, when data of fewer than eight bits in length is received, it is left justified in SCIRD/RDy and padded with trailing zeros. Data read from the SCIRD should be shifted by software to make the received data right justified. **Note**: Data written to the SCITD should be right justified but does not need to be padded with leading zeros.
		0h	The character is 1 bits long.
		1h	The character is 2 bits long.
		2h	The character is 3 bits long.
		3h	The character is 4 bits long.
		4h	The character is 5 bits long.
		5h	The character is 6 bits long.
		6h	The character is 7 bits long.
		7h	The character is 8 bits long.

6.12 Baud Rate Selection Register (BRSR)

The Baud Rate Selection Register (BRSR) is shown in Figure 32 and described in Table 18.

Figure 32. Baud Rate Selection Register (BRSR)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18. Baud Rate Selection Register (BRSR) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved		Reads return zero and writes have no effect.
27-24	M	0-3h	SCI/BLIN 4-bit Fractional Divider Selection. These bits are effective in LIN or SCI asynchronous mode. These bits are used to select a baud rate for the SCI/BLIN module, and they are a fractional part for the baud rate specification. The M divider allows fine-tuning of the baud rate over the P prescaler with 15 additional intermediate values for each of the P integer values.
23-0	P	0–FF FFFFh	PRESCALER . SCI/BLIN 24-bit Integer Prescaler Selection. These bits are used to select a baudrate for the SCI/BLIN module. These bits are effective in LIN mode and SCI compatibility mode. The SCI/BLIN has an internally generated serial clock determined by the LIN module input clock and the prescalers P and M in this register. The SCI/LIN uses the 24-bit integer prescaler P value to select 1 of over 16,700,000 available baud rates. The additional 4-bit fractional prescaler M refines the baudate selection.

The baud rate can be calculated using the formulas shown in Section 2.3.1.

Table 19. P and M values for standard bit-rates(1)

Desired bit rate	Actual bit-rate	Percentage error	P value	M value
115200	115384.62	0.16	15	4
57600	57581.57	0.03	31	9
38400	38412.29	0.03	47	13
19200	19193.86	0.03	96	11
9600	9600	0	194	5
4800	4800	0	389	10
2400	2400	0	780	4
1200	1200	0	1561	8

(1) For a 60 MHz device, LIN module input clock = 30 MHz

6.13 SCI Data Buffers (SCIED, SCIRD, SCITD)

The SCI has three addressable registers in which transmit and receive data is stored.

6.13.1 Receiver Emulation Data Buffer (SCIED)

The SCIED register is addressed at a location different from SCIRD, but is physically the same register.

The Receiver Emulation Data Buffer (SCIED) is shown in Figure 33 and described in Table 20.

Figure 33. Receiver Emulation Data Buffer (SCIED)

31			16
Reserved			
R-0			
15	8	7	0
Reserved		ED	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 20. Receiver Emulation Data Buffer (SCIED) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved		Reads return zero and writes have no effect.
7-0	ED	0–FFh	Receiver Emulation Data. This bit is effective in SCI-compatible mode only. Reading SCIED(7–0) does not clear the RXRDY flag. This register should be used only by an emulator that must continually read the data buffer without affecting the RXRDY flag.

6.13.2 Receiver Data Buffer (SCIRD)

This register provides a location for the receiver data.

The Receiver Data Buffer (SCIRD) is shown in Figure 34 and described in Table 21.

Figure 34. Receiver Data Buffer (SCIRD)

31			16
Reserved			
R-0			
15	8	7	0
Reserved		RD	
R-0		R/WC-0	

LEGEND: R/W = Read/Write; R = Read only; WC = Write in SCI-compatible mode only; -*n* = value after reset

Table 21. Receiver Data Buffer (SCIRD) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved		Reads return zero and writes have no effect.
7-0	RD	0–FFh	Received Data. This bit is effective in SCI-compatible mode only. When a frame has been completely received, the data in the frame is transferred from the receiver shift register SCIRXSHF to this register. As this transfer occurs, the RXRDY flag is set and a receive interrupt is generated if RX INT ENA (SCISETINT0.9) is set. When the data is read from SCIRD, the RXRDY flag is automatically cleared.

NOTE: When the SCI receives data that is fewer than eight bits in length, it loads the data into this register in a left-justified format padded with trailing zeros. Therefore, the Normal software should perform a logical shift on the data by the correct number of positions to make it right justified.

6.13.3 Transmit Data Buffer Register (SCITD)

Data to be transmitted is written to the SCITD register.

The Transmit Data Buffer Register (SCITD) is shown in Figure 35 and described in Table 22.

Figure 35. Transmit Data Buffer Register (SCITD)

31								16
Reserved								
R-0								
15				8	7			0
Reserved					TD			
R-0					R/W-0			

LEGEND: R/W = Read/Write; R = Read only; W = Write in SCI-compatible mode only; -*n* = value after reset

Table 22. Transmit Data Buffer Register (SCITD) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved		Reads return zero and writes have no effect.
7-0	TD	0–FFh	Transmit data. This bit is effective in SCI-compatible mode only. The transfer of data from this register to the transmit shift register SCITXSHF sets the TXRDY flag (SCIFLR[23]; Section 6.8), which indicates that SCITD is ready to be loaded with another byte of data. Note: If TX INT ENA (register SCISETINT[8]; Section 6.4) is set, this data transfer also causes an interrupt.

NOTE: Data written to the SCITD register that is fewer than eight bits long must be right justified, but it need not be padded with leading zeros.

6.14 SCI Pin I/O Control Register 2 (SCIPIO2)

This register enables the current value of LINTX and LINRX pins to be read.

The SCI Pin I/O Control Register 2 (SCIPIO2) is shown in Figure 36 and described in Table 23.

Figure 36. SCI Pin I/O Control Register 2 (SCIPIO2)

31															16
Reserved															
R-0															
15											3	2	1	0	
Reserved												TX IN	RX IN	Reserved	
R-0												R-x	R-x	R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23. SCI Pin I/O Control Register 2 (SCIPIO2) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved		Reads return zero and writes have no effect.
2	TX IN		Transmit data in. This bit is effective in LIN or SCI-compatible mode. This bit contains the current value on the SCITX pin.
		0	The SCITX pin is at logic low (0).
		1	The SCITX pin is at logic high (1).
1	RX IN		Receive data in. . This bit is effective in LIN or SCI-compatible mode. This bit contains the current value on the SCIRX pin
		0	The SCIRX pin is at logic low (0).
		1	The SCIRX pin is at logic high (1).

Table 23. SCI Pin I/O Control Register 2 (SCIPIO2) Field Descriptions (continued)

Bit	Field	Value	Description
0	Reserved		Reads return zero and writes have no effect.

6.15 LIN Compare Register (LINCOMPARE)

The LIN Compare Register (LINCOMPARE) is shown in Figure 37 and described in Section 6.15.

Figure 37. LIN Compare Register (LINCOMPARE)

31	16
Reserved	
R-0	

15	10	9	8	7	3	2	0
Reserved		SDEL		Reserved		SBREAK	
R-0		R/WL-0		R-0		R/WL-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 24. LIN Compare Register (LINCOMPARE) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved		Reads return zero and writes have no effect.
9-8	SDEL		2-bit synch delimiter compare. These bits are effective in LIN mode only. These bits are used to configure the number of T_{bit} for the synch delimiter in the synch field. The time delay value for the synchronization delimiter is $T_{SDEL} = (SDEL + 1)T_{bit}$
		0h	The synch delimiter has 1 T_{bit}.
		1h	The synch delimiter has 2 T_{bit}.
		2h	The synch delimiter has 3 T_{bit}.
		3h	The synch delimiter has 4 T_{bit}.
7-3	Reserved		Reads return zero and writes have no effect.
2-0	SBREAK		3-bit Synch Break Extend. LIN mode only. These bits are used to configure the number of T_{bits} for the synch break to extend the minimum 13 T_{bit} in the Synch Field to a maximum of 20 T_{bit}. **Note**: The default value is 0x0, which adds nothing to the automatically generated SYNCH BREAK. The time delay for the SYNCH BREAK is $T_{SYNBRK} = 13T_{bit} + SBREAK \times T_{bit}$
		0h	The synch break has no additional T_{bit}.
		1h	The synch break has 1 additional T_{bit}.
		2h	The synch break has 2 additional T_{bit}.
		3h	The synch break has 3 additional T_{bit}.
		4h	The synch break has 4 additional T_{bit}.
		5h	The synch break has 5 additional T_{bit}.
		6h	The synch break has 6 additional T_{bit}.
		7h	The synch break has 7 additional T_{bit}.

6.16 LIN Receive Buffer 0 Register (LINRD0)

The LIN Receive Buffer 0 Register (LINRD0) is shown in Figure 38 and described in Table 25.

Figure 38. LIN Receive Buffer 0 Register (LINRD0)

31	24	23	16
RD0		RD1	
R-0		R-0	
15	8	7	0
RD2		RD3	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 25. LIN Receive Buffer 0 Register (LINRD0) Field Descriptions

Bit	Field	Value	Description
31-24	RD0	0–FFh	8-bit Receive Buffer 0. Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received. A read of this byte clears the RXDY byte. **Note**: RD<x-1> is equivalent to Data byte <x> of the LIN frame.
23-16	RD1	0–FFh	8-bit Receive Buffer 1. Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
15-8	RD2	0–FFh	8-bit Receive Buffer 2. Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
7-0	RD3	0–FFh	8-bit Receive Buffer 3. Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.

6.17 LIN Receive Buffer 1 Register (LINRD1)

The LIN Receive Buffer 1 Register (LINRD1) is shown in Figure 39 and described in Table 26.

Figure 39. LIN Receive Buffer 1 Register (LINRD1)

31	24	23	16
RD4		RD5	
R-0		R-0	
15	8	7	0
RD6		RD7	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 26. LIN Receive Buffer 1 Register (LINRD1) Field Descriptions

Bit	Field	Value	Description
31-24	RD4	0–FFh	8-bit Receive Buffer 4. Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
23-16	RD5	0–FFh	8-bit Receive Buffer 5. Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
15-8	RD6	0–FFh	8-bit Receive Buffer 6. Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.

Table 26. LIN Receive Buffer 1 Register (LINRD1) Field Descriptions (continued)

Bit	Field	Value	Description
7-0	RD7	0–FFh	8-bit Receive Buffer 7. Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.

6.18 LIN Mask Register (LINMASK)

The LIN Mask Register (LINMASK) is shown in Figure 40 and described in Table 27.

Figure 40. LIN Mask Register (LINMASK)

31	24	23	16
Reserved		RX ID MASK	
R-0		R-0	
15	**8**	**7**	**0**
Reserved		TX ID MASK	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 27. LIN Mask Register (LINMASK) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved		Reads return zero and writes have no effect.
23-16	RX ID MASK	0–FFh	Receive ID mask. LIN mode only. This 8-bit mask is used for filtering an incoming ID message and compare it to the ID-byte. A compare match of the received ID witht the RX ID mask will set the ID RX flag and trigger and ID interrupt if enabled. A 0 bit in the mask indicates that bit is compared to the ID-byte. A 1 bit in the mask indicates that that bit is filtered and therefore not used in the compare.
15-8	Reserved		Reads return zero and writes have no effect.
7-0	TX ID MASK		Transmit ID mask. LIN mode only. This 8-bit mask is used for filtering an incoming ID message and compare it to the ID-byte. A compare match of the received ID with the TX ID Mask will set the ID TX flag and trigger an ID interrupt if enabled. A 0 bit in the mask indicates that bit is compared to the ID-byte. A 1 bit in the mask indicates that bit is filtered and therefore not used for the compare.

6.19 LIN Identification Register (LINID)

The LIN Identification Register (LINID) is shown in Figure 41 and described in Table 28.

Figure 41. LIN Identification Register (LINID)

31	24	23	16
Reserved		RECEIVED ID	
R-0		R-0	
15	**8**	**7**	**0**
ID-SlaveTask BYTE		ID BYTE	
R/WL-0		R/WL-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 28. LIN Identification Register (LINID) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved		Reads return zero and writes have no effect.

Table 28. LIN Identification Register (LINID) Field Descriptions (continued)

Bit	Field	Value	Description
23-16	Received ID	0–FFh	LIN mode only. This byte contains the current message identifier. During header reception the received ID is copied from the SCIRXSHF register to this byte if there is no ID-parity error and there has been an RX/TX match.
15-8	ID-SlaveTask BYTE	0–FFh	LIN mode only. This byte contains the identifier to which the received ID of an incoming Header will be compared in order to decide whether a RX response, a TX response or no action needs to be done by the LIN node.
7-0	ID BYTE	0–FFh	LIN mode only. This byte is the LIN mode message ID. On a master node, a write to this register by the CPU initiates a header transmission. For a slave task, this byte is used for message filtering when HGENCTRL (SCIGCR1.12) is '0'.

6.20 LIN Transmit Buffer 0 Register (LINTD0)

The LIN Transmit Buffer 0 Register(LINTD0) is shown in Figure 42 and described in Table 29.

Figure 42. LIN Transmit Buffer 0 Register (LINTD0)

31	24	23	16
TD0		TD1	
R/W-0		R/W-0	
15	8	7	0
TD2		TD3	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 29. LIN Transmit Buffer 0 Register (LINTD0) Field Descriptions

Bit	Field	Value	Description
31-24	TD0	0–FFh	8-bit Transmit Buffer 0. Byte 0 to be transmitted is written into this register and then copied to SCITXSHF for transmission. Once byte 0 is written in TDO buffer, transmission will be initiated.
23-16	TD1	0–FFh	8-bit Transmit Buffer 1. Byte 1 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
15-8	TD2	0–FFh	8-bit Transmit Buffer 2. Byte 2 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
7-0	TD3	0–FFh	8-bit Transmit Buffer 3. Byte 3 to be transmitted is written into this register and then copied to SCITXSHF for transmission.

6.21 LIN Transmit Buffer 1 Register (LINTD1)

The LIN Transmit Buffer 1 Register (LINTD1) is shown in Figure 43 and described in Table 30.

Figure 43. LIN Transmit Buffer 1 Register (LINTD1)

31	24	23	16
TD4		TD5	
R/W-0		R/W-0	
15	8	7	0
TD6		TD7	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 30. LIN Transmit Buffer 1 Register (LINTD1) Field Descriptions

Bit	Field	Value	Description
31-24	TD4	0–FFh	8-Bit transmit buffer 4. Byte 4 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
23-16	TD5	0–FFh	8-Bit transmit buffer 5. Byte 5 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
15-8	TD6	0–FFh	8-Bit transmit buffer 6. Byte 6 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
7-0	TD7	0–FFh	8-Bit transmit buffer 7. Byte 7 to be transmitted is written into this register and then copied to SCITXSHF for transmission.

6.22 Maximum Baud Rate Selection Register (MBRS)

The Maximum Baud Rate Selection Register (MBRS) is shown in Figure 44 and described in Table 31.

Figure 44. Maximum Baud Rate Selection Register (MBRS)

31	16
Reserved	
R-0	

15	13	12	0
Reserved		MBR	
R-0		R/WL-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 31. Maximum Baud Rate Selection Register (MBRS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved		Reads return zero and writes have no effect.
12-0	MBR	0–1FFFh	Maximum Baud Rate Prescaler. LIN mode only. This 13-bit prescaler is used during the synchronization phase (see section 1.5.2.3, "Header Reception and Adaptive Baudrate" , page 1- 22) of a slave module if the ADAPT bit is set. In this way, a BLIN slave using an automatic or select bit rate modes detects any LIN bus legal rate automatically. The MBR value should be programmed to allow a maximum baud rate that is not more than 10% above the expected operating baud rate in the LIN network. Otherwise a s 0x00 data byte could misleadingly be detected as synchbreak. The default value is for a 30MHz LINCLK (0x5DC). This MBR prescaler is used by the wake-up and idle time counters for a constant expiration time relative to a 20kHz rate

6.23 I/O Design For Test Control (IODFTCTRL) Register

This register is used to force different error conditions. All the bits in the IODFTCTRL register are used in IODFT (I/O design for test) mode only.

The I/O Design For Test Control (IODFTCTRL) Register is shown in Figure 45 and described in Table 32.

Figure 45. I/O Design For Test Control (IODFTCTRL) Register

31	30	29	28	27	26	25	24
Bit Error Enable	Physical Bus Error Enable	Checksum Error Enable	Inconsistent Synch Field Error Enable	Reserved	Frame Error Enable	Parity Error Enable	Break Detect Error Enable
R/W-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0

23	21	20	19	18	16
Reserved		PIN SAMPLE MASK		TX SHIFT	
R-0		R/W-0		R/W-0	

15	12	11	8
Reserved		IODFTENA	
R-0		R/W-0	

7	2	1	0
Reserved		LPBENA	RXPENA
R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 32. I/O Design For Test Control (IODFTCTRL) Register Field Descriptions

Bit	Field	Value	Description
31	Bit Error Enable		LIN Mode Only This bit is used to create a Bit error. When this bit is set, the bit received is ORed with 1 and passed to the Bit monitor circuitry.
30	Physical Bus Error Enable		LIN Mode only This bit is used to create a Physical Bus Error. When this bit is set, the bit received during Synch Break field transmission is ORed with 1 and passed to the Bit monitor circuitry
29	Checksum Error Enable		LIN Mode only This bit is used to create a checksum error. When this bit is set, the polarity of the CTYPE (checksum type) in the receive checksum calculator is changed so that a checksum error is occurred
28	Inconsistent Synch Field Error Enable		LIN Mode only This bit is used to create an ISF error. When this bit is set, the bit widths in the synch field are varied so that the ISF check fails and the error flag is set.
27	Reserved		Reads return zero and writes have no effect.
26	Frame Error Enable		This bit is used to create a Frame Error. When this bit is set, the stop bit received is ANDed with '0' and passed to the stop bit check circuitry.
25	Parity Error Enable		Compatible Mode only This bit is used to create a Parity Error. When this bit is set, in compatible mode, the parity bit received is toggled so that a parity error occurs.
24	Break Detect Error Enable		Compatible Mode only This bit is used to create BRKDT error (SCI mode only). When this bit is set, the stop bit of the frame is ANDed with '0' and passed to the RSM so that a frame error occurs. Then the RX Pin is forced to continuous low for 10 T_{bits} so that a BRKDT error occurs.
23-21	Reserved		Reads return zero and writes have no effect.

Table 32. I/O Design For Test Control (IODFTCTRL) Register Field Descriptions (continued)

Bit	Field	Value	Description
20-19	PIN SAMPLE MASK		These bits define the sample number at which the TX Pin value that is being transmitted will be inverted to verify the receive pin samples correctly with the majority detection circuitry.
			PIN SAMPLE MASK:
		0h	No Mask
		1h	Invert the TX Pin value at TBIT_CENTER
		2h	Invert the TX Pin value at TBIT_CENTER + SCLK
		3h	Invert the TX Pin value at TBIT_CENTER + 2 SCLK
18-16	TX SHIFT		Transmit shift.
		0	These bits define the delay by which the value on TX pin is delayed so that the value on RX Pin is asynchronous. (Not applicable to Start Bit)
			TX SHIFT:
		0h	No Delay
		1h	Delay by 1 SCLK
		2h	Delay by 2 SCLK
		3h	Delay by 3 SCLK
		4h	Delay by 4 SCLK
		5h	Delay by 5 SCLK
		6h	Delay by 6 SCLK
		7h	Delay by 7 SCLK
15-12	Reserved		Reads return zero and writes have no effect.
11-8	IODFTENA		IO DFT Enable Key
			Normal and EALLOW mode reads.
			Write only in EALLOW mode
			Write
		Ah	IODFT is enabled
		Others	IODFT is disabled
			Read
		Ah	IODFT is enabled
		Others	IODFT is disabled
7-2	Reserved		Reads return zero and writes have no effect.
1	LPBENA		Module loopback enable.
		0	**Note**: In analog loopback mode the complete communication path through the I/Os can be tested, whereas in digital loopback mode the I/O buffers are excluded from this path.
			Normal and mode reads:
			Write only in EALLOW mode:
			write/read :
		0	Digital loopback is enabled.
		1	Analog loopback is enabled in module I/O DFT mode (when IODFTENA = 1010)
0	RXPENA		Module Analog loopback through receive pin enable.
		0	This bit defines whether the I/O buffers for the transmit or the receive pin are included in the communication path (in analog loopback mode).
			Normal and EALLOW mode reads:
			Write only in EALLOW mode:
			write/read :
		0	Analog loopback through the transmit pin is enabled.
		1	Analog loopback through the receive pin is enabled.

7 BLIN SCI vs. Standard SCI

Table 33 compares the BLIN/SCI with the standalone-SCI ("standard" SCI) available in all C2000 devices.

Table 33. SCI vs. LIN-SCI Programming

Standard SCI	BLIN SCI
CCS Register Structure	
SciaRegs.REGISTER	LinaRegs.REGISTER
Example Configurations	
Idle Line Mode: SciaRegs.SCICCR.bit.ADDRIDLE_MODE = 0; **Adress Bit Mode:** SciaRegs.SCICCR.bit.ADDRIDLE_MODE = 1; **FIFO Mode:** SciaRegs.SCIFFTX.bit.SCIFFENA = 1; **No FIFO Mode:** SciaRegs.SCIFFTX.bit.SCIFFENA = 0;	**Idle Line Mode:** LinaRegs.SCIGCR1.bit.COMMMODE = 0; **Adress Bit Mode:** LinaRegs.SCIGCR1.bit.COMMMODE = 1; **Buffered Mode:** LinaRegs.SCIGCR1.bit.MBUFMODE = 1; **Unbuffered Mode:** LinaRegs.SCIGCR1.bit.MBUFMODE = 0;
Configuration Sequence	
//Into software reset SciaRegs.SCICTL1.bit.SWRESET = 0; *(Configuration instructions)* *//Relinquish SCI from reset* SciaRegs.SCICTL1.bit.SWRESET = 1;	*//Into reset* LinaRegs.SCIGCR0.bit.RESET = 0; *//Out of reset* LinaRegs.SCIGCR0.bit.RESET = 1; *//Into software reset* LinaRegs.SCIGCR1.bit.SWnRST = 0; *(Configuration instructions)* *//Bring out of software reset* LinaRegs.SCIGCR1.bit.SWnRST = 1;
Baud Rate Configuration	
Registers: SciaRegs.SCIHBAUD SciaRegs.SCILBAUD **Fields:** BRR = (SciaRegs.SCIHBAUD << 8) + SciaRegs.SCILBAUD **Base Clock Rate:** $LSPCLK = \frac{SYSCLKOUT}{LowSpeedPrescaler}$ **Baud Rate Calculation:** $Baud = \frac{LSPCLK}{(BRR+1)\times 8}$	**Registers**: LinaRegs.BRSR **Fields**: Prescaler(P) = LinaRegs.BRSR.bit.P Fractional Divider(M) = LinaRegs.BRSR.bit.M **Base Clock Rate:** $LM\_CLK = \frac{SYSCLKOUT}{2}$ **Baud Rate Calculation:** $Baud = \frac{LM\_CLK}{(P+1+\frac{M}{16})\times 16}$
Basic Transmission	
SciaRegs.SCITXBUF = data;	LinaRegs.SCITD = data;
FIFO/Data Buffer	
Structure: FIFO **Depth:**	**Structure:** Buffer **Depth:**

Table 33. SCI vs. LIN-SCI Programming (continued)

Standard SCI	BLIN SCI
8 bits x 16 **Fill:** for(iter = 0; iter < depth; iter++) { SciaRegs.SCITXBUF = data[i]; } **Empty:** for(iter = 0; iter < depth; iter++) { data[i] = SciaRegs.SCIRXBUF.all; }	8 bits x 8 **Fill:** LinaRegs.LINTD0.bit.TD0 = data[0]; LinaRegs.LINTD0.bit.TD1 = data[1]; … LinaRegs.LINTD1.bit.TD7 = data[7]; **Empty:** data[0] = LinaRegs.LINRD0.bit.RD0; data[1] = LinaRegs.LINRD0.bit.RD1; … data[7] = LinaRegs.LINRD1.bit.RD7;
Flags	
Data Reception: SciaRegs.SCIRXST.bit.RXRDY **Transmission Completion:** SciaRegs.SCICTL2.bit.TXEMPTY	**Data Reception:** LinaRegs.SCIFLR.bit.RXRDY **Transmission Completion:** LinaRegs.SCIFLR.bit.TXEMPTY
Interrupts	
ISR Mapping: PieVectTable.SCIRXINTA = &sciaRxFifoIsr; PieVectTable.SCITXINTA = &sciaTxFifoIsr; **ISR:** interrupt void sciaTxFifoIsr(void) { *//do TX stuff* *//clear interrupt flag* SciaRegs.SCIFFTX.bit.TXFFINTCLR = 1; *//acknowledge PIE* PieCtrlRegs.PIEACK.all = PIEACK_GROUP9; } interrupt void sciaRxFifoIsr(void) { *//do RX stuff* *// clear overflow flag* SciaRegs.SCIFFRX.bit.RXFFOVRCLR = 1; *// clear interrupt flag* SciaRegs.SCIFFRX.bit.RXFFINTCLR = 1; //acknowledge PIE PieCtrlRegs.PIEACK.all = PIEACK_GROUP9; }	**ISR Mapping:** PieVectTable.LININT0A = &Lina_Level0_ISR; PieVectTable.LININT1A = &Lina_Level1_ISR; **ISR**: interrupt void Lina_Level0_ISR(void) { *//read-clear interrupt vector* LinL0IntVect = LinaRegs.SCIINTVECT0.all; if(LinL0IntVect == TXVect) { *//do TX stuff* { if(LinL0IntVect == RXVect) { *//do RX stuff* } *//Acknowledge PIE* PieCtrlRegs.PIEACK.all = PIEACK_GROUP9; } interrupt void Lina_Level1_ISR(void) { *//read-clear interrupt vector* LinL1IntVect = LinaRegs.SCIINTVECT1.all; if(LinL1IntVect == TXVect) {

Table 33. SCI vs. LIN-SCI Programming (continued)

Standard SCI	BLIN SCI
	//do TX stuff { if(LinL1IntVect == RXVect) { *//do RX stuff* } *//Acknowledge PIE* PieCtrlRegs.PIEACK.all = PIEACK_GROUP9; }

Appendix A Revision History

This document was revised to include the following technical changes.

Revision A Changesb

Location	Additions/Changes/Deletions
Table 6	For bit 4 (STOP), added "This bit specifies the number of stop bits transmitted" to the description.
Global	Removed the Preliminary status from the page headers.

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