**TOSHIBA** TMPN3150B1AF

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# T M P N 3 1 5 0 B 1 A F

## **Neuron<sup>®</sup> Chip** For Distributed Intelligent Control Networks (LonWorks<sup>®</sup>)

The TMPN3150B1AF is a Neuron Chip which configures LONWORKS nodes in combination with external memory. Neuron Chips have all the built-in communications and control functions required to implement LONWORKS nodes. These nodes may then be easily integrated into highly-reliable distributed intelligent control networks. The typical functions for this chip are explained below.



- I/O Functions
  - Eleven programmable I/O pins.
  - Two programmable 16-bit timers and counters built in.
- QFP64-P-1414-0.80A

Weight: 1.0g (Typ.)

- 34 different types of I/O functions to handle a wide range of input and output.
- ROM firmware image containing pre-programmed I/O drivers, greatly simplifying application programs. (Stored in external ROM)
- **Network functions** 
  - Two CPUs for communication protocol processing built in. The communications and application CPUs execute in parallel.
  - Equipped with a built-in LonTalk protocol which supports all seven levels of the OSI reference model with ISO.
  - Highly reliable communication protocol is supplied as firmware.
  - · Built-in twisted-pair wire transceiver with improved common mode and drive current capabilities.
  - Equipped with communications modes and communication speeds which support various types of external transceivers.
    - Supports twisted-pair wire, power line, radio (RF), infrared, coaxial cables and fiber optics.
  - Communication port transceiver modes and logical addresses stored within the EEPROM. Can be amended via the network.

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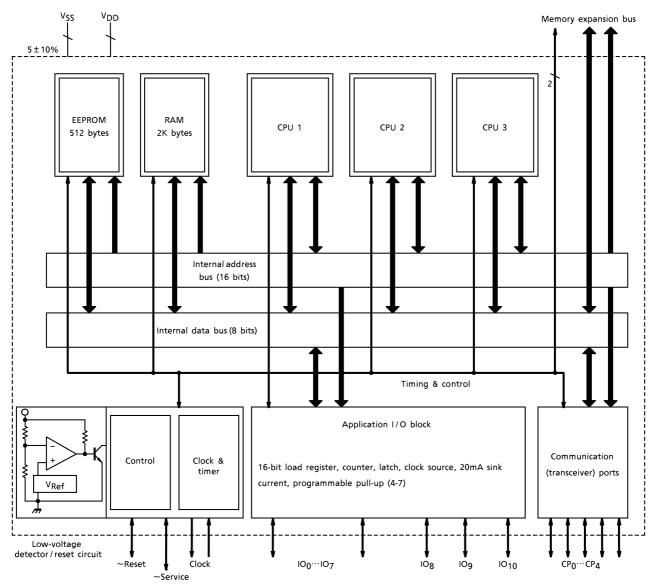
  The information contained herein is subject to change without notice.
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#### Other functions

- Application programs are also stored within the EEPROM.
   May be updated by downloading over the network. EEPROM can be externally added.
- Built-in watch-dog timer.
- Each chip has a unique ID number.
   Effective during the logical installation of networks.
- Low electrical consumption mode supported with a sleep mode.
- Built-in low-voltage detection circuit.

  Prevents incorrect operations and writing errors in the EEPROM during drops in power voltage.
- The package is QFP64-P-1414-0.80A.

### **BLOCK DIAGRAM**



Reference clock input: 10MHz, 5MHz, 2.5MHz, 1.25MHz, 625kHz

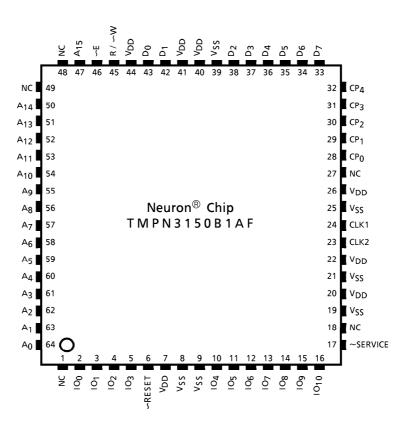
ITEM	TMPN3150B1AF
CPU	8-bit CPU×3
RAM	2,048 bytes
ROM	_
EEPROM	512 bytes
16-bit Timer/Counter	2ch
External Memory Interface	あり
Package	64 pin QFP

### **PIN FUNCTION**

PIN No.	PIN NAME	1/0	PIN FUNCTION
24	CLK1	Input	Oscillator connection, or external clock input.
23	CLK2	Output	Oscillator connection. Leave open when external clock is input to CLK1.
6	~RESET	I/O (built-in pull-up)	Reset pin. (Active low)
17	~SERVICE	I / O (built-in configurable pull-up)	Service pin. Indicator output during operation.
2~5	100~103	1/0	Large current sink capacity (20mA). General I/O port.
10~13	10 <sub>4</sub> ~10 <sub>7</sub>	I/O (built-in configurable pull-up)	General I/O port. One of IO <sub>4</sub> to IO <sub>7</sub> can be specified as No.1 timer/counter input. Output signal can be output to IO <sub>0</sub> . IO <sub>4</sub> can be used as the No.2 timer/counter input with IO <sub>1</sub> as output.
14~16	10 <sub>8</sub> ~10 <sub>10</sub>	1/0	General I/O port. Can be used for serial communication with other device.
43, 42, 38~33	D <sub>0</sub> , D <sub>1</sub> , D <sub>2</sub> ~D <sub>7</sub>	1/0	Data bus for memory expansion
45	R/~W	Output	Output port for controlling read/write for memory expansion
46	~E	Output	Output port for controlling memory expansion
47, 50~64	A <sub>15</sub> , A <sub>14</sub> ~A <sub>0</sub>	Output	Address output port for memory expansion
7, 20, 22, 26, 40, 41, 44	V <sub>DD</sub>	Input	Power input (5.0V Typ.)
8, 9, 19, 21, 25, 39	VSS	Input	Power input (0V GND)
1, 18, 27, 48, 49	NC	_	Do not connect anything. Leave pins open.
28~32	CP <sub>0</sub> ~CP <sub>4</sub>	1/0	Bidirectional port for communications. Supports several communications protocols by specifying mode.

- (\*) The ~SERVICE and IO<sub>4</sub>~IO<sub>7</sub> terminals are programmable pull-ups.
   All V<sub>DD</sub> terminals must be externally connected.
   All V<sub>SS</sub> terminals must be externally connected.

### **PIN ASSIGNMENT**



## MAXIMUM RATINGS ( $V_{SS} = 0V$ , $V_{SS}$ typ.)

ITEM	SYMBOL	RATING	UNIT
Power Supply Voltage	V <sub>DD</sub>	- 0.3~7.0	V
Input Voltage	VIN	-0.3~V <sub>DD</sub> +0.3	٧
Power Dissipation	PD	800	mW
Storage Temperature	T <sub>stg</sub>	<b>- 65∼150</b>	°C

#### **OPERATING CONDITIONS**

ITEM	SYMBOL	MIN	TYP.	MAX	UNIT
Operating Voltage	V <sub>DD</sub>	4.5	5.0	5.5	V
Input Voltage (TTL)	VIH	2.0	-	$V_{DD}$	V
	VIL	Vss		0.8	V
Inner Valtage (CNACC)	V <sub>IH</sub>	V <sub>DD</sub> – 0.8		$V_{DD}$	V
Input Voltage (CMOS)	VIL	Vss	_	0.8	V
Operating Frequency	fosc	0.625	_	10	MHz
Operating Temperature	T <sub>opr</sub>	- 40	_	85	°C

## **ELECTRICAL CHARACTERISTICS**

DC characteristic ( $V_{DD} = 5.0V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = -40 \sim 85$ °C) (Above operating conditions apply unless otherwise states.)

ITEM	SYMBOL	PINS	TEST CONDITION		MIN	MAX	UNIT
LOW Output Valtage (4)	V (1)	10- 10-	I <sub>OL</sub> = 20mA		0	0.8	V
LOW Output Voltage (1)	V <sub>OL</sub> (1)	$IO_0 \sim IO_3$ $IO_L = 10m$		OL = 10mA		0.4	V
LOW Output Voltage (2)	Vo. (2)	~SERVICE	Duty	I <sub>OL</sub> = 20mA	0	0.8	V
LOW Output Voltage (2)	V <sub>OL</sub> (2)	~SERVICE	cycle = 50%	I <sub>OL</sub> = 10mA	0	0.4	٧
LOW Output Voltage (3)	V <sub>OL</sub> (3)	CP <sub>2</sub> , CP <sub>3</sub>	I <sub>OL</sub> = 40mA		0	1.0	V
LOW Output Voltage (4)	V <sub>OL</sub> (4)	Others (Note 1)	I <sub>OL</sub> = 1.4mA		0	0.4	٧
HIGH Output Voltage (1)	VOH (1)	10 <sub>0</sub> ~10 <sub>3</sub>	I <sub>OH</sub> = -1.4mA		V <sub>DD</sub> - 0.4	V <sub>DD</sub>	V
HIGH Output Voltage (2)	V <sub>OH</sub> (2)	~SERVICE	I <sub>OH</sub> = -1.4mA		V <sub>DD</sub> - 0.4	V <sub>DD</sub>	V
HIGH Output Voltage (3)	VOH (3)	CP <sub>2</sub> , CP <sub>3</sub>	I <sub>OH</sub> = -40mA		V <sub>DD</sub> – 1.0	V <sub>DD</sub>	V
HIGH Output Voltage (4)	VOH (4)	Others (Note 1)	I <sub>OH</sub> = -1.4mA		V <sub>DD</sub> - 0.4	V <sub>DD</sub>	٧
Input Current	ΙΙΝ	(Note 2)	VIN = VSS~VDD		- 10	+ 10	$\mu$ A
Pull-up Current	lpU	IO4~IO7 ~SERVICE, ~RESET (Note 3)	V <sub>IN</sub> = 0V		- 30	- 300	μΑ
Current (operating)	I <sub>DD</sub> (1)	V <sub>DD</sub>	V <sub>DD</sub> = 5.5V (no load)		_	30	mA
Current (SLEEP mode)	I <sub>DD</sub> (2)	$V_{DD}$	V <sub>DD</sub> = 5.5V (no load)		_	0.1	mA
Low-voltage Detection Level	VLVD	V <sub>DD</sub>	_		3.8	4.4	V

(Note 1) Output voltage characteristics exclude the  $\sim$ RESET pin and CLK2 pin.

(Note 2) Excludes pull-up input pins.

(Note 3) The IO4 to IO7 and ~SERVICE pins have programmable pull-ups. ~RESET has a fixed pull-up.

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- The Neuron Chip is manufactured by Toshiba under license from Echelon Corporation, USA. A licensing agreement between the customer and Echelon Corporation, USA must be concluded before purchasing any of the neuron chip products.
- This IC (TMPN3150B1AF) is covered by the patent agreement between Toshiba and Bull Cp8 Inc.
  Kindly understand that this product cannot be used in IC cards or other portable devices (refer to
  the definition below).

#### "PORTABLE DEVICES"

- (I) A portable device defined by ISO standard 7816 as having a width or length of ±10mm and a thickness of ±3mm.
- (II) A portable device that conforms to the electrical connection placement and shape stipulated by ISO standard 7816 Part 2.
- (III) A pocket-sized portable device in which the ID or history of the holder or the ID or history of the device can be stored as information.

BULL CP8 patent: America patent number 4,382,279

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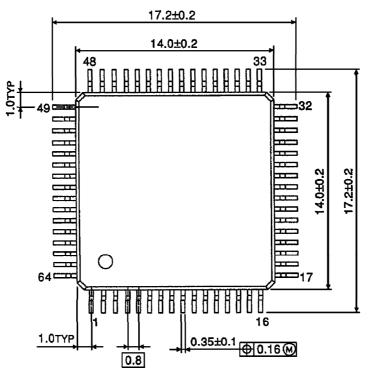
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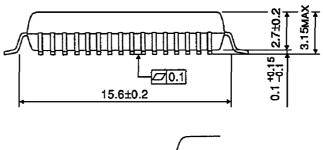
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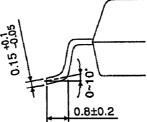
## **OUTLINE DRAWING**

QFP64-P-1414-0.80A

Unit: mm







Weight: 1.0g (Typ.)