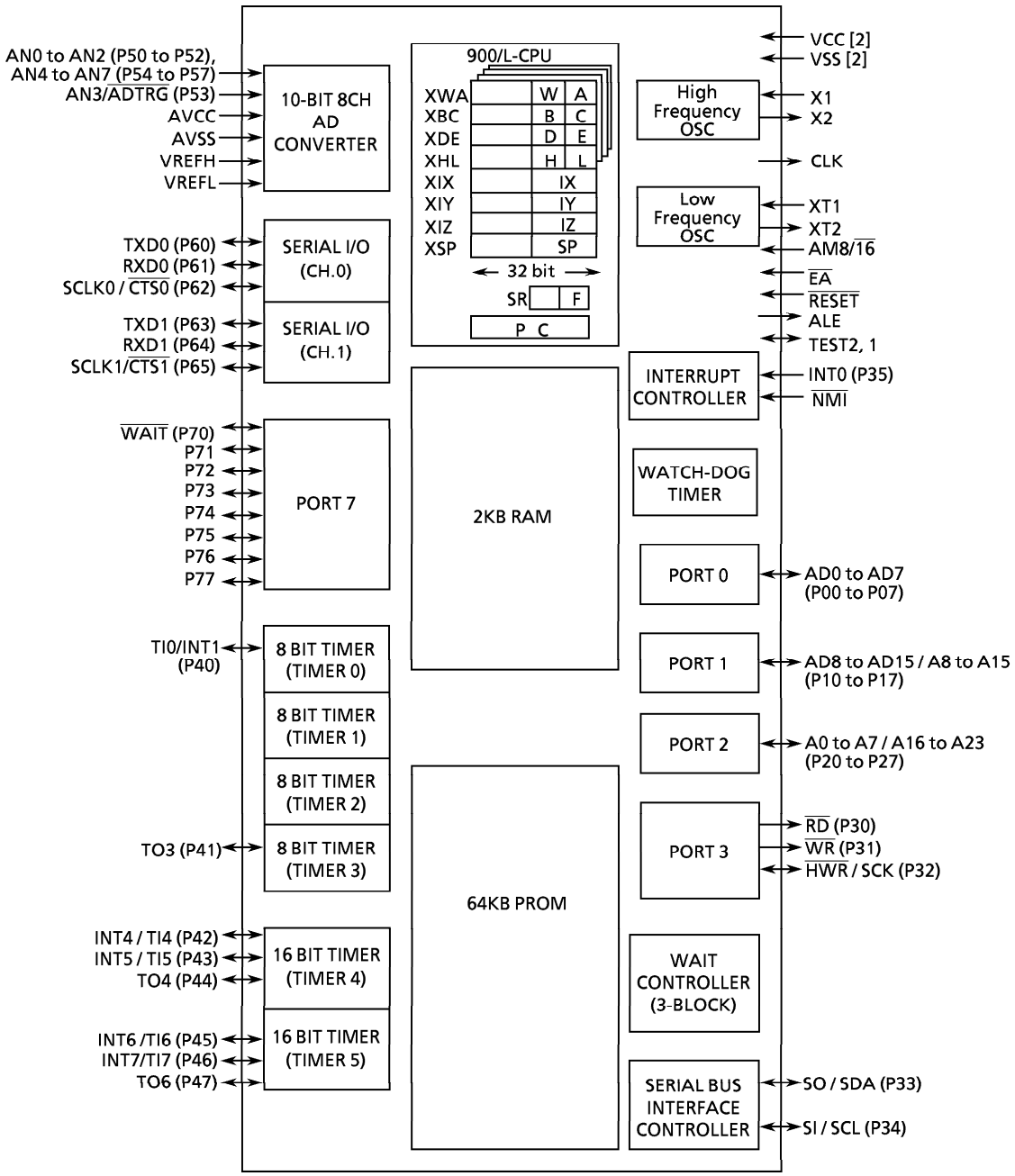
Low Voltage / Low Power CMOS 16-bit Micro-controller

TMP93PS44F

1. Outline and Device Characteristics

The TMP93PS44 is OTP type MCU which includes 64 Kbyte One-time PROM. Using the adapter-socket, you can write and verify the data for the TMP93PS44. The TMP93PS44F has the same pin-assignment as TMP93CS44 (Mask ROM type).
Writing the program to Built-in PROM, the TMP93PS44 operates as the same way as the TMP93CS44.

MCU	ROM	RAM	Package	Adapter Socket
TMP93PS44F	OTP 64 Kbyte	2 Kbyte	P-LQFP80-1212-0.50A	BM11128



Note: The items in parentheses ( ) are the initial setting after reset.

Figure 1.1 TMP93PS44 Block Diagram

2. Pin Assignment and Functions

The assignment of input/output pins for the TMP93PS44, their names and outline functions are described below.

2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of the TMP93PS44F.

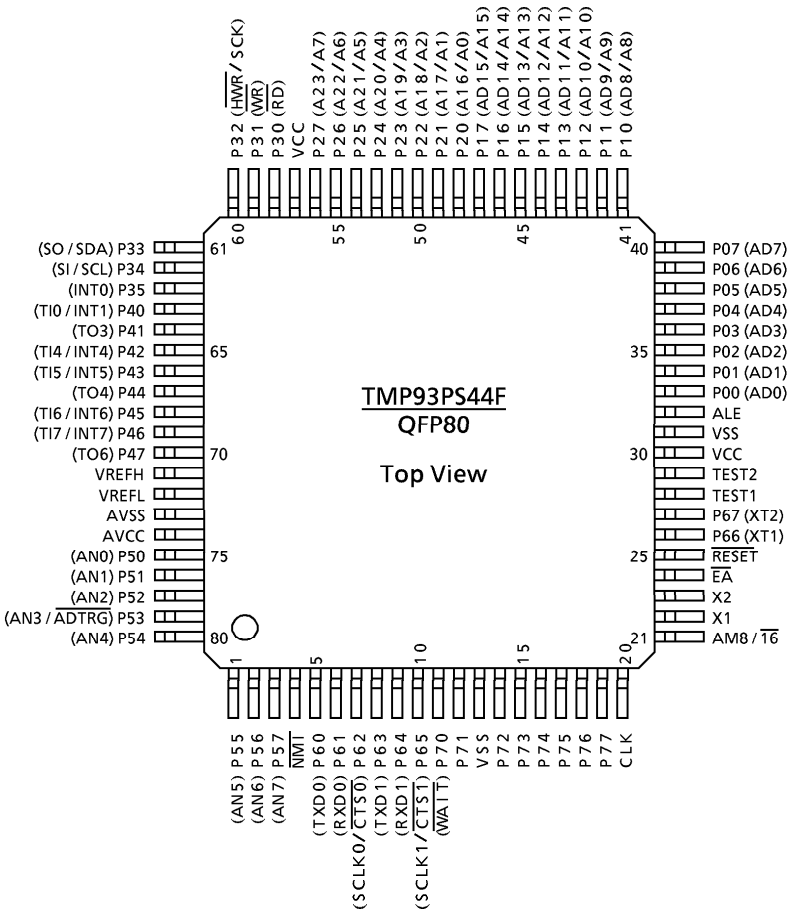


Figure 2.1.1 Pin Assignment (P-LQFP80-1212-0.50A)

2.2 Pin Names and Functions

The TMP93PS44 has MCU mode and PROM mode.

(1) Table 2.2.1 shows pin function of TMP93PS44 in MCU mode.

Table 2.2.1 Pin Names and Function (1/3)

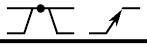
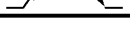
Pin name	Number of pins	I/O	Functions
P00 to P07 / AD0 to AD7	8	I/O	Port 0: I/O port that allows selection of I/O on a bit basis
		3-state	Address/data (lower): Bits 0 to 7 for address/data bus
P10 to P17 / AD8 to AD15 / A8 to A15	8	I/O	Port 1: I/O port that allows selection of I/O on a bit basis
		3-state	Address/data (upper): Bits 8 to 15 for address/data bus
		Output	Address: Bits 8 to 15 for address bus
P20 to P27 / A0 to A7 / A16 to A23	8	I/O	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-up resistor)
		Output	Address: Bits 0 to 7 for address bus
		Output	Address: Bits 16 to 23 for address bus
P30 / $\overline{RD}$	1	Output	Port 30: Output port
		Output	Read: Strobe signal for reading external memory
P31 / $\overline{WR}$	1	Output	Port 31: Output port
		Output	Write: Strobe signal for writing data on pins AD0 to 7
P32 / $\overline{HWR}$ / SCK	1	I/O	Port 32: I/O port (with pull-up resistor)
		Output	High write: Strobe signal for writing data on pins AD8 to 15
		I/O	Mode clock SBI SIO mode clock
P33 / SO / SDA	1	I/O	Port 33: I/O port
		Output	Serial Send Data
		I/O	SBI I^2C bus mode channel data
P34 / SI / SCL	1	I/O	Port 34: I/O port
		Input	Serial Receive Data
		I/O	SBI I^2C bus mode clock
P35 / INT0	1	I/O	Port 35: I/O port
		Input	Interrupt request pin 0: Interrupt request pin with programmable level/rising edge 
P40 / TI0 / INT1	1	I/O	Port 40: I/O port
		Input	Timer input 0: Timer 0 input
		Input	Interrupt request pin 1: Interrupt request pin with rising edge 
P41 / TO3	1	I/O	Port 41: I/O port
		Output	PWM output 3: 8-bit PWM timer 3 output
P42 / TI4 / INT4	1	I/O	Port 42: I/O port
		Input	Timer input 4: Timer 4 count / capture trigger signal input
		Input	Interrupt request pin 4: Interrupt request pin with programmable rising / falling edge 
P43 / TI5 / INT5	1	I/O	Port 43: I/O port
		Input	Timer input 5: Timer 4 count / capture trigger signal input
		Input	Interrupt request pin 5: Interrupt request pin with rising edge 
P44 / TO4	1	I/O	Port: I/O port
		Output	Timer output 4: Timer 4 output pin

Table 2.2.1 Pin Names and Function (2/3)

Pin name	Number of pins	I/O	Functions
P45 / TI6 / INT6	1	I/O	Port 45: I/O port
		Input	Timer input 6: Timer 5 count / capture trigger signal input
		Input	Interrupt request pin 6: Interrupt request pin with programmable rising / falling edge
P46 / TI7 / INT7	1	I/O	Port 46: I/O port
		Input	Timer input 7: Timer 5 count / capture trigger signal input
		Input	Interrupt request pin 7: Interrupt request pin with rising edge
P47 / TO6	1	I/O	Port 47: I/O port
		Output	Timer output 6: Timer 5 output pin
P50 to P52, P54 to P57 / AN0 to AN2, AN4 to AN7	7	Input	Port 50 to Port 52, Port 54 to Port 57: Input port
		Input	Analog input: Analog signal input for AD converter
P53 / AN3 / $\overline{\text{ADTRG}}$	1	Input	Port53: Input Port
		Input	Analog input: Analog signal input for AD converter
		Input	AD converter external start trigger input
P60 / TXD0	1	I/O	Port 60: I/O port (with pull-up resistor)
		Output	Serial send data 0
P61 / RXD0	1	I/O	Port 61: I/O port (with pull-up resistor)
		Input	Serial receive data 0
P62 / $\overline{\text{CTS0}}$ / SCLK0	1	I/O	Port 62: I/O port (with pull-up resistor)
		Input	Serial data send enable 0 (Clear to Send)
		I/O	Serial Clock I/O 0
P63 / TXD1	1	I/O	Port 63: I/O port (with pull-up resistor)
		Output	Serial send data 1
P64 / RXD1	1	I/O	Port 64: I/O port (with pull-up resistor)
		Input	Serial receive data 1
P65 / $\overline{\text{CTS1}}$ / SCLK1	1	I/O	Port 65: I/O port (with pull-up resistor)
		Input	Serial data send enable 1 (Clear to Send)
		I/O	Serial clock I/O 1
P66 XT1	1	I/O	Port 66: I/O port (Open Drain Output)
		Input	Low Frequency Oscillator connecting pin
P67 XT2	1	I/O	Port 67: I/O port (Open Drain Output)
		Output	Low Frequency Oscillator connecting pin
P70 / $\overline{\text{WAIT}}$	1	I/O	Port 70: I/O port (High current output available)
		Input	WAIT: Pin used to request CPU bus wait (It is active in 1 WAIT + N mode. Set by the Bus-width / wait control register.)
P71 to P77	7	I/O	Port 7: I/O port (High current output available)

Table 2.2.1 Pin Names and Function (3/3)

Pin name	Number of pins	I/O	Functions
AVCC	1	Input	Power supply pin for AD converter
AVSS	1	Input	GND pin for AD converter (0 V)
VREFH	1	Input	Pin for high level reference voltage input to AD converter
VREFL	1	Input	Pin for low level reference voltage input to AD converter
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at falling and rising edges by program.
X1	1	Input	High Frequency Oscillator connecting pin
X2	1	Output	High Frequency Oscillator connecting pin
$\overline{RESET}$	1	Input	Reset: Initializes TMP93PS44. (With pull-up resistor)
ALE	1	Output	Address Latch Enable Can be disabled for reducing noise.
CLK	1	Output	Clock output: Outputs "$f_{SYS} \div 2$" Clock. Pulled-up during reset. Can be disabled for reducing noise.
$\overline{EA}$	1	Input	External access: "1" should be inputted
AM8 / $\overline{16}$	1	Input	Address Mode: Selects external Data Bus width. "1" should be inputted. The Data Bus Width for external access is set by Chip Select / WAIT Control register, Port 1 Control register.
VCC	2	Input	Power supply pin
VSS	2	Input	GND pin (All VSS pins are connected to the GND (0 V).)
TEST1 / TEST2	2	Output / Input	TEST1 Should be connected with TEST2 pin.

Note: Built-in pull-up resistors can be released from the pins other than the $\overline{RESET}$ pin by software.

(2) PROM mode

Table 2.2.2 shows pin function of the TMP93PS44 in PROM mode.

Table 2.2.2 Pin Name and function of PROM mode

Pin function	Number of pins	Input / Output	Function	Pin name (MCU mode)
A7 to A0	8	Input	Memory address of program	P27 to P20
A15 to A8	8	Input		P17 to P10
A16	1	Input		P33
D7 to D0	8	I/O	Memory data of pfogram	P07 to P00
$\overline{CE}$	1	Input	Chip enable	P32
$\overline{OE}$	1	Input	Output control	P30
$\overline{PGM}$	1	Input	Program control	P31
VPP	1	Power supply	12.75 V / 5 V (Power supply of program)	$\overline{EA}$
VCC	3	Power supply	6.25 V / 5 V	VCC, AVCC
VSS	3	Power supply	0 V	VSS, AVSS
Pin function	**Number of pins**	**Input / Output**	**Disposal of pin**	
P60	1	Input	Fix to low level (security pin)	
$\overline{RESET}$	1	Input	Fix to low level (PROM mode)	
CLK	1	Input		
ALE	1	Output	Open	
X1	1	Input	Self oscillation with resonator	
X2	1	Output		
P66 to P61 AM8 / $\overline{16}$	7	Input	Fix to high level	
TEST1 / TEST2	2	Input / Output	Short	
P35, P34 P47 to P40 P57 to P50 P67 P77 to P70 VREFH VREFL $\overline{NMI}$	30	I/O	Open	

3. Operation

This section describes the functions and basic operational blocks of the TMP93PS44.
The TMP93PS44 has PROM in place of the mask ROM which is included in the TMP93CS44. The other configuration and functions are the same as the TMP93CS44. Regarding the function of the TMP93PS44 (not described), see the part of TMP93CS44.
The TMP93PS44 has two operational modes: MCU mode and PROM mode.

3.1 MCU mode

(1) Mode-setting and function

The MCU mode is set by opening the CLK pin (pin open). In the MCU mode, the operation is same as TMP93CS44.

(2) Memory-map

The memory map of TMP93PS44 is same as that of TMP93CS44. Figure 3.1.1 shows the memory map in MCU mode. Figure 3.1.2 show that in PROM mode.

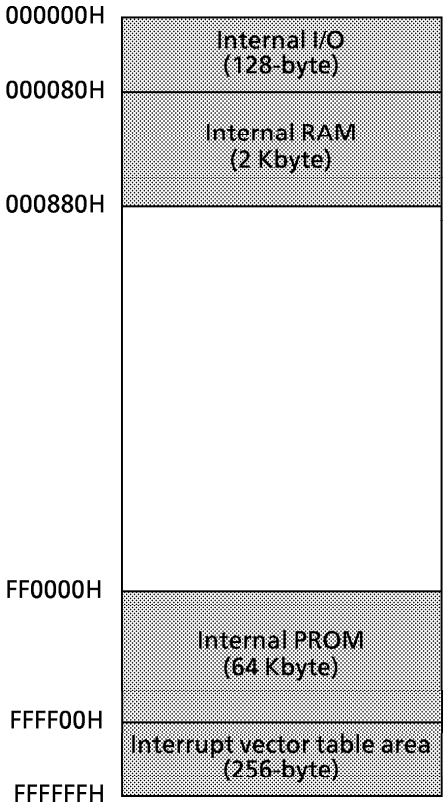


Figure 3.1.1 Memory map in MCU mode

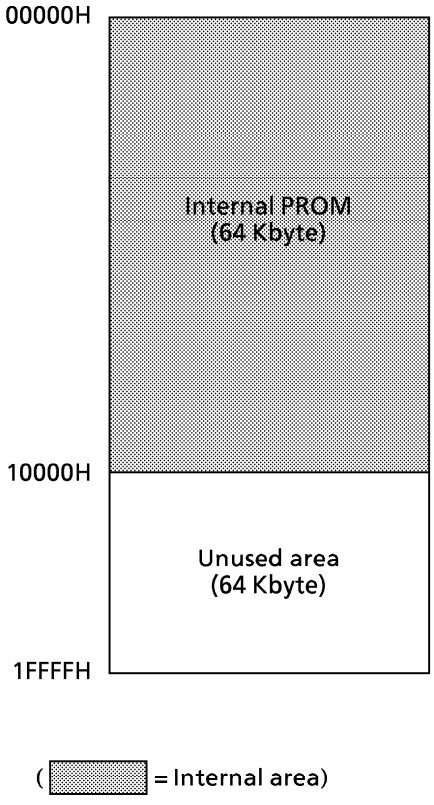


Figure 3.1.2 Memory map in PROM mode

4. Electrical Characteristics

4.1 Absolute Maximum Ratings (TMP93PS44)

"X" used in an expression shows a cycle of clock f_{FPH} selected by SYSCR1<SYSCK>. If a clock gear or a low speed oscillator is selected, a value of "X" is different. The value as an example is calculated at fc, gear = 1/fc (SYSCR1<SYSCK, GEAR 2 to 0> = "0000").

Parameter	Symbol	Rating		Unit
Power Supply Voltage	Vcc	– 0.5 to 6.5		V
Input Voltage	V_{IN}	except $\overline{EA}$ pin	– 0.5 to Vcc + 0.5	V
		$\overline{EA}$ pin	– 0.5 to 14.0	
Output current (Per 1 pin) P7	I_{OL1}	20		mA
Output current (Per 1 pin) except P7	I_{OL2}	2		mA
Output Current (P7 total)	ΣI_{OL1}	80		mA
Output Current (total)	ΣI_{OL}	120		mA
Output Current (total)	ΣI_{OH}	– 80		mA
Power Dissipation (Ta = 85°C)	P_D	350		mW
Soldering Temperature (10 s)	T_{SOLDER}	260		°C
Storage Temperature	T_{STG}	– 65 to 150		°C
Operating Temperature	T_{OPR}	– 40 to 85		°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2)

Ta = – 40 to 85°C

Parameter		Symbol	Condition	Min	Typ. (Note)	Max	Unit
Power Supply Voltage ($AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS} = 0V$)		Vcc	fc = 4 to 20 MHz, fs = 30 to 34 kHz	4.5		5.5	V
			fc = 4 to 12.5 MHz, fs = 30 to 34 kHz	2.7			
Input Low Voltage	AD0 to 15	V_{IL}	Vcc ≧ 4.5 V	– 0.3		0.8	V
			Vcc < 4.5 V			0.6	
	Port2 to 7 (except P35)	V_{IL1}	Vcc = 2.7 to 5.5 V			0.3 Vcc	
	RESET, NMI, INT0	V_{IL2}				0.25 Vcc	
	EA, AM8/16	V_{IL3}				0.3	
	X1	V_{IL4}				0.2 Vcc	
Input High Voltage	AD0 to 15	V_{IH}	Vcc ≧ 4.5 V	2.2		Vcc + 0.3	
			Vcc < 4.5 V	2.0			
	Port2 to 7 (except P35)	V_{IH1}	Vcc = 2.7 to 5.5V	0.7 Vcc			
	RESET, NMI, INT0	V_{IH2}		0.75 Vcc			
	EA, AM8/16	V_{IH3}		Vcc – 0.3			
	X1	V_{IH4}		0.8Vcc			
Output Low Voltage		V_{OL}	I_{OL} = 1.6 mA (Vcc = 2.7 to 5.5 V)			0.45	V
Output Low current (P7)		I_{OL7}	V_{OL} = 1.0V (Vcc = 5 V ± 10%)	16			mA
			V_{OL} = 1.0V (Vcc = 3 V ± 10%)	7			
Output High Voltage		V_{OH1}	I_{OH} = – 400 μA (Vcc = 3 V ± 10%)	2.4			V
		V_{OH2}	I_{OH} = – 400 μA (Vcc = 5 V ± 10%)	4.2			V

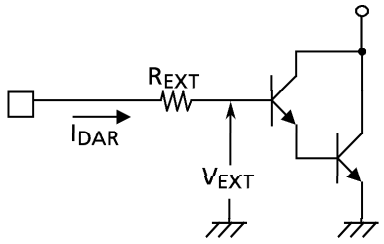
Note: Typical values are for Ta = 25°C and V_{CC} = 5 V unless otherwise noted.

4.2 DC Characteristics (2/2)

Parameter	Symbol	Condition		Min	Typ.(Note1)	Max	Unit
Darlington Drive Current (8 Output Pins Max)	I_{DAR} (Note2)	V_{EXT} = 1.5 V R_{EXT} = 1.1 kΩ (Vcc = 5 V ± 10% only)		−1.0		−3.5	mA
Input Leakage Current	I_{LI}	0.0 ≦ V_{IN} ≦ V_{CC}			0.02	±5	μA
Output Leakage Current	I_{LO}	0.2 ≦ V_{IN} ≦ V_{CC} − 0.2			0.05	±10	
Power Down Voltage (at STOP, RAM Back up)	V_{STOP}	V_{IL2} = 0.2 Vcc, V_{IH2} = 0.8 Vcc		2.0		6.0	V
Pull Up Resistance	R_{PU}	Vcc = 5.5 V		45		130	kΩ
		Vcc = 4.5 V		50		160	
		Vcc = 3.3 V		70		280	
		Vcc = 2.7 V		90		400	
Pin Capacitance	C_{IO}	fc = 1 MHz				10	pF
Schmitt Width RESET, NMI, INT0	V_{TH}			0.4	1.0		V
NORMAL (Note3)	Icc	Vcc = 5 V ± 10% fc = 20 MHz			19	25	mA
RUN					17	25	
IDLE2					12	17	
IDLE1					3.5	5	
NORMAL (Note3)		Vcc = 3 V ± 10% fc = 12.5 MHz (Typ.: Vcc = 3.0 V)			6.5	10	
RUN					5.0	9	
IDLE2					4.5	6.5	
IDLE1					0.8	1.5	
SLOW (Note3)		Vcc = 3 V ± 10% fs = 32.768 kHz (Typ.: Vcc = 3.0 V)			20	35	μA
RUN					16	30	
IDLE2					15	25	
IDLE1					5	15	
STOP		Ta ≦ 50°C	Vcc = 2.7 V to 5.5 V		0.2	10	μA
		Ta ≦ 70°C				20	
		Ta ≦ 85°C				50	

Note 1: Typical values are for Ta = 25°C and V_{CC} = 5 V unless otherwise noted.
Note 2: I_{DAR} is guranteed for total of up to 8 ports.
Note 3: I_{CC} measurement conditions (NORMAL, SLOW):
Only CPU is operational; output pins are open and input pins are fixed.

(Reference) Definition of I_{DAR}



4.3 AC Electrical Characteristics

(1) Vcc = 5 V ± 10%

No.	Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Osc. Period (= x)	t_{OSC}	50	31250	62.5		50		ns
2	CLK width	t_{CLK}	2x – 40		85		60		ns
3	A0 to 23 Valid→ CLK Hold	t_{AK}	0.5x – 20		11		5		ns
4	CLK Valid→ A0 to 23 Hold	t_{KA}	1.5x – 70		24		5		ns
5	A0 to 15 Valid→ ALE fall	t_{AL}	0.5x – 15		16		10		ns
6	ALE fall→ A0 to 15 Hold	t_{LA}	0.5x – 20		11		5		ns
7	ALE High width	t_{LL}	x – 40		23		10		ns
8	ALE fall→ $\overline{RD}$/$\overline{WR}$ fall	t_{LC}	0.5x – 25		6		0		ns
9	$\overline{RD}$/$\overline{WR}$ rise→ ALE rise	t_{CL}	0.5x – 20		11		5		ns
10	A0 to 15 Valid→ $\overline{RD}$/$\overline{WR}$ fall	t_{ACL}	x – 25		38		25		ns
11	A0 to 23 Valid→ $\overline{RD}$/$\overline{WR}$ fall	t_{ACH}	1.5x – 50		44		25		ns
12	$\overline{RD}$/$\overline{WR}$ rise→ A0 to 23 Hold	t_{CA}	0.5x – 25		6		0		ns
13	A0 to 15 Valid→ D0 to 15 input	t_{ADL}		3.0x – 55		133		95	ns
14	A0 to 23 Valid→ D0 to 15 input	t_{ADH}		3.5x – 65		154		110	ns
15	$\overline{RD}$fall → D0 to 15 input	t_{RD}		2.0x – 60		65		40	ns
16	$\overline{RD}$ Low pulse width	t_{RR}	2.0x – 40		85		60		ns
17	$\overline{RD}$rise→ D0 to 15 Hold	t_{HR}	0		0		0		ns
18	$\overline{RD}$rise→ A0 to 15output	t_{RAE}	x – 15		48		35		ns
19	$\overline{WR}$ Low pulse width	t_{WW}	2.0x – 40		85		60		ns
20	D0 to 15 Valid→ $\overline{WR}$ rise	t_{DW}	2.0x – 55		70		45		ns
21	$\overline{WR}$ rise →D0 to 15 Hold	t_{WD}	0.5x – 15		16		10		ns
22	A0 to 23 Valid→ $\overline{WAIT}$ input (1 WAIT + n mode)	t_{AWH}		3.5x – 90		129		85	ns
23	A0 to 15 Valid→ $\overline{WAIT}$ input (1 WAIT + n mode)	t_{AWL}		3.0x – 80		108		70	ns
24	$\overline{RD}$/$\overline{WR}$ fall→$\overline{WAIT}$ Hold (1 WAIT + n mode)	t_{CW}	2.0x + 0		125		100		ns
25	A0 to 23 Valid→ PORT input	t_{APH}		2.5x – 120		36		5	ns
26	A0 to 23 Valid→ PORT Hold	t_{APH2}	2.5x + 50		206		175		ns
27	$\overline{WR}$ rise→ PORT Valid	t_{CP}		200		200		200	ns

AC Measuring Conditions

- Output Level: High 2.2 V / Low 0.8 V, CL = 50 pF
  (However CL = 100 pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, CLK)
- Input Level: High 2.4 V / Low 0.45 V (AD0 to AD15)
  High 0.8 Vcc / Low 0.2 Vcc (Except for AD0 to AD15)

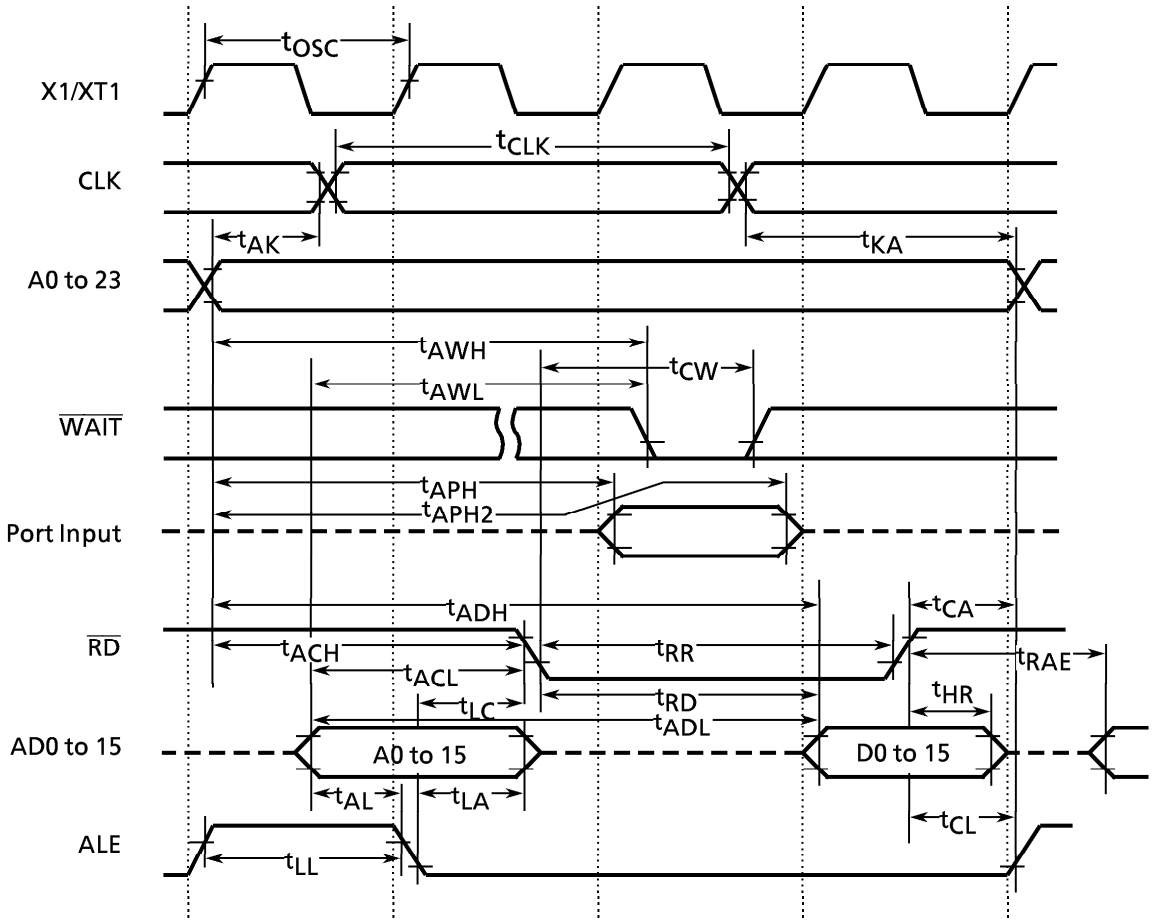
(2) Vcc = 3 V ± 10%

No.	Parameter	Symbol	Variable		12.5 MHz		Unit
			Min	Max	Min	Max	
1	Osc. Period (= x)	t_{OSC}	80	31250	80		ns
2	CLK width	t_{CLK}	2x – 40		120		ns
3	A0 to 23 Valid→ CLK Hold	t_{AK}	0.5x – 30		10		ns
4	CLK Valid→ A0 to 23 Hold	t_{KA}	1.5x – 80		40		ns
5	A0 to 15 Valid→ ALE fall	t_{AL}	0.5x – 35		5		ns
6	ALE fall→ A0 to 15 Hold	t_{LA}	0.5x – 35		5		ns
7	ALE High width	t_{LL}	x – 60		20		ns
8	ALE fall→ $\overline{RD}/\overline{WR}$ fall	t_{LC}	0.5x – 35		5		ns
9	$\overline{RD}/\overline{WR}$ rise→ ALE rise	t_{CL}	0.5x – 40		0		ns
10	A0 to 15 Valid→ $\overline{RD}/\overline{WR}$ fall	t_{ACL}	x – 50		30		ns
11	A0 to 23 Valid→ $\overline{RD}/\overline{WR}$ fall	t_{ACH}	1.5x – 50		70		ns
12	$\overline{RD}/\overline{WR}$ rise→ A0 to 23 Hold	t_{CA}	0.5x – 40		0		ns
13	A0 to 15 Valid→ D0 to 15 input	t_{ADL}		3.0x – 110		130	ns
14	A0 to 23 Valid→ D0 to 15 input	t_{ADH}		3.5x – 125		155	ns
15	$\overline{RD}$fall → D0 to 15 input	t_{RD}		2.0x – 115		45	ns
16	$\overline{RD}$ Low pulse width	t_{RR}	2.0x – 40		120		ns
17	$\overline{RD}$rise→ D0 to 15 Hold	t_{HR}	0		0		ns
18	$\overline{RD}$rise→ A0 to 15output	t_{RAE}	x – 25		55		ns
19	$\overline{WR}$ Low pulse width	t_{WW}	2.0x – 40		120		ns
20	D0 to 15 Valid→ $\overline{WR}$rise	t_{DW}	2.0x – 120		40		ns
21	$\overline{WR}$ rise →D0 to 15 Hold	t_{WD}	0.5x – 40		0		ns
22	A0 to 23 Valid→ $\overline{WAIT}$ input $\left(\begin{smallmatrix}1\,WAIT\\+\,n\,mode\end{smallmatrix}\right)$	t_{AWH}		3.5x – 130		150	ns
23	A0 to 15 Valid→ $\overline{WAIT}$ input $\left(\begin{smallmatrix}1\,WAIT\\+\,n\,mode\end{smallmatrix}\right)$	t_{AWL}		3.0x – 100		140	ns
24	$\overline{RD}/\overline{WR}$ fall→$\overline{WAIT}$ Hold $\left(\begin{smallmatrix}1\,WAIT\\+\,n\,mode\end{smallmatrix}\right)$	t_{CW}	2.0x + 0		160		ns
25	A0 to 23 Valid→ PORT input	t_{APH}		2.5x – 120		80	ns
26	A0 to 23 Valid→ PORT Hold	t_{APH2}	2.5x + 50		250		ns
27	$\overline{WR}$ rise→ PORT Valid	t_{CP}		200		200	ns

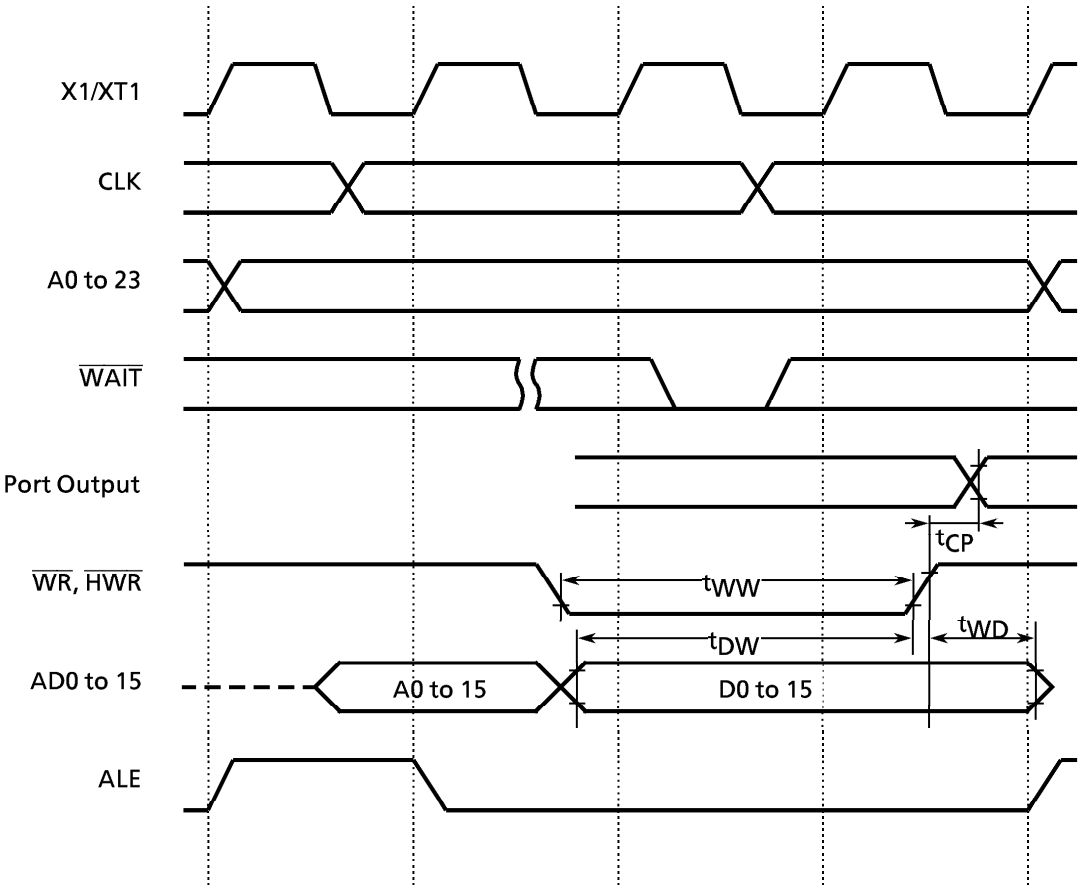
AC Measuring Conditions

- Output Level: High 0.7 × V_{CC} / Low 0.3 × V_{CC}, CL = 50 pF
- Input Level: High 0.9 × V_{CC} / Low 0.1 × V_{CC}

(3) Read Cycle


X1/XT1
CLK
A0 to 23
WAIT
Port Input
RD
AD0 to 15
ALE
tOSC
tCLK
tAK
tKA
tAWH
tAWL
tCW
tAPH
tAPH2
tADH
tCA
tACH
tRR
tRAE
tACL
tLC
tRD
tHR
tADL
A0 to 15
D0 to 15
tAL
tLA
tCL
tLL

(4) Write Cycle



4.4 Serial Channel Timing

(1) I/O Interface Mode

① SCLK Input Mode

Parameter	Symbol	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
SCLK cycle	t_{SCY}	16X		488 μs		1.28		0.8		μs
Output Data → falling edge of SCLK	t_{OSS}	t_{SCY}/2 – 5X – 50		91.5 μs		190		100		ns
SCLK rising / falling edge → Output Data hold	t_{OHS}	5X – 100		152 μs		300		150		ns
SCLK rising / falling edge → Input Data hold	t_{HSR}	0		0		0		0		ns
SCLK rising / falling edge → effective data input	t_{SRD}		t_{SCY} – 5X – 100		336 μs		780		450	ns

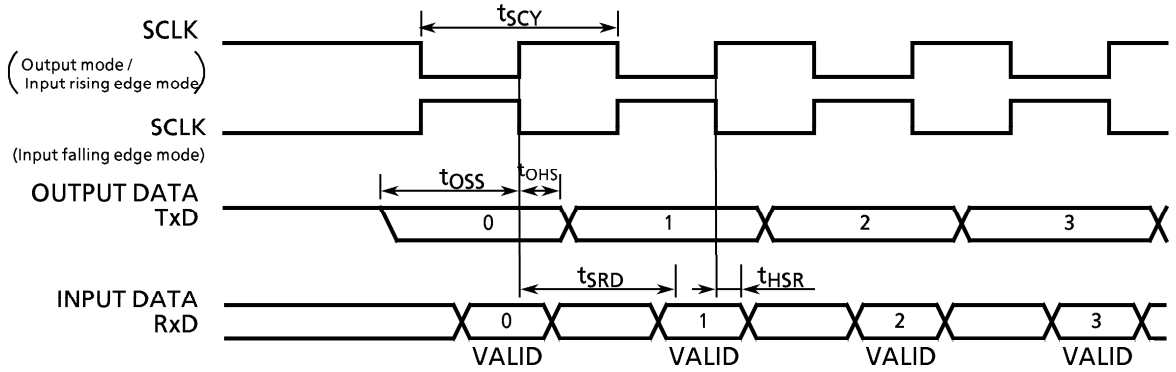
Note 1: When fs is used as system clock or fs divided by 4 is used as input clock to prescaler.

Note 2: SCLK rising/falling timing; SCLK rising in the rising mode of SCLK, SCLK falling in the falling mode of SCLK.

② SCLK Output Mode

Parameter	Symbol	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
SCLK cycle (Programmable)	t_{SCY}	16X	8192X	488 μs	250 ms	1.28	655.36	0.8	409.6	μs
Output Data → SCLK rising edge	t_{OSS}	t_{SCY} – 2X – 150		427 μs		970		550		ns
SCLK rising edge → Output Data hold	t_{OHS}	2X – 80		60 μs		80		20		ns
SCLK rising edge → Input Data hold	t_{HSR}	0		0		0		0		ns
SCLK rising edge → effective Data input	t_{SRD}		t_{SCY} – 2X – 150		428 μs		970		550	ns

Note: When fs is used as system clock or fs divided by 4 is used as input clock to prescaler.



(2) UART Mode (SCLK0, 1 are external input)

Parameter	Symbol	Variable		32.768 kHz (Note)		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
SCLK cycle	t_{SCY}	4x + 20		122 μs		340		220		ns
SCLK Low level pulse width	t_{SCYL}	2x + 5		6 μs		165		105		ns
SCLK High level pulse width	t_{SCYH}	2x + 5		6 μs		165		105		ns

Note: When fs is used as system clock or fs divided by 4 is used as input clock to prescaler.

4.5 AD Conversion Characteristics

$AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$

Parameter	Symbol	Power Supply	Min	Typ.	Max	Unit
Analog reference voltage (+)	V_{REFH}	V_{CC} = 5 V ± 10%	V_{CC} – 0.2 V	V_{CC}	V_{CC}	V
		V_{CC} = 3 V ± 10%	V_{CC} – 0.2 V	V_{CC}	V_{CC}	
Analog reference voltage (–)	V_{REFL}	V_{CC} = 5 V ± 10%	V_{SS}	V_{SS}	V_{SS} + 0.2 V	
		V_{CC} = 3 V ± 10%	V_{SS}	V_{SS}	V_{SS} + 0.2 V	
Analog input voltage range	V_{AIN}		VREFL		VREFH	
Analog current for analog reference voltage <VREFON> = 1	I_{REF} (V_{REFL} = 0 V)	V_{CC} = 5 V ± 10%		0.5	1.5	mA
		V_{CC} = 3 V ± 10%		0.3	0.9	
<VREFON> = 0		V_{CC} = 2.7 to 5.5 V		0.02	5.0	μA
Error (except quantization errors)	–	V_{CC} = 5 V ± 10%		± 1.0	± 3.0	LSB
		V_{CC} = 3 V ± 10%		± 1.0	± 5.0	

Note 1: 1LSB = (VREFH – VREFL) / 2^{10} [V]
Note 2: The operation above is guaranteed for $f_{FPH} \geqq 4$ MHz.
Note 3: The value I_{CC} includes the current which flows through the AVCC pin.

4.6 Event Counter Input Clock (external input clock: TI0, TI4, TI5, TI6, TI7)

Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock Cycle	t_{VCK}	8X + 100		740		500		ns
Low level clock Pulse width	t_{VCKL}	4X + 40		360		240		ns
High level clock Pulse width	t_{VCKH}	4X + 40		360		240		ns

4.7 Interrupt and Capture Operation

(1) $\overline{NMI}$, INT0 Interrupts

Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{NMI}$, INT0 Low level Pulse width	t_{INTAL}	4X		320		200		ns
$\overline{NMI}$, INT0 High level Pulse width	t_{INTAH}	4X		320		200		ns

(2) INT1, 4 to 7 Interrupts and Capture

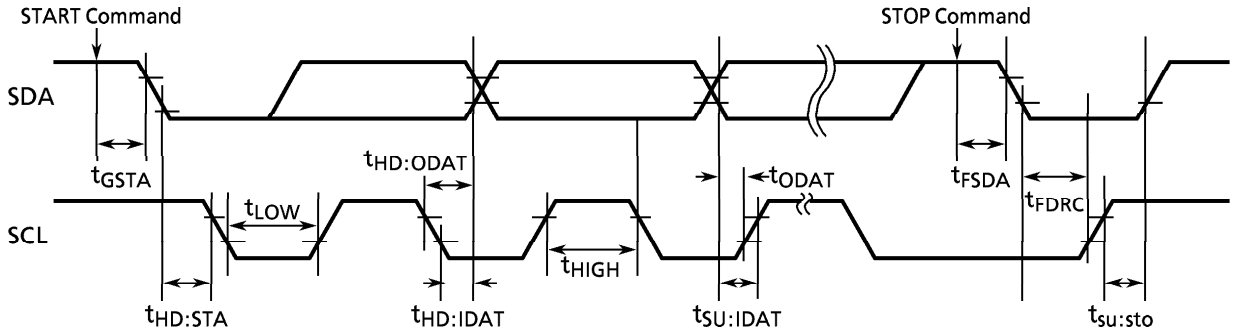
Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
INT1, INT4 to INT7 Low level Pulse width	t_{INTBL}	4X + 100		420		300		ns
INT1, INT4 to INT7 High level Pulse width	t_{INTBH}	4X + 100		420		300		ns

4.8 Serial Bus Interface Timing

(1) I^2C bus Mode

Parameter	Symbol	Variable			Unit
		Min	Typ.	Max	
START command → SDA fall	t_{GSTA}	3X			s
Hold time START condition	$t_{HD:STA}$	2^nX			s
SCL Low level pulse width	t_{LOW}	2^nX			s
SCL High level pulse width	t_{HIGH}	2^nX + 12X			s
Data hold time (input)	$t_{HD:IDAT}$	0			ns
Data set-up time (input)	$t_{SU:IDAT}$	250			ns
Data hold time (output)	$t_{HD:ODAT}$	7X		11X	s
Data output → SCL Rising edge	t_{ODAT}		2^nX – $t_{HD:ODAT}$		s
STOP command → SDA fall	t_{FSDA}	3X			s
SDA Falling edge → SCL Rising edge	t_{FDRC}	2^nX			s
Set-up time STOP condition	$t_{SU:STO}$	2^nX + 16X			s

Note: "n" value is set by SBICR1 <SCK2 to 0>



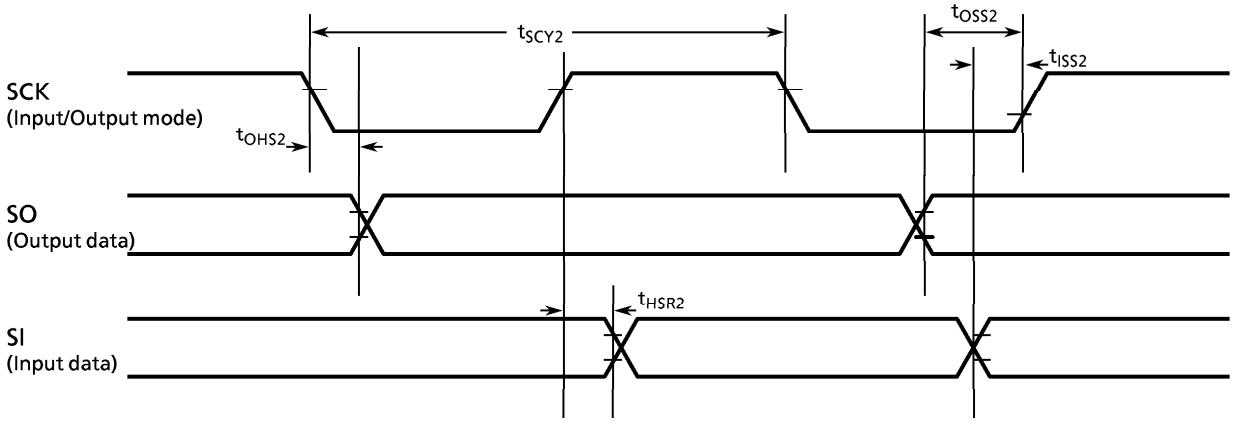
(2) Clocked-synchronous 8-bit SIO Mode

① SCK Input Mode

Parameter	Symbol	Variable		Unit
		Min	Max	
SCK cycle	t_{SCY2}	2^5X		s
SCK falling edge→ Output data hold	t_{OHS2}	6X		s
Output data → SCK rising edge	t_{OSS2}	t_{SCY2} – 6X		s
SCK rising edge→ Input data hold	t_{HSR2}	6X		ns
Input data→ SCK rising edge	t_{ISS2}	0		ns

② SCK Output Mode

Parameter	Symbol	Variable		Unit
		Min	Max	
SCK cycle	t_{SCY2}	2^5X	$2^{11}X$	s
SCK falling edge → Output data hold	t_{OHS2}	2X		s
Output data→ SCK rising edge	t_{OSS2}	t_{SCY2} – 2X		s
SCK rising edge→ Input data hold	t_{HSR2}	2X		s
Input data→ SCK rising edge	t_{ISS2}	0		ns



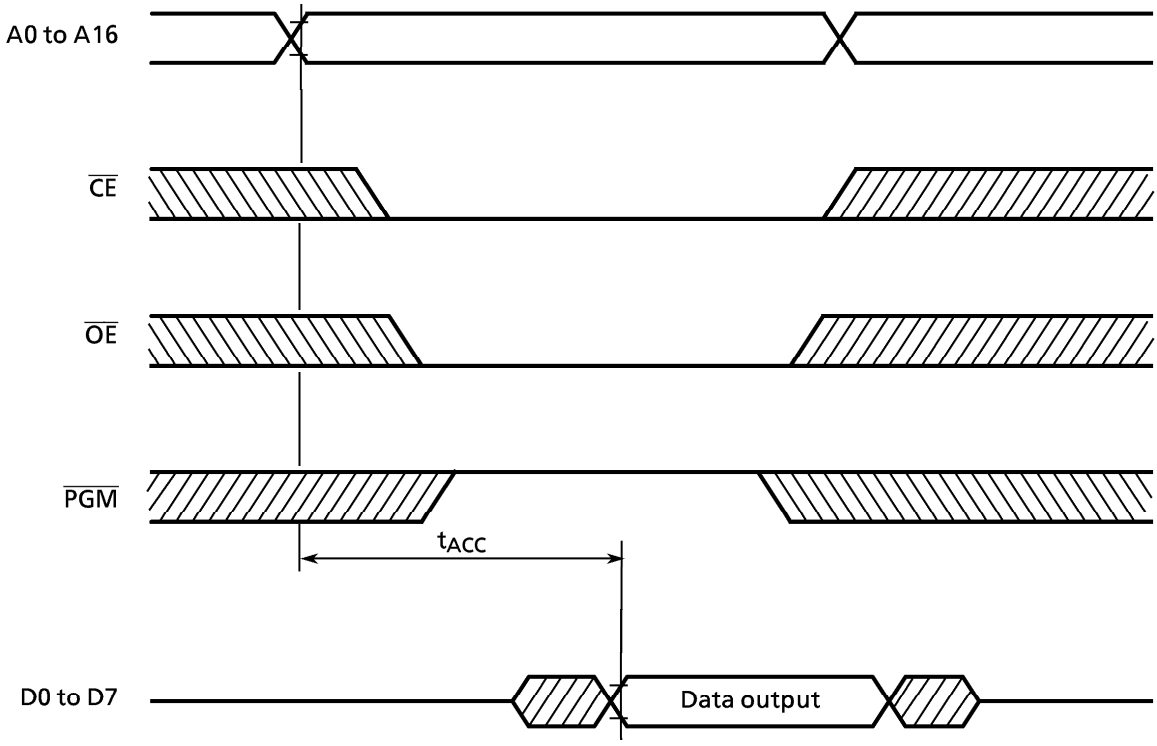
4.9 Read operation in PROM mode

DC / AC characteristics

Ta = 25 ± 5°C Vcc = 5 V ± 10%

Parameter	Symbol	Condition	Min	Max	Unit
V_{PP} Read Voltage	V_{PP}	–	4.5	5.5	V
Input High Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IH1}	–	2.2	V_{CC} + 0.3	V
Input Low Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IL1}	–	– 0.3	0.8	V
Address to Output Delay	t_{ACC}	C_L = 50 pF	–	2.25TCYC + α	ns

TCYC = 400 ns (10 MHz Clock)
α = 200 ns

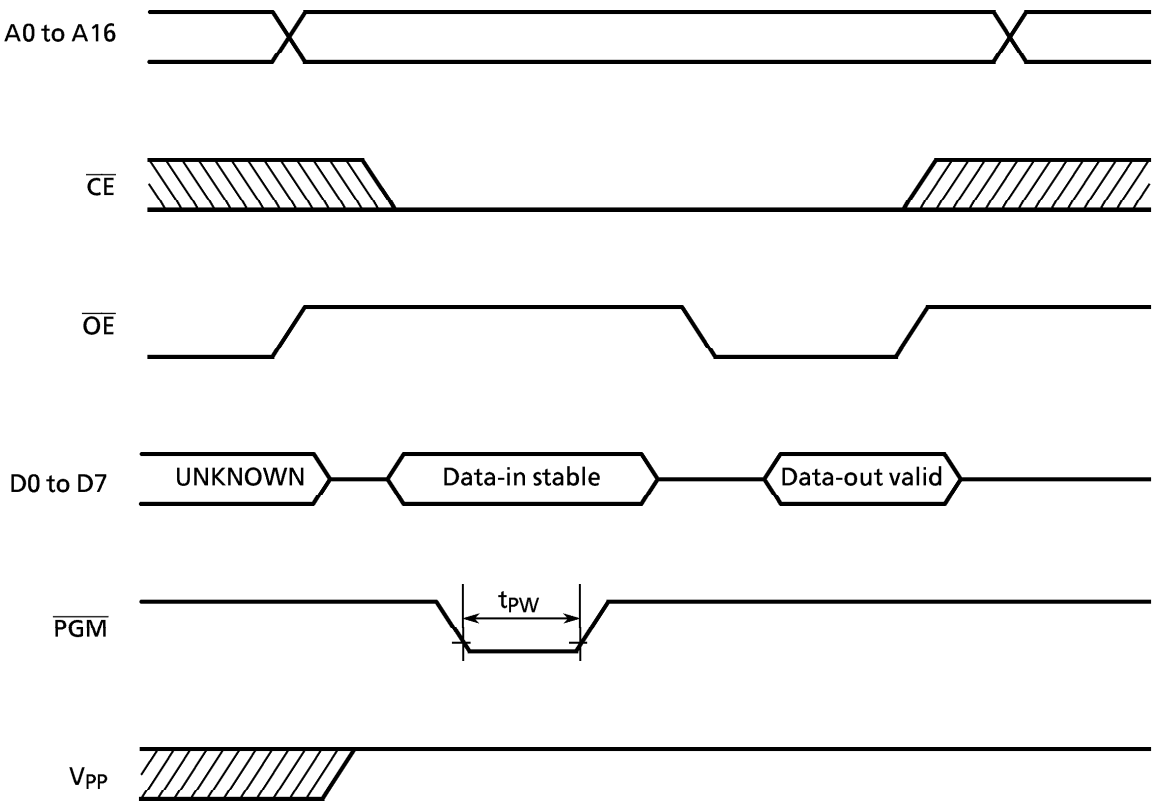


4.10 Program operation in PROM mode

DC / AC characteristics

Ta = 25 ± 5°C Vcc = 6.25 V ± 0.25 V

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Programming Supply Voltage	V_{PP}	–	12.50	12.75	13.00	V
Input High Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IH}	–	2.6		V_{CC} + 0.3	V
Input Low Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IL}	–	– 0.3		0.8	V
V_{CC} Supply Current	I_{CC}	fc = 10 MHz	–		50	mA
V_{PP} Supply Current	I_{PP}	V_{PP} = 13.00 V	–		50	mA
$\overline{PGM}$ Program Pulse Width	t_{PW}	C_L = 50 pF	0.095	0.1	0.105	ms



Note 1: The power supply of V_{PP} (12.75 V) must br set power-on at the same time or the later time for a power supply of V_{CC} and must be clear power-on at the same time or early time for a power supply of V_{CC}.

Note 2: The pulling up/down device on condition of V_{PP} = 12.75 V suffers a damage for the device.

Note 3: The maximum spec of V_{PP} pin is 14.0 V. Be carefull a overshoot at the programming.