Low Voltage / Low Power CMOS 16-bit Microcontrollers

TMP93CM40F

1. Outline and Device Characteristics

The TMP93CM40 is high-speed, advanced 16-bit microcontrollers developed for controlling medium to large-scale equipment. They enable low-voltage and low-power-consumption operation.
The TMP93CM40 is housed in 100-pin flat packages.
The device characteristics are as follows:

(1) Original 16-bit CPU (900/L CPU)

- TLCS-90 instruction mnemonic upward compatible
- 16 Mbyte linear address space
- General-purpose registers, register bank system
- 16-bit multiplication, 16-bit division, bit transfer and bit manipulation instructions
- Micro DMA: 4 channels (1.6 μs per 2 bytes at 20 MHz)

(2) Minimum instruction execution time: 200 ns at 20 MHz

(3) Internal RAM: 2 Kbytes

Internal ROM: 32 Kbytes

(4) External memory expansion

- Can be expanded up to16 Mbytes (for both programs and data).
- AM8/$\overline{16}$ pin (select the external data bus width)
- Can mix 8- and 16-bit external data buses. (Dynamic bus sizing)

(5) 8-bit timer: 2 channels

(6) 8-bit PWM timer: 2 channels

(7) 16-bit timer: 2 channels

(8) 4-bit pattern generator: 2 channels

(9) Serial interface:2 channels

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(10) 10-bit AD converter: 8 channels

(11) Watchdog timer

(12) Chip select and wait controller: 3 blocks

(13) Interrupt functions: 29

- 9 CPU interrupts (SWI instruction, and Illegal instruction)
- 14 internal interrupts
- 6 external interrupts

7-level priority can be set.

(14) I/O ports: 79

(15) Standby function: 4 Halt modes (Run, Idle2, Idle1, Stop)

(16) Clock gear function

- Dual clock Operation
- Clock gear: High-frequency clock can be changed from fc to fc / 16.

(17) Wide Range of Operating Voltage

- Vcc = 2.7 to 5.5 V

(18) Package

Type No.	Package
TMP93CM40F	P-QFP100-1414-0.50

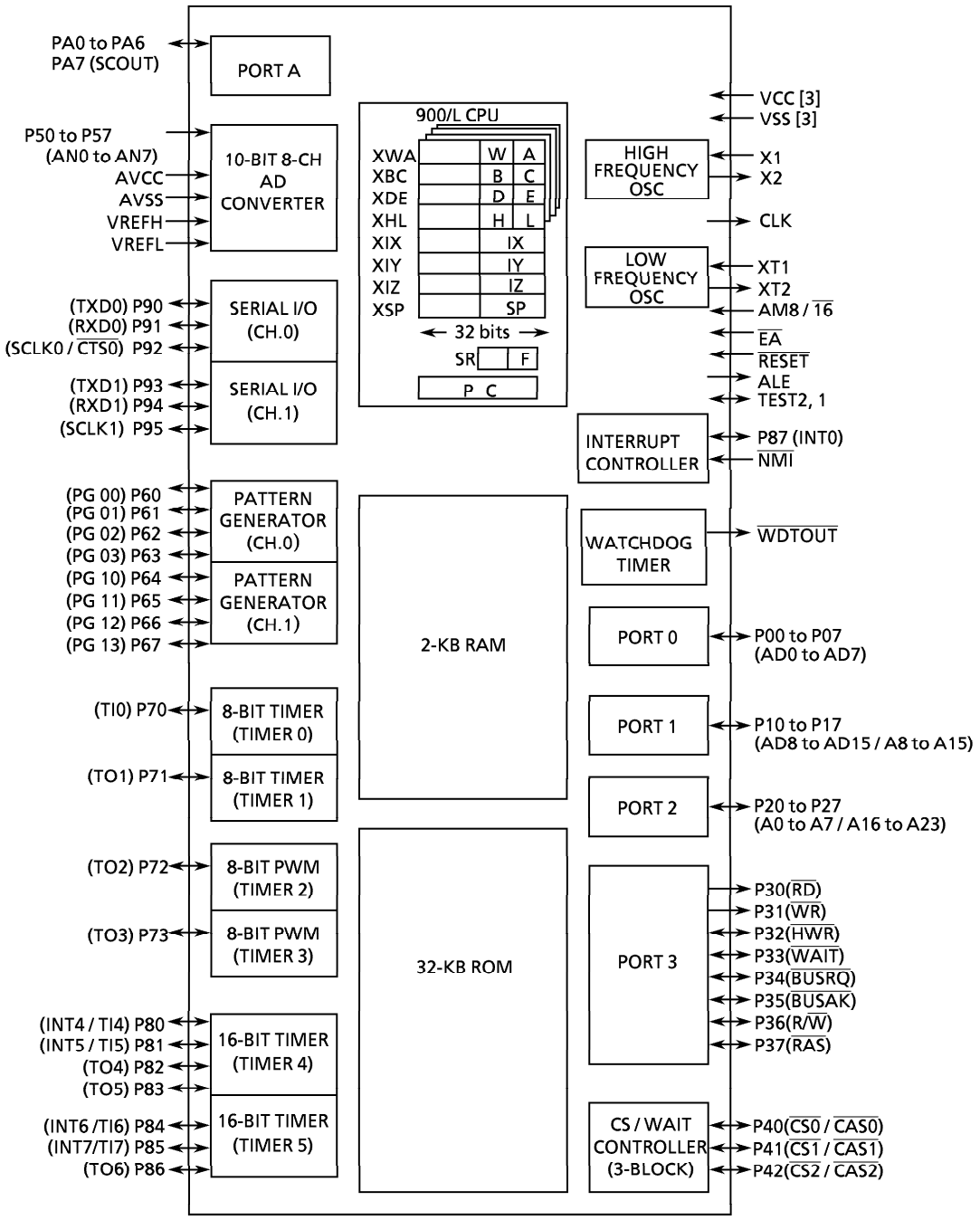


Figure 1.1 TMP93CM40 Block Diagram

2. Pin Assignment and Functions

The assignment of input and output pins for the TMP93CM40, their names and functions are described below.

2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of the TMP93CM40F.

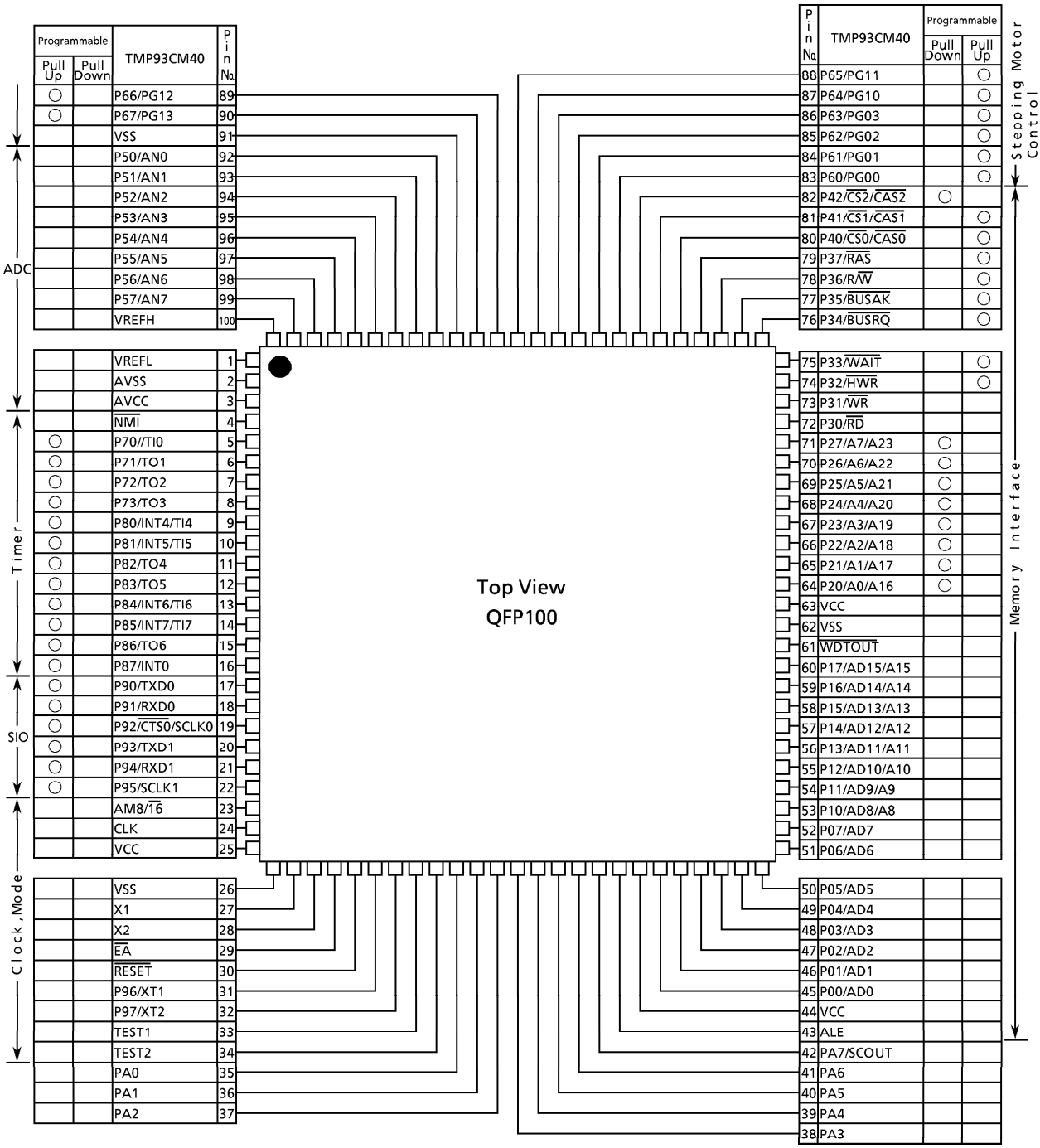


Figure 2.1.1 Pin Assignment (100-pin QFP)

2.2 Pin Names and Functions

The names of the input / output pins and their functions are described below.
Table 2.2.1 Pin Names and Functions.

Table 2.2.1 Pin Names and Functions (1/4)

Pin name	Number of pins	I/O	Functions
P00 to P07 AD0 to AD7	8	I/O 3-state	Port 0: I/O port that allows I/O to be selected at the bit level Address and data (lower): Bits 0 to 7 for address and data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O 3-state Output	Port 1: I/O port that allows I/O to be selected at the bit level Address and data (upper): Bits 8 to 15 for address and data bus Address: Bits 8 to 15 for address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows to be selected at the bit level (with pull-down resistor) Address: Bits 0 to 7 for address bus Address: Bits 16 to 23 for address bus
P30 $\overline{RD}$	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory
P31 $\overline{WR}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data on pins AD0 to 7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data on pins AD8 to 15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait
P34 $\overline{BUSRQ}$	1	I/O Input	Port 34: I/O port (with pull-up resistor) Bus request: Signal used to request bus release.
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus acknowledge: Signal used to acknowledge bus release.
P36 R/$\overline{W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/write: 1 represents read or dummy cycle; 0 represents write cycle.
P37 $\overline{RAS}$	1	I/O Output	Port 37: I/O port (with pull-up resistor) Row address strobe: Outputs $\overline{RAS}$ strobe for DRAM.
P40 $\overline{CS0}$ $\overline{CAS0}$	1	I/O Output Output	Port 40: I/O port (with pull-up resistor) Chip select 0: Outputs 0 when address is within specified address area. Column address strobe 0: Outputs $\overline{CAS}$ strobe for DRAM when address is within specified address area.

Note: This device's built-in memory or built-in I/O cannot be accessed by an external DMA controller, using the $\overline{BUSRQ}$ and $\overline{BUSAK}$ signals.

Table 2.2.1 Pin Names and Functions (2/4)

Pin name	Number of pins	I/O	Functions
P41 $\overline{CS1}$ $\overline{CAS1}$	1	I/O Output Output	Port 41: I/O port (with pull-up resistor) Chip select 1: Outputs 0 if address is within specified address area. Column address strobe 1: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P42 $\overline{CS2}$ $\overline{CAS2}$	1	I/O Output Output	Port 42: I/O port (with pull-down resistor) Chip select 2: Outputs 0 if address is within specified address area. Column address strobe 2: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P50 to P57 AN0 to AN7	8	Input Input	Port 5: Pin used to input port Analog input: Pin used to input to AD converter
VREFH	1	Input	Pin for reference voltage input to AD converter (H)
VREFL	1	Input	Pin for reference voltage input to AD converter (L)
P60 to P63 PG00 to PG03	4	I/O Output	Ports 60 - 63: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor) Pattern generator ports: 00 - 03
P64 to P67 PG10 to PG13	4	I/O Output	Ports 64 - 67: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor) Pattern generator ports: 10 - 13
P70 TI0	1	I/O Input	Port 70: I/O port (with pull-up resistor) Timer input 0: Timer 0 input
P71 TO1	1	I/O Output	Port 71: I/O port (with pull-up resistor) Timer output 1: Timer 0 or 1 output
P72 TO2	1	I/O Output	Port 72: I/O port (with pull-up resistor) PWM output 2: 8-bit PWM timer 2 output
P73 TO3	1	I/O Output	Port 73: I/O port (with pull-up resistor) PWM output 3: 8-bit PWM timer 3 output
P80 TI4 INT4	1	I/O Input Input	Port 80: I/O port (with pull-up resistor) Timer input 4: Timer 4 count / capture trigger signal input Interrupt request pin 4: Interrupt request pin with programmable rising / falling edge
P81 TI5 INT5	1	I/O Input Input	Port 81: I/O port (with pull-up resistor) Timer input 5: Timer 4 count / capture trigger signal input Interrupt request pin 5: Interrupt request pin with rising edge
P82 TO4	1	I/O Output	Port 82: I/O port (with pull-up resistor) Timer output 4: Timer 4 output pin
P83 TO5	1	I/O Output	Port 83: I/O port (with pull-up resistor) Timer output 5: Timer 4 output pin

Table 2.2.1 Pin Names and Functions (3/4)

Pin name	Number of pins	I/O	Functions
P84 TI6 INT6	1	I/O Input Input	Port 84: I/O port (with pull-up resistor) Timer input 6: Timer 5 count / capture trigger signal input Interrupt request pin 6: Interrupt request pin with programmable rising / falling edge
P85 TI7 INT7	1	I/O Input Input	Port 85: I/O port (with pull-up resistor) Timer input 7: Timer 5 count / capture trigger signal input Interrupt request pin 7: Interrupt request pin with rising edge
P86 TO6	1	I/O Output	Port 86: I/O port (with pull-up resistor) Timer output 6: Timer 5 output pin
P87 INT0	1	I/O Input	Port 87: I/O port (with pull-up resistor) Interrupt request pin 0: Interrupt request pin with programmable level / rising edge
P90 TXD0	1	I/O Output	Port 90: I/O port (with pull-up resistor) Serial send data 0
P91 RXD0	1	I/O Input	Port 91: I/O port (with pull-up resistor) Serial receive data 0
P92 $\overline{CTS0}$ SCLK0	1	I/O Input I/O	Port 92: I/O port (with pull-up resistor) Serial data send enable 0 (Clear to Send) Serial Clock I/O 0
P93 TXD1	1	I/O Output	Port 93: I/O port (with pull-up resistor) Serial send data 1
P94 RXD1	1	I/O Input	Port 94: I/O port (with pull-up resistor) Serial receive data 1
P95 SCLK1	1	I/O I/O	Port 95: I/O port (with pull-up resistor) Serial clock I/O 1
PA0 to PA6	7	I/O	Port A0 to A6: I/O ports
PA7 SCOUT	1	I/O Output	Port A7: I/O port System Clock Output: Outputs f_{FPH} or f_{SYS} clock.
$\overline{WDTOUT}$	1	Output	Watchdog timer output pin
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge or both edges.
CLK	1	Output	Clock output: Outputs $\lceil f_{SYS} \div 2 \rfloor$ Clock. Pulled-up during reset. can be disabled for reducing noise.
$\overline{EA}$	1	Input	External access: The VCC pin should be connected.

Table 2.2.1 Pin Names and Functions (4/4)

Pin name	Number of pins	I/O	Functions
AM8 / $\overline{16}$	1	Input	Address Mode: Selects external Data Bus width. The VCC pin should be connected. The Data Bus Width for external access is set by the Chip Select / WAIT Control register, Port 1 Control register.
ALE	1	Output	Address Latch Enable Can be disabled for reducing noise.
$\overline{\text{RESET}}$	1	Input	Reset: Initializes TMP93CM40. (With pull-up resistor)
X1/X2	2	I/O	High Frequency Oscillator connecting pin
P96 XT1	1	I/O Input	Port 96: I/O port (Open Drain Output) Low Frequency Oscillator connecting pin
P97 XT2	1	I/O Output	Port 97: I/O port (Open Drain Output) Low Frequency Oscillator connecting pin
TEST1 / TEST2	2	Output / Input	TEST1 should be connected with TEST2 pin.
VCC	3		Power supply pin (All VCC pins should be connected with the power supply pin.)
VSS	3		GND pin (0 V) (All VSS pins should be connected with GND (0 V).)
AVCC	1		Power supply pin for AD converter
AVSS	1		GND pin for AD converter (0 V)

Note: All pins that have built-in pull-up / pull-down resistors (other than the $\overline{\text{RESET}}$ pin) can be disconnected from the built-in pull-up / down resistor by software.

3. Operation

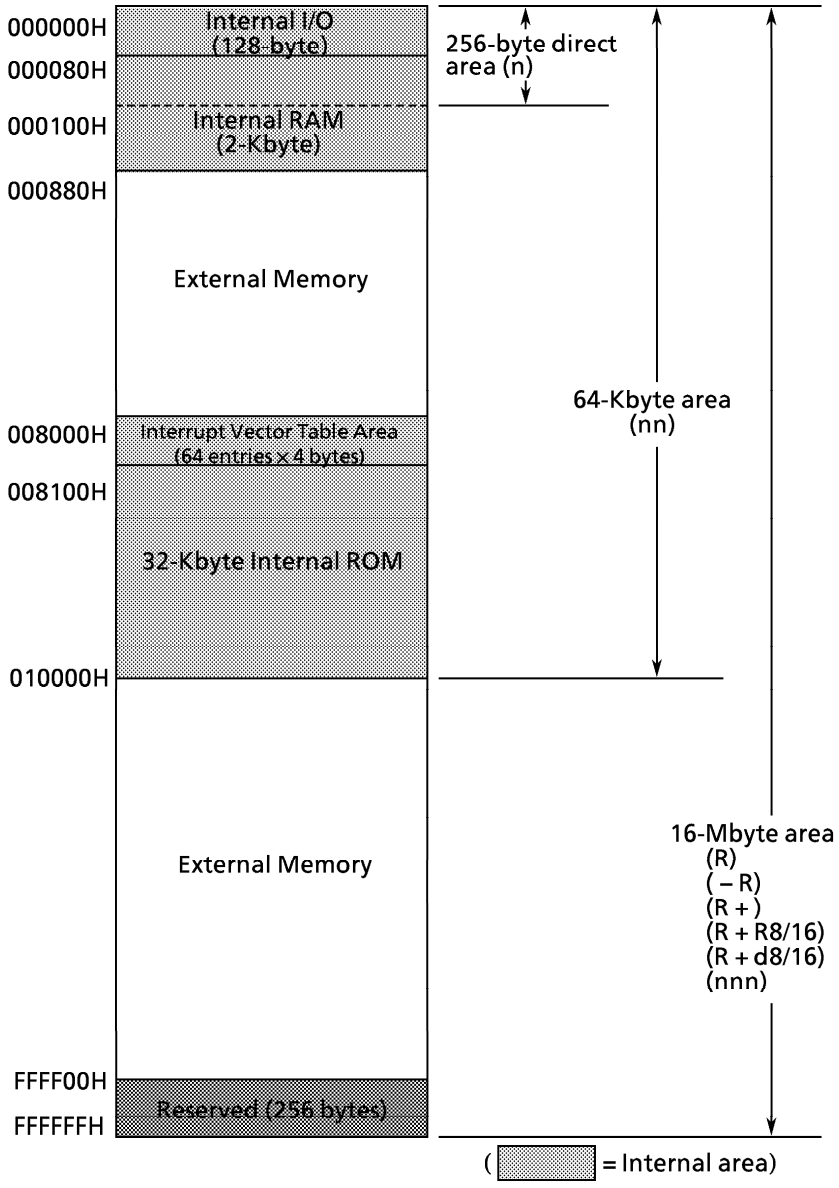
This section describes the functions and basic operation of all blocks of the TMP93CM40 devices.

3.1 CPU

The TMP93CM40 has a built-in high-performance 16-bit CPU (900/L CPU). (For a description of this CPU's operation, see the sub-section TLCS-900/L CPU in the previous section.

3.2 Memory Map

Figure 3.2.1 is a memory map of the TMP93CM40.



Note: The 256-byte area from FFFF00H to FFFFFFH cannot be used.

Figure 3.2.1 Memory Map

4. Electrical Characteristics

4.1 Absolute Maximum Ratings (TMP93CM40F)

"X" used in an expression shows a frequency for the clock f_{FPH} selected by SYSCR1<SYSCK>. The value of X changes according to whether a clock gear or a low speed oscillator is selected. An example value is calculated for fc, with gear = 1/fc (SYSCR1<SYSCK, GEAR 2 to 0> = 0000).

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 6.5	V
Input Voltage	V_{IN}	– 0.5 to V_{CC} + 0.5	V
Output Current (total)	ΣI_{OL}	120	mA
Output Current (total)	ΣI_{OH}	– 80	mA
Power Dissipation (Ta = 85℃)	P_D	600	mW
Soldering Temperature (10 s)	T_{SOLDER}	260	℃
Storage Temperature	T_{STG}	– 65 to 150	℃
Operating Temperature	T_{OPR}	– 40 to 85	℃

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2)

Parameter		Symbol	Condition	Min	Typ. (Note 1)	Max	Unit
Power Supply Voltage ($AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS} = 0V$)		V_{CC}	fc = 4 to 16 MHz fs = 30 to 34 kHz (Ta = − 40 to 85°C)	4.5		5.5	V
			fc = 4 to 20 MHz fs = 30 to 34 kHz (Ta = − 20 to 70°C)				
			fc = 4 to 10 MHz fs = 30 to 34 kHz (Ta = − 40 to 85°C)	2.7 (Note 2)			
Input Low Voltage	AD0 to 15	V_{IL}	$V_{CC} \geqq 4.5$ V	−0.3		0.8	V
			$V_{CC} < 4.5$ V			0.6	
	Port 2 to A (except P87, P5)	V_{IL1}	V_{CC} = 2.7 to 5.5 V			0.3 V_{CC}	
	RESET,NMI,INT0	V_{IL2}				0.25 V_{CC}	
	EA, AM8/16	V_{IL3}				0.3	
	X1, P5	V_{IL4}				0.2 V_{CC}	
Input High Voltage	AD0 to 15	V_{IH}	$V_{CC} \geqq 4.5$ V	2.2		V_{CC} + 0.3	
			$V_{CC} < 4.5$ V	2.0			
	Port 2 to A (except P87)	V_{IH1}	V_{CC} = 2.7 to 5.5 V	0.7V_{CC}			
	RESET, NMI, INT0	V_{IH2}		0.75V_{CC}			
	EA, AM8/16	V_{IH3}		V_{CC} − 0.3			
	X1	V_{IH4}		0.8V_{CC}			
Output Low Voltage		V_{OL}	I_{OL} = 1.6 mA (V_{CC} = 2.7 to 5.5 V)			0.45	V
Output High Voltage		V_{OH1}	I_{OH} = − 400 μA (V_{CC} = 3 V ± 10%)	2.4			
		V_{OH2}	I_{OH} = − 400 μA (V_{CC} = 5 V ± 10%)	4.2			

Note 1: Typical values are for Ta = 25°C and V_{CC} = 5 V unless otherwise noted.

Note 2: The operation of the AD converter is guaranteed at V_{CC} = 5 V ± 10%.

4.2 DC Characteristics (2/2)

Parameter	Symbol	Condition	Min	Typ. (Note 1)	Max	Unit
Darlington Drive Current (8 Output Pins Max)	I_{DAR} (Note 2)	V_{EXT} = 1.5 V, R_{EXT} = 1.1 kΩ (only when V_{CC} = 5 V ± 10%)	−1.0		−3.5	mA
Input Leakage Current	I_{LI}	$0.0 \leqq V_{IN} \leqq V_{CC}$		0.02	±5	μA
Output Leakage Current	I_{LO}	$0.2 \leqq V_{IN} \leqq V_{CC} - 0.2$		0.05	±10	μA
Powerdown Voltage (at Stop, RAM Back-up)	V_{STOP}	V_{IL2} = 0.2V_{CC}, V_{IH2} = 0.8V_{CC}	2.0		6.0	V
$\overline{RESET}$ Pull-up Resistor	R_{RST}	V_{CC} = 5 V ± 10%	50		150	kΩ
		V_{CC} = 3 V ± 10%	80		200	kΩ
Pin Capacitance	C_{IO}	fc = 1 MHz			10	pF
Schmitt Width $\overline{RESET}$, $\overline{NMI}$, INT0	V_{TH}		0.4	1.0		V
Programmable Pull-down Resistor	RKL	V_{CC} = 5 V ± 10%	10		80	kΩ
		V_{CC} = 3 V ± 10%	30		150	kΩ
Programmable Pull-up Resistor	RKH	V_{CC} = 5 V ± 10%	50		150	kΩ
		V_{CC} = 3 V ± 10%	100		300	kΩ
Normal (Note 3)	I_{CC}	V_{CC} = 5 V ± 10%, fc = 20 MHz		19	25	mA
Normal2 (Note 4)				24	30	mA
Run				17	25	mA
Idle2				10	15	mA
Idle1				3.5	5	mA
Normal (Note 3)		V_{CC} = 3 V ± 10%, fc = 10 MHz (Typ: V_{CC} = 3.0 V)		5.5	8	mA
Normal2 (Note 4)				8.5	11	mA
Run				4.0	7	mA
Idle2				2.5	4	mA
Idle1				0.7	1.2	mA
Slow (Note 3)		V_{CC} = 3 V ± 10%, fs = 32.768 kHz (Typ: V_{CC} = 3.0 V)		20	35	μA
Run				16	30	μA
Idle2				10	20	μA
Idle1				5	15	μA
Stop		V_{CC} = 2.7 to 5.5 V		0.2	10	μA

Note 1: Typical values are for Ta = 25°C and V_{CC} = 5 V unless otherwise noted.
Note 2: I_{DAR} is guaranteed for up to eight ports.
Note 3: I_{CC} measurement conditions (Normal, Slow):
Only CPU is operational; output pins are open and input pins are fixed.
Note 4: I_{CC} measurement conditions (Normal 2):
All functions are operational; output pins are open and input pins are fixed.

4.3 AC Electrical Characteristics

(1) V_{CC} = 5 V ± 10%

No.	Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Osc. Period (= x)	t_{OSC}	50	31250	62.5		50		ns
2	CLK pulse width	t_{CLK}	2x – 40		85		60		ns
3	A0 to A23 Valid→ CLK Hold	t_{AK}	0.5x – 20		11		5		ns
4	CLK Valid→ A0 to A23 Hold	t_{KA}	1.5x – 70		24		5		ns
5	A0 to A15 Valid→ ALE Fall	t_{AL}	0.5x – 15		16		10		ns
6	ALE fall→ A0 to A15 Hold	t_{LA}	0.5x – 20		11		5		ns
7	ALE High pulse Width	t_{LL}	x – 40		23		10		ns
8	ALE Fall→ $\overline{RD}$/$\overline{WR}$ Fall	t_{LC}	0.5x – 25		6		0		ns
9	$\overline{RD}$/$\overline{WR}$ Rise→ ALE Rise	t_{CL}	0.5x – 20		11		5		ns
10	A0 to A15 Valid→ $\overline{RD}$/$\overline{WR}$ Fall	t_{ACL}	x – 25		38		25		ns
11	A0 to A23 Valid→ $\overline{RD}$/$\overline{WR}$ Fall	t_{ACH}	1.5x – 50		44		25		ns
12	$\overline{RD}$/$\overline{WR}$ Rise → A0 to A23 Hold	t_{CA}	0.5x – 25		6		0		ns
13	A0 to A15 Valid→ D0 to D15 Input	t_{ADL}		3.0x – 55		133		95	ns
14	A0 to A23 Valid→ D0 to D15 Input	t_{ADH}		3.5x – 65		154		110	ns
15	$\overline{RD}$ Fall → D0 to D15 Input	t_{RD}		2.0x – 60		65		40	ns
16	$\overline{RD}$ Low Pulse Width	t_{RR}	2.0x – 40		85		60		ns
17	$\overline{RD}$ Rise→ D0 to D15 Hold	t_{HR}	0		0		0		ns
18	$\overline{RD}$ Rise→ A0 to A15 Output	t_{RAE}	x – 15		48		35		ns
19	$\overline{WR}$ Low Pulse Width	t_{WW}	2.0x – 40		85		60		ns
20	D0 to D15 Valid→ $\overline{WR}$ Rise	t_{DW}	2.0x – 55		70		45		ns
21	$\overline{WR}$ Rise →D0 to D15 Hold	t_{WD}	0.5x – 15		16		10		ns
22	A0 to A23 Valid→ $\overline{WAIT}$ Input (1WAIT + n mode)	t_{AWH}		3.5x – 90		129		85	ns
23	A0 to A15 Valid→ $\overline{WAIT}$ Input (1WAIT + n mode)	t_{AWL}		3.0x – 80		108		70	ns
24	$\overline{RD}$/$\overline{WR}$ Fall→$\overline{WAIT}$ Hold (1WAIT + n mode)	t_{CW}	2.0x + 0		125		100		ns
25	A0 to A23 Valid→ PORT Input	t_{APH}		2.5x – 120		36		5	ns
26	A0 to A23 Valid→ PORT Hold	t_{APH2}	2.5x + 50		206		175		ns
27	$\overline{WR}$ Rise→ PORT Valid	t_{CP}		200		200		200	ns
28	A0 to A23 Valid→ $\overline{RAS}$ Fall	t_{ASRH}	1.0x – 40		23		10		ns
29	A0 to A15 Valid→ $\overline{RAS}$ Fall	t_{ASRL}	0.5x – 15		16		10		ns
30	$\overline{RAS}$ Fall→ D0 to D15 Input	t_{RAC}		2.5x – 70		86		55	ns
31	$\overline{RAS}$ Fall→ A0 to A15 Hold	t_{RAH}	0.5x – 15		16		10		ns
32	$\overline{RAS}$ Low Pulse Width	t_{RAS}	2.0x – 40		85		60		ns
33	$\overline{RAS}$ High Pulse Width	t_{RP}	2.0x – 40		85		60		ns
34	$\overline{CAS}$ Fall→ $\overline{RAS}$ Rise	t_{RSH}	1.0x – 40		23		10		ns
35	$\overline{RAS}$ Rise→ $\overline{CAS}$ Rise	t_{RSC}	0.5x – 25		6		0		ns
36	$\overline{RAS}$ Fall→ $\overline{CAS}$ Fall	t_{RCD}	1.0x – 40		23		10		ns
37	$\overline{CAS}$ Fall→ D0 to D15 Input	t_{CAC}		1.5x – 65		29		10	ns
38	$\overline{CAS}$ Low Pulse Width	t_{CAS}	1.5x – 30		64		40		ns

AC Measuring Conditions

- Output Level: High 2.2 V / Low 0.8 V, CL = 50 pF
  (However, CL = 100 pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, CLK, $\overline{RAS}$, $\overline{CAS0}$ to $\overline{CAS2}$)
- Input Level: High 2.4 V / Low 0.45 V (AD0 to AD15)
  High 0.8 × V_{CC} / Low 0.2 × V_{CC} (except for AD0 to AD15)

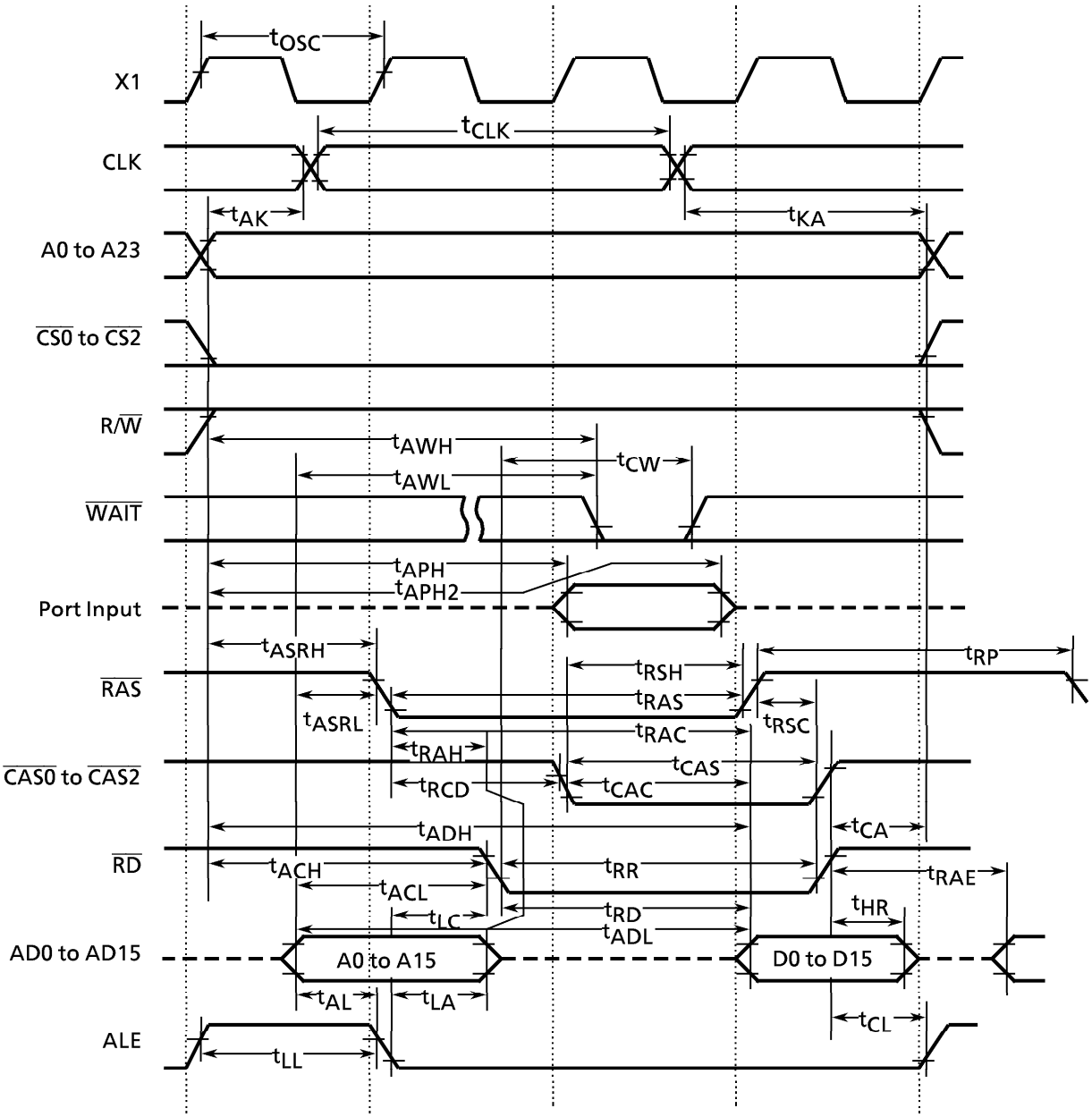
(2) V_{CC} = 3 V ± 10% (TMP93CM40 is guaranteed up to 10 MHz operation)

No.	Parameter	Symbol	Variable		10 MHz		Unit
			Min	Max	Min	Max	
1	Osc. Period (= x)	t_{OSC}	100	31250	100		ns
2	CLK pulse Width	t_{CLK}	2x – 40		160		ns
3	A0 to A23 Valid→ CLK Hold	t_{AK}	0.5x – 30		20		ns
4	CLK Valid→ A0 to A23 Hold	t_{KA}	1.5x – 80		70		ns
5	A0 to A15 Valid→ ALE Fall	t_{AL}	0.5x – 35		15		ns
6	ALE Fall→ A0 to A15 Hold	t_{LA}	0.5x – 35		15		ns
7	ALE High pulse Width	t_{LL}	x – 60		40		ns
8	ALE Fall→ $\overline{RD}/\overline{WR}$ Fall	t_{LC}	0.5x – 35		15		ns
9	$\overline{RD}/\overline{WR}$ Rise→ ALE Rise	t_{CL}	0.5x – 40		10		ns
10	A0 to A15 Valid→ $\overline{RD}/\overline{WR}$ Fall	t_{ACL}	x – 50		50		ns
11	A0 to A23 Valid→ $\overline{RD}/\overline{WR}$ Fall	t_{ACH}	1.5x – 50		100		ns
12	$\overline{RD}/\overline{WR}$ Rise→ A0 to A23 Hold	t_{CA}	0.5x – 40		10		ns
13	A0 to A15 Valid→ D0 to D15 Input	t_{ADL}		3.0x – 110		190	ns
14	A0 to A23 Valid→ D0 to D15 Input	t_{ADH}		3.5x – 125		225	ns
15	$\overline{RD}$ Fall →D0 to D15 Input	t_{RD}		2.0x – 115		85	ns
16	$\overline{RD}$ Low Pulse Width	t_{RR}	2.0x – 40		160		ns
17	$\overline{RD}$ Rise→ D0 to D15 Hold	t_{HR}	0		0		ns
18	$\overline{RD}$ Rise→ A0 to A15output	t_{RAE}	x – 25		75		ns
19	$\overline{WR}$ Low Pulse Width	t_{WW}	2.0x – 40		160		ns
20	D0 to D15 Valid→ $\overline{WR}$ Rise	t_{DW}	2.0x – 120		80		ns
21	$\overline{WR}$ Rise →D0 to D15 Hold	t_{WD}	0.5x – 40		10		ns
22	A0 to A23 Valid→ $\overline{WAIT}$ Input (1WAIT + n mode)	t_{AWH}		3.5x – 130		220	ns
23	A0 to A15 Valid→ $\overline{WAIT}$ Input (1WAIT + n mode)	t_{AWL}		3.0x – 100		200	ns
24	$\overline{RD}/\overline{WR}$ Fall→$\overline{WAIT}$ Hold (1WAIT + n mode)	t_{CW}	2.0x + 0		200		ns
25	A0 to A23 Valid→ PORT input	t_{APH}		2.5x – 245		5	ns
26	A0 to A23 Valid→ PORT Hold	t_{APH2}	2.5x + 50		300		ns
27	$\overline{WR}$ Rise→ PORT Valid	t_{CP}		200		200	ns
28	A0 to A23 Valid→ $\overline{RAS}$ Fall	t_{ASRH}	1.0x – 60		40		ns
29	A0 to A15 Valid→ $\overline{RAS}$ Fall	t_{ASRL}	0.5x – 40		10		ns
30	$\overline{RAS}$ Fall→ D0 to D15 Input	t_{RAC}		2.5x – 90		160	ns
31	$\overline{RAS}$ Fall→ A0 to A15 Hold	t_{RAH}	0.5x – 25		25		ns
32	$\overline{RAS}$ Low Pulse Width	t_{RAS}	2.0x – 40		160		ns
33	$\overline{RAS}$ High Pulse Width	t_{RP}	2.0x – 40		160		ns
34	$\overline{CAS}$ Fall→ $\overline{RAS}$ Rise	t_{RSH}	1.0x – 55		45		ns
35	$\overline{RAS}$ Rise→ $\overline{CAS}$ Rise	t_{RSC}	0.5x – 25		25		ns
36	$\overline{RAS}$ Fall→ $\overline{CAS}$ Fall	t_{RCD}	1.0x – 40		60		ns
37	$\overline{CAS}$ Fall→ D0 to D15 Input	t_{CAC}		1.5x – 120		30	ns
38	$\overline{CAS}$ Low Pulse Width	t_{CAS}	1.5x – 40		110		ns

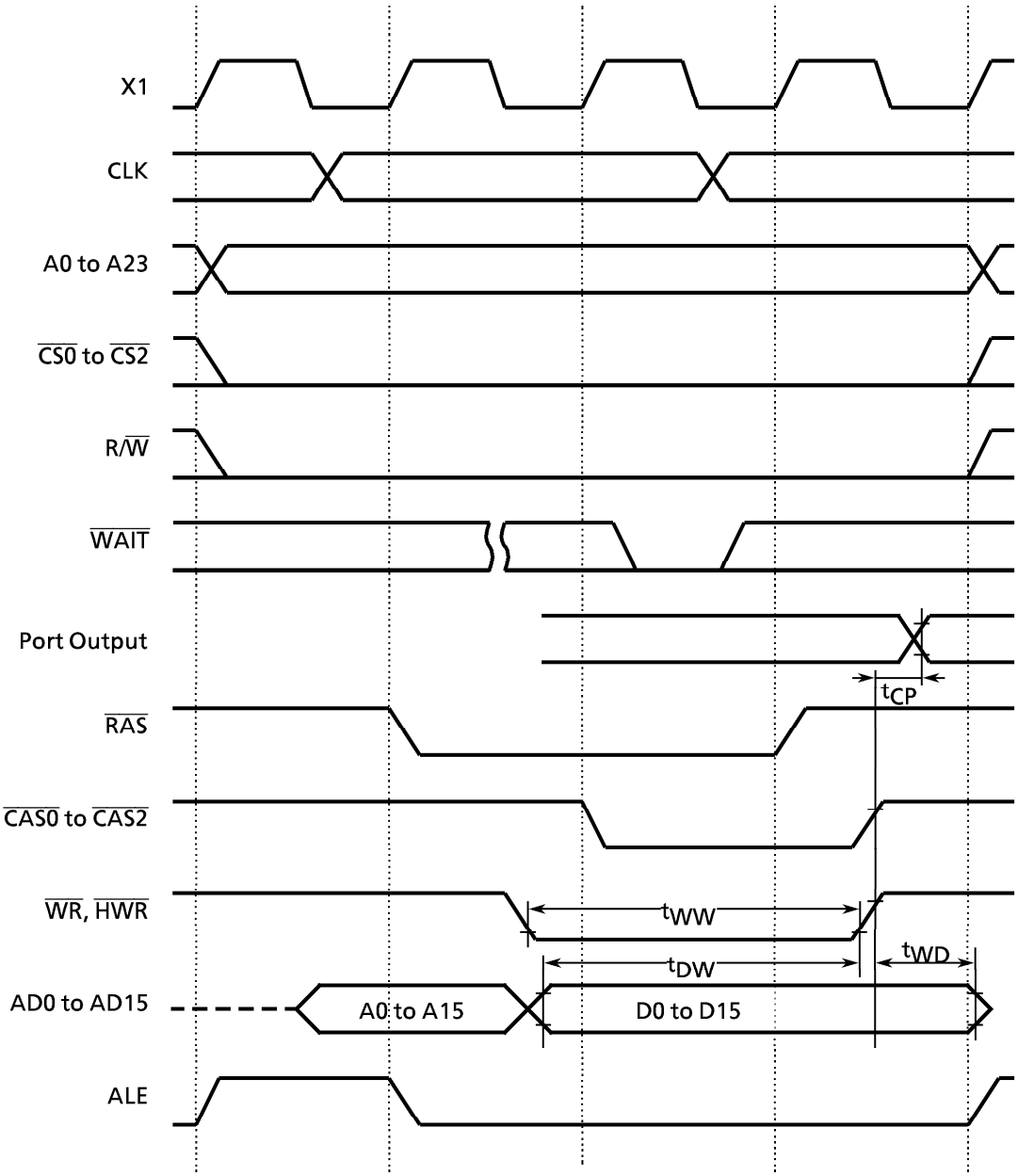
AC Measuring Conditions

- Output Level: High 0.7 × V_{CC} / Low 0.3 × V_{CC}, CL = 50 pF
- Input Level: High 0.9 × V_{CC} / Low 0.1 × V_{CC}

(1) Read Cycle


X1
CLK
A0 to A23
CS0 to CS2
R/W
WAIT
Port Input
RAS
CAS0 to CAS2
RD
AD0 to AD15
ALE
tOSC
tCLK
tAK
tKA
tAWH
tAWL
tCW
tAPH
tAPH2
tASRH
tASRL
tRSH
tRAS
tRAC
tRAH
tRCD
tCAS
tCAC
tRSC
tRP
tADH
tACH
tACL
tLC
tRR
tRD
tADL
tCA
tRAE
tHR
A0 to A15
D0 to D15
tAL
tLA
tLL
tCL

(2) Write Cycle



4.4 AD Conversion Characteristics

$AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$

Parameter	Symbol	Min	Typ.	Max	Unit
Analog Reference Voltage (+)	V_{REFH}	V_{CC} – 0.2 V	V_{CC}	V_{CC}	V
Analog Reference Voltage (–)	V_{REFL}	V_{SS}	V_{SS}	V_{SS} + 0.2 V	V
Analog Input Voltage Range	V_{AIN}	V_{REFL}		V_{REFH}	V
Analog Current for Analog Reference Voltage V_{CC} = 5 V ± 10% <VREFON> = 1	I_{REF} (V_{REFL} = 0 V)		0.5	1.5	mA
V_{CC} = 5 V ± 10% <VREFON> = 0			0.02	5.0	μA
Error (not including quantizing errors)	–		± 3.0	± 6	LSB

Note 1: $1LSB = (V_{REFH} - V_{REFL}) / 2^{10}$ [V]
Note 2: The operation above is guaranteed for $f_{FPH} \geqq 4$ MHz.
Note 3: The value I_{CC} includes the current which flows through the AVCC pin.
Note 4: The operation of this AD converter is guaranteed at 5 V ± 10%.

4.5 Serial Channel Timing

(1) I/O Interface Mode

① SCLK Input Mode

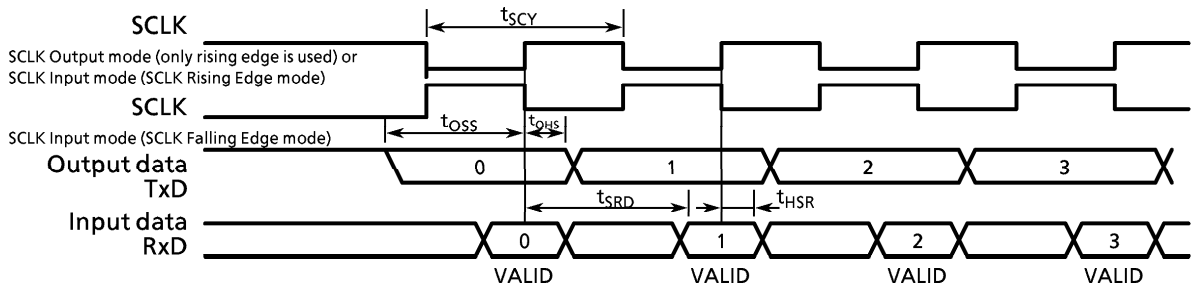
Parameter	Symbol	Variable		32.768 kHz (Note)		10 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
SCLK Cycle	t_{SCY}	16X		488		1.6		0.8		μs
Output Data → Rising Edge or Falling Edge* of SCLK	t_{OSS}	t_{SCY}/2 – 5X – 50		91.5 μs		250		100		ns
SCLK Rising Edge or Falling Edge* → Output Data Hold	t_{OHS}	5X – 100		152 μs		400		150		ns
SCLK Rising Edge or Falling Edge* → Input Data Hold	t_{HSR}	0		0		0		0		ns
SCLK Rising Edge or Falling Edge* → Effective Data Input	t_{SRD}		t_{SCY} – 5X – 100		336 μs		1000		450	ns

Note: System clock is fs, or input clock to prescaler is divisor clock of fs.
*) The rising edge is used in SCLK Rising mode.
The falling edge is used SCLK Falling mode.

② SCLK Output Mode

Parameter	Symbol	Variable		32.768 kHz (Note)		10 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
SCLK Cycle (Programmable)	t_{SCY}	16X	8192X	488 μs	250 ms	1.6	819.2	0.8	409.6	μs
Output Data → SCLK Rising Edge	t_{OSS}	t_{SCY} – 2X – 150		427 μs		1250		550		ns
SCLK Rising Edge → Output Data Hold	t_{OHS}	2X – 80		60 μs		120		20		ns
SCLK Rising Edge → Input Data Hold	t_{HSR}	0		0		0		0		ns
SCLK Rising Edge → Effective Data Input	t_{SRD}		t_{SCY} – 2X – 150		428 μs		1250		550	ns

Note: System clock is fs, or input clock to prescaler is divisor clock of fs.



4.6 Timer / Counter Input Clock (TI0, TI4, TI5, TI6, TI7)

Parameter	Symbol	Variable		10 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock Cycle	t_{VCK}	8X + 100		900		500		ns
Low Level Clock Pulse Width	t_{VCKL}	4X + 40		440		240		ns
High Level Clock Pulse Width	t_{VCKH}	4X + 40		440		240		ns

4.7 Interrupt and Capture

(1) $\overline{NMI}$, INT0 interrupts

Parameter	Symbol	Variable		10 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{NMI}$, INT0 Low Level Pulse Width	t_{INTAL}	4X		400		200		ns
$\overline{NMI}$, INT0 High Level Pulse Width	t_{INTAH}	4X		400		200		ns

(2) INT4 to 7 interrupts, capture

The INT4 to 7 input pulse width depends on the CPU operation clock and timer (9-bit prescaler). The following shows the pulse width for each clock.

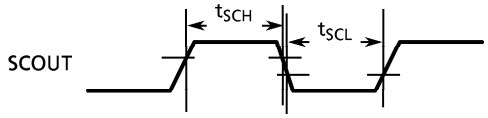
System clock selected <SYSCK>	Prescaler clock selected <PRCK1 to 0>	t_{INTBL} (INT4 to 7 low-level pulse width)		t_{INTBH} (INT4 to 7 high-level pulse width)		Unit
		Variable	20 MHz	Variable	20 MHz	
		Min	Min	Min	Min	
0 (fc)	00 (f_{FPH})	8X + 100	500	8X + 100	500	ns
	01 (fs)	8XT + 0.1	244.3	8XT + 0.1	244.3	μs
	10 (fc/16)	128X + 0.1	6.5	128X + 0.1	6.5	
1 (fs) (Note 2)	00 (f_{FPH})	8XT + 0.1	244.3	8XT + 0.1	244.3	
	01 (fs)					

Note 1: XT represents the frequency of the low-frequency clock fs. It is calculated at fs = 32.768 kHz.
Note 2: When using fs as the system clock, fc/16 cannot be selected as the prescaler clock.

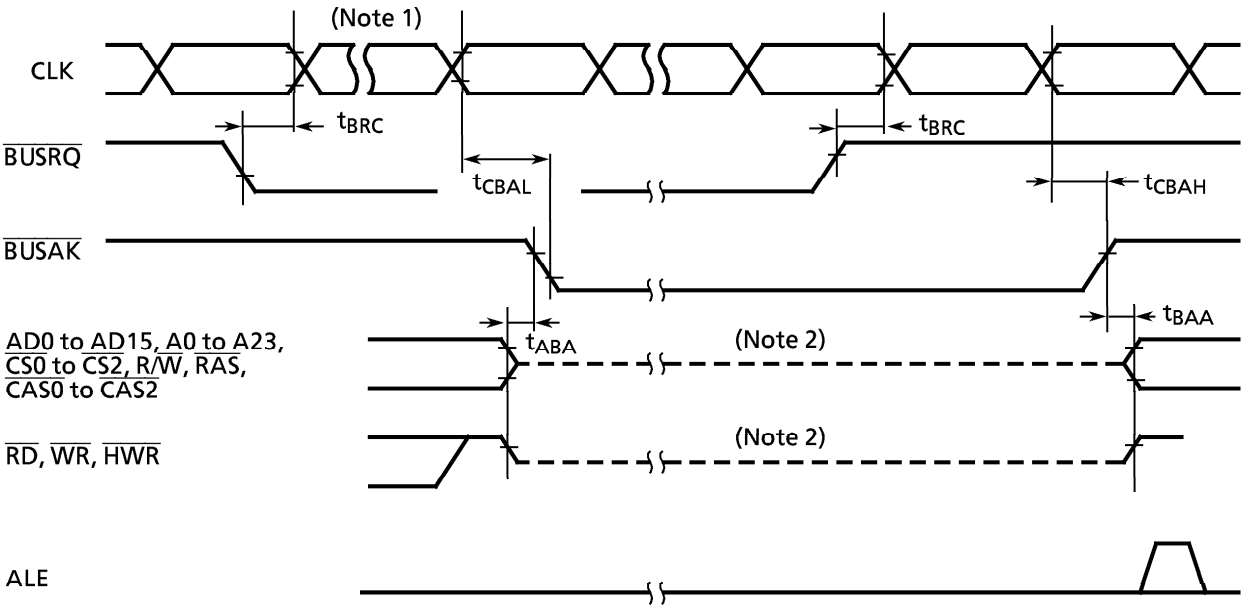
4.8 SCOUT pin AC characteristics

Parameter	Symbol	Variable		10 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
High-Level Pulse Width V_{CC} = 5 V ± 10%	t_{SCH}	0.5X – 10		40		15		ns
High-Level Pulse Width V_{CC} = 3 V ± 10%		0.5X – 20		30		–	–	
Low-Level Pulse Width V_{CC} = 5 V ± 10%	t_{SCL}	0.5X – 10		40		15		ns
Low-Level Pulse Width V_{CC} = 3 V ± 10%		0.5X – 20		30		–	–	

Measurement condition
- Output level: High 2.2 V / Low 0.8 V, CL = 10 pF



4.9 Timing Chart for Bus Request ($\overline{BUSRQ}$) / Bus Acknowledge ($\overline{BUSAK}$)



Parameter	Symbol	Variable		10 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{BUSRQ}$ Set-up Time to CLK	t_{BRC}	120		120		120		ns
CLK→ $\overline{BUSAK}$ Falling Edge	t_{CBAL}		1.5X + 120		270		195	ns
CLK→ $\overline{BUSAK}$ Rising Edge	t_{CBAH}		0.5X + 40		90		65	ns
Output Buffer off to $\overline{BUSAK}$ ↓	t_{ABA}	0	80	0	80	0	80	ns
$\overline{BUSAK}$ ↑ to Output Buffer on	t_{BAA}	0	80	0	80	0	80	ns

Note 1: Even if the $\overline{BUSRQ}$ signal goes low, the bus will not be released while the $\overline{WAIT}$ signal is low. The bus will only be released when $\overline{BUSRQ}$ goes low while $\overline{WAIT}$ is high.

Note 2: This line shows only that the output buffer is in the off state.
It does not indicate that the signal level is fixed.
Just after the bus is released, the signal level set before the bus was released is maintained dynamically by the external capacitance. Therefore, to fix the signal level using an external resistor during bus release, careful design is necessary, as fixing of the level is delayed.
The internal programmable pull-up / pull-down resistor is switched between the active and non-active states by the internal signal.

4.10 Recommended Oscillator

The TMP93CM40 is evaluated with various resonators. The evaluation results are displayed below to enable appropriate selection for any given application.

Note: The load capacitance of the resonator consists of the load capacitors C1 and C2 which are to be connected, and the floating capacitance of the target board.
Even if the specified values of C1 and C2 are used, there is a possibility that the oscillator will malfunction due to varying load capacitance on the target boards. Hence the oscillator's wiring patterns on the board should be designed to be as short as possible.
It is recommended that evaluation of the resonators be conducted on the target board.

(1) Examples of Resonator Connection

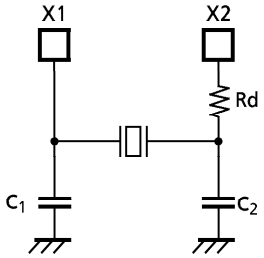


Figure 1: Example of High Frequency Resonator Connection

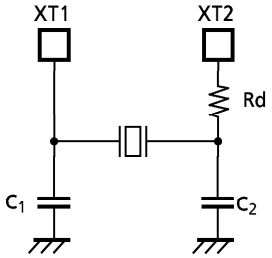


Figure 2: Example of Low Frequency Resonator Connection

(2) Ceramic resonator: Toyama Murata Mfg. Co., Ltd (Note 1)

Ta = – 20 to 80°C

Parameter	Frequency (MHz)	Recommended resonator	Recommended value			Vcc [V]
			C_1 [pF]	C_2 [pF]	Rd [kΩ]	
High-frequency oscillation	4.00	CSA4.00MGU	30	30	0	2.7 to 5.5
		CST4.00MGWU	(30) (Note 2)	(30) (Note 2)		
	10.00	CSA10.0MTZ093	30	30		
		CST10.0MTW093	(30) (Note 2)	(30) (Note 2)		
	16.00	CSA16.00MXZ040	5	5		4.5 to 5.5
	20.00	CSA20.00MXZ040	3	3		

Note 1: TOYAMA MURATA MFG. CO., LTD. (JAPAN)
These product numbers and the corresponding specifications are subject to change. For up-to-date information, please refer to the following URL;
http://www.murata.co.jp/search/index.html

Note 2: For built-in condenser type