TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/L1 Series

TMP91PW10

TOSHIBA CORPORATION

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, “Points of Note and Restrictions”.
Especially, take care below cautions.

****CAUTION****
How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 5 clocks of f_{FPH}) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

Low-Voltage CMOS 16-Bit Microcontroller

TMP91PW10F

1. Outline and Device Characteristics

The TMP91PW10 is an OTP-type MCU which includes a 128-K one-time programmable ROM. Data for TMP91PW10 can be written and verified using the adapter socket. The TMP91PW10 has the same pin-assignment as the TMP91CU10 (mask ROM-type).

A program can be written to the TMP91PW10's built-in PROM in the same way as on the TMP91CU10.

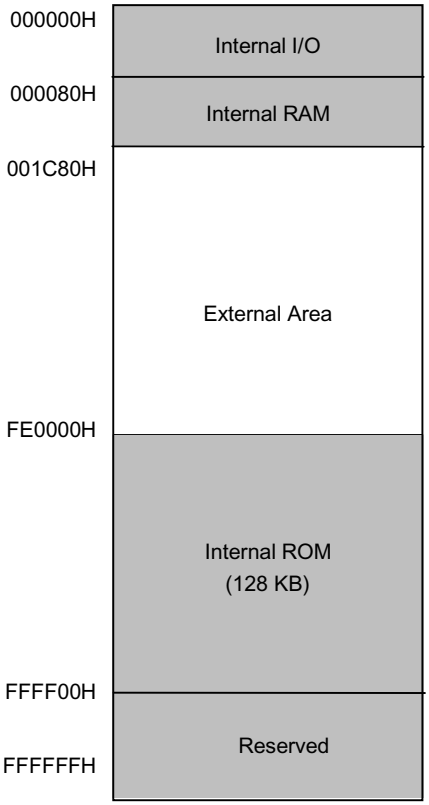
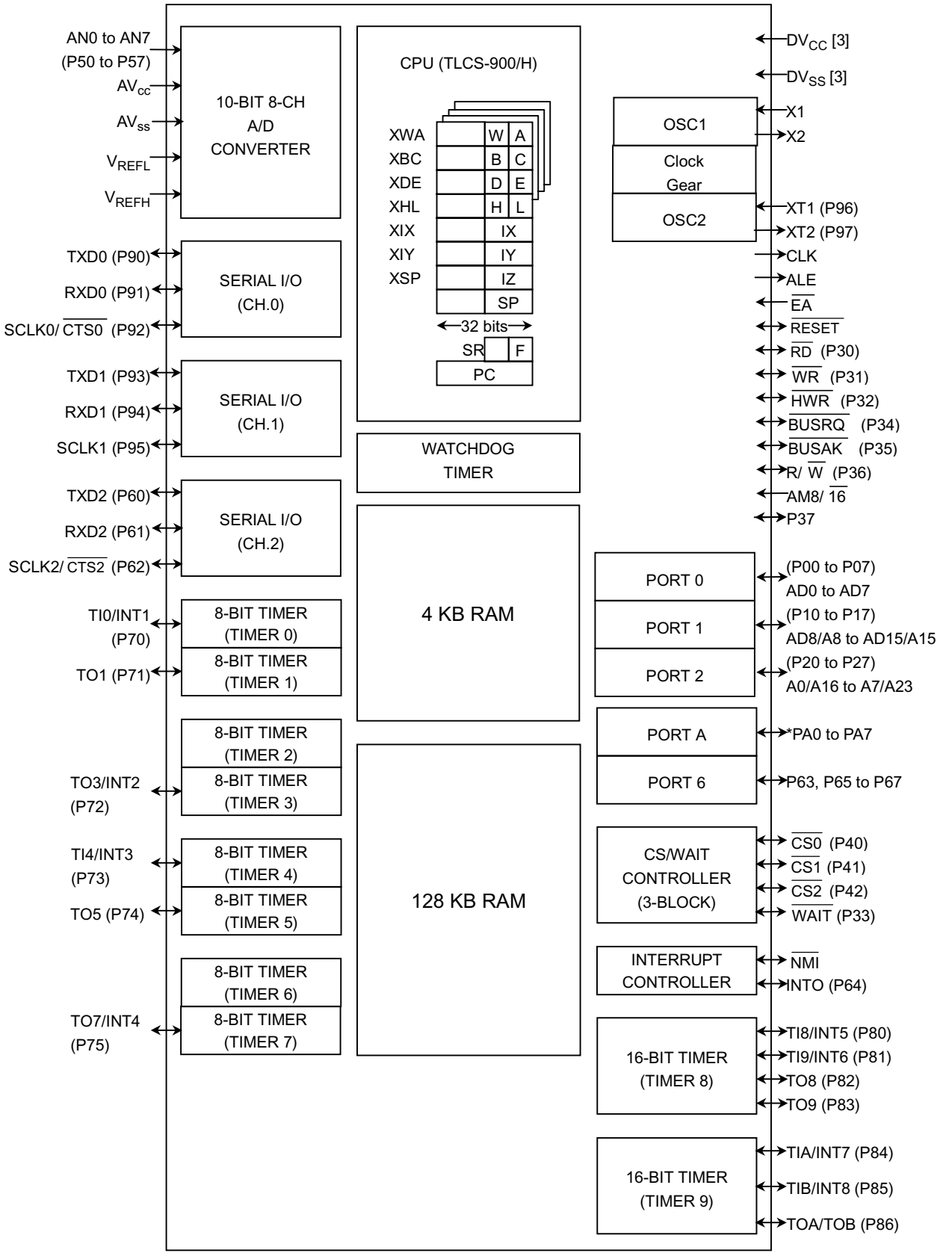


Figure 2.1.1 Memory map of TMP91PW1

MCU	ROM	RAM	Package	Adapter Socket
TMP91PW10F	128-Kbyte OTP	4 Kbytes	QFP100	BM11129

000707EBP1



( ) : Default function after reset

Figure 2.1.2 TMP91PW10 Block Diagram

2. Pin Assignment and Functions

The assignment of input and output pins for the TMP91PW10, their names and functions are described as follows:

2.1 Pin Assignment

Figure 2.1.1 shows the pin assignment of the TMP91PW10.

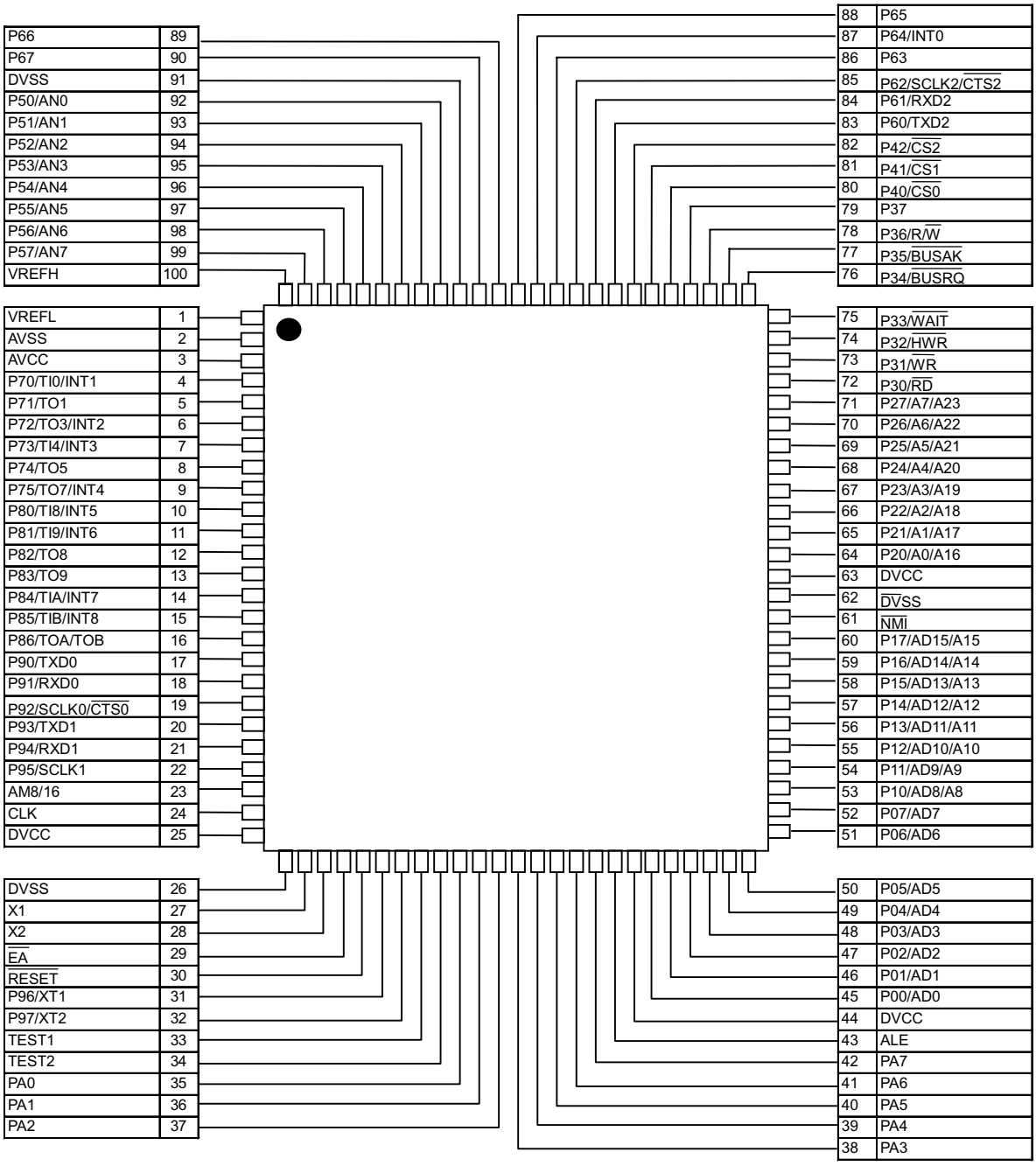


Figure 2.1.1 Pin Assignment diagram

2.2 Pin Names and Functions

The names of the input/output pins and their functions are described in Table 2.2.1.

Table 2.2.1 Pin names and Functions (1/3)

Pin name	Number of pins	I/O	Functions
P00 to P07 AD0 to AD7	8	I/O I/O	Port 0: I/O port that allows I/O to be selected at the bit level Address (lower): Bits 0 to 7 for address and data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O I/O Output	Port 1: I/O port that allows I/O to be selected at the bit level Address and data (upper): Bits 8 to 15 for address and data bus Address: Bits 8 to 15 for address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows I/O to be selected at the bit level (with pull-up resistor) Address: Bits 0 to 7 for address bus Address: Bits 16 to 23 for address bus
P30 $\overline{RD}$	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory When P3<RDE> = 0 and P3FC<P30F> = 1, $\overline{RD}$ is output and internal memory is read.
P31 $\overline{WR}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data to pins D0 to 7
P32 HWR	1	I/O Output	Port 32: I/O port (with pull-up resistor) High Write: Strobe signal for writing data to pins D8 to 15
P33 WAIT	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU Bus Wait
P34 $\overline{BUSRQ}$	1	I/O Input	Port 34: I/O port (with pull-up resistor) Bus Request: Signal used to request high impedance on pins D0 to 15, A0 to 23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, $\overline{CS0}$, $\overline{CS1}$ and $\overline{CS2}$.
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus Acknowledge: Signal used to acknowledge high impedance on pins D0 to 15, A0 to 23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, $\overline{CS0}$, $\overline{CS1}$ and $\overline{CS2}$ by receiving $\overline{BUSRQ}$.
P36 R/$\overline{W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/Write: 1 represents Read or Dummy cycle; 0 represents Write cycle.
P37	1	I/O	Port 37: I/O port
P40 $\overline{CS0}$	1	I/O Output	Port 40: I/O port (with pull-up resistor) Chip Select 0: Outputs 0 when address is within specified address area.
P41 $\overline{CS1}$	1	I/O Output	Port 41: I/O port (with pull-up resistor) Chip Select 1: Outputs 0 when address is within specified address area.
P42 $\overline{CS2}$	1	I/O Output	Port 42: I/O port (with pull-down resistor) Chip Select 2: Outputs 0 when address is within specified address area.
P50 to P57 AN0 to AN7	8	Input Input	Port 5: Input port Analog input: Pin used to input to AD converter
P60 TXD2	1	I/O Output	Port 60: I/O port (level shift pin) Serial Send Data 2
P61 RXD2	1	I/O Input	Port 61: I/O port (level shift pin) Serial Receive Data 2
P62 SCLK2 $\overline{CTS2}$	1	I/O I/O Input	Port 62: I/O port (level shift pin) Serial Clock I/O 2 Serial Data Send Enable 2 (Clear to Send)
P63	1	I/O	Port 63: I/O port
P64 INT0	1	I/O Input	Port 64: I/O port Interrupt Request pin 0: Interrupt triggered on either level or rising edge (programmable)
P65 to P67	3	I/O	Port 65 to 67: I/O ports

Note: A DMAC controller's internal memory or I/O devices cannot be accessed using $\overline{BUSRQ}$ and $\overline{BUSAK}$.

Table 2.2.1 Pin names and Functions (2/3)

Pin name	Number of pins	I/O	Functions
P70	1	I/O	Port 70: I/O port
TI0		Input	Timer Input 0: Timer 0 input pin
INT1		Input	Interrupt Request pin 1: Interrupt request on rising edge
P71	1	I/O	Port 71: I/O port
TO1		Output	Timer Output 1: Timer 0 or 1 output
P72	1	I/O	Port 72: I/O port
TO3		Output	Timer Output 3: Timer 2 or 3 output
INT2		Input	Interrupt Request pin 2: Interrupt request on rising edge
P73	1	I/O	Port 74: I/O port
TI4		Input	Timer Input 4: Timer 4 input
INT3		Input	Interrupt Request pin 3: Interrupt request on rising edge
P74	1	I/O	Port 75: I/O port
TO5		Output	Timer Output 5: Timer 4 or 5 output
P75	1	I/O	Port 76: I/O port
TO7		Output	Timer Output 7: Timer 6 or 7 output
INT4		Input	Interrupt Request pin 4: Interrupt request on rising edge
P80	1	I/O	Port 80: I/O port
TI8		Input	Timer Input 8: Timer 8 count or capture trigger signal input
INT5		Input	Interrupt Request pin 5: Interrupt request on programmable rising / falling edge
P81	1	I/O	Port 81: I/O port
TI9		Input	Timer Input 9: Timer 8 count or capture trigger signal input
INT6		Input	Interrupt Request pin 6: Interrupt request on rising edge
P82	1	I/O	Port 82: I/O port
TO8		Output	Timer Output 8: Timer 8 output pin
P83	1	I/O	Port 83: I/O port
TO9		Output	Timer Output 9: Timer 9 output pin
P84	1	I/O	Port 84: I/O port
TIA		Input	Timer Input A: Timer 9 count or capture trigger signal input
INT7		Input	Interrupt Request pin 7: Interrupt request on programmable rising / falling edge
P85	1	I/O	Port 85: I/O port
TIB		Input	Timer Input B: Timer 9 count or capture trigger signal input
INT8		Input	Interrupt Request pin 8: Interrupt request on rising edge
P86	1	I/O	Port 86: I/O port
TOA		Output	Timer Output A: Timer A output pin
TOB		Output	Timer Output B: Timer B output pin
P90	1	I/O	Port 90: I/O port
TXD0		Output	Serial Send Data 0
P91	1	I/O	Port 91: I/O port
RXD0		Input	Serial Receive Data 0
P92	1	I/O	Port 92: I/O port
SCLK0		I/O	Serial Clock I/O 0
$\overline{CTS0}$		Input	Serial Data Send Enable 0 (Clear to Send)
P93	1	I/O	Port 93: I/O port
TXD1		Output	Serial Send Data 1
P94	1	I/O	Port 94: I/O port
RXD1		Input	Serial Receive Data 1
P95	1	I/O	Port 95: I/O port
SCLK1		I/O	Serial Clock I/O 1
P96	1	I/O	Port 96: I/O port (open drain output)
XT1		Input	Low-frequency oscillator connecting pin
P97	1	I/O	Port 97: I/O port (open drain output)
XT2		Output	Low-frequency oscillator connecting pin

Table 2.2.1 Pin names and Functions (3/3)

Pin name	Number of pins	I/O	Functions
PA0 to PA7	3	I/O	Port A0 to A7: I/O ports (Level Shift port)
ALE	1	Output	Address Latch Enable (can be disabled for reducing noise.)
$\overline{NMI}$	1	Input	Non-Maskable Interrupt Request pin: Interrupt request pin with programmable falling edge or both edges.
CLK	1	Output	Clock Output: Outputs (external input clock / 4) clock. Pulled up during reset
$\overline{EA}$	1	Input	The Vcc pin should be connected.
AM8/$\overline{16}$	1	Input	Address Mode: Selects external data bus width. The Vcc pin should be connected. The data bus width for external access is set by the Chip Select / WAIT Control register and the Port 1 Control register.
$\overline{RESET}$	1	Input	Reset: Initializes LSI. (With pull-up resistor)
VREFH	1	Input	Reference power supply input pin for AD converter (H)
VREFL	1	Input	Reference power supply input pin for AD converter (L)
AVCC	1		Power supply pin for AD converter
AVSS	1		GND power supply pin for AD converter (0 V)
X1/X2	2	I/O	Oscillator connecting pin
TEST1/TEST2	2	Output /Input	TEST1 should be connected with TEST2 pin.
DVCC	3		Power supply pin
DVSS	3		GND pin (0 V)

Note: All pins that have built-in pull-up/pull-down resistors (other than the RESET pin) can be disconnected from their built-in pull-up/pull-down resistors by software.

(1) PROM mode

Pin Function	Pin Number	Input/Output	Function	Pin Name (MCU mode)
A7 to A0	8	Input	Memory address of program	P27 to P20
A15 to A8	8	Input		P17 to P10
A16	1	Input		P33
D7 to D0	8	I/O	Memory data of program	P07 to P00
CE	1	Input	Chip enable	P32
OE	1	Input	Output control	P30
$\overline{PGM}$	1	Input	Program control	P31
VPP	1	Power supply	12.75 V/5 V (Power supply used for programming)	$\overline{EA}$
VCC	4	Power supply	6.25 V/5 V	VCC, AVCC
VSS	4	Power supply	0 V	VSS, AVSS

Pin Function	Pin Number	Input/Output	Pin setting
P34	1	Input	Fix to Low level (security pin)
$\overline{RESET}$	1	Input	Fix to Low level (PROM mode)
CLK	1	Input	
ALE	1	Output	Open
X1	1	Input	Crystal
X2	1	Output	
P42 to P40 P37 to P35 AM8/16	7	Input	Fix to High level
TEST1/TEST2	2	Input/Output	Short
P57 to P50 P67 to P60 P73 to P70 P87 to P80 P97 to P90 PA7 to PA0 VREFH VREFL $\overline{NMI}$ WDTOUT	48	I/O	Open

3. Operation

This section describes the functions and basic operations of the TMP91PW10.

The TMP91PW10 has a PROM instead of the mask ROM which of the TMP91CU10. All other configuration details and functions are the same as for the TMP91CU10.

For information of functions of the TMP91PW10 which are not described here, see the TMP91CU10.

The TMP91PW10 has two operational modes: MCU mode and PROM mode.

3.1 MCU mode

(1) Mode setting and functions

Setting the CLK pin to open selects MCU Mode. In MCU mode, operation is same as for the TMP91CU10.

3.2 Memory Map

Figure 3.2.1, Figure 3.2.2 are memory maps of theTMP91PW10.

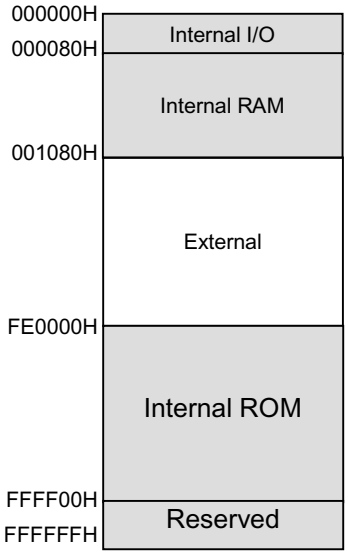


Figure 3.2.1 Memory map for MCU mode

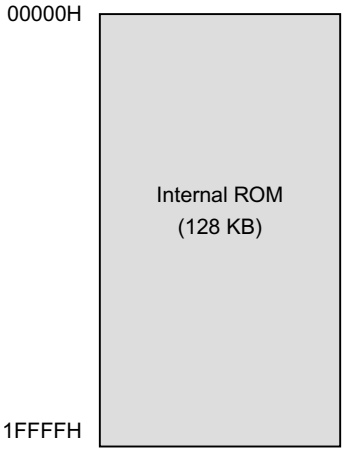


Figure 3.2.2 Memory map for PROM mode,

3.3 PROM Mode

(1) Mode setting and functions

PROM mode is set by setting the RESET and CLK pins to L. Programming and verification of the internal PROM is carried out using a general PROM programmer with an adapter socket.

(1) OTP adaptor

BM11129: TMP93PS40DF, TMP93PW40DF, TMP91PW10F adapters

(2) Setting OTP adapter

Set the switch (SW1) to N side.

4. Electrical Characteristics

X used in an expression shows a frequency for the clock (f_{FPH}) as selected by SYSCR1<SYSCK>. The value of X changes according to whether a clock gear or a low-speed oscillator is selected. An example value of fc, is calculated with gear = 1/fc (SYSCR1<SYSCK, GEAR 2 to 0> = 0000).

4.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	−0.5 to 6.5	V
Input Voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
Output Current (total)	Σ_{IOL}	120	mA
Output Current (total)	Σ_{IOH}	−80	mA
Power Dissipation (T_a = 8°C)	P_D	600	mW
Soldering Temperature (10 s)	T_{SOLDER}	260	°C
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_{OPR}	−40 to 85	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics

Parameter		Symbol	Condition	Min	Typ. (Note 1)	Max	Unit
Power Supply Voltage $AV_{CC} = V_{CC}$ $AV_{SS} = V_{SS} = 0$ V		V_{CC}	f_c = 4 to 13.5 MHz f_s = 30 to 34 kHz (Ta = −40 to 85°C)	2.7		3.6	V
Input High Voltage	AD0 to AD15	V_{IL}	$V_{CC} \geq 2.7$ V	−0.3		0.8	V
	Port 2 to A (except P87, P5)	$V_{IL}1$	V_{CC} = 2.7 to 3.6 V			0.3 V_{CC}	
	$\overline{RESET}$, $\overline{NMI}$, INT0	$V_{IL}2$				0.25 V_{CC}	
	EA, AM8/$\overline{16}$	$V_{IL}3$				0.3	
	X1, Port 5	$V_{IL}4$				0.2 V_{CC}	
Input High Voltage	AD0 to AD15	V_{IH}	$V_{CC} \geq 2.7$ V	2.2		V_{CC} + 0.3	
	Port 2 to A (except P87)	$V_{IH}1$	V_{CC} = 2.7 to 3.6 V	0.7 V_{CC}			
	$\overline{RESET}$, $\overline{NMI}$, INT0	$V_{IH}2$		0.75 V_{CC}			
	EA, AM8/$\overline{16}$	$V_{IH}3$		V_{CC} − 0.3			
	X1	$V_{IH}4$		0.8 V_{CC}			
Output Low Voltage		V_{OL}	I_{OL} = 1.6 mA (V_{CC} = 2.7 to 3.6 V)			0.45	V
Darlington Drive Current (8 output pins max)		I_{DAR} (Note2)	V_{EXT} = 1.5 V R_{EXT} = 1.1 kΩ (V_{CC} = 3 V ± 10%)	−1.0		−3.5	mA
Input Leakage Current		I_{LI}	0.0 ≤ V_{IN} ≤ V_{CC}		0.02	±5	mA
Output Leakage Current		I_{LO}	0.2 ≤ V_{IN} ≤ V_{CC} − 0.2		0.05	±10	

Note 1: Typical values are for T_a = 25°C and V_{CC} = 5 V unless otherwise noted.

Note 2: I-DAR is guranteed for total of up to 8 ports.

Parameter	Symbol	Condition		Min	Typ. (Note 1)	Max	Unit
Power-down Voltage (@STOP, RAM backup)	V_{STOP}	$V_{IL}2 = 0.2\ V_{CC}$, $V_{IH}2 = 0.8\ V_{CC}$		2.0		6.0	V
RESET Pull-up Resistor	R_{RST}	V_{CC} = 3 V ± 10%		30		250	kΩ
Pin Capacitance	C_{IO}	fc = 1 MHz				10	pF
Schmitt Width $\overline{RESET}$, $\overline{NMI}$, INT0	V_{TH}			0.4	1.0		V
Programmable Pull-down Resistor	PKL	V_{CC} = 3 V ± 10%		30		200	kΩ
Programmable Pull-up Resistor	PKH	V_{CC} = 3 V ± 10%		80		300	kΩ
NORMAL (Note2)	I_{CC}	V_{cc} = 3 V ± 10% fc = 12.5 MHz (Typ.: V_{CC} = 3.0 V)			13	20	mA
RUN					8.6	14	
IDLE2					5.5	9.5	
IDLE1					0.95	2.5	
SLOW (Note2)		V_{CC} =3 V ± 10% fs = 32.768 kHz (Typ.: v = 3.0 V)			40	55	mA
RUN					32	45	
IDLE2					18	35	
IDLE1					6	20	
STOP		Ta ≤ 50°C	V_{CC} = 2.0 to 3.6 V		0.2	10	mA
		Ta ≤ 70°C				20	
		Ta ≤ 85°C				50	

Note 1: Typical values are for T_a = 25°C and V_{CC} = 3 V unless otherwise noted.

Note 2: ICC measurement condition (NORMAL):
All functions are operational: Output pins are open and input pins are fixed.

4.3 AC Characteristics

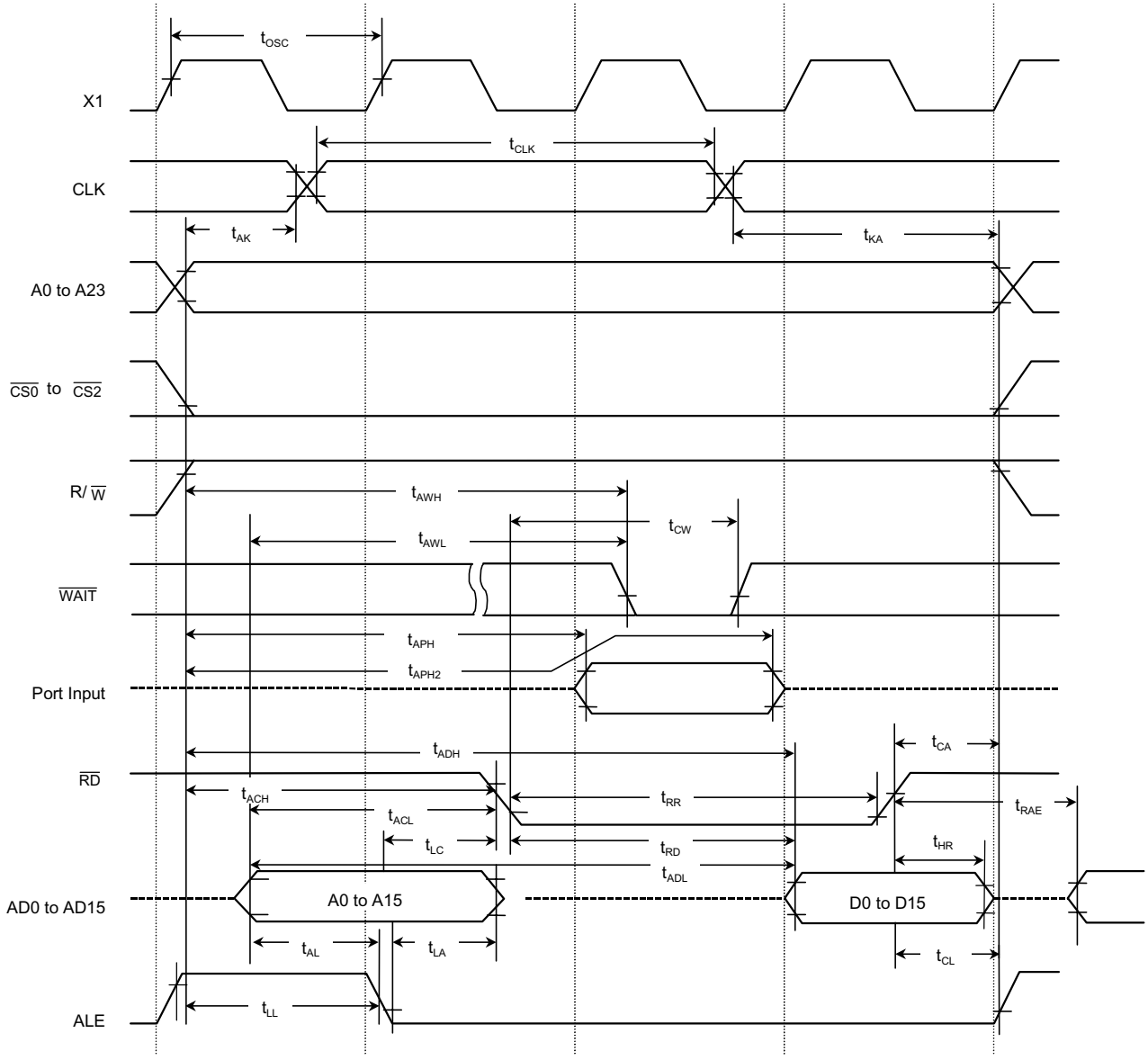
(1) V_{CC} = 3.0 V ± 10% V

No.	Parameter	Symbol	Value		13.5 MHz		Unit
			Min	Max	Min	Max	
1	Osc. Period (=x)	t_{OSC}	72	31250	74		ns
2	CLK Width	t_{CLK}	2x – 40		108		ns
3	A0 to A23 Valid → CLK Hold	t_{AK}	0.5x – 30		7		ns
4	CLK Valid → A0 to A23 Hold	t_{KA}	1.5x – 85		26		ns
5	A0 to A15 Valid → ALE Fall	t_{AL}	0.5x – 34		30		ns
6	ALE Fall → A0 to A15 Hold	t_{LA}	0.5x – 30		7		ns
7	ALE High Width	t_{LL}	x – 50		24		ns
8	ALE Fall → $\overline{RD}$ / $\overline{WR}$ Fall	t_{LC}	0.5x – 27		10		ns
9	$\overline{RD}$ / $\overline{WR}$ Rise → ALE Rise	t_{CL}	0.5x – 30		7		ns
10	A0 to A15 Valid → $\overline{RD}$ / $\overline{WR}$ Fall	t_{ACL}	x – 40		34		ns
11	A0 to A23 Valid → $\overline{RD}$ / $\overline{WR}$ Fall	t_{ACH}	1.5x – 50		61		ns
12	$\overline{RD}$ / $\overline{WR}$ Rise → A0 to A23 Hold	t_{CA}	0.5x – 37		0		ns
13	A0 to A15 Valid → D0 to D15 Input	t_{ADL}		3.0x – 55		130	ns
14	A0 to A23 Valid → D0 to D15 Input	t_{ADH}		3.5x – 65		215	ns
15	$\overline{RD}$ Fall → D0 to D15 Input	t_{RD}		2.0x – 45		100	ns
16	$\overline{RD}$ -Low Pulse Width	t_{RR}	2.0x – 40		108		ns
17	$\overline{RD}$ Rise → D0 to D15 Hold	t_{HR}	0		0		ns
18	$\overline{RD}$ Rise → A0 to A15 Output	t_{RAE}	x – 20		54		ns
19	$\overline{WR}$ -Low Pulse Width	t_{WW}	2.0x – 40		108		ns
20	D0 to D15 Valid → $\overline{WR}$ Rise	t_{DW}	2.0x – 80		68		ns
21	$\overline{WR}$ Rise → D0 to D15 Hold	t_{WD}	0.5x – 32		5		ns
22	A0 to A23 Valid → $\overline{WAIT}$ Input (1 WAIT + n mode)	t_{AWH}		3.5x – 60		199	ns
23	A0 to A15 Valid → $\overline{WAIT}$ Input (1 WAIT + n mode)	t_{AWL}		3.0x – 60		162	ns
24	$\overline{RD}$ / $\overline{WR}$ Fall → $\overline{WAIT}$ Hold (1 WAIT + n mode)	t_{CW}	2.0x + 0		148		ns
25	A0 to A23 Valid → Port Input	t_{APH}		2.5x – 120		65	ns
26	A0 to A23 Valid → Port Hold	t_{APH2}	2.5x + 50		235		ns
27	A0 to A23 Valid → Port Valid	t_{AP}		3.5 × +100		359	ns

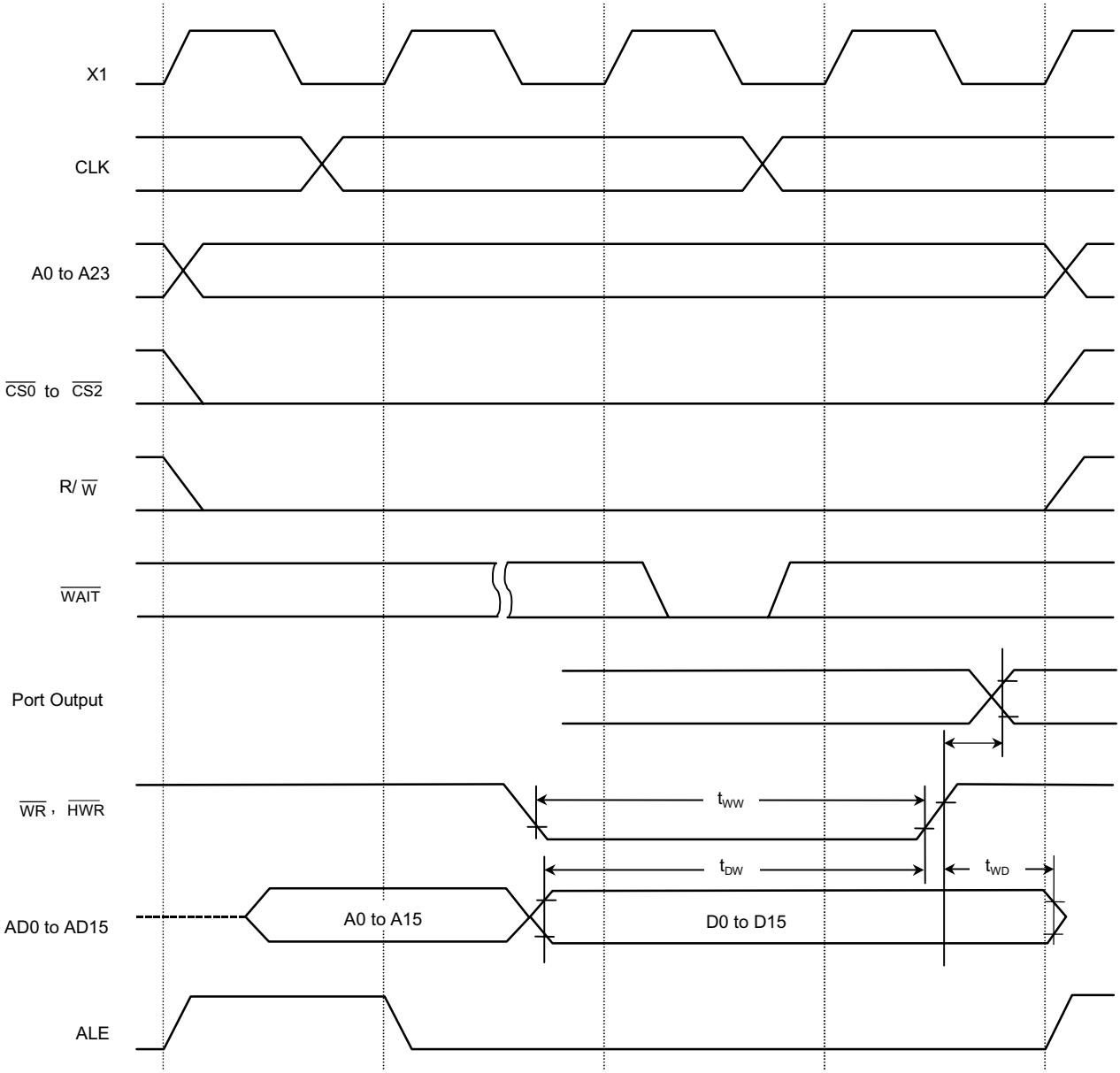
AC Measuring Conditions

- Output Level: High 2.2 V/Low 0.8 V, CL = 50 pF
  (However, CL = 100 pF for AD0 to AD15, A0 to A23, ALE $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, $\overline{CLK}$)
- Input Level: High 2.4 V/Low 0.45 V (AD0 to AD15)
  High 0.8Vcc/Low 0.2Vcc (except for AD0 to AD15)

(2) Read Cycle


X1
CLK
A0 to A23
CS0 to CS2
R/W
WAIT
Port Input
RD
AD0 to AD15
ALE
tOSC
tCLK
tAK
tKA
tAWH
tAWL
tCW
tAPH
tAPH2
tADH
tCA
tACH
tRR
tRAE
tACL
tLC
tRD
tHR
tADL
A0 to A15
D0 to D15
tAL
tLA
tCL
tLL

(3) Write Cycle



4.4 AD Conversion Characteristics

$AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$

Parameter	Symbol	Min	Typ.	Max	Unit
Analog Reference Voltage (+)	V_{refH}	$V_{CC} - 0.2$ V	V_{CC}	V_{CC}	V
Analog Reference Voltage (−)	V_{refL}	V_{SS}	V_{SS}	$V_{SS} + 0.2$ V	
Analog Input Voltage Range	V_{ain}	V_{refL}		V_{refH}	
Analog Current for Analog Reference Voltage $V_{CC} = 3$ V ± 10% <V_{ref}ON> = 1	I_{ref} (V_{refL} = 0 V)		0.5	1.5	mA
$V_{CC} = 3$ V ± 10% <V_{ref}ON> = 0			0.02	5.0	μA
Error (except for quantizing errors)	———		± 1	± 3	LSB

Note 1: LSB = $(V_{refH} - V_{refL})/2^{10}$ V

Note 2: The operation of the AD converter is guaranteed only when fc (the high frequency oscillator) is used (it is not guaranteed when f_s is used). It is guaranteed when $f_{FPH} \geq 4$ MHz

Note 3: The value I_{cc} includes the current which flows through the AV_{CC} pin.

4.5 Serial Channel Timing

(1) I/O Interface Mode

- SCLK Input Mode

Parameter	Symbol	Value		32.768 kHz [1]		13.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK Cycle	t_{SCY}	16x		488		1.18		ms
Output Data → Rising Edge or Falling Edge[2] of SCLK	t_{OSS}	t_{SCY}/2–5x–50		91.5		172		ns
SCLK Rising Edge or Falling Edge → Output Data Hold	t_{OHS}	5x–100		152		270		ns
SCLK Rising Edge or Falling Edge[2] → Input Data Hold	t_{HSR}	0		0		0		ns
SCLK Rising Edge or Falling Edge[2] → Effective Data input	t_{SRD}		t_{SCY}–5x–100		336		714	ns

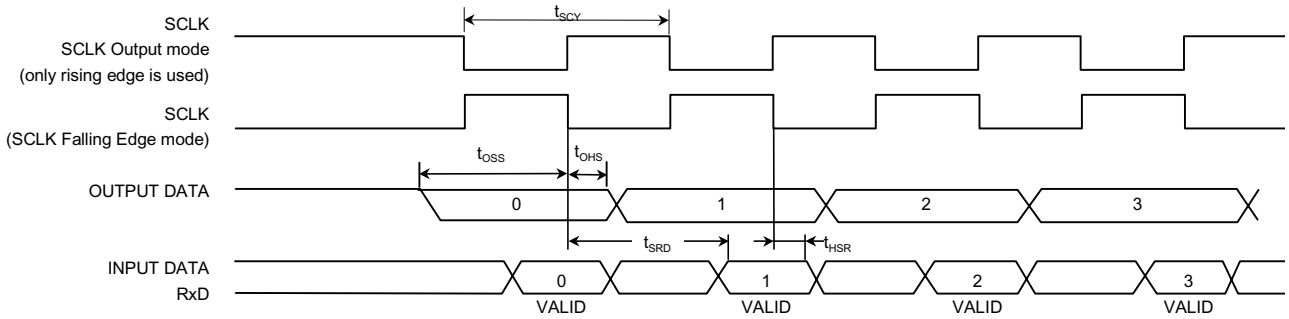
Note 1: System clock is fs or input clock to prescaler is divisor clock of fs.

Note 2: The rising edge is used in SCLK Rising mode. The falling edge is used SCLK Falling mode.

- SCLK Output Mode

Parameter	Symbol	Variable Frequency		32.768 kHz[1]		13.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK Cycle (Programmable)	t_{SCY}	16x	8192x	488	250	1.18	606.2	μs
Output Data→ SCLK Rising Edge	t_{OSS}	t_{SCY}–2x–150		427		886		ns
SCLK Rising Edge→ Output Data Hold	t_{OHS}	2x–80		60		68		ns
SCLK Rising Edge→ Input Data Hold	t_{HSR}	0		0		0		ns
SCLK Rising Edge→ Effective Data Input	t_{SRD}		t_{SCY}–2x–150		428		886	ns

Note 1: System clock is fs, or input clock to prescaler is divisor clock of fs.



4.6 Event Counter (TI0, TI4, TI8, TI9, TIA, TIB)

Parameter	Symbol	Variable Frequency		13.5 MHz		Unit
		Min	Max	Min	Max	
Clock Cycle	t_{VCK}	8X + 100		692		ns
Low Level Clock Pulse Width	t_{VCKL}	4X + 40		336		ns
High Level Clock Pulse Width	t_{VCKH}	4X + 40		336		ns

4.7 Interrupt and Capture

(1) NMI, INT0 interrupts

Parameter	Symbol	Variable Frequency		13.5 MHz		Unit
		Min	Max	Min	Max	
$\overline{NMI}$, INT0 to INT 4 Low Level Pulse Width	t_{INTAL}	4X		296		ns
$\overline{NMI}$, INT0 High Level Pulse Width	t_{INTAH}	4X		296		ns

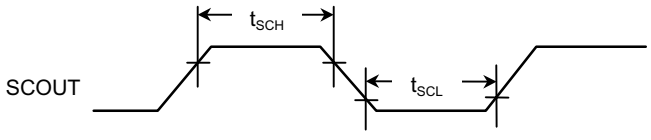
(2) INT5 to INT8 interrupts, capture

The INT5 to INT8 input pulse width depends on the CPU operation clock and the timer (9-bit prescaler). The following shows the pulse width for each clock.

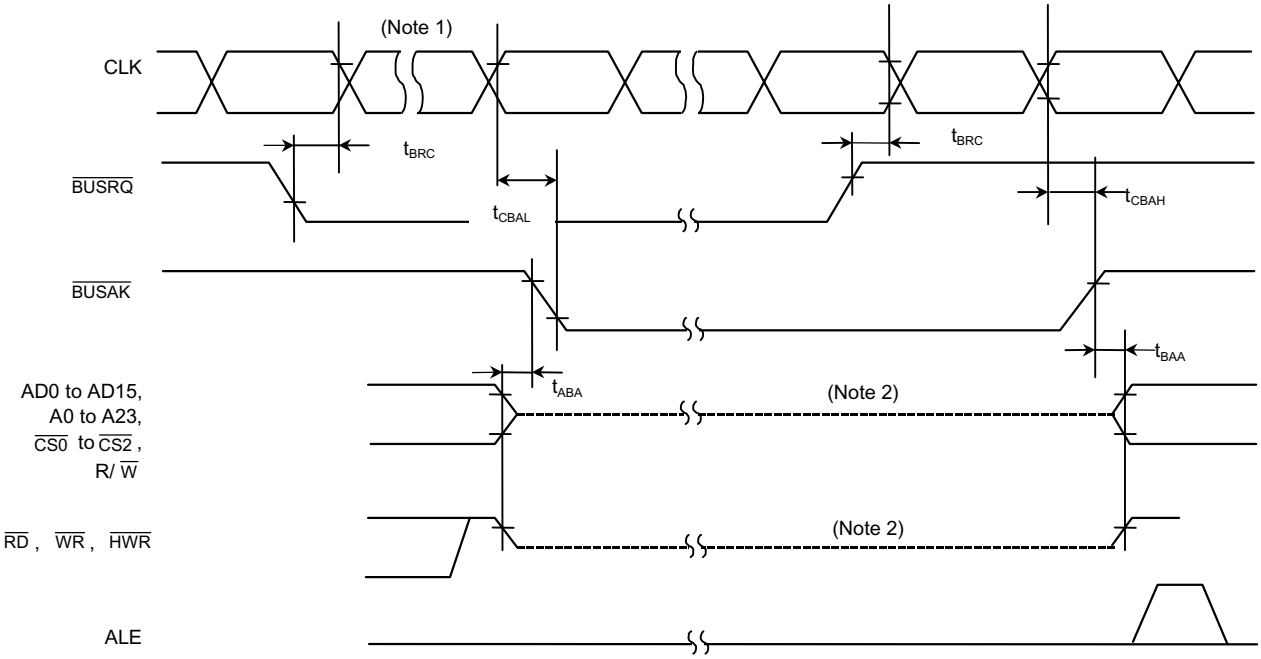
System clock selected <SYSCK>	Prescaler clock selected <PRCK1 to 0>	t_{INTBL} (INT5 to INT8 low level pulse width)		t_{INTBH} (INT5 to INT8 high level pulse width)		Unit
		Variable Frequency	13.5 MHz	Variable Frequency	13.5 MHz	
		Min	Min	Min	Min	
0 (fc)	00 (f_{FPH})	8X + 100	692	8X + 100	692	ns
	01 (fs)	8XT + 0.1	244.3	8XT + 0.1	244.3	μs
	10 (fc/16)	128X + 0.1	9.572	128X + 0.1	9.572	
1 (fs)Note	00 (f_{FPH})	8XT + 0.1	244.3	8XT + 0.1	244.3	
	01 (fs)					

Note1: XT shows cycle of low clock (fs).
A calculation value is (fs) = 32.768 [kHz]

Note2: When fs is used as the system clock, fc/16 cannot be selected as the prescaler clock.



4.8 Timing Chart for Bus Request / Bus Acknowledge



Parameter	Symbol	Value		13.5 MHz		Unit
		Min	Max	Min	Max	
$\overline{BUSRQ}$ Set-up Time to CLK	t_{BRC}	120		120		ns
CLK→$\overline{BUSAK}$ Falling Edge	t_{CBAL}		1.5x + 120		231	ns
CLK→$\overline{BUSAK}$ Rising Edge	t_{CBAH}		0.5x + 40		80	ns
$\overline{Output}$ Buffer off to BUSAK	t_{ABA}	0	80	0	77	ns
$\overline{BUSAK}$ to Output Buffer on	t_{BAA}	0	80	0	80	ns

Note 1: Even if the BUSRQ signal goes Low, the bus will not be released while the WAIT signal is Low. The bus will only be released when BUSRQ goes Low while WAIT is High.

Note 2: This line shows only that the output buffer is in the OFF state. Just after the bus is released, the signal level set before the bus was released is maintained dynamically by the external capacitance. Therefore, to fix the signal level using an external resistor during bus release, careful design is necessary, as fixing of the level is delayed.
The internal programmable pull-up/pull-down resistor is switched between the active and non-active states by the internal signal.

4.9 Read operation in PROM mode

DC/AC characteristics

$T_a = 25 \pm 5°C$ $V_{CC} = 5\ V \pm 10\%$

Parameter	Symbol	Condition	Min	Max	Unit
Vpp Read Voltage	Vpp	–	4.5	5.5	V
Input High Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$ and $\overline{PGM}$)	$V_{IH}1$	–	2.2	V_{CC} + 0.3	V
Input High Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$ and $\overline{PGM}$)	$V_{IL}1$	–	–0.3	0.8	V
Address to Output Delay	TACC	CL = 50 pF	-	$2.25T_{CYC} + \alpha$	ns

TCYC = 400 ns (10 MHz Clock) α = 200 ns

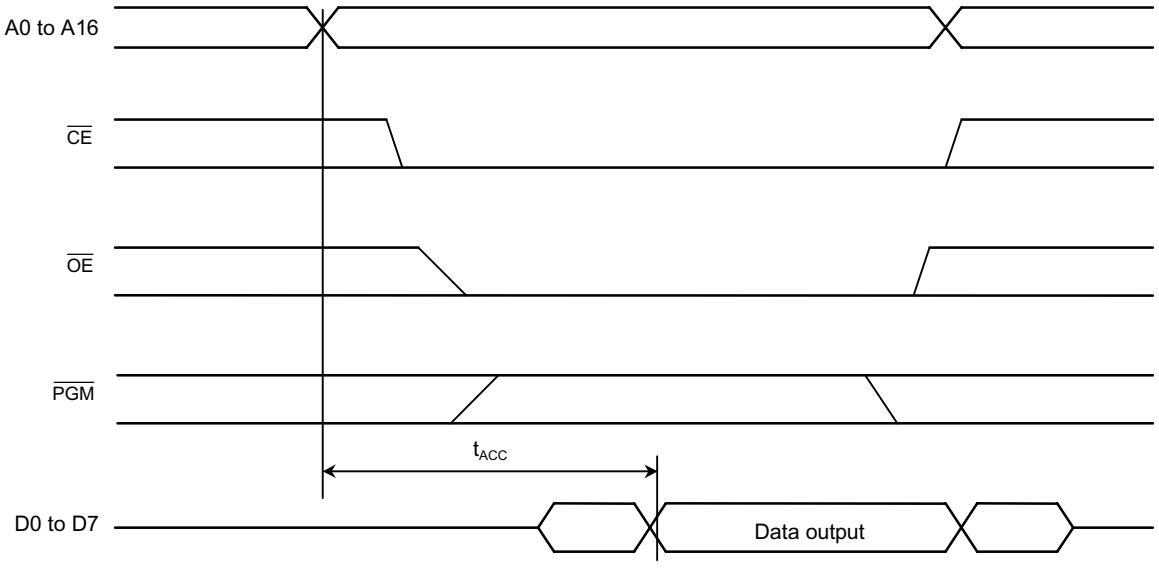
4.10 Program operation in PROM mode

DC/AC characteristics

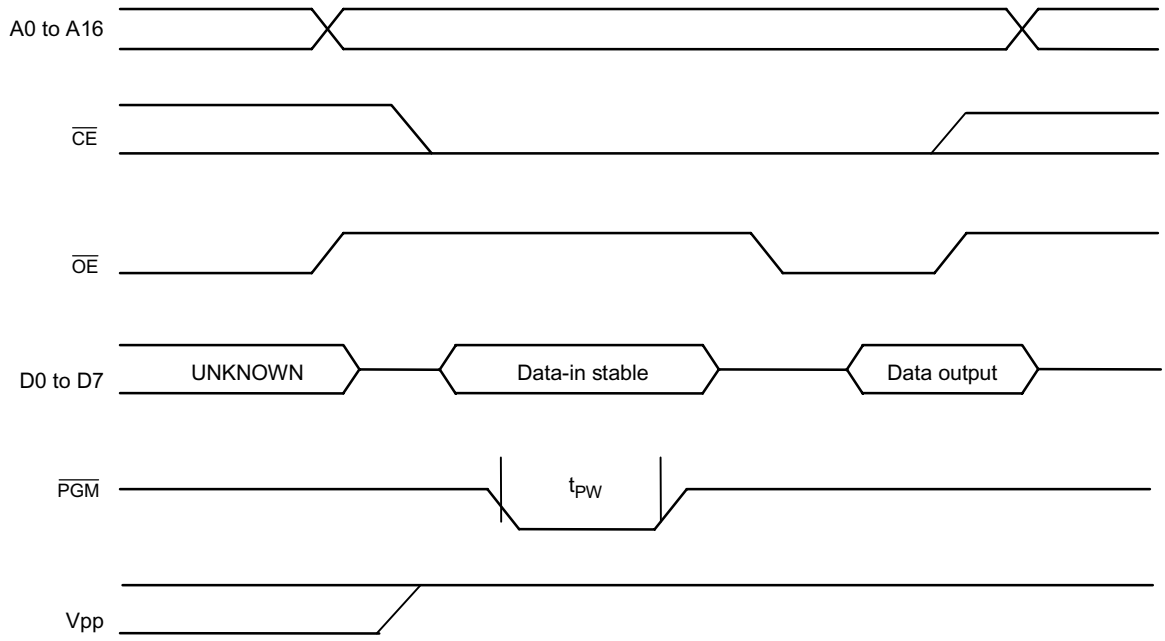
$T_a = 25 \pm 5°C$ $V_{CC} = 6.25\ V \pm 0.25\ V$

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Programming Supply Voltage	Vpp	–	12.5	12.75	13.00	V
Maximum Input Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$ and $\overline{PGM}$)	V_{IH}	–	2.6		V_{CC} + 0.3	V
Minimum Input Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$ and $\overline{PGM}$)	V_{IL}	–	–0.3		8	V
V_{CC} Supply Current	I_{CC}	fc = 10 MHz			50	mA
V_{CC} Supply Current	I_{PP}	V_{PP} = 13.00 V			50	mA
$\overline{PGM}$ Program Pulse Width	t_{PW}	CL = 50 pF	0.095	0.1	0.105	ns

4.11 Timing chart of Read operation in PROM mode



4.12 Timing chart of Program operation in PROM mode



Note 1. The power supply V_{pp} (12.75 V) must be turned on at the same time as or later than the power supply V_{CC} and must be turned off at the same time as or early than the power supply V_{CC}.

Note 2. If V_{pp} =12.75 V, do not remove or insert the device, as this may damage it. If V_{pp} = 5 V the device can be removed and replaced without risk.

Note 3. The maximum rating for the V_{pp} pin is 14.0 V. Ensure that this rating is never exceeded.