CMOS 8-Bit Microcontroller

TMP87CM39N/F, TMP87CP39N/F, TMP87CS39N/F

The TMP87CM39/P39/S39 are the high-speed and high-performance 8-bit single chip microcomputers. These MCU contain CPU core, ROM, RAM, input/output ports, six multi-function timer/counters, serial bus interface, on-screen display, PWM outputs, 8-bit A/D converter, remote control signal preprocessor, and two clock generators on a chip.

Part No.	ROM	RAM	Package	OTP
TMP87CM39N/F	32 Kbytes	1 Kbytes	P-SDIP64-750-1.78 P-QFP64-1420-1.00A	TMP87PS39N TMP87PS39F
TMP87CP39N/F	48 Kbytes	2 Kbytes		
TMP87CS39N/F	60 Kbytes			

Features

◆8-bit single chip microcomputer TLCS-870 Series
◆Instruction execution time : 0.5 μs (at 8 MHz), 122 μs (at 32.768 kHz)
◆412 basic instructions
- Multiplication and Division (8 bits × 8 bits , 16 bits ÷ 8 bits)
- Bit manipulations (Set/Clear/Complement/Move/Test/Exclusive or)
- 16-bit data operations
- 1-byte jump/subroutine-call (Short relative jump/Vector call)

◆15 interrupt sources (External: 6, Internal: 9)
- All sources have independent latches each, and nested interrupt control is available.
- 4 edge-selectable external interrupts with noise reject
- High-speed task switching by register bank changeover

◆Program Corrective Function
◆8 Input/Output ports (55 pins)
- High current output : 4 pins (typ. 20 mA)

◆Two 16-bit Timer/Counters
- Timer, Event counter, Programmable pulse generator output, Pulse width measurement, External trigger timer, Window modes

Purchase of TOSHIBA I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

◆Two 8-bit Timer/Counters
- Timer, Event counter, Capture (Pulse width/duty measurement) modes

◆Time Base Timer (Interrupt frequency: 1 Hz to 16 kHz)
◆Divider output function (frequency: 1 kHz to 8 kHz)
◆Watchdog Timer
- Interrupt source/reset output (programmable)

◆Serial Bus Interface
- I²C-bus, 8-bit SIO modes
  Selectable two I/O channels

◆On-screen display circuit
- Character patterns : 256 characters
- Characters displayed : 24 columns × 12 lines
- Composition : 14 × 18 dots
- Size of character : 3 kinds (line by line)
- Color of character : 8 kinds (character by character)
- Variable display position : Horizontal 128 steps, Vertical 256 steps
- Fringing, Smoothing function

◆DA conversion (Pulse Width Modulation) outputs
- 14-bit resolution (1 channel)
- 7-bit resolution (9 channels)

◆8-bit successive approximate type AD converter with sample and hold
- 8 analog inputs
- Conversion time : 23 μs at 8 MHz

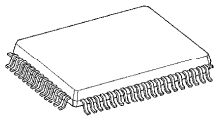
◆Remote control signal preprocessor
◆Jitter Elimination
◆Dual clock operation
- Single/Dual-clock mode (option)

◆Five Power saving operating modes
- STOP mode : Oscillation stops. Battery/Capacitor back-up. Port output hold/high-impedance.
- SLOW mode : Low power consumption operation using low-frequency clock (32.768 kHz).
- IDLE1 mode : CPU stops, and Peripherals operate using high-frequency clock. Release by interrupts.
- IDLE2 mode : CPU stops, and Peripherals operate using high and low frequency clock. Release by interrupts.
- SLEEP mode : CPU stops, and Peripherals operate using low-frequency clock. Release by interrupts.

◆Wide operating voltage : 2.7 to 5.5 V at 32.768 kHz, 4.5 to 5.5 V at 8 MHz
◆Emulation Pod : BM87CS39N0A

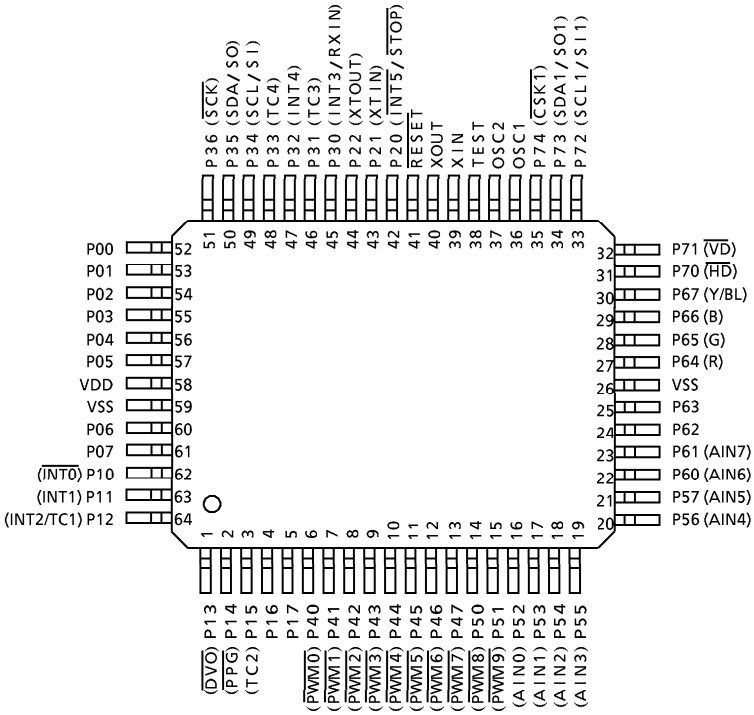
Pin Assignments (Top View)

P-QFP1420-1.00A



TMP87CM39F
TMP87CP39F
TMP87CS39F
TMP87PS39F

P-QFP64-1420-1.00A



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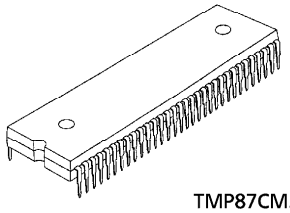

TMP87CM39N
TMP87CP39N
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TMP87PS39N

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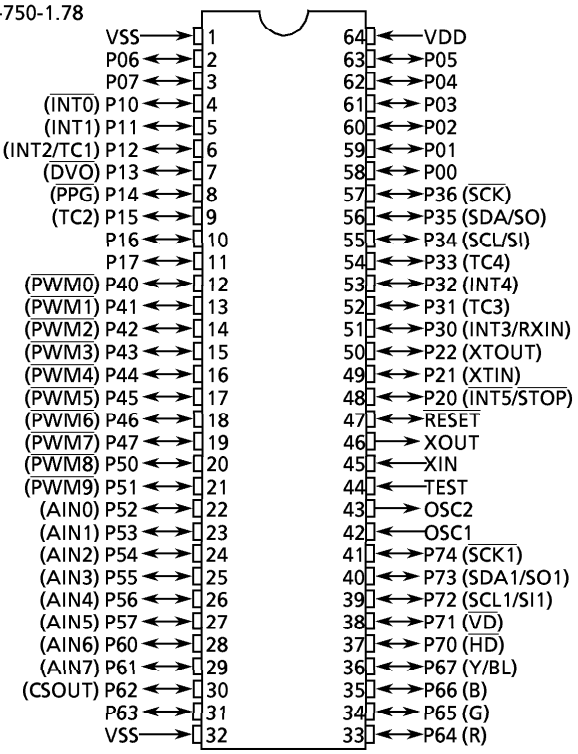
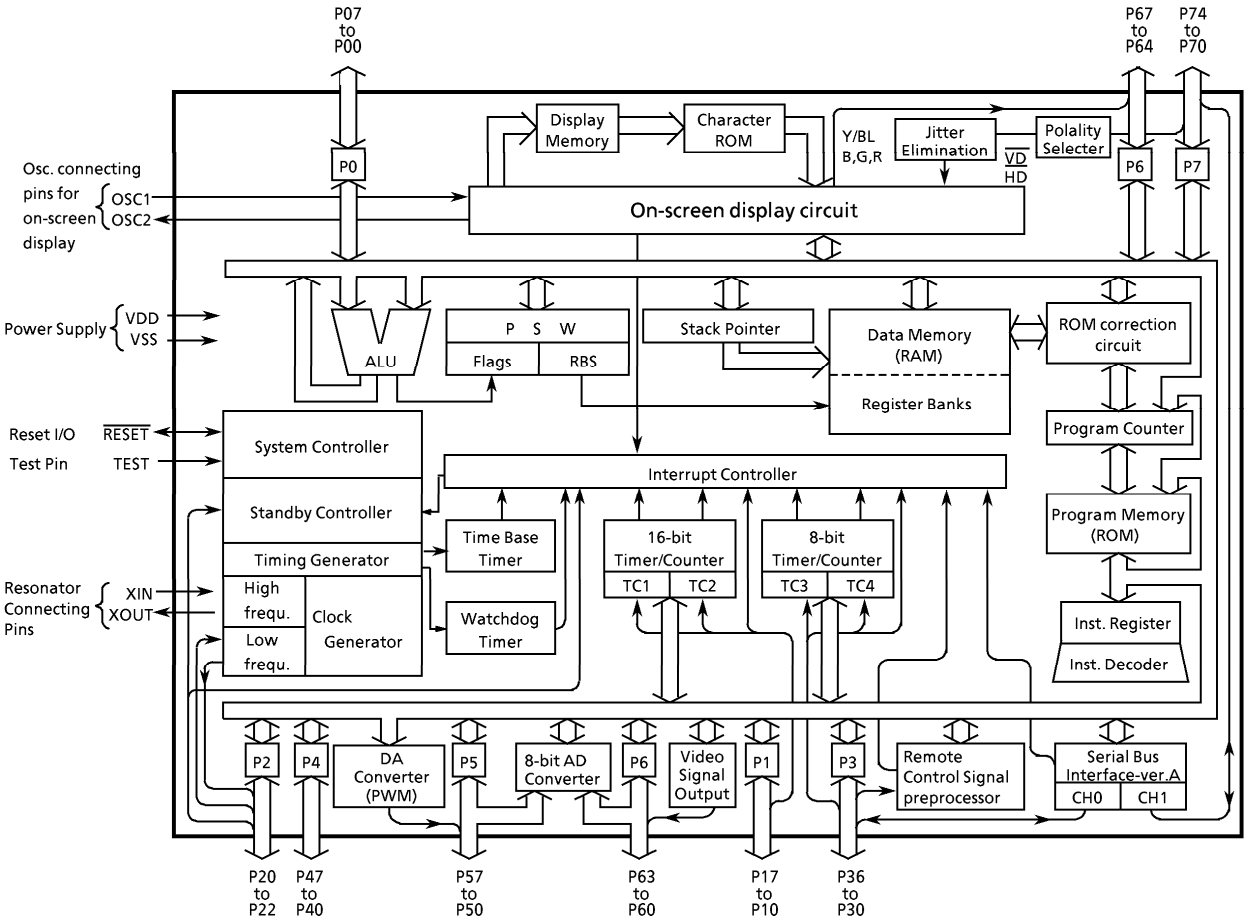


Block Diagram



Pin Function

Pin Name	Input/Output	Function		
P07 to P00	I/O	Two 8-bit programmable input/output ports (tri-state). Each bit of these ports can be individually configured as an input or an output under software control. During reset, all bits are configured as inputs. When used as a divider output or a PPG output, the latch must be set to "1".		
P17, P16	I/O			
P15 (TC2)	I/O (Input)		Timer/Counter 2 input	
P14 ($\overline{PPG}$)	I/O (Output)		Programmable pulse generator output	
P13 ($\overline{DVO}$)			Divider output	
P12 (INT2/TC1)	I/O (Input)		External interrupt input 2 or Timer/Counter 1 input	
P11 ($\overline{INT1}$)			External interrupt input 1	
P10 ($\overline{INT0}$)			External interrupt input 0	
P22 (XTOUT)	I/O (Output)	3-bit input/output port with latch. When used as an input port, the latch must be set to "1".	Resonator connecting pins (32.768 kHz). For inputting external clock, XTIN is used and XTOUT is opened.	
P21 (XTIN)	I/O (Input)			
P20 ($\overline{INT5}$/$\overline{STOP}$)			External interrupt input 5 or STOP mode release signal input	
P36 ($\overline{SCK0}$)	I/O (I/O)	7-bit input/output port with latch. When used as an input port, a serial bus interface input/output, a timer/counter input, a remote control signal preprocessor input, or an external interrupt input, the latch must be set to "1".	SIO serial clock input/output 0	
P35 (SDA0/SO0)	I/O (I/O/Output)		I^2Cbus serial data input/output or SIO serial data output 0	
P34 (SCL0/SI0)	I/O (I/O/Input)		I^2Cbus serial clock input/output or SIO serial data input 0	
P33 (TC4)	I/O (Input)		Timer/Counter 4 input	
P32 ($\overline{INT4}$)			External interrupt input 4	
P31 (TC3)			Timer/Counter 3 input	
P30 (INT3/RXIN)	I/O (Input/Input)		External interrupt input 3 or remote control signal preprocessor input	
P47 ($\overline{PWM7}$) to P41 ($\overline{PWM1}$)	I/O (Output)	8-bit programable input/output port (tri-state). Each bit of this port can be individually configured as an input or an output under software control. During reset, all bits are configured as inputs. When used as a PWM output, the latch must be set to "1".	7-bit DA conversion (PWM) outputs	
P40 ($\overline{PWM0}$)			14-bit DA conversion (PWM) output	
P57 (AIN5) to P52 (AIN0)	I/O (Input)	8-bit programable input/output port (tri - state) . Each bit of this port can be individually configured as an input or an output under software control. When used as an input port, analog input, or a PWM output, the latch must be set to "1".	AD converter analog inputs	
P51 ($\overline{PWM9}$)	I/O (Output)		7-bit DA conversion (PWM) outputs	
P50 ($\overline{PWM8}$)				
P67 (Y/BL)	I/O (Output)	8-bit programable input/output port (P67 to P64 : tri-state, P63 to P60 : High current output). Each bit of this port can be individually configured as an input or an output under software control. During reset, all bits are configured as inputs. When used as the R, G, B, Y/BL outputs of on-screen display circuit, each bit of the P6 port data selection register (bits 7 to 4 in address $0F91_H$) must be set to "1".	Focus signal output or Background blanking control signal output	
P66 (B)			RGB outputs	
P65 (G)				
P64 (R)				
P63	I/O		High current outputs	Test video signal output
P62 (CSOUT)				
P61 (AIN7)	I/O (Input)			AD converter analog inputs
P60 (AIN6)				

Pin Name	Input/Output	Function	
P74 ($\overline{SCK1}$)	I/O (I/O)	5-bit input/output port with latch. When used as an input port, a serial bus interface input/output, or a vertical synchronous signal input and horizontal synchronous signal input, the latch must be set to "1".	SIO serial clock input/output 1
P73 (SDA1/SO1)	I/O (I/O/Output)		I2Cbus serial data input/output or SIO serial data output 1
P72 (SCL1/SI1)	I/O (I/O/Input)		I2Cbus serial data input/output or SIO serial data input 1
P71 ($\overline{VD}$)	I/O (Input)		Vertical synchronous signal input
P70 ($\overline{HD}$)			Horizontal synchronous signal input
OSC1, OSC2	Input, Output	Resonator connecting pins for on-screen display circuitry.	
XIN, XOUT		Resonator connecting pins. For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	I/O	Reset signal input or watchdog timer output/address-trap- reset output/system-clock-reset output.	
TEST	Input	Test pin for out-going test. Be tied to low.	
VDD, VSS	Power Supply	+ 5 V, 0 V (GND)	

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

The TLCS-870 Series is capable of addressing 64 Kbytes of memory. Figure 1-1 shows the memory address maps of the TMP87CM39/P39/S39. In the TLCS-870 Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR/DBR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the first 128 bytes of the RAM address space.

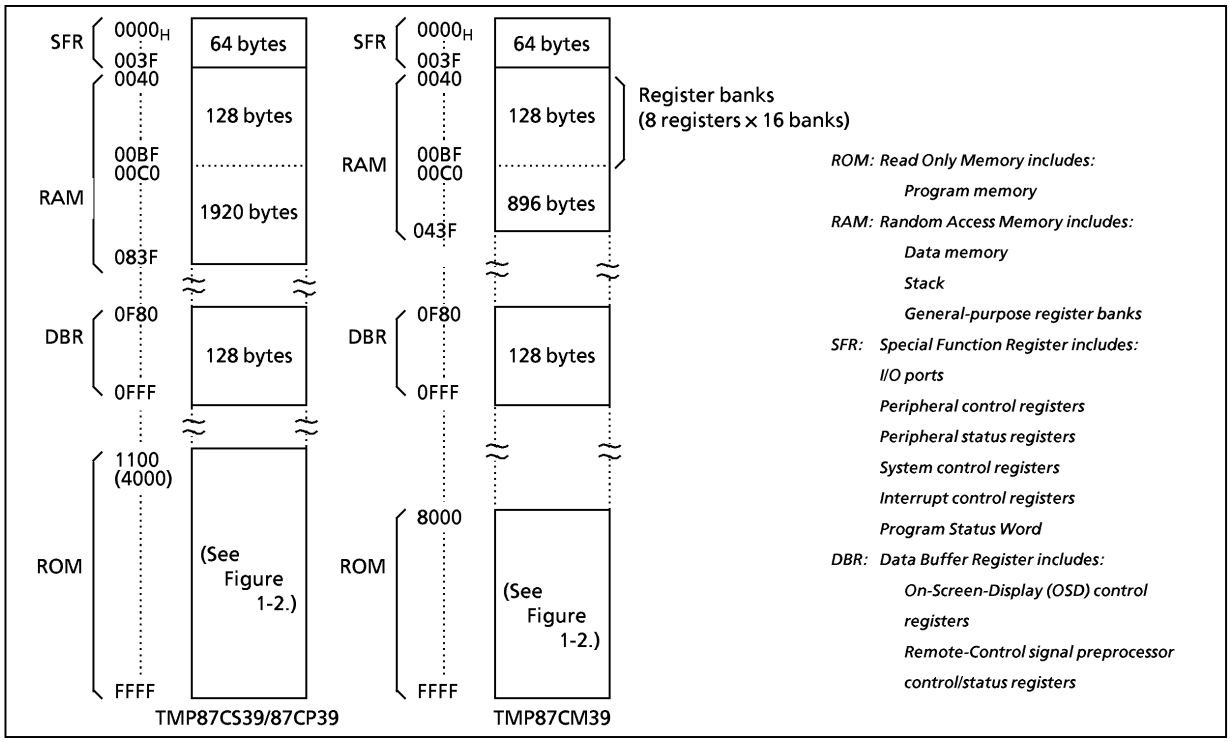


Figure 1-1. Memory Address Map

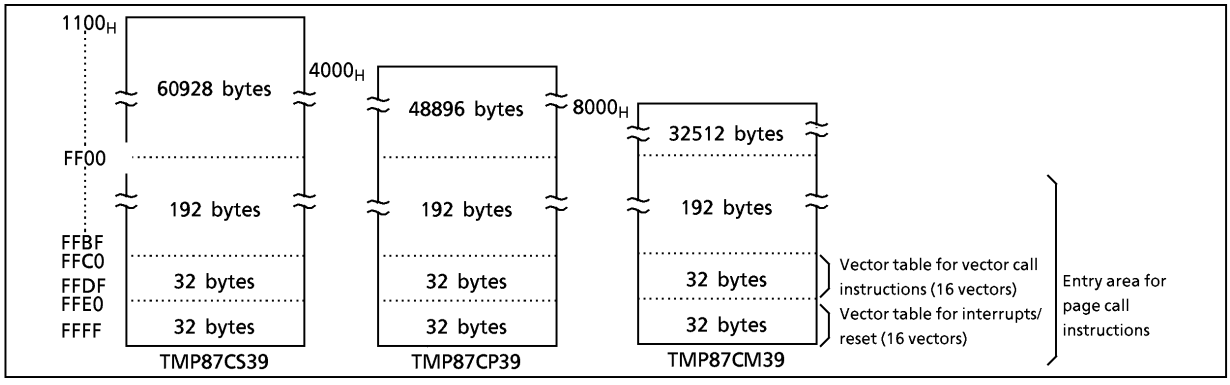


Figure 1-2. ROM Address Maps

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Rating	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	
Output Voltage	V_{OUT1}		– 0.3 to V_{DD} + 0.3	
Output Current (Per 1 pin)	I_{OUT1}	Ports P0, P1, P2, P3, P4, P5, P64 to P67, P7	3.2	mA
	I_{OUT2}	Ports P60 to P63	30	
Output Current (Total)	ΣI_{OUT1}	Ports P0, P1, P2, P3, P4, P5, P64 to P67, P7	120	
	ΣI_{OUT2}	Ports P60 to P63	120	
Power Dissipation [Topr = 70°C]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10 s)	°C
Storage Temperature	T_{stg}		– 55 to 125	
Operating Temperature	T_{opr}		– 30 to 70	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 8 MHz	NORMAL1, 2 mode	4.5	5.5	V
				IDLE1, 2 mode			
			fs = 32.768 kHz	SLOW mode	2.7		
				SLEEP mode			
				STOP mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5V$		$V_{DD} \times 0.70$	V_{DD}	
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.90$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5V$		0	$V_{DD} \times 0.30$	
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IH3}		$V_{DD} < 4.5V$			$V_{DD} \times 0.01$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5V		4.0	8.0	MHz
	f_{OSC}	OSC1, OSC2	Normal frequency mode (FORS = 0, V_{DD} = 4.5 to 5.5 V)		4.0	fosc ≦ fc × 1.2 ≦ 8.0	
			Double frequency mode (FORS = 1, V_{DD} = 4.5 to 5.5 V)		2.0	fosc ≦ fc × 0.6 ≦ 4.0	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc ; The condition of supply voltage range is the value in NORMAL 1/2 mode and IDLE 1/2 mode.

Note 3: When using test video signal circuit, high frequency must be 8 MHz.

Note 4: When the OSD circuit is used, the supply voltage must be from 4.5 V to 5.5 V.

DC Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis inputs		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V, V_{IN} = 5.5 V/0 V	–	–	± 2	μA
	I_{IN2}	Open drain ports	V_{DD} = 5.5 V, V_{IN} = 5.5 V/0 V	–	–	± 2	
	I_{IN3}	Tri-state ports	V_{DD} = 5.5 V, V_{IN} = 5.5 V/0 V	–	–	± 2	
	I_{IN4}	$\overline{RESET}$, $\overline{STOP}$	V_{DD} = 5.5 V, V_{IN} = 5.5 V/0 V	–	–	± 2	
Input Resistance	R_{IN2}	$\overline{RESET}$		100	220	450	kΩ
Output Leakage Current	I_{LO1}	Sink open drain ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
	I_{LO2}	Tri-state ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V/0 V	–	–	± 2	
Output High Voltage	V_{OH2}	Tri-state ports	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	V
Output Low Voltage	V_{OL}	Except XOUT, OSC2 and ports P63 to P60	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	
Output Low current	I_{OL3}	Ports P63 to P60	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	20	–	mA
Supply Current in NORMAL 1, 2 modes	I_{DD}		V_{DD} = 5.5 V, V_{IN} = 5.3 V/0.2 V fc = 8 MHz fs = 32.768 kHz	–	13	20	
Supply Current in IDLE 1, 2 modes				–	6.5	10	
Supply Current in SLOW mode			V_{DD} = 3.0 V fs = 32.768 kHz V_{IN} = 2.8 V/0.2 V	–	30	70	μA
Supply Current in SLEEP mode				–	15	35	
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V	–	0.5	10	

Note 1 : Typical values show those at Topr = 25°C , V_{DD} = 5 V.

Note 2 : Input Current I_{IN1}, I_{IN4} ; The current through pull-up or pull-down resistor is not included.

Note 3 : Supply Current I_{DD} ; The current (Typ. 0.5 mA) through ladder resistors of ADC is included in NORMAL mode and IDEL mode.

AD Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{DD}	supplied from V_{DD} pin	–	V_{DD}	–	V
	V_{SS}	supplied from V_{SS} pin	–	0	0	
Analog Reference Voltage Range	ΔV_{AREF}	= V_{DD} – V_{SS}	–	V_{DD}	–	
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{DD}	
Nonlinearity Error		V_{DD} = 4.5V to 5.5V	–	–	± 1	LSB
Zero Point Error			–	–	± 2	
Full Scale Error			–	–	± 2	
Total Error			–	–	± 3	

AC Characteristics

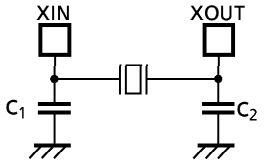
(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	t_{cy}	In NORMAL1, 2 modes	0.5	–	1.0	μs
		In IDLE1, 2 modes				
		In SLOW mode	117.6	–	133.3	
		In SLEEP mode				
High-Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input), fc = 8 MHz	62.5	–	–	ns
Low-Level Clock Pulse Width	t_{WCL}					
Low-Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	14.7	–	–	μs
Low-Level Clock Pulse Width	t_{WSL}					

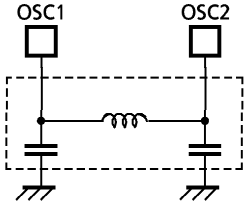
Recommended Oscillating Conditions

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

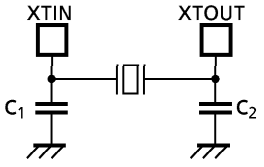
Parameter	Oscillator	Oscillation Frequency	Recommended Oscillator	Recommended Constant	
				C_1	C_2
High-frequency Oscillation	Ceramic Resonator	8 MHz	KYOCERA KBR8.0M	30 pF	30 pF
		4 MHz	KYOCERA KBR4.0MS		
			MURATA CSA4.00MG		
	Crystal Oscillator	8 MHz	TOYOCOM 210B 8.0000	20 pF	20 pF
		4 MHz	TOYOCOM 204B 4.0000		
OSD	LC Resonator	8 MHz	TOKO A285TNIS-11695	–	–
		7 MHz	TOKO TBEKSES-30375FBY		
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	NDK MX-38T	15 pF	15 pF



(1) High-frequency Oscillation



(2) LC Resonator for OSD



(3) Low-frequency Oscillation

Note: On our OSD circuit, the horizontal display start position is determined by counting the clock from LC oscillator. So, the unstable start of oscillation after the rising edge of Horizontal Sync. Signal will be cause the OSD distortion. Generally, smaller C and larger L make clearer wave form at the beginning of oscillation. We recommend that the value of LC oscillator should be equal and bigger than 33μH.

Note: To keep reliable operation, shield the device electrically with the metal plate on its package mold surface against the high electric field, for example, be CRT (Cathode Ray Tube).