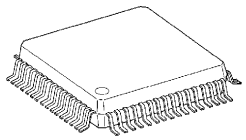
CMOS 8-Bit Microcontroller

TMP86FS41F

The TMP86FS41F is a high-speed, high-performance 8-bit microcomputer built around the TLCS870/C Series core with built-in 60-Kbyte ROM and it is pin compatible with its mask ROM version, the TMP86CM41F. Writing programs in the built-in flash memory enables this microcomputer to perform the same operations as the TMP86CM41F. The built-in flash memory can be rewritten on-board (without removing it from the PCB) by a built-in boot program and it can also be rewritten by executing a user-made rewrite program on RAM.

Part No.	Flash EEPROM	RAM	Package
TMP86FS41F	60 Kbyte	2 Kbyte	P-QFP64-1414-0.80B

P-QFP64-1414-0.80B



TMP86FS41F

Features

- 8-bit single chip microcomputer TLCS-870/C series
- Instruction execution time: 0.25 μs (at 16 MHz)
  122 μs (at 32.768 kHz)
- 132 types & 731 basic instructions
- 21 interrupt sources (External: 6, Internal: 15)
- Input / Output ports (55 pins)
  High current output: 8 pins (typ. 20 mA)
- 16-bit timer counter: 2 ch
  - Timer, Event counter, Pulse width measurement, Programmable pulse Generator (PPG), External-triggered timer, Window modes
- 8-bit timer counter: 4 ch
  - Timer, Event counter, Pulse Width Modulation (PWM) output, Programmable Divider Output (PDO), PPG modes

- Time Base Timer (TBT)
- Divider output function
- Watchdog Timer
  - Interrupt source/reset output (programmable)
- Serial interface
  - 8-bit SIO: 1ch
  - 8-bit UART: 1ch (IrDA output, selection of used pin)
- 10-bit successive approximation type AD converter
  - Analog input: 16 ch
- Key On Wake Up: 4 ch
- Dual clock operation
  - Single/Dual-clock mode
- Nine power saving operating modes
  - STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/High-impedance.
  - SLOW 1, 2 mode: Low power consumption operation using low-frequency clock (32.768 kHz)
  - IDLE 0 mode: CPU stops, and peripherals operate using high-frequency clock of Time-Base-Timer. Release by INTTBT interrupt.
  - IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock. Release by interrupts.
  - IDLE 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release by interrupts.
  - SLEEP 0 mode: CPU stops, and peripherals operate using low-frequency clock of Time-Base-Timer. Release by INTTBT interrupt.
  - SLEEP 1 mode: CPU stops, and peripherals operate using low-frequency clock. Release by interrupts.
  - SLEEP 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release by interrupts.
- Wide operating voltage: 4.5 to 5.5 V at 16 MHz/32.768 kHz

Difference between TMP86CM41F, TMP86CS41F, TMP86FS41F

The functions and the electrical characteristics between above products have some difference. Please refer the notice below.

1. Functions

a) Memory size

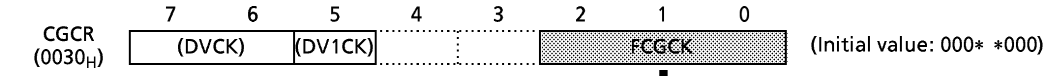
Product No.	ROM	RAM
TMP86CM41F	32 kbyte	1 kbyte
TMP86CS41F	60 kbyte	2 kbyte
TMP86FS41F	60 kbyte	2 kbyte

b) Clock gear

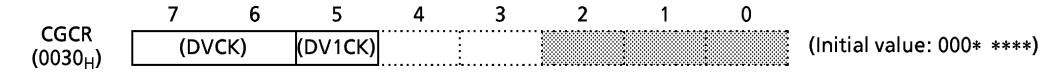
Product No.	Clock gear
TMP86CM41F	Support
TMP86CS41F	Not support
TMP86FS41F	Support

When developing a software for TMP86CS41F by using TMP86FS41F, CGCR<FCGCK> must be set to "000".

● TMP86CM41F/TMP86FS41F



● TMP86CS41F



c) Port5

Product No.	Input
TMP86CM41F	CMOS
TMP86CS41F	Schmitt
TMP86FS41F	Schmitt

2. Electrical Characteristics

The some electrical characteristics except below are different. Please refer the technical data book of TMP86CM41F, TMP86CS41F and TMP86FS41F.

a) Absolute maximum ratings (VSS = 0)

Parameter	Symbol	Pin	Rating			Unit
			TMP86CM41F	TMP86CS41F	TMP86FS41F	
Output current (Total)	Σ IOUT1	Except P5	80	60	80	mA
	Σ IOUT2	P5 (Large current)	120	60	120	
Operating Temperature	Topr		-40 to 85	-40 to 85	-20 to 70	°C

b) Recommended operating condition

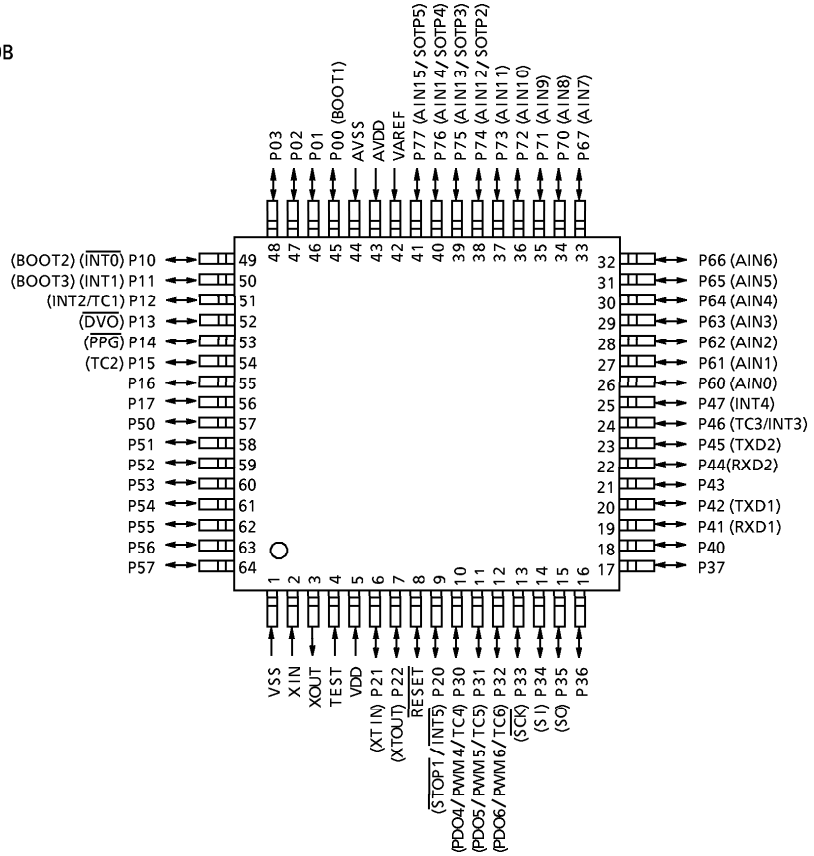
The supply voltage and the clock frequency have difference.

Recommended operating condition (Vss = 0 V, Topr = −40 to 85°C (Except TMP86FS41F))

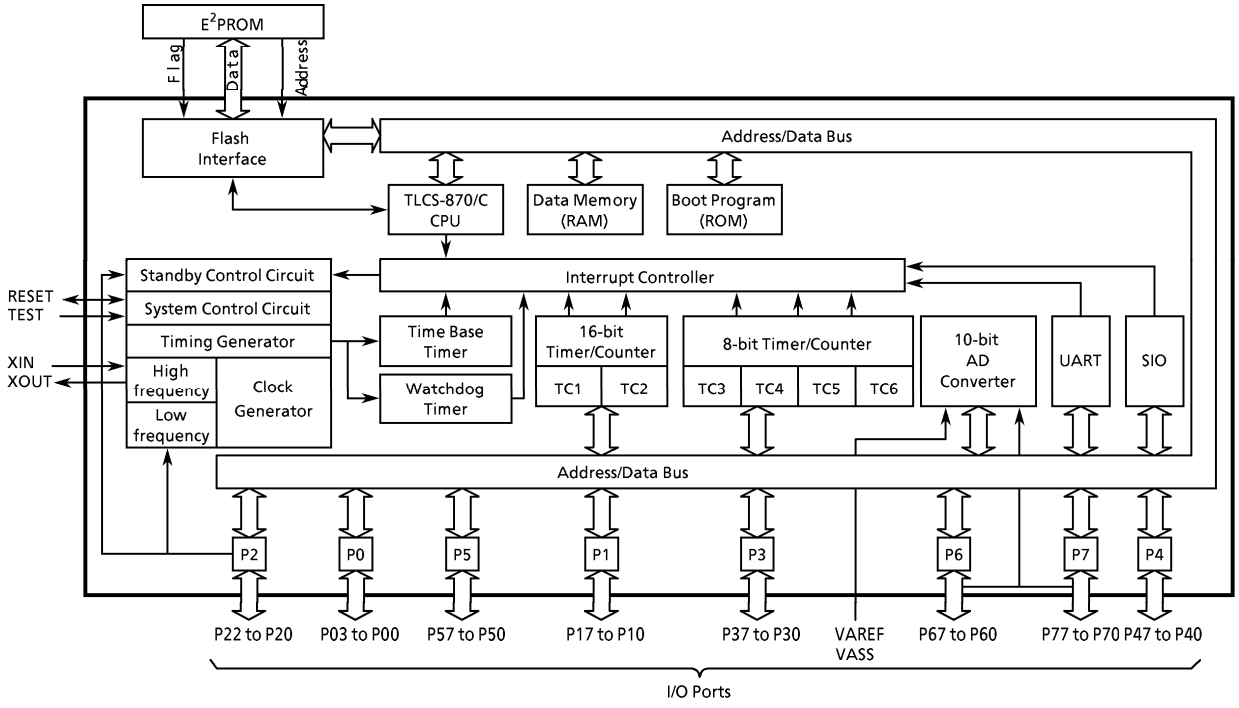
Parameter	Symbol	Pin	Condition		TMP86CM41F		TMP86CS41F		TMP86FS41F		Unit
					Min	Max	Min	Max	Min	Max	
Supply voltage	VDD		fc = 1 to 16 MHz	NOMAL1, 2 mode	4.5	5.5	4.5	5.5	4.5	5.5	V
			fc = 1 to 8 MHz	IDLE0, 1, 2 mode			2.7				
			fs = 32.768 kHz	SLOW1, 2 mode							
				SLEEP0, 1, 2 mode							
				STOP mode	2.0		2.0				
Clock frequency	fc	XIN, XOUT	VDD = 4.5 to 5.5 V		1.0	16.0	1.0	16.0	1.0	16.0	MHz
			VDD = 2.7 to 5.5 V		–	–	1.0	8.0	–	–	
	fs	XIN, XOUT	VDD = 4.5 to 5.5 V		30.0	34.0	30.0	34.0	30.0	34.0	kHz
			VDD = 2.7 to 5.5 V		–	–			–	–	

Pin Assignments (Top View)

P-QFP64-1414-0.80B



Block Diagram



Pin Function

The TMP86FS41 has MCU mode and single boot mode.

(1) MCU Mode

This mode is the same as that of the TMP86CM41 except that TEST pin does not have a built-in pull-down resister. (Be sure to fix TEST pin at low level.)

(2) Single Boot Mode

The boot mode is set by fixing TEST pin at "H", P00 pin at "H", P10 pin at "H" and P11 pin at "H" respectively when RESET pin is set to "L". Setting RESET pin to "H" (releasing RESET) activates the built-in boot ROM and the flash memory is rewritten by serial transfer (UART).

Pin Name	Input / Output	Function		Single Boot Mode
P00	I/O	4-bit I/O port. Each bit of these ports can be individually configured as an input or an output under software control.	–	High level (Boot1)
P01				
P02				
P03				
P10 ($\overline{INT0}$)	I/O (Input)	8-bit I/O port with latch. Each bit of these ports can be individually configured as an input or an output under software control. When used as divider output, PPG output, the latch of used bit must be set to "1", and used bits are configured outputs.	External Interrupt input	Low level (Boot2)
P11 (INT1)			External Interrupt input	High level (Boot3)
P12 (INT2/TC1)			External interrupt input Timer	
P13 ($\overline{DVO}$)	I/O (Output)		Divider output	
P14 ($\overline{PPG}$)			PPG output	
P15 (TC2)	I/O (Input)		Timer/Counter input	
P16	I/O		–	
P17				
P20 ($\overline{INT5}$/$\overline{STOP1}$)	I/O (Input)	3-bit I/O port with latch. When used as input port, external interrupt input, and STOP mode release signal input, the latch must be set to "1".	External interrupt input STOP mode release signal input	
P21 (XTIN)	I/O (Output)		Low Frequency Clock input	
P22 (XOUT)			Low Frequency Clock output	
P30 (TC4/PWM4/PDO4)	I/O (Input/Output /Output)	8-bit I/O port with latch. Each bit of these ports can be individually configured as an input or an output under software control. When used as Timer / Counter input, SI, used bits are configured inputs. When used as PWM output, PDO output, and SO, used bits are configured outputs.	Timer/Counter input PWM output PDO output	
P31 (TC5/PWM5/PDO5)				
P32 (TC6/PWM6/PDO6)				
P33 ($\overline{SCK}$)	I/O (I/O)		SIO input / output	
P34 (SI)	I/O (Input)			
P35 (SO)	I/O (Output)			
P36	I/O		–	
P37				
P40	I/O	8-bit I/O port with latch. Each bit of these ports can be individually configured as an input or an output under software control. When used as UART mode, the latch must be set to "1". When used as Open-Drain output, P4ODE and P4CR must be set to "1".	–	
P41 (RXD1)	I/O (Input)		UART Data input	Data input
P42 (TXD1)	I/O (Output)		UART Data output	Data output
P43	I/O		–	
P44 (RXD2)	I/O (Input)		UART Data input	
P45 (TXD2)	I/O (Output)		UART Data output	
P46 (TC3/INT3)	I/O (Input)		Timer/Counter input External Interrupt input	
P47 (INT4)			External Interrupt input	

Pin Name	Input / Output	Function		Single Boot Mode
P50 P51 P52 P53 P54 P55 P56 P57	I/O	8-bit I/O port. Each bit of these ports can be individually configured as an input or output under software control. These ports are High current output ports, can be drive LED direct.	–	
P60 (AIN0) P61 (AIN1) P62 (AIN2) P63 (AIN3) P64 (AIN4) P65 (AIN5) P66 (AIN6) P67 (AIN7)	I/O (Input)	8-bit I/O port. Each bit of these ports can be individually configured as an input or output under software control.	AD Convertor analog inputs	
P70 (AIN8) P71 (AIN9) P72 (AIN10) P73 (AIN11) P74 (AIN12/STOP2) P75 (AIN13/STOP3) P76 (AIN14/STOP4) P77 (AIN15/STOP5)	I/O (Input)	8-bit I/O port. Each bit of these ports can be individually configured as an input or output under software control.	AD Convertor analog inputs AD Convertor analog input STOP mode release signal input	
TEST	Input	Test pin for out-going test. Be fixed to Low.		Low level
$\overline{\text{RESET}}$	I/O	Reset signal input or watchdog timer output/address-trap-reset output.		Low → High level
XIN	Input	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.		
XOUT	Output			
VSS	Power Supply	00 [V] (GND)		0.0 [V] (GND)
VDD		+ 5.0 [V]		+ 5.0 [V]
AVSS		0.0 [V] (GND)		
AVDD		+ 5.0 [V] AD circuit power supply		
VAREF		Analog reference voltage inputs (High, Low)		

Operational Description

The TMP86FS41 is a version of the TMP86CM41 incorporating flash memory in place of the built-in mask ROM. The configuration and functions of the TMP86FS41 is the same as those of the TMP86CM41 except that TEST pin does not have a built-in pull-down resister.
For functions not included herein, please refer to the data sheets of the TMP86CM41.

1. Operational Mode

The TMP86FS41 has MCU mode, single boot mode and user boot mode.

1.1 MCU Mode

The MCU mode is set by fixing TEST pin at "L" level.
Operations in the MCU mode are the same as those of the TMP86CM41.
(Because TEST pin does not have a pull-down register, it cannot be used in the released state.)

1.2 Single Boot Mode

The boot mode is set by fixing TEST pin at "H", P00 pin at "H", P10 pin at "L" and P11 pin at "H" respectively when RESET pin is fixed at "L". After release of reset, the built-in boot ROM program is activated and the built-in flash memory is rewritten by serial transfer (UART).

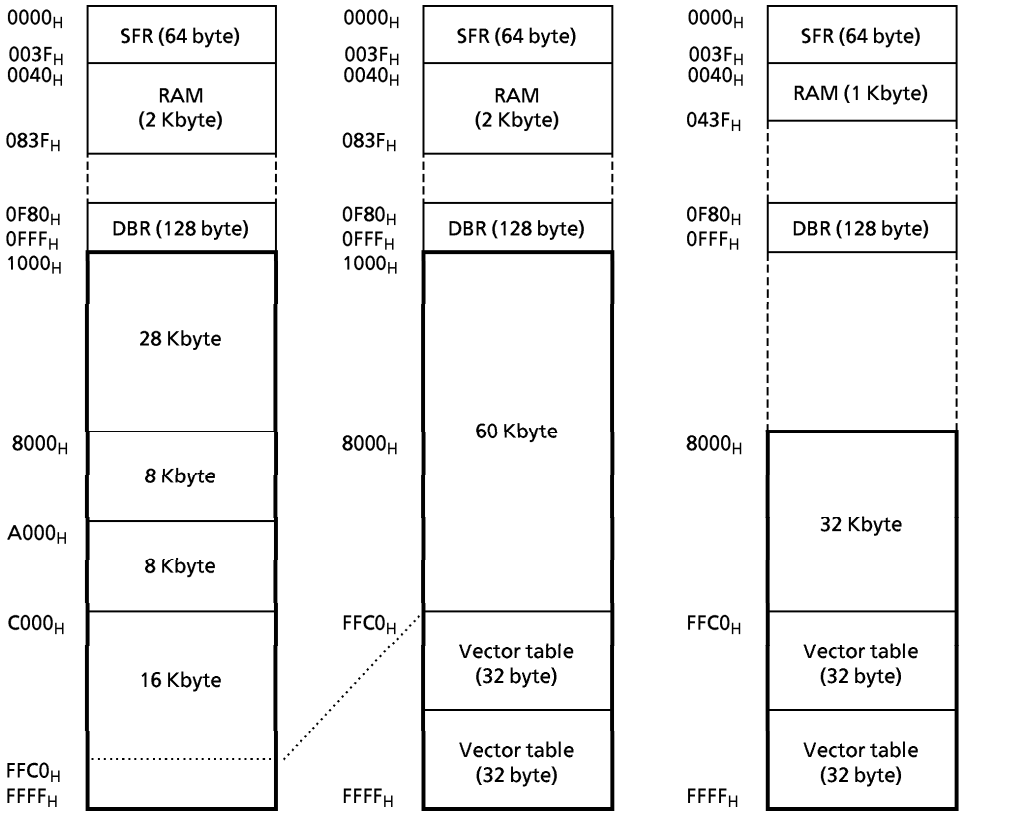
1.3 User Boot Mode

In this mode, rewriting is performed by running a user-made flash memory rewrite program on RAM. After transferring the rewrite program to RAM in the user program, set the address trap area to only the SFR area and then jump to the start address of the rewrite program on RAM. Running that rewrite program effects the rewrite of flash memory.

2. Program Memory

The TMP86FS41 has a 60K×8-bit (address 1000_H to $FFFF_H$: MCU/Boot mode) of Flash memory.

2.1 Address map



Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	
Output Voltage	V_{OUT}		– 0.3 to V_{DD} + 0.3	
Output Current (Per 1 pin)	I_{OUT1}	P0, P1, P3, P4, P5, P6, P7 Port	– 3.2	mA
	I_{OUT2}	P0, P1, P2, P3, P4, P6, P7 Port	3.2	
	I_{OUT3}	P5 Port	30	
Output Current (Total)	ΣI_{OUT1}	P0, P1, P2, P3, P4, P6, P7 Port	80	
	ΣI_{OUT2}	P5 Port	120	
Power Dissipation (Topr = 70°C)	PD		700	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	
Operating Temperature	Topr		– 20 to 70	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition (V_{SS} = 0 V, Topr = – 20 to 70°C)

Parameter	Symbol	Pins	Condition	Min	Max	Unit
Supply Voltage	V_{DD}		fc = 1 to 16 MHz fs = 32.768 kHz (NORMAL1,2 mode IDLE 0,1,2 mode SLEEP 0,1,2 mode SLOW1,2 mode STOP mode)	4.5	5.5	V
Input high Level	V_{IH1}	Except Hysterisis, TTL input	$V_{DD} \geqq 4.5$ V	$V_{DD} \times 0.70$	V_{DD}	
	V_{IH2}	Hysteresis input		$V_{DD} \times 0.75$		
Input low Level	V_{IL1}	Except Hysterisis, TTL input	$V_{DD} \geqq 4.5$ V	0	$V_{DD} \times 0.30$	
	V_{IL2}	Hysteresis input			$V_{DD} \times 0.25$	
Clock Frequency	fc	XIN, XOUT		1.0	16.0	MHz
	fs	XTIN, XTOUT		30.0	34.0	kHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

D.C. Characteristics

(V_{SS} = 0 V, Topr = – 20 to 70°C)

Parameter	Symbol	Pins	Condition	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis inputs		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V V_{IN} = 5.5 V/0 V	–	–	± 2	μA
	I_{IN2}	Sink Open Drain, Tri-st Port					
	I_{IN3}	$\overline{\text{RESET}}$					
Input Resistance	R_{IN}	$\overline{\text{RESET}}$		100	220	450	kΩ
Osec. Feedback Resistance	Rfx	XIN-XOUT		–	1.2	–	MΩ
	Rfxt	XTIN-XTOUT		–	6	–	
Output Leakage Current	I_{LO1}	Sink Open Drain Port	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
	I_{LO2}	Tri-st Port	V_{DD} = 5.5 V, V_{OUT} = 5.5 V/0V	–	–	± 2	
Output High Voltage	V_{OH}	Tri-st Port	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	V
Output Low Voltage	V_{OH3}	P5	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	
Output Low Current	I_{OL1}	Except P5	V_{DD} = 4.5 V, V_{OL} = 0.4 V	–	1.6	–	mA
	I_{OL3}	P5 (High Current Output port)	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	20	–	
Supply Current in NORMAL 1, 2 mode	I_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V fc = 16 MHz fs = 32.768 kHz	–	30	40	
Supply Current in IDLE 1, 2 mode				–	9	13	
Supply Current in SLOW 1 mode			V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V fs = 32.768 kHz	–	11	16.5	
Supply Current in SLEEP 0, 1 mode				–	28	55	μA
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V	–	200	400	

Note 1: Typical values show those at Topr = 25°C, V_{DD} = 5 V

Note 2: Input current (I_{IN1}, I_{IN4}); The current through pull-up or pull-down resistor is not included.

AD Conversion Characteristics (V_{SS} = 0 V, Topr = – 20 to 70°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		4.5	–	V_{DD}	V
	A_{VDD}		V_{DD}			
	A_{VSS}		V_{SS}			
Analog Reference Voltage Range	ΔV_{AREF}	$V_{AREF} - A_{VSS}$	4.5	–	–	
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power Supply Current of Analog Reference Voltage	I_{REF}	$V_{DD} = A_{VDD} = V_{AREF}$ = 5.5 V VSS = A_{VSS} = 0.0 V	–	0.6	1.0	mA
Non linearity Error		V_{DD} = 4.5 to 5.5 V V_{SS} = 0.0 V $A_{VDD} = V_{AREF}$ = VDD A_{VSS} = 0.0 V	–	–	± 2	LSB
Zero Point Error			–	–	± 2	
Full Scale Error			–	–	± 2	
Total Error			–	–	± 4	

Note 1: Total errors includes all errors, except quantization error.
Note 2: Conversion time is different in recommended value by power supply voltage.
About conversion time, please refer to "2.10.2 Register Framing".
Note 3: Please use input voltage to AIN input Pin in limit of V_{AREF} - V_{SS}.
When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.