#### CMOS 8-Bit Microcontroller

# TMP86CM25F, TMP86CS25F

The TMP86CM25/S25 are the high-speed, high-performance and low power consumption 8-bit microcomputer, including ROM, RAM, Dot matrix LCD driver, multi-function timer/counter, serial interface (UART/SIO), a 8-bit AD converter and two clock generators on chip.

| Product No. | lo. ROM       |              | Package             | OTP MCU     |
|-------------|---------------|--------------|---------------------|-------------|
| TMP86CM25F  | 32 K × 8 bits | 2 K v 9 hita | D OFB100 1430 0 654 | TMADOCDCOEF |
| TMP86CS25F  | 60 K × 8 bits | 2 K × 8 bits | P-QFP100-1420-0.65A | TMP86PS25F  |

#### **Features**

◆ 8-bit single chip microcomputer TLCS-870/C series

 Instruction execution time: 0.25 μs (at 16 MHz)  $122 \mu s$  (at 32.768 kHz)

◆ 132 types and 731 basic instructions

20 interrupt sources (External: 5, Internal: 15)

◆ Input/Output ports (42 pins) (Out of which 20 pins are also used as SEG pins.)

♦ 18-bit timer counter: 1 ch

• Timer, Event counter, Pulse width measurement, Frequencymeasurement modes

♦ 8-bit timer counter: 4 ch

• Timer, Event counter, PWM output, Programmable Divider Output, PPG modes

- ◆ Time Base Timer
- Divider output function
- Watchdog Timer
  - Interrupt source/internal reset generate (programmable)



P-QFP100-1420-0.65A

TMP86CM25F

For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled

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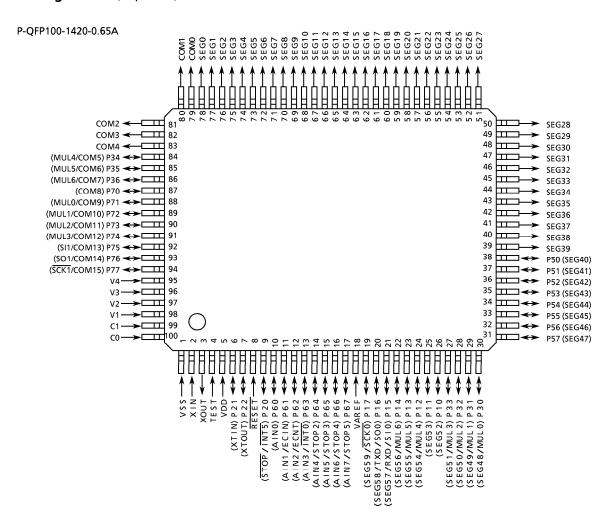
2002-10-10 86CS25-1

◆ Serial interface: 2ch◆ 8-bit UART/SIO: 1ch

• 8-bit SIO: 1ch

- ♦ 8-bit successive approximation type AD converter
  - Analog input: 8 ch
- ♦ Four Key On Wake Up pins
- ◆ LCD driver/controller
  - Built-in voltage booster for LCD driver
  - With displaymemory
  - LCD direct drive capability (60 seg  $\times$  16 com, 60 seg  $\times$  8 com, 60 seg  $\times$  4 com)
  - 1/16, 1/8, 1/4 duties drive are programmably selectable
- ◆ Dual clock operation
  - Single/Dual-clock mode
- ♦ Nine power saving operating modes
  - STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/high-impedance.
  - SLOW 1, 2 mode: Low power consumption operation using low-frequency clock (32.768 kHz)
  - IDLE0 mode: CPU stops, and peripherals stop except Time-Base-Timer.
    - Release by falling edge of TBTCR < TBTCK > setting.
  - IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock. Release by
    - interruputs.
  - IDLE 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release
    - by interruputs.
  - SLEEP 0 mode: CPU stops, and peripherals stop except Time-Base-Timer.
    - Release by falling edge of TBTCR < TBTCK > setting.
  - SLEEP 1 mode: CPU stops, and peripherals operate using low-frequency clock. Release by
    - interrupts.
  - SLEEP 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release
    - by interrupts.
- ♦ Wide operating voltage: 1.8 to 5.5 V at 4.2 MHz/32.768 kHz,
  - 2.7 to 5.5 V at 8 MHz/32.768 kHz,
  - 4.5 to 5.5 V at 16 MHz/32.768 kHz

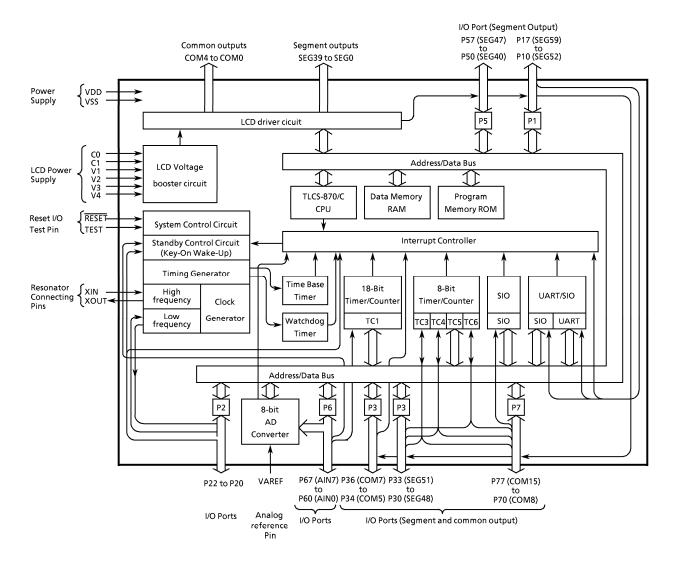
# Pin Assignments (Top View)



Note: Ports assigned as MUL6 to MUL0 can switch pin assignment by the multifunction register (MULSEL). For functions assigned to each pin, see the table below.

| Pin name | Function              | Pin assignment |
|----------|-----------------------|----------------|
| MUL0     | DVO                   | P30 or P71     |
| MUL1     | PWM3, PDO3, TC3       | P31 or P72     |
| MUL2     | PPG4, PWM4, PDO4, TC4 | P32 or P73     |
| MUL3     | PPG6, PWM6, PDO6, TC6 | P33 or P74     |
| MUL4     | INT1                  | P12 or P34     |
| MUL5     | INT2                  | P13 or P35     |
| MUL6     | INT3                  | P14 or P36     |

# **Block Diagram**



# **Pin Function**

| Pin Name                      | Input/Output               |  | Function  |                      |  |
|-------------------------------|----------------------------|--|---|----------------------|--|
| P17 (SEG59, <u>SCK</u> )      | I/O (I/O)                  |  | Serial clock input/Output   |                      |  |
| P16 (SEG58, TxD, SO)          | I/O (Output)               | 8-bit input/output port with latch.  | UART data output<br>Serial data output                              |                      |  |
| P15 (SEG57, RxD, SI)          | 1/0 (1/0)                  | When used as input port, an external interruput input, serial clock input/                                 | UART data input<br>Serial data input                                | I CD commont         |  |
| P14 (SEG56, MUL6)             | I/O (I/O)                  | output, serial data input/output and UART data input/output, the latch                                     | External interrupt 3 input  | LCD segment outputs. |  |
| P13 (SEG55, MUL5)             | I/O (I/O)                  | must be set to "1".  | External interrupt 2 input  |                      |  |
| P12 (SEG54, MUL4)             | I/O (I/O)                  | When used as a LCD segment output, the P1LCR must be set to "1".   | External interrupt 1 input  |                      |  |
| P11 (SEG53)                   | I/O (Output)               |  |   |                      |  |
| P10 (SEG52)                   | I/O (Output)               |  |   |                      |  |
| P22 (XTOUT)                   | I/O (Output)               |  | Resonator connecting pins (32.76 For inputting external clock, XTIN | 8 kHz)               |  |
| P21 (XTIN)                    | I/O (Input)                | 3-bit input/output port with latch. When used as an input port, the latch                                  | XTOUT is opened.  | i is used and        |  |
| P20 (INT5, STOP)              | I/O (Input)                | must be set to "1".  | External interrupt input 5 or STOI signal input                     | P mode release       |  |
| P36 (COM7, MUL6)              | I/O (I/O)                  | 7 hit I/O manturith latel  | External interrupt 3 input  |                      |  |
| P35 (COM6, MUL5)              | I/O (I/O)                  | 7-bit I/O port with latch. When used as input port, an external  | External interrupt 2 input  |                      |  |
| P34 (COM5, MUL4)              | I/O (I/O)                  | interruput input, serial clock input/  | External interrupt 1 input  |                      |  |
| P33 (SEG51, MUL3)             | I/O (I/O)                  | output, serial data input/output and UART data input/output, the latch                                     | Timer/Counter 6 input/output  | LCD segment          |  |
| P32 (SEG50, MUL2)             | I/O (I/O)                  | must be set to "1".  | Timer/Counter 4 input/output  | outputs.             |  |
| P31 (SEG49, MUL1)             | 1/0 (1/0)                  | When used as a LCD segment output, the P3LCR must be set to "1".   | Timer/Counter 3 input/output  |                      |  |
| P30 (SEG48, MUL0)             | I/O (Output)               | the 1 SECK must be set to 1.   | Divider output  |                      |  |
| P57 (SEG16) to<br>P50 (SEG23) | I/O (Output)               | 8-bit input/output port with latch.<br>When used as a LCD segment output,<br>the P5LCR must be set to "1". | LCD segment outputs   |                      |  |
| P67 (AIN7, STOP5)             | I/O (Input)                |  | STOP5 input   |                      |  |
| P66 (AIN6, STOP4)             | I/O (Input)                | 8-bit programmable input/output  | STOP4 input   |                      |  |
| P65 (AIN5, STOP3)             | I/O (Input)                | ports (tri-state). Each bit of these ports can be individually configured                                  | STOP3 input   |                      |  |
| P64 (AIN4, STOP2)             | I/O (Input)                | as an input or an output under   | STOP2 input   | AD converter         |  |
| P63 (AIN3, <u>INT0</u> )      | I/O (Input)                | software control. When used as a key   | External interrupt 0 input  | analog inputs        |  |
| P62 (AIN2, ECNT)              | I/O (Input)                | on wake up input, an external interrupt input and timer/counter  | Time and Community and the second                                   |                      |  |
| P61 (AIN1, ECIN)              | I/O (Input)                | input, the P6CR must be set to "1".  | Timer/Counter 1 input   |                      |  |
| P60 (AIN0)                    | I/O (Input)                |  |   |                      |  |
| P70 (COM8)                    | I/O (Output)               |  |   |                      |  |
| P71 (COM9, MUL0)              | 1/0 (1/0)                  |  | Divider output  |                      |  |
| P72 (COM10, MUL1)             | 1/0 (1/0)                  | 8 hit I/O nort   | Timer/Counter 3 input/output  |                      |  |
| P73 (COM11, MUL2)             | I/O (I/O)                  | 8-bit I/O port. When used common output, P7 port   | Timer/Counter 4 input/output  |                      |  |
| P74 (COM12, MUL3)             | I/O (I/O)                  | control register (P7LCR) should be set   | Timer/Counter 6 input/output  |                      |  |
| P75 (COM13, SI1)              | I/O (I/O)                  | to 1.  | Serial data input   |                      |  |
| P76 (COM14, SO1)              | I/O (Output)               |  | Serial data output  |                      |  |
| P77 (COM15, SCK1)             | I/O (I/O)                  |  | Serial clock input/output   |                      |  |
| SEG39 to SEG0<br>COM4 to COM0 | Output                     | LCD segment outputs LCD common outputs   |   |                      |  |
| V 4 to V 1<br>C1 to C0        | LCD voltage<br>booster pin | LCD voltage booster pin. Capacitors at V4 pin and GND.   | re required between C0 and C1 pi                                    | n and V1/V2/V3/      |  |
| XIN, XOUT                     | Input Output               | Resonator connecting pins for high-fre used and XOUT is opened.  | equency clock. For inputting exter                                  | nal clock, XIN is    |  |
| RESET                         | Input                      | Reset signal input   |   |                      |  |
| TEST                          | Input                      | Test pin for out-going test. Be fixed to   | low.  |                      |  |
|                               |                            | · · · · · · · · · · · · · · · · · · ·  |   |                      |  |
|                               | Power Supply               |  |   |                      |  |
| VDD, VSS<br>VAREF             |                            | + 5 V, 0 (GND)  Analog reference voltage input.  |   |                      |  |

## **Operational Description**

#### 1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

## 1.1 Memory Address Maps

The TMP86CM25/S25 memory consist of 4 blocks: ROM, RAM, DBR (Data Buffer Register) and SFR (Special Function Register). They are all mapped in 64 Kbyte address space. Figure 1-1 shows the TMP86CM25/S25 memory address maps. The general-purpose registers are not assigned to the RAM address space.

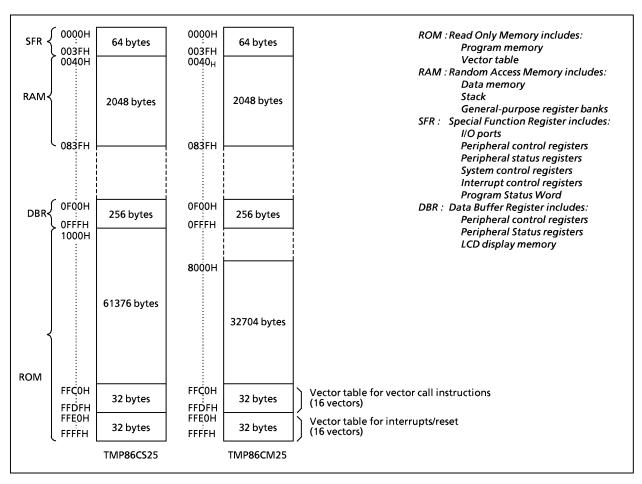


Figure 1-1. Memory Address Maps

#### 1.2 Program Memory (ROM)

The TMP86CM25 has a 32 K×8-bit (address 8000H to FFFFH), and the TMP86CS25 has a 60 K×8-bit (address 1000H to FFFFH) of program memory (mask programmed ROM). However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See 2.5.5 Address Trap).

#### **Electrical Characteristics**

Absolute Maximum Ratings  $(V_{SS} = 0 V)$ 

| Parameter                                  | Symbol             | Pins                                | Rating                         | Unit |
|--|--------------------|-------------------------------------|--------------------------------|------|
| Supply Voltage                             | V <sub>DD</sub>    |                                     | - 0.3 to 6.5                   |      |
| Input Voltage                              | V <sub>IN</sub>    |                                     | - 0.3 to V <sub>DD</sub> + 0.3 | V    |
| Output Voltage                             | V <sub>OUT1</sub>  |                                     | - 0.3 to V <sub>DD</sub> + 0.3 |      |
|  | I <sub>OUT1</sub>  | P6 Port                             | - 1.8                          |      |
| Output Current (Per 1 pin)                 | I <sub>OUT2</sub>  | P1, P2, P34 to P36, P5, P6, P7 Port | 3.2                            | ]    |
|  | I <sub>OUT3</sub>  | P30 to P33 Port                     | 30                             | mA   |
| Output Current (Total)                     | Σl <sub>OUT1</sub> | P1, P2, P34 to P36, P5, P6, P7 Port | 60                             | ]    |
| Output current (Total)                     | Σl <sub>OUT2</sub> | P30 to P33 Port                     | 80                             | ]    |
| Power Dissipation [T <sub>opr</sub> = 85℃] | PD                 |                                     | 350                            | mW   |
| Soldering Temperature (time)               | Tsld               |                                     | 260 (10 s)                     |      |
| Storage Temperature                        | Tstg               |                                     | – 55 to 125                    | °C   |
| Operating Temperature                      | Topr               |                                     | - 40 to 85                     |      |

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant.

Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition

 $(V_{SS} = 0 \text{ V, Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

| Parameter                          | Symbol           | Pins                    | С   | ondition               | Min                  | Max                  | Unit |  |
|------------------------------------|------------------|-------------------------|---|------------------------|----------------------|----------------------|------|--|
|                                    |                  |                         |   | NORMAL1, 2 mode        | 4.5                  |                      |      |  |
|                                    |                  |                         | fc = 16 MHz   IDLE0, 1, 2 mod   |                        | 4.5                  |                      |      |  |
|                                    |                  |                         | fc = 8 MHz  | NORMAL1, 2 mode        | 2.7                  |                      |      |  |
|                                    |                  |                         |   | IDLE0, 1, 2 mode       | 2.7                  |                      |      |  |
| Supply Voltage                     | V <sub>DD</sub>  |                         |   | NORMAL1, 2 mode        |                      | 5.5                  |      |  |
|                                    |                  |                         | fc = 4.2 MHz  | IDLE0, 1, 2 mode       |                      |                      |      |  |
|                                    |                  |                         | fs =  | SLOW1, 2 mode          | 1.8                  |                      |      |  |
|                                    |                  |                         | 32.768 kHz  | SLEEP0, 1, 2 mode      |                      |                      |      |  |
|                                    |                  |                         |   | STOP mode              |                      |                      |      |  |
|                                    | V <sub>IH1</sub> | Except Hysteresis input | $V_{DD} \ge 4.5 V$  |                        | $V_{DD} \times 0.70$ |                      |      |  |
| Input high Level V <sub>IH</sub> ; | V <sub>IH2</sub> | Hysteresis input        |   |                        | $V_{DD} \times 0.75$ | $V_{DD}$             | V    |  |
|                                    | V <sub>IH3</sub> |                         | $V_{DD} < 4.5 V$  |                        | $V_{DD} \times 0.90$ |                      |      |  |
|                                    | V <sub>IL1</sub> | Except Hysteresis input | $\frac{input}{V_{DD}} \geq 4.5V$  |                        |                      | $V_{DD} \times 0.30$ |      |  |
| Input low Level                    | $V_{IL2}$        | Hysteresis input        |   |                        | 0                    | $V_{DD} \times 0.25$ |      |  |
|                                    | V <sub>IL3</sub> |                         | $V_{DD} < 4.5 V$  |                        |                      | $V_{DD} \times 0.10$ |      |  |
|                                    | V1 <sub>IN</sub> | V1                      |   |                        | 1.0                  | 1.375                |      |  |
| LCD reference                      | V2 <sub>IN</sub> | V2                      | LCDCTL1 <ri< td=""><td>EFV &gt; = "1"</td><td>2.0</td><td>2.750</td><td></td></ri<>             | EFV > = "1"            | 2.0                  | 2.750                |      |  |
| voltage range                      | V3 <sub>IN</sub> | V3                      | VDD< V4 (N  | ote 2)                 | 3.0                  | 4.125                |      |  |
| l voltage range                    | V4 <sub>IN</sub> | V4                      |   |                        | 4.0                  | 5.500                |      |  |
|                                    | V4 <sub>IN</sub> | V4 (Note 3)             | LCDCTL1 <ri< td=""><td colspan="2">LCDCTL1 &lt; REFV &gt; = "0"</td><td>VDD</td><td></td></ri<> | LCDCTL1 < REFV > = "0" |                      | VDD                  |      |  |
|                                    |                  |                         | $V_{DD} = 1.8 \text{ to}$   | 5.5 V                  |                      | 4.2                  |      |  |
| Clock Frequency                    | fc               | XIN, XOUT               | V <sub>DD</sub> = 2.7 to 5.5 V  |                        | 1.0                  | 8.0                  | MHz  |  |
| Clock Frequency                    |                  |                         | V <sub>DD</sub> = 4.5 to 5.5 V  |                        |                      | 16.0                 | 1    |  |
|                                    | fs               | XTIN, XTOUT             |   |                        | 30.0                 | 34.0                 | kHz  |  |

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: When LCDCTL1 < REFV > is set to "1", always keep the condition of VDD < V4. Note 3: When LCDCTL1 < REFV > is set to "0", always supply the reference voltage from V4 pin.

DC Characteristics

 $(V_{SS} = 0 \text{ V, Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

| Parameter                           | Symbol           | Pins Condition                         |   | ion         | Min | Тур. | Max | Unit    |    |
|-------------------------------------|------------------|--|---|-------------|-----|------|-----|---------|----|
| Hysteresis Voltage                  | V <sub>HS</sub>  | Hysteresis input                       |   |             | _   | 0.9  | _   | ٧       |    |
|                                     | I <sub>IN1</sub> | TEST                                   |   |             |     |      |     |         |    |
| Input Current                       | I <sub>IN2</sub> | Sink Open Drain, Tri-state             | $V_{DD} = 5.5  V, V_{IN} =$   | 5.5 V/0 V   | _   | -    | ± 2 | μA      |    |
|                                     | I <sub>IN3</sub> | RESET, STOP                            |   |             |     |      |     |         |    |
| Input Resistance                    | R <sub>IN1</sub> | TEST Pull-Down                         |   |             | -   | 70   | _   | kΩ      |    |
| input Resistance                    | R <sub>IN2</sub> | RESET Pull-Up                          |   |             | 100 | 220  | 450 | K32     |    |
| Output Leakage<br>Current           | I <sub>LO</sub>  | Sink Open Drain, Tri-state             | V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub>                             | = 5.5 V/0 V | -   | -    | ± 2 | μA      |    |
| Output High Voltage                 | V <sub>OH2</sub> | Tri-st Port                            | V <sub>DD</sub> = 4.5 V, I <sub>OH</sub> =                            | – 0.7 mA    | 4.1 | -    | -   |         |    |
| Output Low Voltage                  | V <sub>OL</sub>  | Except XOUT and P30 to P33<br>Port     | $V_{DD} = 4.5 \text{ V}, I_{OL} =$                                    | 1.6mA       | -   | -    | 0.4 | V       |    |
| Output Low Current                  | loL              | High Current Port<br>(P30 to P33 Port) | $I V_{DD} = 4.5 \text{ V}, V_{DI} = 1.0 \text{ V}$                    |             | _   | 20   | -   |         |    |
| Supply Current in NORMAL 1, 2 mode  |                  |  | $V_{DD} = 5.5 V$<br>$V_{IN} = 5.3/0.2 V$                              |             | 1   | 4.5  | 7.0 | mA      |    |
| Supply Current in IDLE 0, 1, 2 mode |                  |  | fc = 16 MHz<br>fs = 32.768 kHz  |             | ı   | 2.7  | 3.5 |         |    |
| Supply Current in SLOW 1 mode       |                  |  | V <sub>DD</sub> = 3.0 V   |             | ı   | 6.0  | 25  |         |    |
| Supply Current in SLEEP 1 mode      |                  |  | V <sub>IN</sub> = 2.8 V/0.2 V<br>fs = 32.768 kHz<br>LCD driver is not | TMP86CM25   | ı   | 4.0  | 15  | $\mu$ A |    |
| Supply Current in SLEEP 0 mode      |                  |  | enable.   |             | -   | 2.5  | 13  |         |    |
| Supply Current in STOP mode         | ] .              |  | $V_{DD} = 5.5 V$<br>$V_{IN} = 5.3 V/0.2 V$                            |             | -   | 0.5  | 10  |         |    |
| Supply Current in NORMAL 1, 2 mode  | l <sub>DD</sub>  |  | $V_{DD} = 5.5 \text{ V}$<br>$V_{IN} = 5.3/0.2 \text{ V}$              |             | -   | 6.0  | 7.0 |         |    |
| Supply Current in IDLE 0, 1, 2 mode |                  |  | fc = 16 MHz<br>fs = 32.768 kHz  |             | -   | 4.2  | 5.0 | mA      |    |
| Supply Current in SLOW 1 mode       |                  |  | V <sub>DD</sub> = 3.0 V   |             | ı   | 8.5  | 25  |         |    |
| Supply Current in SLEEP 1 mode      |                  |  | $V_{IN} = 2.8 \text{ V}/0.2 \text{ V}$<br>fs = 32.768 kHz             | TMP86CS25   | -   | 5.0  | 15  | ]       |    |
| Supply Current in SLEEP 0 mode      |                  |  | LCD driver is not enable.   |             |     | _    | 3.0 | 13      | μA |
| Supply Current in STOP mode         |                  |  | $V_{DD} = 5.5 \text{ V}$<br>$V_{IN} = 5.3 \text{ V}/0.2 \text{ V}$    |             | -   | 0.5  | 10  |         |    |

Note 1: Typical values show those at Topr =  $25^{\circ}$ C,  $V_{DD} = 5 \text{ V}$ 

Note 2: Input current ( $I_{IN1}$ ,  $I_{IN2}$ ); The current through pull-up or pull-down resistor is not included.

Note 3: IDD does not include IREF current.

Note 4: The supply currents of SLOW 2 and SLEEP 2 modes are equivalent to IDLE 0, 1, 2.

### **AD Conversion Characteristics**

## $(V_{SS} = 0.0 \text{ V}, 4.5 \text{ V} \le V_{DD} \le 5.5 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$

| Parameter   | Symbol            | Condition   | Min                   | Тур. | Max               | Unit |
|---|-------------------|---|-----------------------|------|-------------------|------|
| Analog Reference Voltage                            | V <sub>AREF</sub> |   | V <sub>DD</sub> – 1.5 | -    | $V_{DD}$          |      |
| Analog Reference Voltage Range (Note 4)             | $\Delta V_{AREF}$ |   | 3.0                   | ı    | _                 | V    |
| Analog Input Voltage                                | V <sub>AIN</sub>  |   | V <sub>SS</sub>       | -    | V <sub>AREF</sub> |      |
| Power Supply Current of<br>Analog Reference Voltage | I <sub>REF</sub>  | $V_{DD} = V_{AREF} = 5.5 \text{ V}$<br>$V_{SS} = 0.0 \text{ V}$ | -                     | 0.6  | 1.0               | mA   |
| Non linearity Error                                 |                   |   | _                     | ı    | ± 1               |      |
| Zero Point Error                                    |                   | $V_{DD} = 5.0 \text{ V}, V_{SS} = 0.0 \text{ V}$                | _                     | -    | ± 1               | LSB  |
| Full Scale Error                                    |                   | V <sub>AREF</sub> = 5.0 V                                       | _                     | -    | ± 1               | 136  |
| Total Error   |                   |   | _                     | -    | ± 2               |      |

## $(V_{SS} = 0.0 \text{ V}, 2.7 \text{ V} \le V_{DD} < 4.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

| Parameter   | Symbol            | Condition   | Min                   | Тур. | Max               | Unit |
|---|-------------------|---|-----------------------|------|-------------------|------|
| Analog Reference Voltage                            | V <sub>AREF</sub> |   | V <sub>DD</sub> – 1.5 | -    | V <sub>DD</sub>   |      |
| Analog Reference Voltage Range (Note 4)             | $\Delta V_{AREF}$ |   | 2.5                   | -    | -                 | \ \  |
| Analog Input Voltage                                | V <sub>AIN</sub>  |   | V <sub>SS</sub>       | -    | V <sub>AREF</sub> |      |
| Power Supply Current of<br>Analog Reference Voltage | I <sub>REF</sub>  | $V_{DD} = V_{AREF} = 4.5 \text{ V}$<br>$V_{SS} = 0.0 \text{ V}$ | -                     | 0.5  | 0.8               | mA   |
| Non linearity Error                                 |                   |   | _                     | -    | ± 1               |      |
| Zero Point Error                                    |                   | $V_{DD} = 2.7 \text{ V}, V_{SS} = 0.0 \text{ V}$                | _                     | -    | ± 1               | LSB  |
| Full Scale Error                                    |                   | $V_{AREF} = 2.7 V$  | _                     | _    | ± 1               | LOB  |
| Total Error   |                   |   | _                     | _    | ± 2               |      |

# (V<sub>SS</sub> = 0.0 V, 2.0 V $\leq$ V<sub>DD</sub> <2.7 V, Topr = -40 to 85°C) Note 5 (V<sub>SS</sub> = 0.0 V, 1.8 V $\leq$ V<sub>DD</sub> <2.0 V, Topr = -10 to 85°C) Note 5

| Parameter   | Symbol            | Condition   | Min                   | Тур. | Max               | Unit |
|---|-------------------|---|-----------------------|------|-------------------|------|
| Analog Reference Voltage                            | V <sub>AREF</sub> |   | V <sub>DD</sub> - 0.9 | -    | V <sub>DD</sub>   |      |
| Analog Reference Voltage Range (Note 4)             | $\Delta V_{AREF}$ | $1.8 \text{ V} \le \text{V}_{DD} < 2.0 \text{ V}$               | 1.8                   | _    | _                 | ] ,, |
| Analog Reference Voltage Range (Note 4)             | △ V AREF          | $2.0 \text{ V} \le \text{V}_{DD} < 2.7 \text{ V}$               | 2.0                   | -    | _                 | V    |
| Analog Input Voltage                                | V <sub>AIN</sub>  |   | V <sub>SS</sub>       | -    | V <sub>AREF</sub> |      |
| Power Supply Current of<br>Analog Reference Voltage | I <sub>REF</sub>  | $V_{DD} = V_{AREF} = 2.7 \text{ V}$<br>$V_{SS} = 0.0 \text{ V}$ | -                     | 0.3  | 0.5               | mA   |
| Non linearity Error                                 |                   |   | _                     | -    | ± 2               |      |
| Zero Point Error                                    |                   | $V_{DD} = 1.8 \text{ V}, V_{SS} = 0.0 \text{ V}$                | _                     | -    | ± 2               | LSB  |
| Full Scale Error                                    |                   | V <sub>AREF</sub> = 1.8 V                                       | _                     | -    | ± 2               | 136  |
| Total Error   |                   |   | _                     | -    | ± 4               |      |

- Note 1: The total error includes all errors except a quantization error, and is defined as maximum deviation from the ideal conversion line.
- Note 2: Conversion time is different in recommended value by power supply voltage.

  About conversion time, please refer to "2.11.2 Register Configuration".
- Note 3: Please use input voltage to AIN input Pin in limit of  $V_{AREF}$   $V_{SS}$ .
  - When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.
- Note 4: Analog Reference Voltage Range:  $\triangle V_{AREF} = V_{AREF} V_{SS}$
- Note 5: When AD is used with  $V_{DD}$  < 2.7 V, the guaranteed temperature range varies with the operating voltage.

## **AC Characteristics**

 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$ 

| Parameter                    | Symbol | Condition                                 | Min   | Тур.  | Max   | Unit |
|------------------------------|--------|---|-------|-------|-------|------|
| Machine Cycle Time           |        | NORMAL 1, 2 mode                          |       |       |       |      |
|                              | +0.4   | IDLE 0, 1, 2 mode 0.25                    |       | _     | 4     |      |
|                              | tcy    | SLOW 1, 2 mode                            | 447.6 | -     | 133.3 | μS   |
|                              |        | SLEEP 0, 1, 2 mode                        | 117.6 |       |       |      |
| High Level Clock Pulse Width | twcH   | For external clock operation (XIN input)  |       |       |       | ns   |
| Low Level Clock Pulse Width  | twcL   | fc = 16 MHz                               | _     | 31.25 | _     | 115  |
| High Level Clock Pulse Width | twcH   | For external clock operation (XTIN input) |       | 15.26 | -     |      |
| Low Level Clock Pulse Width  | twcL   | fc = 32.768 kHz                           | _     |       |       | μS   |

# $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 4.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

| Parameter                    | Symbol | Condition                                 | Min   | Тур.  | Max   | Unit |
|------------------------------|--------|---|-------|-------|-------|------|
|                              |        | NORMAL 1, 2 mode                          |       | -     |       |      |
| Machine Cycle Time           | +0.4   | IDLE 0, 1, 2 mode                         | 0.5   |       | 4     |      |
|                              | tcy    | SLOW 1, 2 mode                            | 447.6 | -     | 133.3 | μS   |
|                              |        | SLEEP 0, 1, 2 mode                        | 117.6 |       |       |      |
| High Level Clock Pulse Width | twcH   | For external clock operation (XIN input)  |       |       |       | ns   |
| Low Level Clock Pulse Width  | twcL   | fc = 8 MHz                                | _     | 62.5  | _     | ''3  |
| High Level Clock Pulse Width | twcH   | For external clock operation (XTIN input) |       | 15.26 | -     | μS   |
| Low Level Clock Pulse Width  | twcL   | fc = 32.768 kHz                           | _     |       |       |      |

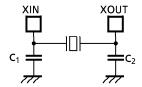
# $(V_{SS} = 0 \text{ V}, V_{DD} = 1.8 \text{ to } 2.7 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

| Parameter                    | Symbol | Condition                                 | Min   | Тур.   | Max   | Unit    |
|------------------------------|--------|---|-------|--------|-------|---------|
|                              |        | NORMAL 1, 2 mode                          |       | -      |       |         |
| Machine Cycle Time           | tor    | IDLE 0, 1, 2 mode                         | 0.95  |        | 4     |         |
|                              | tcy    | SLOW 1, 2 mode                            | 447.6 | _      | 133.3 | $\mu$ S |
|                              |        | SLEEP 0, 1, 2 mode                        | 117.6 |        |       |         |
| High Level Clock Pulse Width | twcH   | For external clock operation (XIN input)  |       |        |       | ns      |
| Low Level Clock Pulse Width  | twcL   | fc = 4.2 MHz                              | _     | 119.05 | -     | 115     |
| High Level Clock Pulse Width | twcH   | For external clock operation (XTIN input) |       | 45.26  |       |         |
| Low Level Clock Pulse Width  | twcL   | fc = 32.768 kHz                           | -     | 15.26  | -     | μS      |

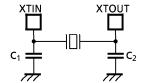
# Timer Counter 1 input (ECIN) Characteristics $(V_{SS} = 0 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$

| Parameter              | Symbol           | Condition   |                   | Min | Тур. | Max   | Unit |
|------------------------|------------------|---|-------------------|-----|------|-------|------|
| TC1 input (ECIN input) | t <sub>TC1</sub> | Frequency measurement mode $V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$ | Single edge count | -   | -    | 1.0   | MHz  |
|                        |                  | Frequency measurement mode $V_{DD} = 2.7 \text{ to } 4.5 \text{ V}$ | Single edge count | I   | I    | 0.5   |      |
|                        |                  | Frequency measurement mode $V_{DD} = 1.8 \text{ to } 2.7 \text{ V}$ | Single edge count | -   | _    | 0.262 |      |

## **Recommended Oscillating Conditions**



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.

Note 2: TOYAMA MURATA MFG. CO., LTD. (JAPAN)

These product numbers and the corresponding specifications are subject to change.

For up-to-date information, please refer to the following URL;

http://www.murata.co.jp/search/index.html