CMOS 4-Bit Microcontroller

# TMP47C222N, TMP47C422N
# TMP47C222F, TMP47C422F
# TMP47C222U, TMP47C422U

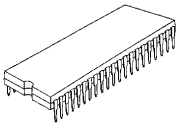
The TMP47C222/422 are high speed and high performance 4-bit single chip micro computers, integrating AD converter, pulse output, zero-cross detector and LCD driver based on the TLCS-470 series.

| Part No. | ROM | RAM | Rackage | OTP |
|---|---|---|---|---|
| TMP47C222N | 2048 × 8-bit | 192 × 4-bit | P-SDIP42-600-1.78 | TMP47P422VN |
| TMP47C222F | | | P-QFP44-1414-0.80D | TMP47P422VF |
| TMP47C222U | | | P-QFP44-1010-0.80 | TMP47P422VU |
| TMP47C422N | 4096 × 8-bit | 256 × 4-bit | P-SDIP42-600-1.78 | TMP47P422VN |
| TMP47C422F | | | P-QFP44-1414-0.80D | TMP47P422VF |
| TMP47C422U | | | P-QFP44-1010-0.80 | TMP47P422VU |

## Features

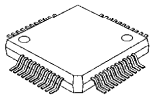
- ◆4-bit single chip microcomputer
- ◆Instruction execution time: 1.0 μs (at 8 MHz)
- ◆Low voltage operation: 2.2 V (at 4.2 MHz)
- ◆92 basic instructions
  - Table look-up instructions
- ◆Subroutine nesting: 15 levels max
- ◆6 interrupt sources (External: 2, Internal: 4)
  All sources have independent latches each, and multiple interrupt control is available.
- ◆I/O port (SDIP: 20 pins, QFP: 22 pins)
- ◆Interval Timer
- ◆Two 12-bit Timer/Counters
  Timer, event counter,and pulse width measurement mode
- ◆Watchdog Timer
- ◆Serial Interface with 8-bit buffer
  - Simultaneous transmission and reception capability
  - 8/4-bit transfer, external/internal clock, and leading/trailing edge shift mode

P-SDIP42-600-1.78



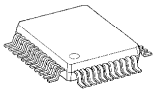
TMP47C222N
TMP47C422N
TMP47P422VN

P-QFP44-1414-0.80D



TMP47C222F
TMP47C422F
TMP47P422VF

P-QFP44-1010-0.80



TMP47C222U
TMP47C422U
TMP47P422VU

000707EBA1

◆8-bit successive approximate type AD converter
- With sample and hold
- 4 analog inputs
- Conversion time: 24 $\mu$s (at 8 MHz)

◆Pulse output
Buzzer drive/Remocon carrier

◆Zero-cross detector

◆LCD driver
- LCD direct drive capability (max 10-digit display at 1/4 duty LCD)
- 1/4, 1/3, 1/2 duties or static drive are programmably selectable.

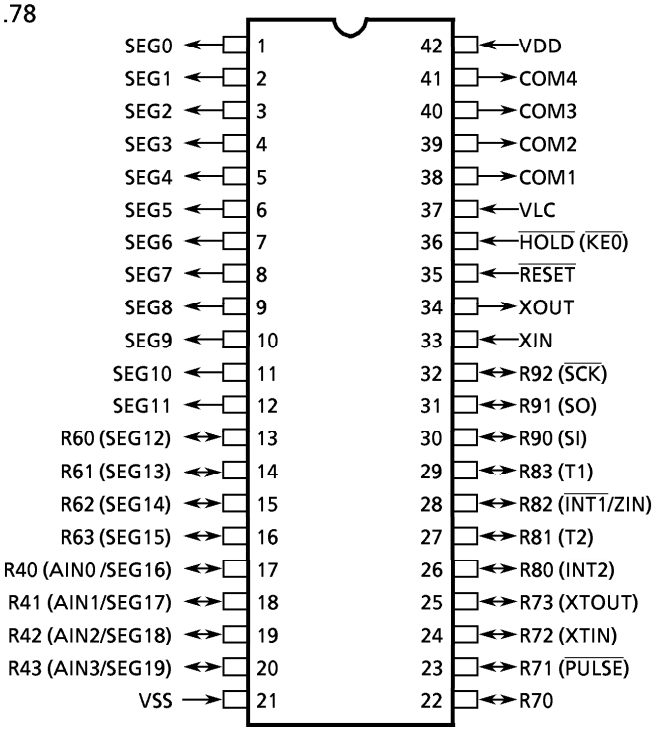
◆Dual-clock operation
High-speed / Low-power-consumption operating mode

◆Hold function
Battery/Capacitor back-up

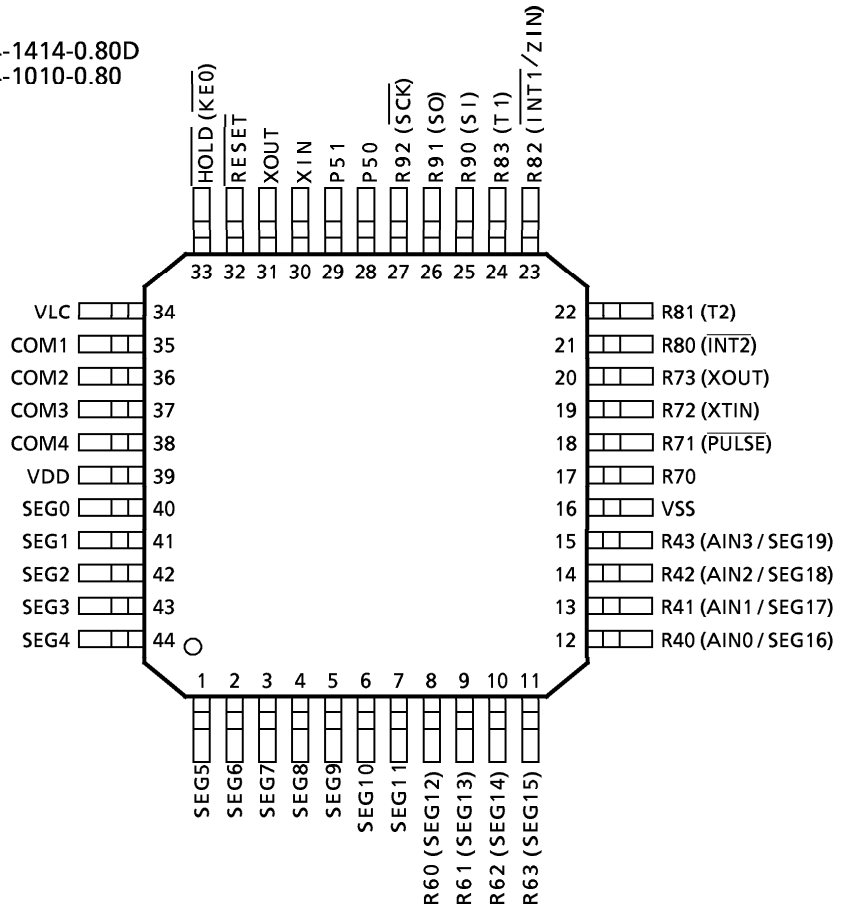
◆Emulation pod: BM47C422

## Pin Assignments (Top View)

P-SDIP42-600-1.78




P-QFP44-1414-0.80D
P-QFP44-1010-0.80



## Pin Function

| Pin Name | Input / Output | Function | |
|---|---|---|---|
| R43 (AIN3/SEG19) to R40 (AIN0/SEG16) | I/O (I /O) | 4-bit I/O ports with latch (P5 port has only 2-bit). These ports can be set, cleared and tested for each bit as specified by L-register indirect addressing bit manipulation instruction. | AD converter analog input / LCD segment drive output |
| P51, P50 | Output | | (Note) |
| R63 (SEG15) to R60 (SEG12) | I/O (Output) | | LCD segment drive output |
| R73 (XTOUT) | I/O (Output) | | Resonator connecting pins (Low-frequency). |
| R72 (XTIN) | I/O (Input) | | |
| R71 ($\overline{\text{PULSE}}$) | I/O (Output) | | Pulse output |
| R70 | I/O | | |
| R83 (T1) | I/O (Input) | 4-bit I/O ports with latch When used as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1". | Timer / Counter1 external input |
| R82 ($\overline{\text{INT1}}$/ZIN) | | | External interrupt1 and zero-cross input |
| R81 (T2) | | | Timer / Counter2 external input |
| R80 ($\overline{\text{INT2}}$) | | | External interrupt2 input |
| R92 ($\overline{\text{SCK}}$) | I/O (I/O) | 3-bit I/O ports with latch When used as input port or serial port, the latch must be set to "1". | Serial clock I/O |
| R91 (SO) | I/O (Output) | | Serial data output |
| R90 (SI) | I/O (Input) | | Serial data input |
| SEG11 to SEG0 | Output | LCD segment drive output | |
| COM4 to COM1 | | LCD Common drive output | |
| XIN | Input | Resonator connecting pins (High-frequency). For inputting external clock, XIN is used and XOUT is opened | |
| XOUT | Output | | |
| $\overline{\text{RESET}}$ | Input | Reset signal input | |
| $\overline{\text{HOLD}}$ ($\overline{\text{KE0}}$) | I/O (Input) | HOLD request/release signal input | sense input |
| VDD (VAREF) | Power Supply | + 5 V | AD converter analog reference voltage |
| VSS (VASS) | | 0 V (GND) | AD converter analog reference voltage (GND) |
| VLC | | LCD drive power supply | |

*Note: TMP47C222/422N (SDIP) do not have port P5.*

## Operational Description

Concerning the TMP47C222/422 the configuration and functions of hardware are described.
The basic instruction of configuration in the TMP47C222/422 is the same as those of TLCS-470 series.

## 1. System Configuration

◆Internal CPU Function
- 2.1 Program Counter (PC)
- 2.2 Program Memory (ROM)
- 2.3 H Register, L Register
- 2.4 Data Memory (RAM)
  - a. Stack,
  - b. Stack Pointer Word (SPW),
  - c. Data Counter (DC)
- 2.5 ALU, Accumulator
- 2.6 Flags
- 2.7 System Clock Controller
- 2.8 Interrupt Controller
- 2.9 Reset Controller
- Watchdog Timer

◆Peripheral Hardware Function
- 3.1 I/O Ports
- 3.2 Interval Timer
- 3.3 Timer/Counters (TC1, TC2)
- 3.4 Pulse output
- 3.5 Zero-cross detector
- 3.6 AD converter
- 3.7 Serial Interface
- 3.8 LCD Driver

## 2. Internal CPU Function

### 2.1 Program Counter (PC)

The program counter is a 12-bit binary counter which indicates the address of the program memory storing the next instruction to be executed. Normally, the PC is incremented by the number of bytes of the instruction every time it is fetched. When a branch instruction or a subroutine instruction has been executed or an interrupt has been accepted, the specified values listed in Table 2-1 are set to the PC. The PC is initialized to "0" during reset. In the TMP47C222/422, the long franch instruction [BSL a] should not be used.

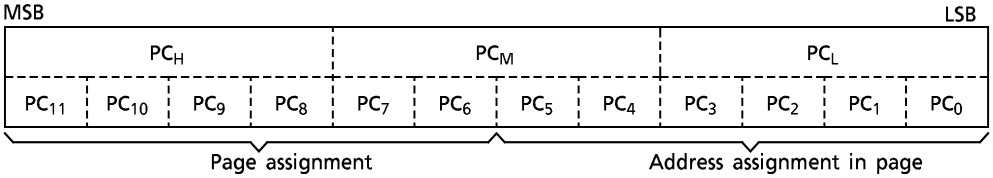



Figure 2-1. Configuration of Program Counter

The PC can directly address a 4096-byte address space. However, with the short branch and subroutine call instructions, the following points must be considered In the TMP47C222/422, the long branch instruction [BSL a] should not be used.

(1) Short branch instruction [BSS a]
In [BSS a] instruction execution, when the branch condition is satisfied, the value specified in the instruction is set to the lower 6 bits of the PC. That is, [BSS a] becomes the in-page branch instruction. When [BSS a] is stored at the last address of the page, the upper 6 bits of the PC point the next page, so that branch is made to the next page.

(2) Subroutine call instruction [CALL a]
In [CALL a] instruction execution, the contents of the PC are saved to the stack then the value specified in the instruction is set to the PC. The address which can be specified by the instruction consists of 11 bits and the most significant bit of the PC is always "0". Therefore, the entry address of the subroutine should be within an addrress range of $000_H$ through $7FF_H$.

Table 2-1. Status Change of Program Counter

| Instruction or Operation | | Condition | | Program Counter (PC) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $PC_{11}$ | $PC_{10}$ | $PC_9$ | $PC_8$ | $PC_7$ | $PC_6$ | $PC_5$ | $PC_4$ | $PC_3$ | $PC_2$ | $PC_1$ | $PC_0$ |
| Execution of Instruction | BS a | SF = 1 (Branch condition is satisfied) | | Immediate data specified by the instruction | | | | | | | | | | | |
| | | SF = 0 (Branch condition is not satisfied) | | + 2 | | | | | | | | | | | |
| | BSS a | SF = 1 | Lower 6-bit address ≠ 111111 | Hold | | | | Immediate data specified by the instruction | | | | | | | |
| | | | Lower 6-bit address = 111111 (last address in page) | + 1 | | | | Immediate data specified by the instruction | | | | | | | |
| | | SF = 0 | | + 1 | | | | | | | | | | | |
| | CALL a | | | 0 | Immediate data specified by the instruction | | | | | | | | | | |
| | CALLS a | | | 0 | 0 | 0 | 0 | The data generated by the immediate data specified by the instruction | | | | | 1 | 1 | 0 |
| | RET | | | The return address restored from stack | | | | | | | | | | | |
| | RETI | | | The return address restored from stack | | | | | | | | | | | |
| | Others | | | Incremented by the number of bytes in the instruction | | | | | | | | | | | |
| Interrupt acceptance | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Interrupt vector | | | 0 |
| Reset | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## 2.2 Program Memory (ROM)

Programs and fixed data are stored in the program memory. The instruction to be executed next is read from the address indicated by the contents of the PC.

The fixed data can be read by using the table look-up instructions.

- Table look-up instructions

  [LDL A, @DC], [LDH A, @DC + ]

  The table look-up instructions read the lower and upper 4 bits of the fixed data stored at the address specified in the data counter (DC) to place them into the accumulator. [LDL A, @DC] instruction reads the lower 4 bits of fixed data, and [LDH A, @DC + ] instruction reads the upper 4 bits.

  The DC is a 12-bit register, allowing it to address the entire program memory space.

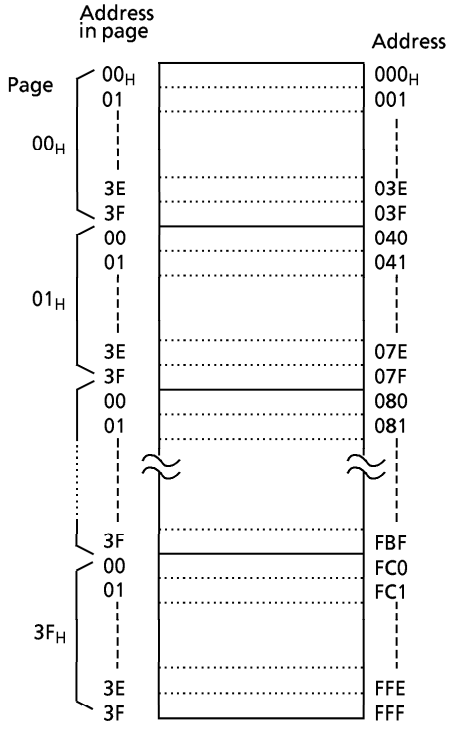



Figure 2-2. Configuration of Program Meory

### 2.2.1 Program Memory Capacity

Figure 2-3 shows the program memory map. Address $000_H$ to $086_H$ of the program memory are also used for special purposes.

### 2.2.2 Program Memory Map

The TMP47C222 has 2048 × 8 bits (addresses $000_H$ to $7FF_H$) of program memory (mask ROM), the TMP47C422 has 4096 × 8 bits (addresses $000_H$ to $FFF_H$).

On the TMP47C222, no physical program memory exists in the address range $800_H$ to $FFF_H$. However, if this space is accessed by program, the most significant bit of each address is always regarded as "0" and the contents of the program memory corresponding to the address $000_H$ to $7FF_H$ are read.

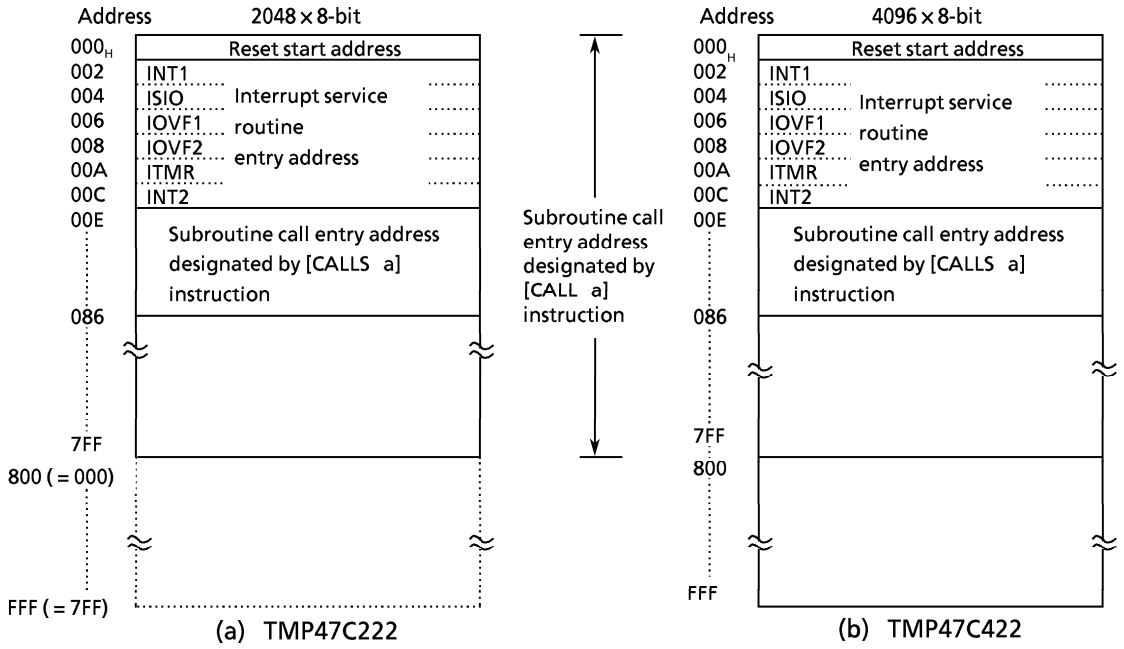



Figure 2-3. Program Memory Map

## 2.3 H Register and L Register

The H register and the L register are 4-bit general registers. They are also used as a register pair (HL) for the data memory (RAM) addressing pointer. The RAM consists of pages, each page being 16 words long (1 word = 4 bits). The H register specifies a page and the L register specifies an address in the page.

The L register has the auto-post-increment/decrement capability, implementing the execution of composite instructions. For example, [ST A, @HL + ] instruction automatically increments the contents of the L register after data transfer.

During the execution of [SET @L], [CLR @L], or [TEST @L] instructions, the L register is also used to specify the bits corresponding to I/O port pins R73 through R40 (the indirect addressing of port bits by the L register).

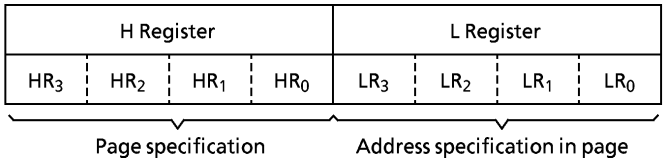



Figure 2-4. Configuration of H and L Registers

## Electrical Characteristics

### Absolute Maximum Ratings ($V_{SS}$ = 0 V)

| Parameter | Symbol | Pins | Ratings | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | – 0.3 to 6.5 | V |
| Input Voltage | $V_{IN}$ | | – 0.3 to $V_{DD}$ + 0.3 | V |
| Output Voltage | $V_{OUT}$ | | – 0.3 to $V_{DD}$ + 0.3 | V |
| Output Current (Per 1 pin) | $I_{OUT1}$ | Port R4, R7 | 30 | mA |
| | $I_{OUT2}$ | Port R5, R6, R8, R9 | 3.2 | |
| Power Dissipation [Topr = 70°C] | $ZI_{OUT1}$ | Port R4, R7 | 120 | mW |
| | PD | | 400 | |
| Soldering Temperature (time) | Tsld | | 260 (10 s) | °C |
| Storage Temperature | Tstg | | – 55 to 125 | °C |
| Operating Temperature | Topr | | – 30 to 70 | °C |

*Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.*

### Recommended Operating Conditions ($V_{SS}$ = 0 V, Topr = – 30 to 70°C)

| Parameter | Symbol | Pins | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | fc = 8.0 MHz | 2.7 | 5.5 | V |
| | | | fc = 4.2 MHz | 2.2 | | |
| | | | In the SLOW mode | 2.2 | | |
| | | | In the HOLD mode | 2.0 | | |
| Input High Voltage | $V_{IH1}$ | Except Hysteresis Input | In the normal operating area | $V_{DD}$ × 0.7 | $V_{DD}$ | V |
| | $V_{IH2}$ | Hysteresis Input | | $V_{DD}$ × 0.75 | | |
| | $V_{IH3}$ | | In the HOLD mode | $V_{DD}$ × 0.9 | | |
| Input Low Voltage | $V_{IL1}$ | Except Hysteresis Input | In the normal operating area | 0 | $V_{DD}$ × 0.3 | V |
| | $V_{IL2}$ | Hysteresis Input | | | $V_{DD}$ × 0.25 | |
| | $V_{IL3}$ | | In the HOLD mode | | $V_{DD}$ × 0.1 | |
| Clock Frequency | fc | XIN, XOUT | $V_{DD}$ = 2.7 to 5.5 V | 0.4 | 8.0 | MHz |
| | | | $V_{DD}$ = 2.2 to 5.5 V | | 4.2 | |
| | | | In the RC oscillation | | 2.5 | |
| | fs | XTIN, XTOUT | $V_{DD}$ = 2.2 to 5.5 V | 30 | 34 | |

*Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.*

DC Characteristics ($V_{SS}$ = 0 V, Topr = – 30 to 70°C)

| Parameter | Symbol | Pins | Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Hysteresis Voltage | $V_{HS}$ | Hysteresis Input | | – | 0.7 | – | V |
| Input Current | $I_{IN1}$ | $\overline{RESET}$, $\overline{HOLD}$ | $V_{DD}$ = 5.5 V, $V_{IN}$ = 5.5V / 0V | – | – | ± 2 | μA |
| | $I_{IN2}$ | Open drain output ports | | | | | |
| Input Resistance | $R_{IN}$ | $\overline{RESET}$ | | 100 | 220 | 450 | kΩ |
| Output Leakage Current | $I_{LO}$ | Open drain output ports | $V_{DD}$ = 5.5 V, $V_{OUT}$ = 5.5 V | – | – | 2 | μA |
| Output Low Current | $I_{OL}$ | Port R4, R7 | $V_{DD}$ = 4.5 V, $V_{OL}$ = 1.0 V | 7 | 10 | – | mA |
| Output Low Voltage | $V_{OL}$ | Port P5, R6, R8, R9 | $V_{DD}$ = 4.5 V, $I_{OL}$ = 1.6 mA | – | – | 0.4 | V |
| | | | $V_{DD}$ = 2.2 V, $I_{OL}$ = 20 μA | – | – | 0.1 | |
| Segment Output Low Resistance | $R_{OS1}$ | SEG pin | $V_{DD}$ = 5 V, $V_{DD}$ – $V_{LC}$ = 3 V | — | 10 or 20 | — | kΩ |
| Common Output Low Resistance | $R_{OC1}$ | COM pin | | | | | |
| Segment Output High Resistance | $R_{OS2}$ | SEG pin | | — | 70 or 200 | — | kΩ |
| Common Output High Resistance | $R_{OC2}$ | COM pin | | | | | |
| Segment/Common Output Registance | $V_{O2/3}$ | SEG / COM pin | | 3.8 | 4.0 | 4.2 | V |
| | $V_{O1/2}$ | | | 3.3 | 3.5 | 3.7 | |
| | $V_{O1/3}$ | | | 2.8 | 3.0 | 3.2 | |
| Supply Current (in the Normal mode) | $I_{DD}$ | | $V_{DD}$ = 5.5 V, fc = 4 MHz | – | 2 | 4 | mA |
| | | | $V_{DD}$ = 3.0 V, fc = 4 MHz | – | 1 | 2 | |
| | | | $V_{DD}$ = 3.0 V, fc = 400 kHz | – | 0.5 | 1 | |
| Supply Current (in the SLOW mode) | $I_{DDS}$ | | $V_{DD}$ = 3.0 V, fs = 32.768 kHz | – | 20 | 40 | μA |
| Supply Current (in the HOLD mode) | $I_{DDH}$ | | $V_{DD}$ = 5.5 V | – | 0.5 | 10 | μA |

*Note 1: Typ. values show those at Topr = 25°C, $V_{DD}$ = 5 V.*

*Note 2: Input Current $I_{IN1}$: The current through resistor is not included.*

*Note 3: Output Resistance $R_{os}$, $R_{oc}$ ; Shows on-resistance at the level switching.*

*Note 4: $V_{O2/3}$ ; Shows 2/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.*
*$V_{O1/2}$ ; Shows 1/2 level output voltage, when the 1/2 duty or static LCD is used.*
*$V_{O1/3}$ ; Shows 1/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.*

*Note 5: Supply Current $I_{DD}$, $I_{DDH}$: $V_{IN}$ = 5.3 V / 0.2 V ($V_{DD}$ = 5.5 V), 2.8 V / 0.2 V ($V_{DD}$ = 3.0 V)*
*Supply Current $I_{DDS}$ ; $V_{IN}$ = 2.8 V / 0.2 V. Low frequency clock is only osillated .*

*Note 6: When using LCD, it is necessary to consider values of Ros 1/2 and Roc 1/2.*

*Note 7: Times fou SEG/COM output switching on ; Ros1, Roc1: 2/fc (s)*
*Ros2, Roc2: 1/(n · $f_F$) (1/n ; duty, $f_{F:\ frame\ frequency}$)*

## AD Conversion Characteristics

(Topr = – 30 to 70°C)

| Parameter | Symbol | Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Analog Reference Voltage Range | $\Delta V_{AREF}$ | $V_{DD} - V_{SS}$ | 2.7 | – | – | V |
| Analog Input Voltage | $V_{AIN}$ | | $V_{SS}$ | – | $V_{DD}$ | V |
| Analog Supply current | $I_{REF}$ | | – | 0.5 | 1.0 | mA |
| Nonlinearity Error | | $V_{DD}$ = 2.7 V to 5.5 V<br>$V_{SS}$ = ± 0.000 V | – | – | ± 1 | LSB |
| Zero Point Error | | | – | – | ± 1 | |
| Full Scale Error | | | – | – | ± 1 | |
| Total Error | | | – | – | ± 2 | |

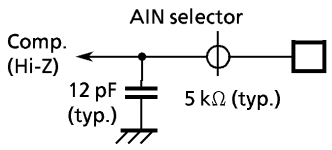
## AC Characteristics

($V_{SS}$ = 0 V, Topr = – 30 to 70°C)

| Parameter | Symbol | Conditions | | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Instruction Cycle Time | tcy | In the normal mode | $V_{DD}$ = 2.7 to 5.5V | 1.0 | – | 20 | μs |
| | | | $V_{DD}$ = 2.2 to 5.5V | 1.9 | | | |
| | | | RC oscillation | 3.2 | | | |
| | | In the SLOW mode | | 235 | | 267 | |
| High level clock pulse width | $t_{WCH}$ | For external clock (XIN input) | $V_{DD} \geqq 2.7$ V | 60 | – | – | ns |
| | | | $V_{DD} < 2.7$ V | 120 | | | |
| Low level clock pulse width | $t_{WCL}$ | | $V_{DD} \geqq 2.7$ V | 60 | | | |
| | | | $V_{DD} < 2.7$ V | 120 | | | |
| AD Conversion Time | $t_{ADC}$ | | | – | 24 tcy | – | μs |
| AD Sampling Time | $t_{AIN}$ | | | – | 2 tcy | – | |
| Shift data Hold Time | $t_{SDH}$ | | | 0.5 tcy – 0.3 | – | – | μs |

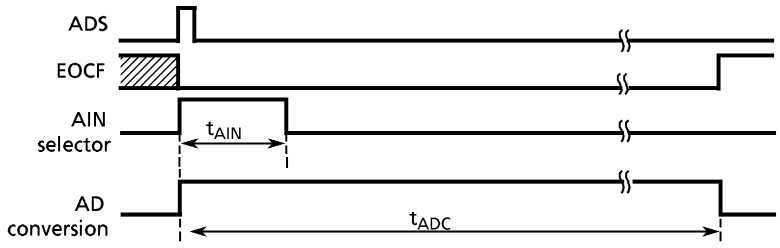
*Note 1: AD conversion timing:*

*Internal circuit for pins AIN0 to 7*

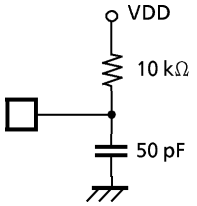



* Electrical change inust be loaded into the buit-in condensen during $t_{AIN}$ for normal AD conversion.

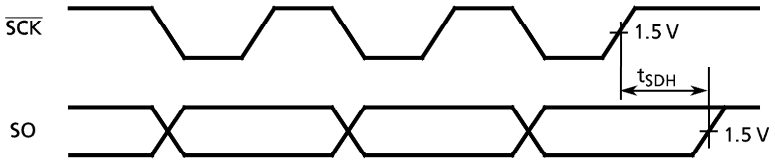
AD conversion timing



*Note 2: Shift data Hold Time:*
*External circuit for pins* $\overline{SCK}$ *and SO*



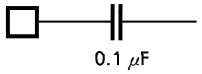

Serial port (completed of transmission)

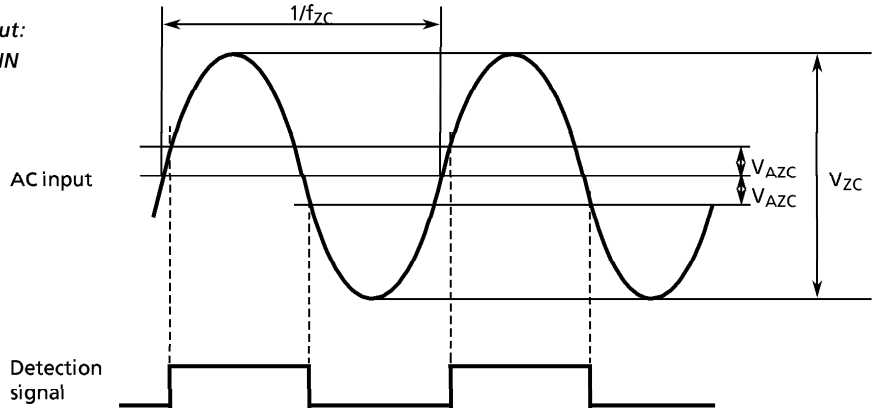



**Zero-Cross Detection Characteristics** (Vss = 0V, Topr = − 30 to 70℃)

| Parameter | Symbol | Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Zero-cross Input Voltage | $V_{ZC}$ | AC coupling (C = 0.1 μF) | 1.0 | — | 3.0 | $V_{P-P}$ |
| Zero-cross Accuracy | $V_{AZC}$ | $f_{ZC}$ = 50 to 60 Hz (sine curve) | — | — | ± 135 | mV |
| Zero-cross input frequensy | $f_{ZC}$ | | 40 | — | 1000 | Hz |

*Note 3: Zero-cross detection input:*
*External circuit for pin ZIN*

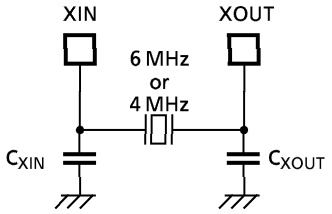


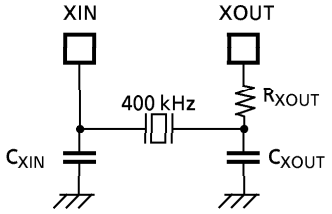



Recommended Oscillating Conditions ($V_{SS}$ = 0 V, $V_{DD}$ = 2.2 to 5.5 V, Topr = – 30 to 70°C)

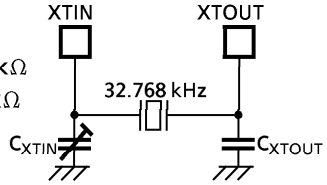
(1) 6 MHz
Ceramic Resonator
CSA6.00MGU (MURATA) $C_{XIN} = C_{XOUT}$ = 30 pF
KBR-6.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30 pF
EFOEC6004A4 (NATIONAL) $C_{XIN} = C_{XOUT}$ = 30 pF

(2) 4 MHz
Ceramic Resonator
CSA4.00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30 pF
KBR-4.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30 pF
EFOEC4004A4 (NATIONAL) $C_{XIN} = C_{XOUT}$ = 30 pF
Crystal Oscillator
204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20 pF



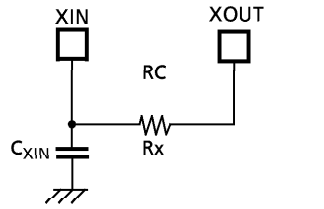




(3) 400 kHz
Ceramic Resonator
CSB400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220 pF, $R_{XOUT}$ = 6.8 kΩ
KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100 pF, $R_{XOUT}$ = 10 kΩ
EFOA400K04B (NATIONAL) $C_{XIN} = C_{XOUT}$ = 470 pF, $R_{XOUT}$ = 0 Ω




(4) 32.768 kHz
Crystal Oscillator $C_{XTIN}$, $C_{XTOUT}$ ; 10 to 33 pF (Note)

(5) RC Oscillation ($V_{SS}$ = 0 V, $V_{DD}$ = 5.0 V, $T_{opr}$ = 25°C)
2 MHz (Typ.) $C_{XIN}$ = 33 pF, $R_X$ = 10 kΩ
400 kHz (Typ.) $C_{XIN}$ = 100 pF, $R_X$ = 30 kΩ




*Note: In order to get the accurate oscillation frequency, the adjustment of capacitors must be required.*

## Typical Characteristics