SIEMENS

Smart Power Stepper Motor with Diagnostic Interface

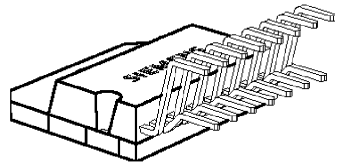
TLE 5250

Preliminary Data

SPT-IC

Features

- Single phase driver for stepper motor 2.5 A
- Low ON-resistance (typical 0.35 Ω)
- Short circuit protection
- Under voltage shutdown
- Overtemperature shutdown
- Serial diagnostic interface
- Fast freewheeling diodes
- Fast nominal/actual comparator for micro stepper mode
- Wide temperature range
- Wide supply range 6 V to 45 V
- TTL-compatible inputs



P-SIP-15-1

	Type	Ordering Code	Package
▼	TLE 5250	Q67000-A9103	P-SIP-15-1

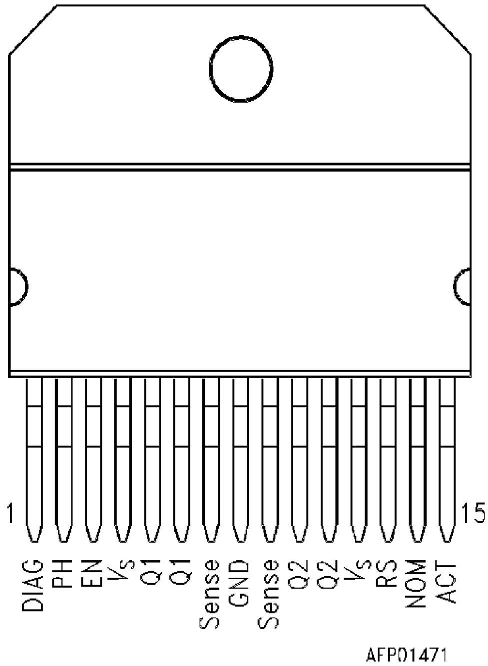
▼ New type

Functional Description

TLE 5250 is a monolithic IC in Smart Power technology for controlling and regulating the motor current in one phase of a bipolar stepping motor. There are other applications in driving DC motors and inductive loads that are operated on constant current.

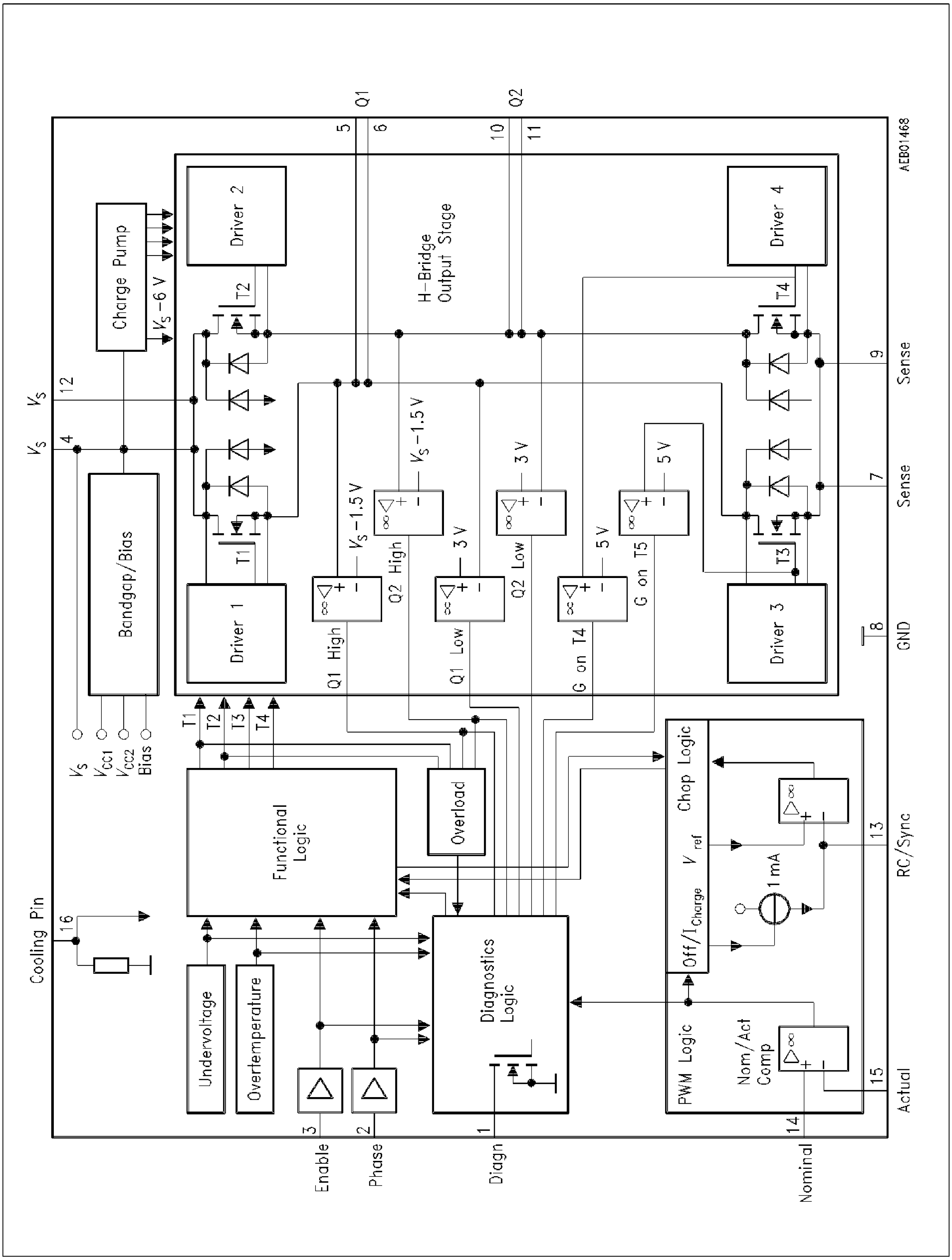
The device has TTL-compatible logic inputs, includes a H-bridge with integrated, fast free-wheeling diodes plus dynamic limiting of the motor current by a chopper mode. The nominal current can be set continuously by a control voltage. Microstep mode can be produced by applying a sinusoidal control voltage. Two TLE 5250s, with a minimum of external circuitry and a single supply voltage, form a complete system - that can be driven direct by an MC - for two-phase, bipolar stepping motors with output current of up to 2.5 A per phase. The outputs of the IC are internally protected against shorted to ground, supply voltage and shorted load. The output stages are also disabled by undervoltage and overtemperature. All fault functions can be detected by the internal diagnostics, which can be read out serially.

Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	DIAG	Open-drain diagnostics output
2	PH	Input for determining source/sink on outputs Q1 and Q2; when Enable = Low, this pin serves as clock input for reading out diagnostics
3	EN	Input for activating or turning off device (all output transistors turned off); Enable High = output active, Enable Low = diagnostics
4, 12	V_S	Supply voltage of IC
5, 6	Q1	Power output with integrated free-wheeling diodes
7, 9	Sense	Actual-current output: shared, open-source output of sink transistors
8	GND	Ground
10, 11	Q2	Power output with integrated free-wheeling diodes
13	RS	Determines turning back on of sink transistor by internally driven, external RC element or external TTL trigger signal
14	NOM	Input for reference potential (nominal current) for nominal/actual comparator
15	ACT	Input for actual current for nominal/actual comparator



Block Diagram

1 Application

Two TLE 5250 drivers are required to operate a bipolar stepping motor. To implement full-step operation, a squarewave voltage with the required stepping frequency is applied to the phase input of the upper driver, and the same squarewave voltage, but offset in phase by 90°el, to the phase input of the lower driver. Motor-current limiting is produced by a DC signal that is applied to both nominal-current inputs. In microstep operation the nominal current tracks sinusoidally and synchronously with the required stepping frequency. This produces a sinusoidal current in the motor windings to ensure very smooth running and a high stepping frequency. If an instantaneous nominal value (sine or cosine) is held on the second driver, it is possible to set a certain angle of rotation while the motor is stationary. The motor current produced by this depends on nominal voltage and sense resistance (normally 0.5 Ω), i.e.

$$I_{\mathrm{M}}[\mathrm{V}] = \frac{V_{\mathrm{nom}}[\mathrm{V}]}{R_{\mathrm{S}}[\Omega]}$$

The actual voltage should be thoroughly filtered for precise current regulation, especially in microstep operation. So the actual input is accessible, and an RC element is necessary between the Sense output and Actual input. The resistance R_{R} should correspond to the internal resistance of the nominal-current input-voltage source to prevent additional voltage offset on the nominal/actual comparator.

Circuit Description

Outputs

Outputs Q1 and Q2 are fed by push-pull output stages. Four integrated free-wheeling diodes referred to ground or the supply voltage protect the integrated circuit against reverse voltages from an inductive load.

Enable and Phase

Outputs Q1 and Q2 can be disabled by a voltage V_{Inh} of ≤ 0.8 V on the Enable pin. The sink transistors are enabled by $V_{\mathrm{Inh}} \geq 2$ V.

The voltage on the Phase input determines the phase of the output current. Output Q1 acts as a sink for $V_{\mathrm{Ph}} \leq 0.8$ V and as a source for $V_{\mathrm{Ph}} \geq 2$ V.

For output Q2 this is reversed: sink for $V_{\mathrm{Ph}} \geq 2$ V and source for $V_{\mathrm{Ph}} \leq 0.8$ V.

The sink transistors are chopped. Low signal on the Enable pin plus a clock signal on the Phase pin enable readout of the multiplexer.

Nominal-Current Input

The peak current in the motor winding is defined by the voltage on the Nominal input. This is compared by a fast comparator to the voltage drop on the actual-current sensor. If the nominal current is exceeded, the sink transistors of the outputs are turned off by the logic.

RC/Sync Input

The outputs are turned on by the signal applied to the RC input. Synchronization is possible by TTL signal or chopper mode with an external RC combination.

Chopper Mode

After the supply voltage is applied, capacitor CT is charged with constant current of 1 mA. A regulator limits the maximum voltage on the capacitor to 2.3 V. As a result of the rising current in the motor winding, the voltage on the actual sensor increases. Once the value defined by the nominal-current input is exceeded, the fast comparator resets an RS flipflop. Thus sink transistors T3 and T4 are turned off by the logic. The charge current is turned off and the parallel RT discharges CT.

The internal logic is designed so that capacitor CT is always charged before the discharge operation is triggered. This guarantees a constant charge time, even for very small coil currents (**see Diagram 1**).

Sync Operation

If a sync signal with TTL level is applied to the RC input, the negative edge will set the RS flipflop - by way of the combined Schmitt trigger and monoflop - if the voltage on the current sensor is smaller than the nominal value on the nominal-current input. As in chopper mode, the appropriate output transistors conduct. They are again turned off by resetting the RS flipflop when the voltage on the current sensor becomes greater than the nominal value (**see Diagram 2**).

Output-Stage Control

This part of the circuit handles turn-off of the output stages when the output is shorted to ground. There is separate current monitoring for this purpose in the source transistors. The temperature of the output stages is also monitored. If this exceeds 175 °C, all output stages are turned off, and then turned on again when the temperature drops. Undervoltage also causes turn-off of the transistors in the output stages. These possible fault states are stored in the diagnostics register.

Diagnostics

The information from the different parts of the circuit is collected in the diagnostics and stored in the fault logic. The information is read out on the Diagnostics output (open collector).

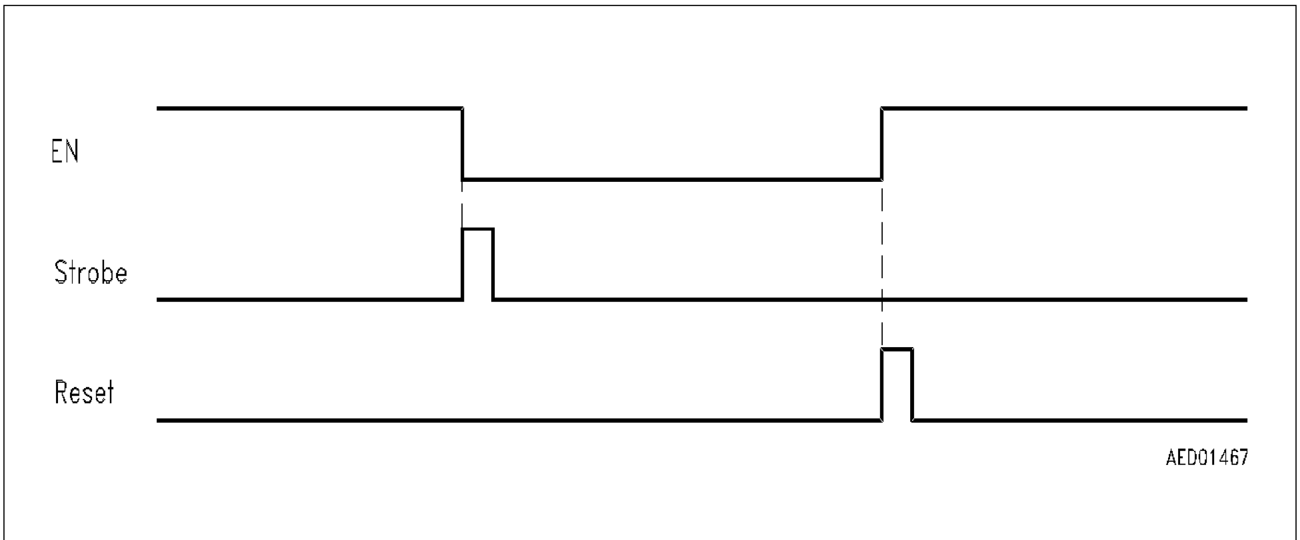
The fault logic consists of a 16-bit multiplexer that switches information in three categories through to the Diagnostics output.

Bit 0 always appears inverted on DIAG when EN is High. This means that, if there is overcurrent on the upper transistor, undervoltage or overtemperature, it will be signaled immediately on the Diagnostics output. DIAG changes from High to Low.

Bit 1: check bit.

Bits 2, 3, 4 and 5 indicate the momentary status of the comparators on the two outputs (**see Block Diagram**). Changes in the status of the comparators for output monitoring can be observed on DIAG when EN is Low and the counter of the multiplexer is on 2, 3, 4 or 5. This is necessary for detecting underload.

Bits 6, 7, 8, 9
The monoflop generates a short strobe signal when the EN edge changes from High to Low. The status of the comparators for output monitoring is stored with this signal and can be read out in bits 6, 7, 8 and 9.
When Enable is Low, the Phase input is used as a clock input. As the edge rises, an internal counter is incremented and the corresponding channel of the multiplexer is switched through. As the edge falls, the signal is output inverted. When Enable is High, the counter is reset to zero.



Bits 10, 11
With these bits it is possible to detect the status of the gate voltages of the lower output-stage transistors T3 and T4. Bit 10: status for EN edge transition. Bit 11: whether the lower transistor has at all been turned on.

Bit 12 indicates whether the nominal/actual comparator has switched. The comparator switches when the output current is regulated.

Bits 13, 14, 15
These bits indicate the presence of overcurrent, undervoltage or overtemperature. A fault is ORed and output direct by bit 0 on DI.

When the multiplexer is read out, bits 0 through 15 are output once non-inverted (Phase = Low) and once inverted (Phase = High).

Bit Assignment in Error Register

Bit 0	=	High for overtemperature/undervoltage/overcurrent
Bit 1	=	always High
Bit 2	=	High when sink transistor Q1 turned on
Bit 3	=	High when sink transistor Q2 turned on
Bit 4	=	High when source transistor Q1 turned on
Bit 5	=	High when source transistor Q2 turned on
Bits 2-5	=	momentary states for readout
Bit 6	=	bit 2 state for falling edge of Enable signal
Bit 7	=	bit 3 state for falling edge of Enable signal
Bit 8	=	bit 4 state for falling edge of Enable signal
Bit 9	=	bit 5 state for falling edge of Enable signal
Bits 6-10		represent status of outputs for negative change in edge of Enable signal
Bit 11	=	High if gate-source voltage of sink transistors is > 5 V at moment of readout
Bits 11-15		are set if event occurs during switching (Enable = High)
Bit 11	=	High if sink transistor V_{GS} > 5 V
Bit 12	=	High if actual current lower than nominal current
Bit 13	=	High if overcurrent detected on source transistors
Bit 14	=	High if undervoltage detected
Bit 15	=	High if thermal link tripped

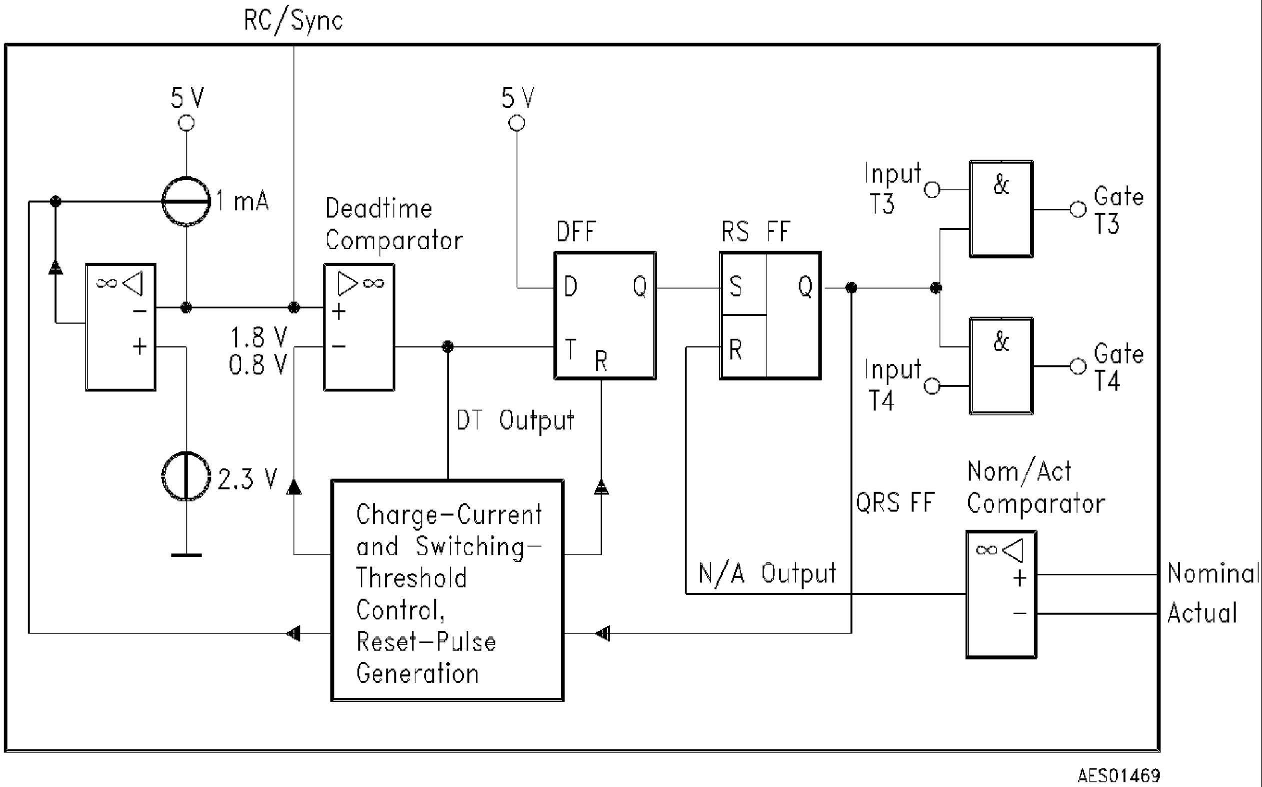
The memories are erased by a rising edge on the Enable input.

Logic Assignment: Control Inputs, Output Transistors

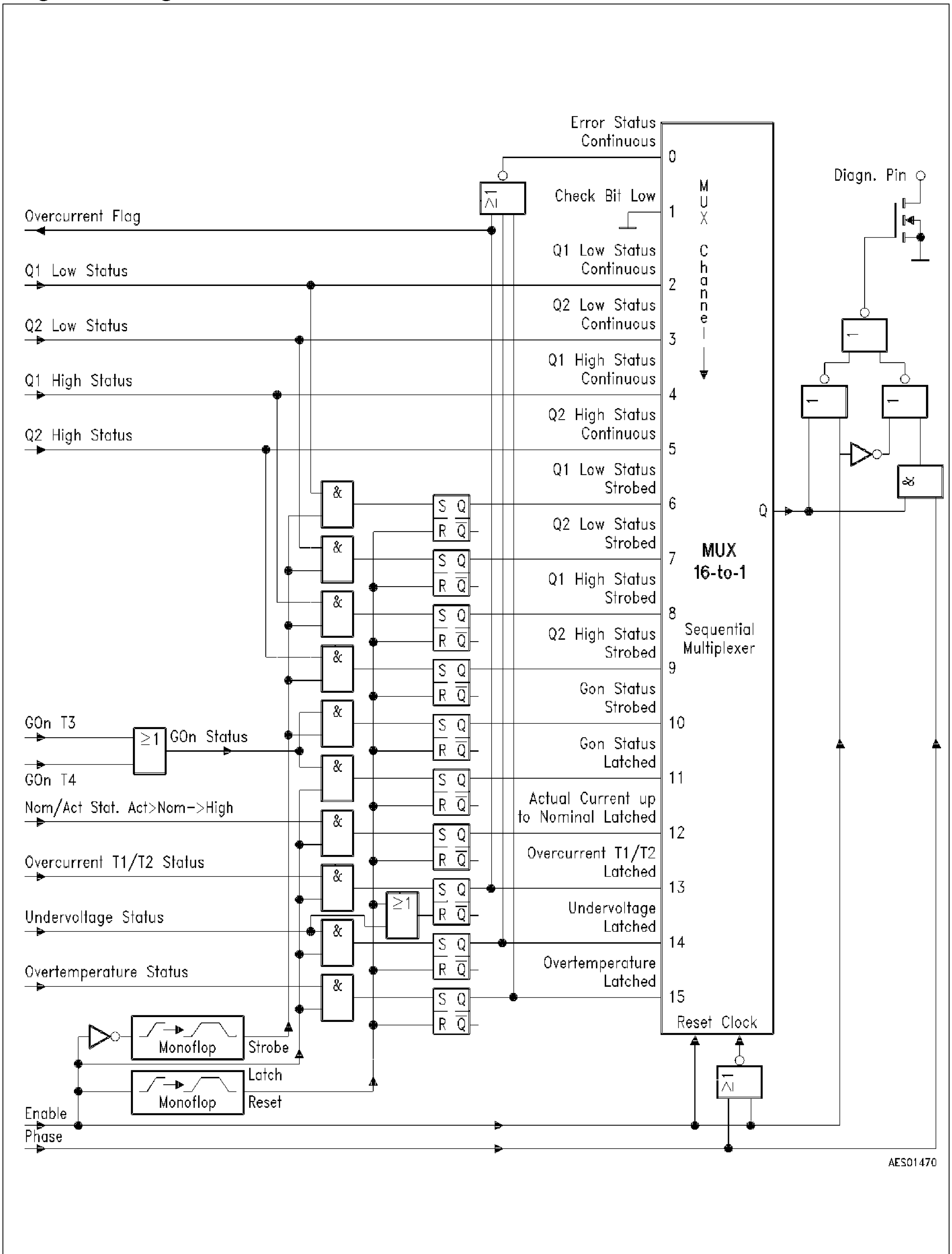
Enable	L	L	H	H
Phase	L	H	L	H
Output Q1	/	/	L	H
Output Q2	/	/	H	L
Transistor T1 Transistor T2 Transistor T3 Transistor T4	X X X X	X X X X	X – – X	– X X –

L = Low voltage level, input open
H = High voltage level
X = transistor turned off
– = transistor conducting
– = transistor conducting, switched in current limiting
/ = output high-impedance

PWM Logic


RC/Sync
5 V
1 mA
Deadtime
Comparator
5 V
DFF
D
Q
T
R
RS FF
S
Q
R
Input
T3
&
Gate
T3
Input
T4
&
Gate
T4
1.8 V
0.8 V
DT Output
2.3 V
Charge-Current
and Switching-
Threshold
Control,
Reset-Pulse
Generation
QRS FF
Nom/Act
Comparator
N/A Output
Nominal
Actual
AES01469

Diagnostics Logic



Absolute Maximum Ratings
T_J = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	– 0.3	45	V
Supply current	I_S	0	3	A
Peak currents on outputs	I_Q	– 3	3	A
Diode Forward Currents				
Diode to + V_S	I_{FH}		3	A
Diode to Sense	I_{FL}		3	A
Output current on actual-current pin	I_{Act}		3	A
Voltage on actual-current pin	V_{Act}	– 0.3	5	V
Ground current, pin 6	I_{GND}		3	A
Chip temperature	T_C	– 40	150	°C
Storage temperature	T_{stg}		125	°C
Thermal Resistances				
System-air	R_{thSA}		70	K/W
System-case	R_{thSC}		3	K/W

Operating Range

Parameter	Symbol	min.	max.	Unit
Supply voltage	V_S	6	40	V
Input voltage Enable, Phase, RC/Sync	V_I	– 0.3	5.5	V
Voltage on Nominal pin	V_{NOM}	– 0.3	2	V
Voltage on Actual pin	V_{ACT}		2	V
Output current Q1, Q2	I_Q	– 2.5	2.5	A
Chip temperature	T_J	– 40	150	°C
Enable and Phase Inputs				
H input voltage	V_{IH}	2		V
L input voltage	V_{IL}		0.8	V

Characteristics

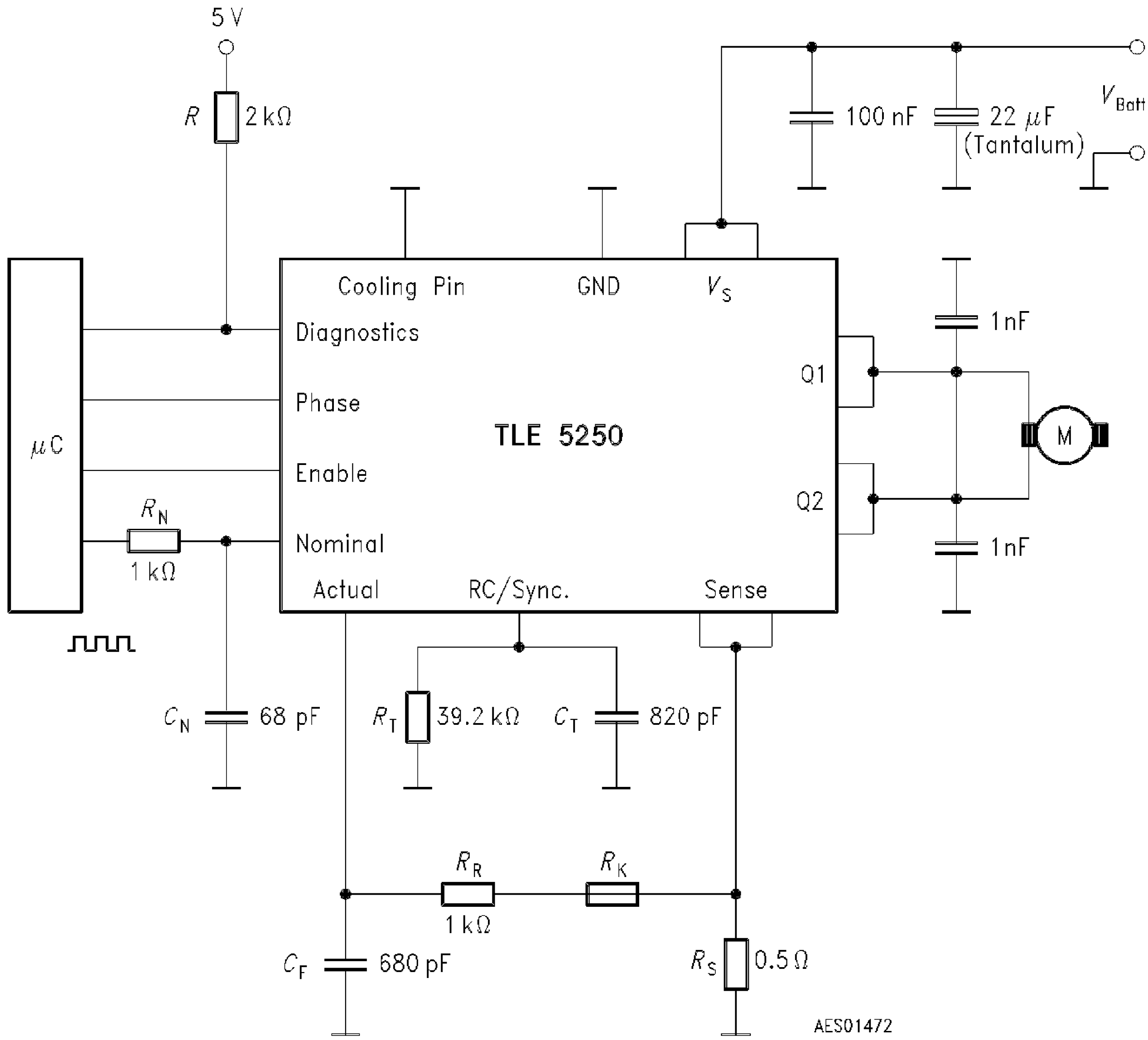
$V_S = 6$ to 25 V; $T_J \leq 150$ °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply current	I_S			11	mA	Enable = High
Output Q1, Q2						
Turn-on resistance of output transistors	$R_{DS\ ON}$	0.3		0.6	Ω	I = 2.5 A, 150 °C
Phase deadtime	t_D		10		µs	
Diode forward voltage output to + V_S	V_{FQ}			1.5	V	I_{FH} = 2.5 V
Diode forward voltage actual-current pin to output				1.5	V	I_{FH} = 2.5 V
Nominal Current						
Input current	I_{I8}	0	1	2	µA	
Offset voltage measured for 0 V actual/nominal pin	$V_{I(8-4)}$	– 4		8	mV	
Actual Current						
Turn-off delay of nom/act comparator	t_d			0.5	µs	
Common-mode error	V_{Comm}	– 5		10	mV	
RC/Sync						
Sync frequency	f		20	100	kHz	
Trigger threshold lower upper	 V_{tL} V_{tH}	 0.8 1.7		 1 2	 V V	
Maximum charge voltage	V_{Chm}	2.2	2.3	2.4	V	R = 39 kΩ C = 820 pF

Characteristics (cont'd)

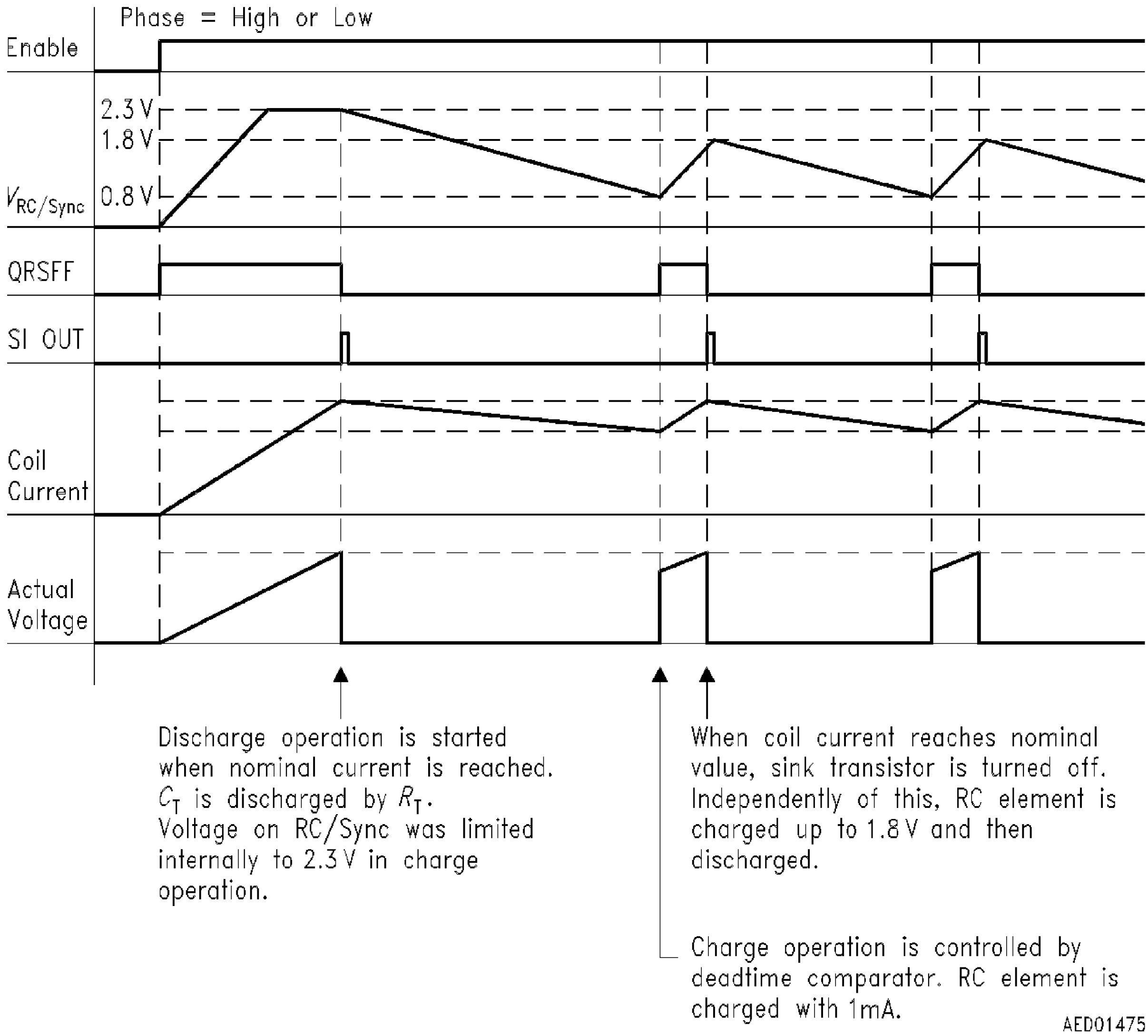
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Undervoltage Cutout						
Disable	V_{UDIAG}	4			V	
Enable	V_{UEN}			5.3	V	
Hysteresis	V_{UH}			400	mV	
Diagnostics Output						
Activating delay (Enable High → Low)	t_{def}			400	ns	
Delay phase low to high	t_{ddr}			500	ns	Enable = Low $V_S > 5.5$ V
Delay phase high to low	t_{ddf}			450	ns	Enable = Low $V_S > 5.5$ V
Output voltage low	V_{Diag}			0.4	V	I_{QL} = 5 mA
Leakage current high	I_{Diag}			10	µA	V_{QH} = 5 V

Test Circuit



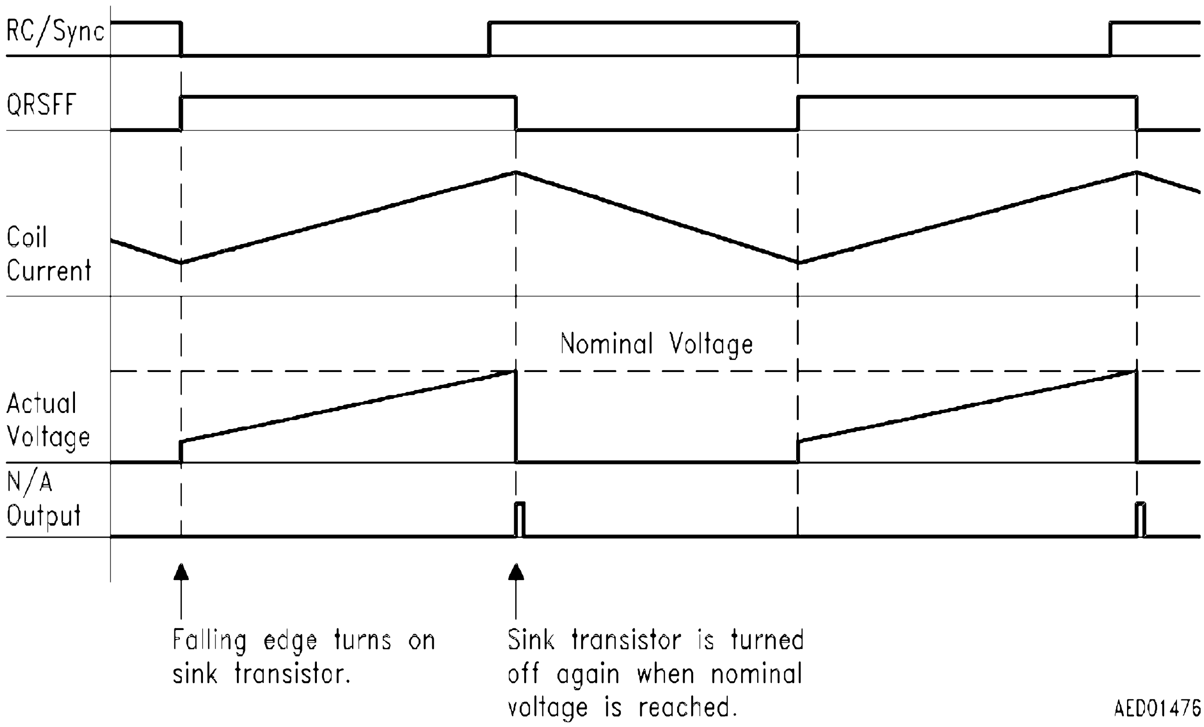
Application Circuit 1

Diagram 1



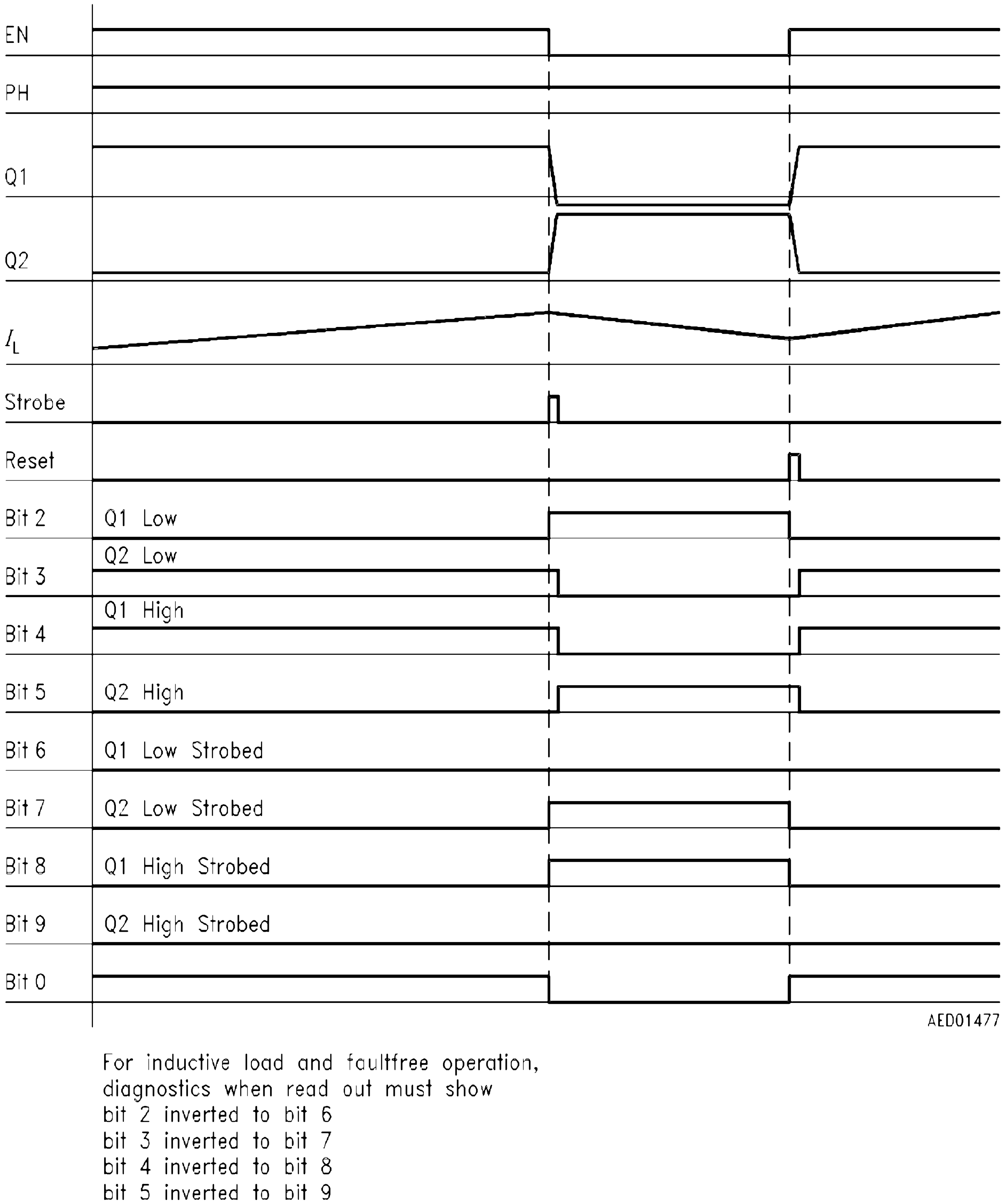
Chopper Mode with External Capacitor CT and Resistor RT

Diagram 2



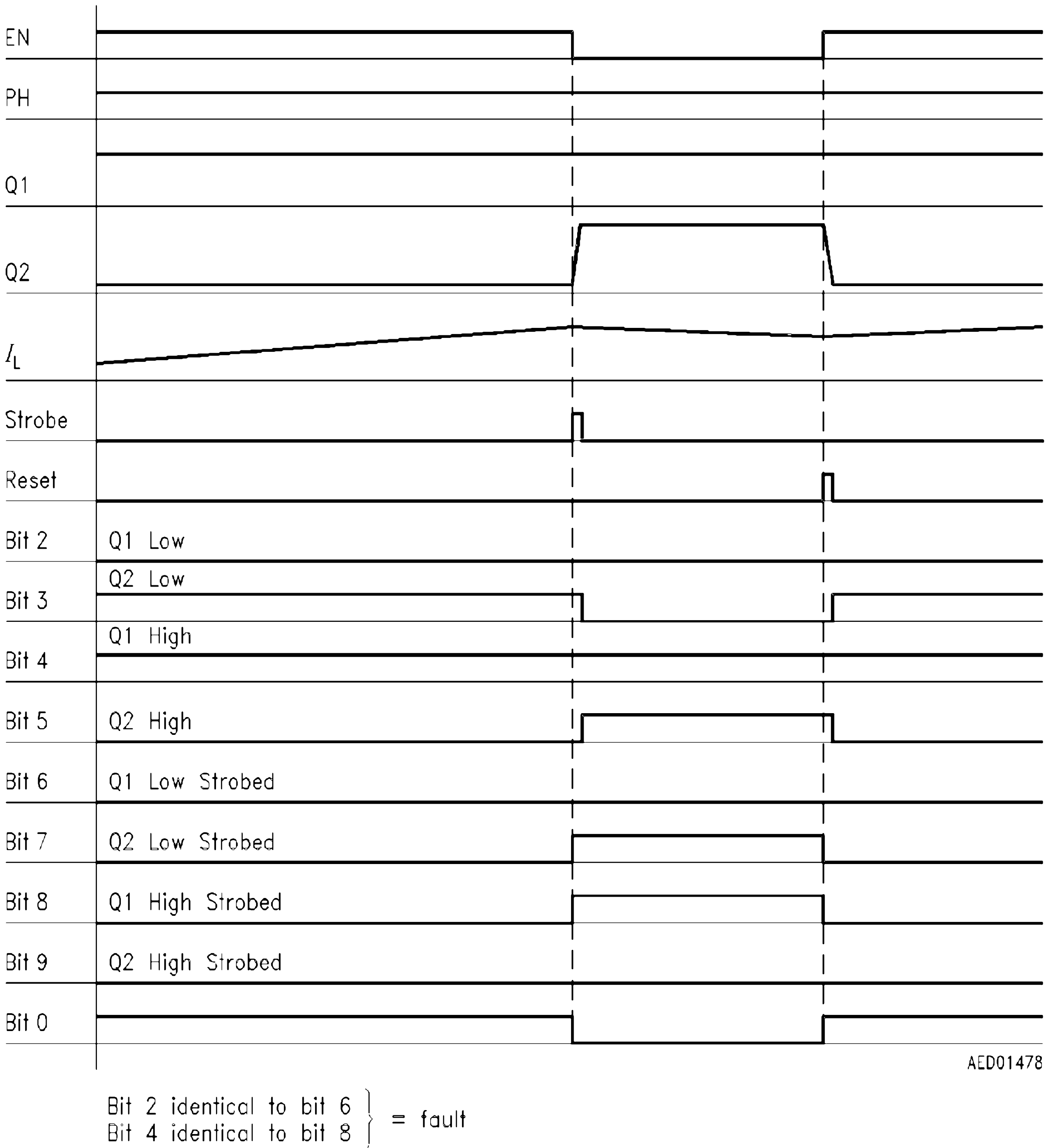
Synchron Mode

Diagram 3



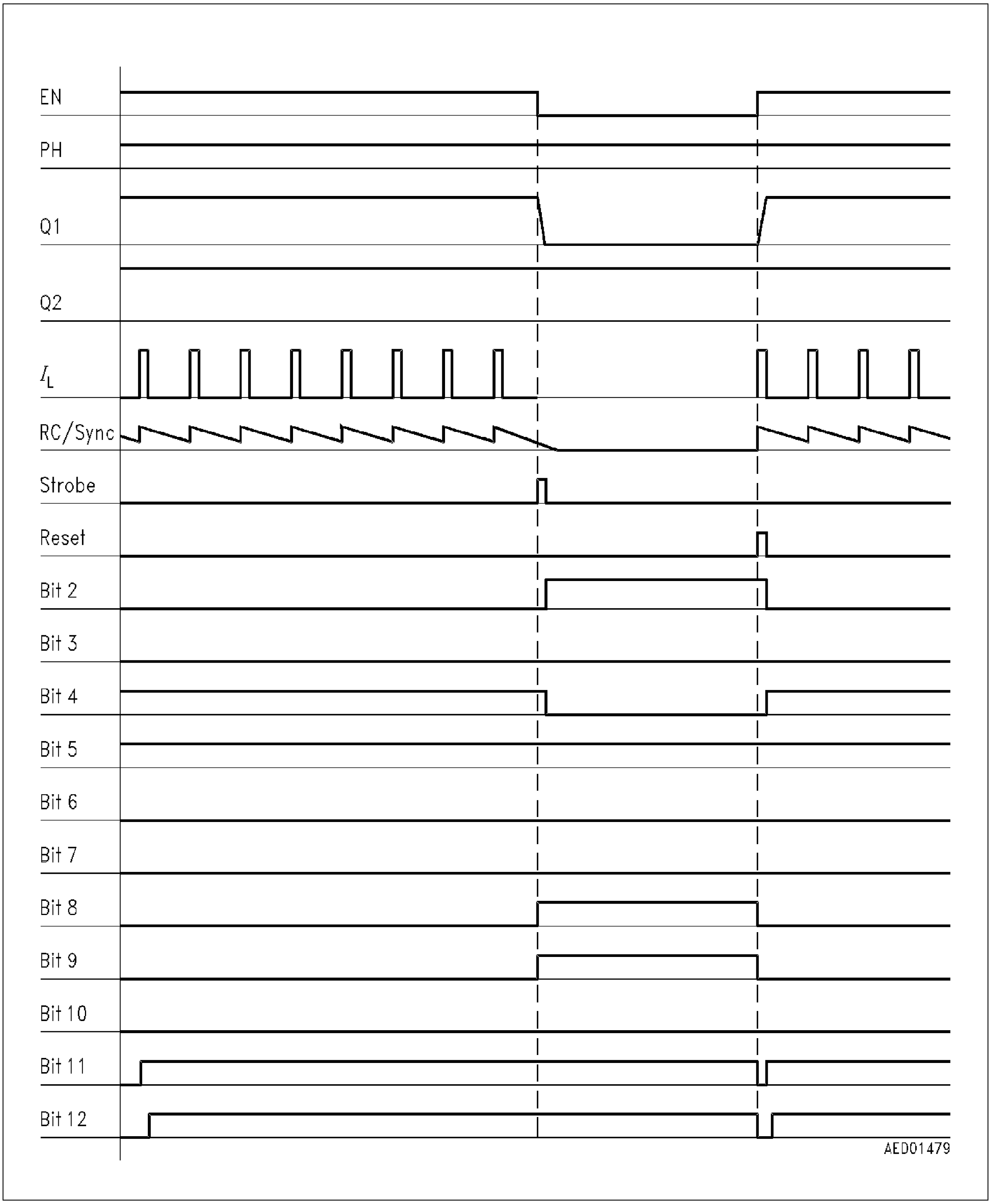
Response to Inductive Loads
a) Normal Operation (no current regulation)

Diagram 4



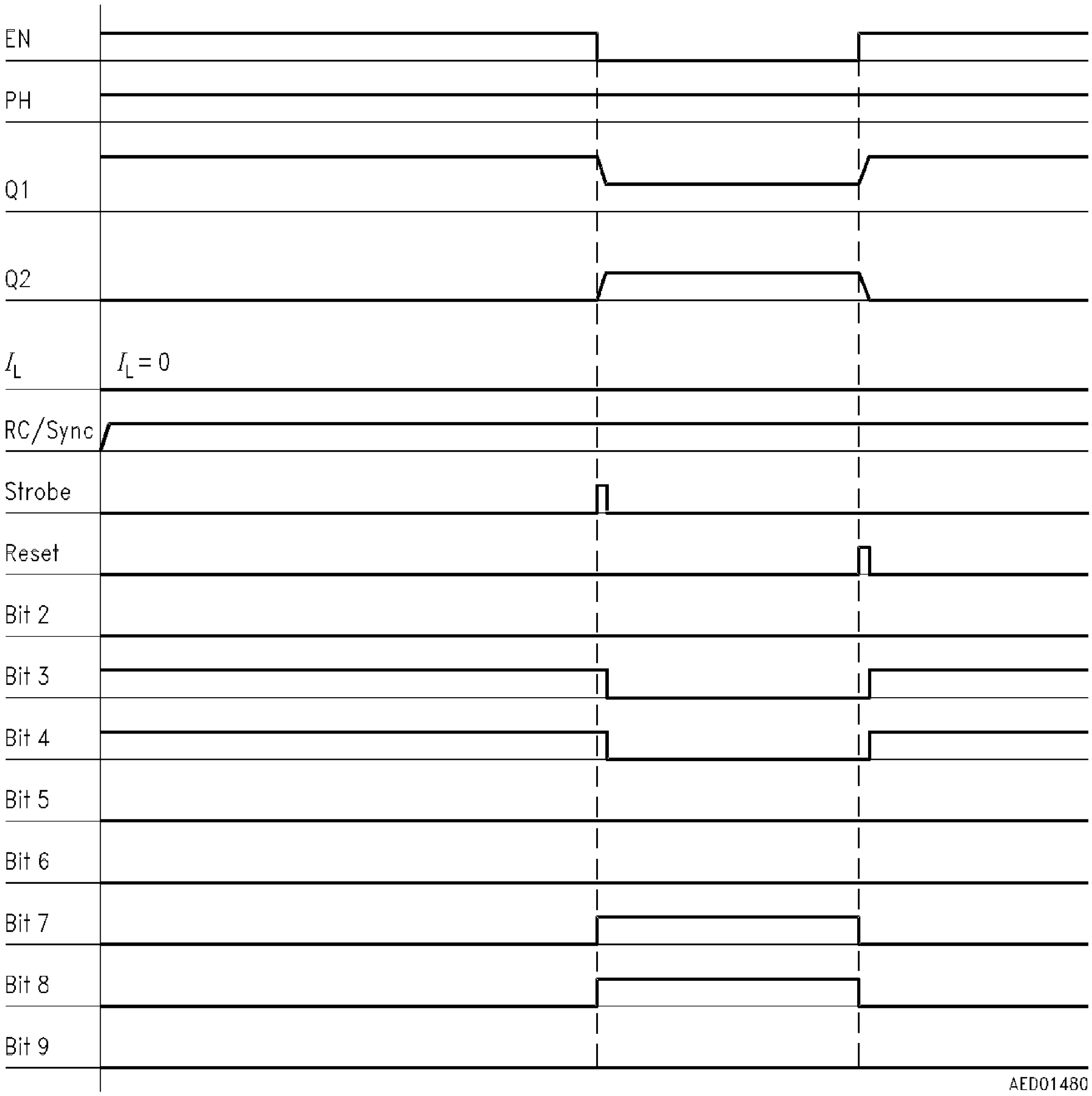
Response to Inductive Loads
b) Q1 Shorted to + V_S (Phase = High)

Diagram 5



Response to Inductive Loads
c) Q2 Shorted to + V_S (Phase = High)

Diagram 6



Indication of low load: bit 2 = bit 3
bit 4 = bit 5
while Enable = Low

And conditions bit 2 = /bit 6
bit 3 = /bit 7
bit 4 = /bit 8
bit 5 = /bit 9 are not all satisfied

Response to Inductive Loads
d) Low Load