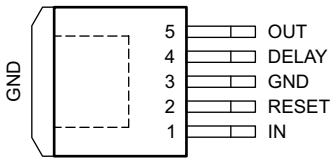
5-V LOW-DROPOUT VOLTAGE REGULATOR

Check for Samples: TLE4275-Q1

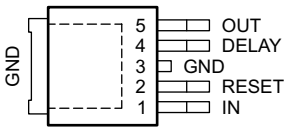
FEATURES

- **Qualified for Automotive Applications**
- **Output Voltage 5 V ± 2%**
- **Very Low Current Consumption**
- **Power-On and Undervoltage Reset**
- **Reset Low-Level Output Voltage < 1 V**
- **Very Low Dropout Voltage**
- **Short-Circuit Proof**
- **Reverse-Polarity Proof**

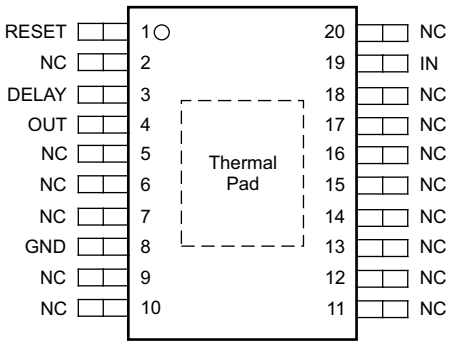
KTT (TO-263-5) Package
(Top View)



KVU (TO-252-5) Package
(Top View)



PWP (HTSSOP) Package
(Top View)



DESCRIPTION

The TLE4275 is a monolithic integrated low-dropout voltage regulator offered in a 5-pin TO package. An input voltage up to 45 V is regulated to V_{OUT} = 5 V (typ). The device can drive loads up to 450 mA and is short-circuit proof. At overtemperature, the TLE4275 is turned off by the incorporated temperature protection. A reset signal is generated for an output voltage, $V_{OUT,rt}$, of 4.65 V (typ). The reset delay time can be programmed by the external delay capacitor.

The input capacitor, C_{IN}, compensates for line fluctuation. Using a resistor of approximately 1 Ω in series with C_{IN} dampens the oscillation of input inductance and input capacitance. The output capacitor, C_{OUT}, stabilizes the regulation circuit. Stability is specified at C_{OUT} ≥ 22 µF and ESR ≤ 5 Ω, within the operating temperature range. Stability for electrolytic capacitors specifically is set at C_{OUT} ≥ 68 µF within the operating temperature range. See the application report on low-temperature stability, SLVA501, for further details.

The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The device also incorporates a number of internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity

ORDERING INFORMATION(1)

T_J	ORDERABLE PART NUMBER(2)	TOP-SIDE MARKING
–40°C to 150°C	TLE4275QKVURQ1	TLE4275Q
	TLE4275QKTTRQ1	TLE4275Q
	TLE4275QPWPRQ1	Preview

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

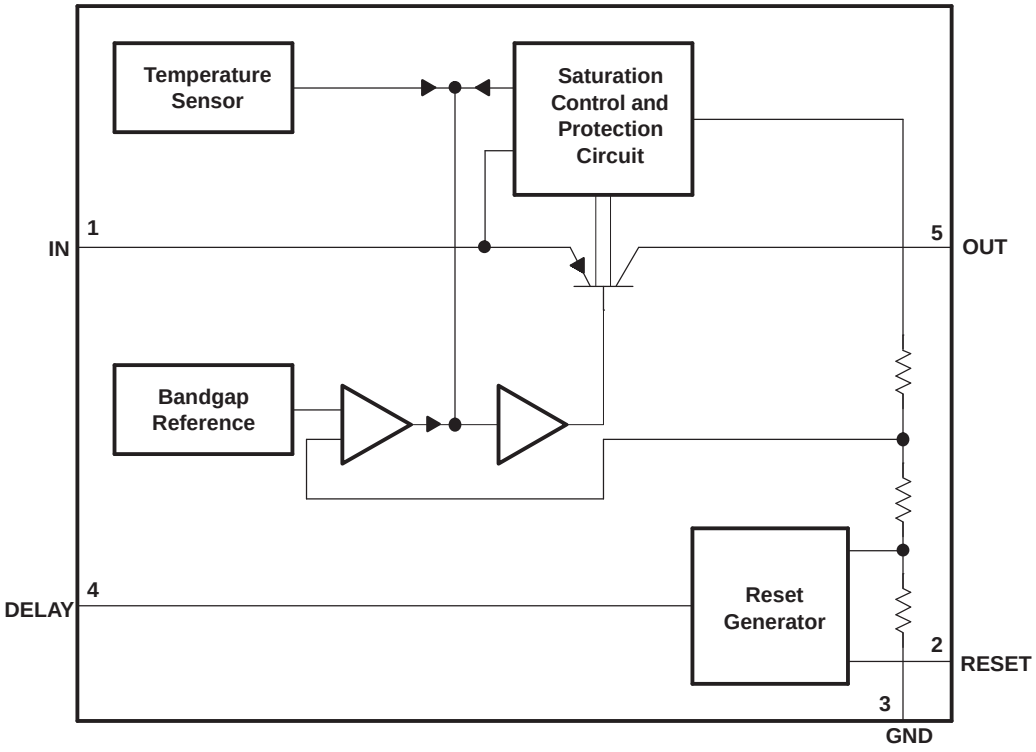
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PIN FUNCTIONS

NAME	NO.			DESCRIPTION
	KTT	KVU	PWP	
IN	1	1	19	Input. Connect to ground as close to device as possible, through a ceramic capacitor.
RESET	2	2	1	Reset output. Open-collector output
GND	3	3	8	Ground. Internally connected to heatsink
DELAY	4	4	3	Reset delay. Connect to ground with a capacitor to set delay time.
OUT	5	5	4	Output. Connect to ground with ≥ 22-µF capacitor, ESR < 5 Ω at 10 kHz.
NC	–	–	2, 5–7, 9–18, 20	Not connected

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_I	Input voltage range(2)	IN	–42	45	V
		DELAY	–0.3	7	
V_O	Output voltage range	OUT	–1	16	V
		RESET	–0.3	25	
I_I	Input current	DELAY		±2	mA
I_O	Output current	RESET		±5	mA
θ_{JA}	Package thermal impedance, junction to free air(3) (4)	KTT package		26.5	°C/W
		KVU package		38.6	
T_J	Operating junction temperature range		–40	150	°C
T_{stg}	Storage temperature range		–65	150	°C
ESD	Electrostatic discharge rating	Human-body model (HBM)(5)		6000	V
		Machine model (MM)(6)		400	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.
(3) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) HBM ESD rating tested per JESD22-A114.
(6) MM ESD rating tested per JESD22-A115.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I	Input voltage	5.5	42	V
T_J	Junction temperature	–40	150	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, V_I = 13.5 V, T_J = −40°C to 150°C (unless otherwise noted) (see Figure 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage	I_O = 5 mA to 400 mA, V_I = 6 V to 28 V		4.9	5	5.1	V
		I_O = 5 mA to 200 mA, V_I = 6 V to 40 V		4.9	5	5.1	
I_O	Output current limit			450	700	950	mA
I_q	Current consumption $I_q = I_I - I_O$	I_O = 1 mA	T_J = 25°C		150	200	µA
			$T_J \le$ 85°C		150	220	
		I_O = 250 mA			5	10	mA
		I_O = 400 mA			12	22	
V_{DO}	Dropout voltage(1)	I_O = 300 mA, $V_{do} = V_I - V_O$			250	500	mV
	Load regulation	I_O = 5 mA to 400 mA			15	30	mV
	Line regulation	ΔV_I = 8 V to 32 V, I_O = 5 mA		–15	5	15	mV
PSRR	Power-supply ripple rejection	f_r = 100 Hz, V_r = 0.5 V_{pp}			60		dB
$\frac{\Delta V_O}{\Delta T}$	Temperature output-voltage drift				0.5		mV/K
$V_{O,rt}$	RESET switching threshold			4.5	4.65	4.8	V
V_{ROL}	RESET output low voltage	$R_{ext} \ge$ 5 kΩ, V_O > 1 V			0.2	0.4	V
I_{ROH}	RESET output leakage current	V_{ROH} = 5 V			0	10	µA
$I_{D,c}$	RESET charging current	V_D = 1 V		3	5.5	9	µA
V_{DU}	RESET upper timing threshold			1.5	1.8	2.2	V
V_{DRL}	RESET lower timing threshold			0.2	0.4	0.7	V

(1) Measured when the output voltage V_O has dropped 100 mV from the nominal value obtained at V_I = 13.5 V

SWITCHING CHARACTERISTICS

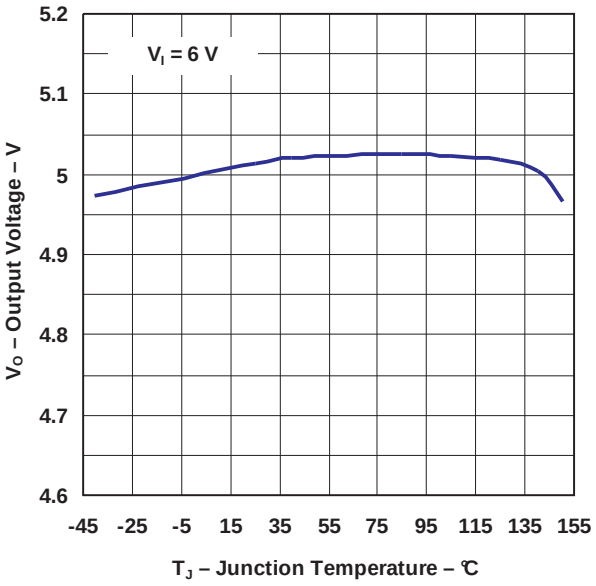
over operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rd}	RESET delay time	C_D = 47 nF	10	16	22	ms
t_{rr}	RESET reaction time	C_D = 47 nF		0.5	2	µs

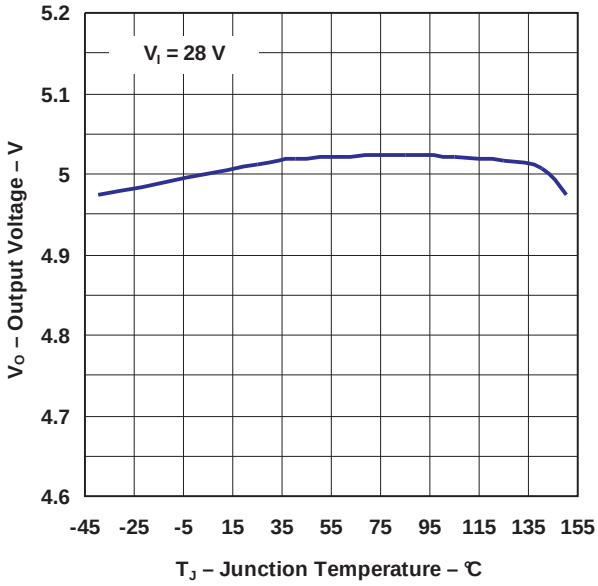
TYPICAL CHARACTERISTICS

At T_A = 25ºC

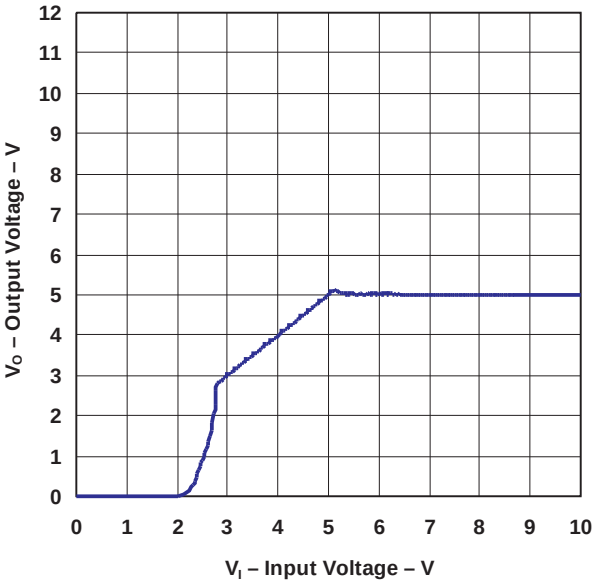
OUTPUT VOLTAGE vs JUNCTION TEMPERATURE



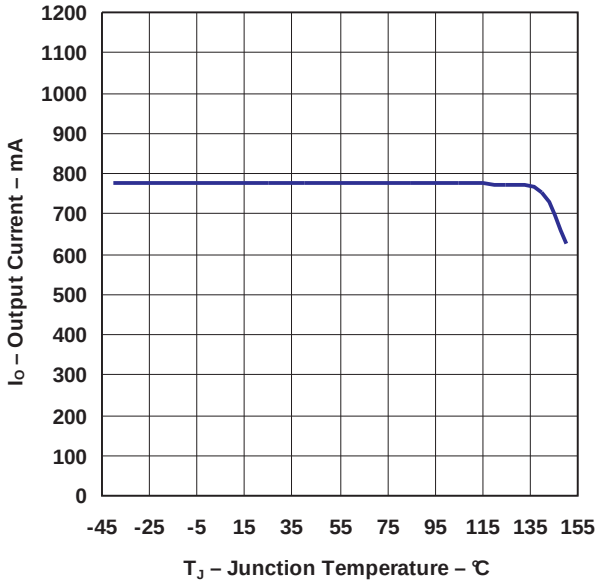
OUTPUT VOLTAGE vs JUNCTION TEMPERATURE



OUTPUT VOLTAGE vs INPUT VOLTAGE



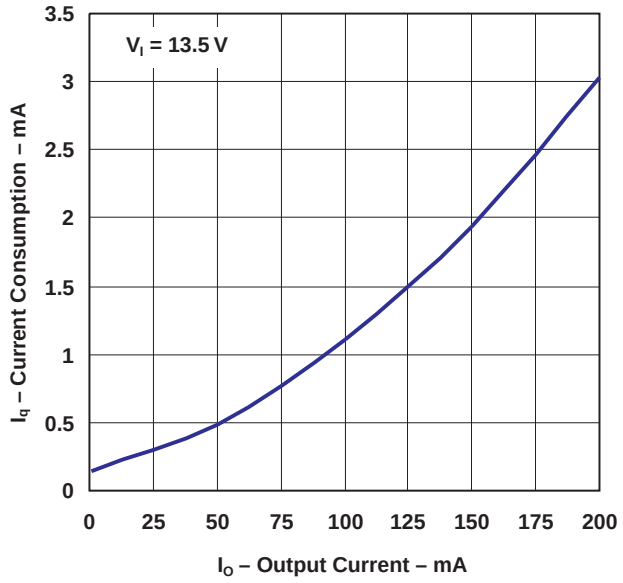
OUTPUT CURRENT vs JUNCTION TEMPERATURE



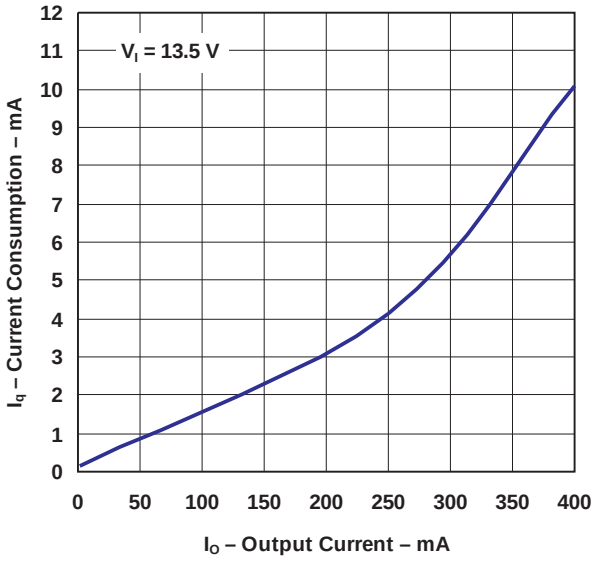
TYPICAL CHARACTERISTICS (continued)

At T_A = 25ºC

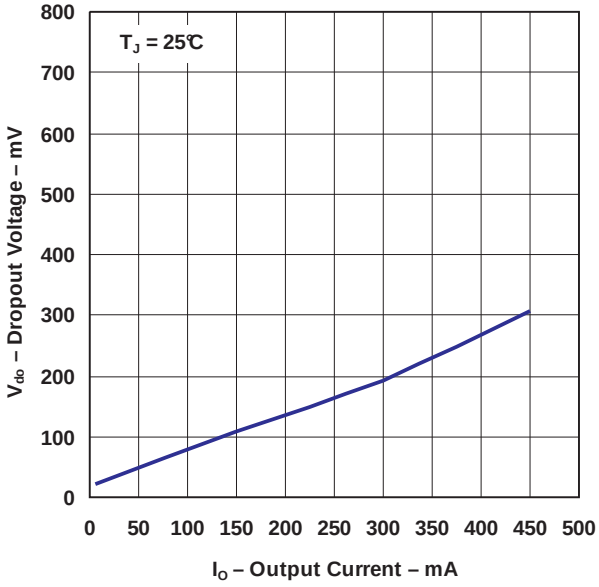
CURRENT CONSUMPTION vs OUTPUT CURRENT



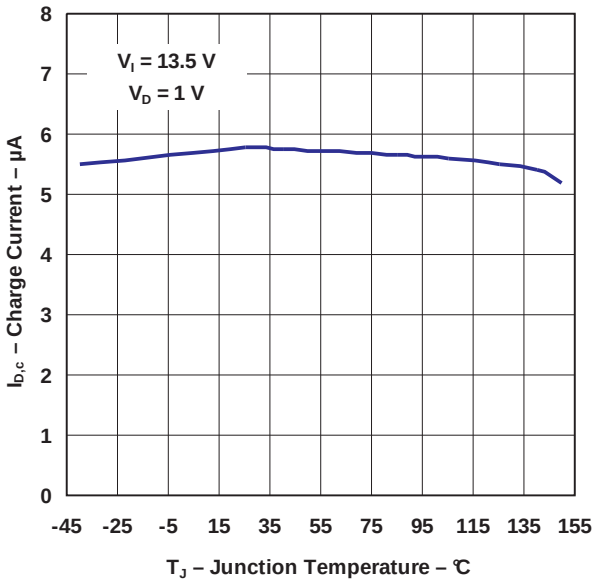
CURRENT CONSUMPTION vs OUTPUT CURRENT



DROPOUT VOLTAGE vs OUTPUT CURRENT



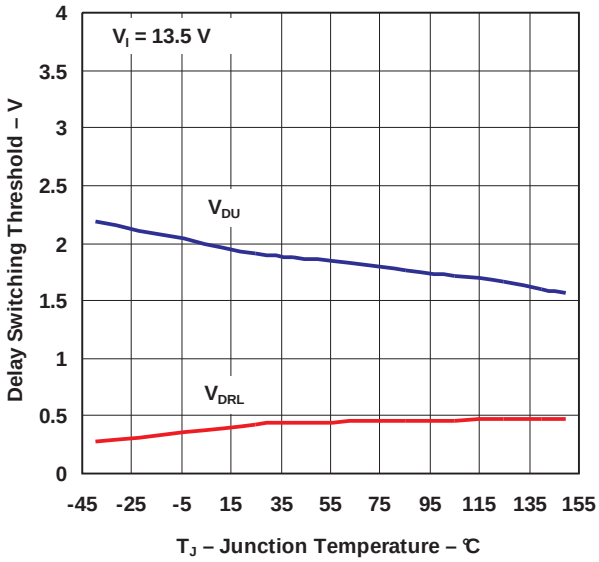
CHARGE CURRENT vs JUNCTION TEMPERATURE



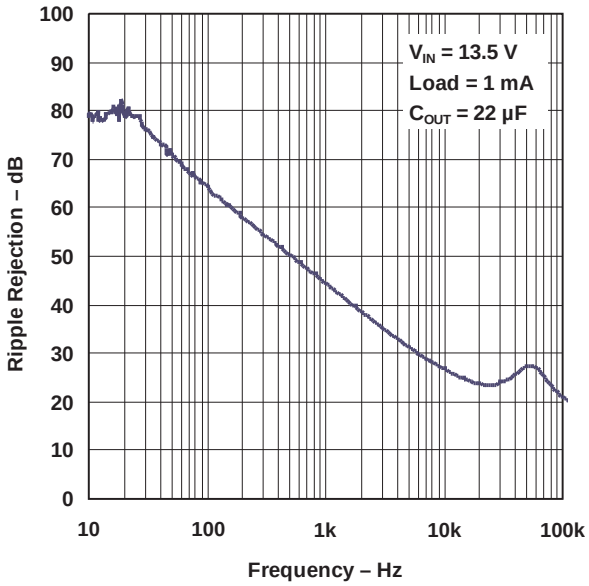
TYPICAL CHARACTERISTICS (continued)

At T_A = 25ºC

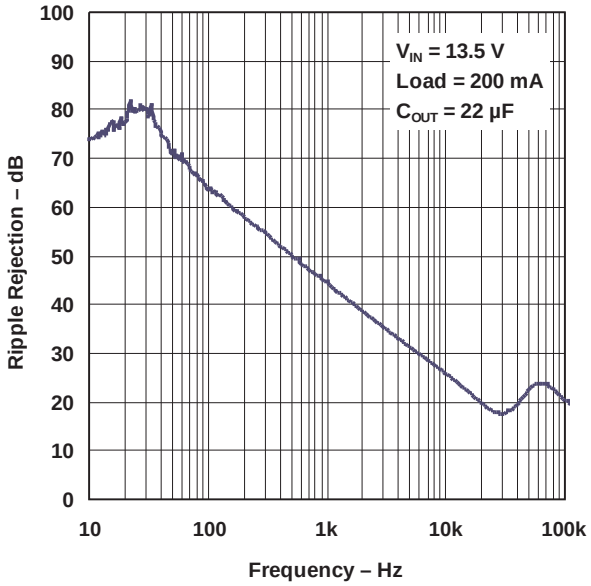
DELAY SWITCHING THRESHOLD vs JUNCTION TEMPERATURE



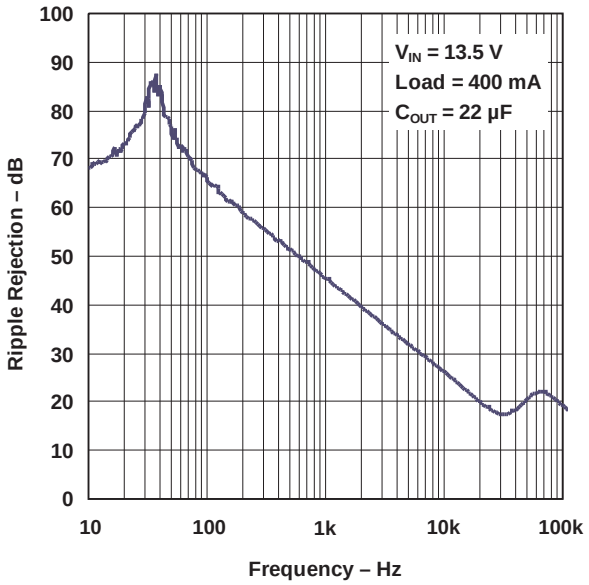
POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY



POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY

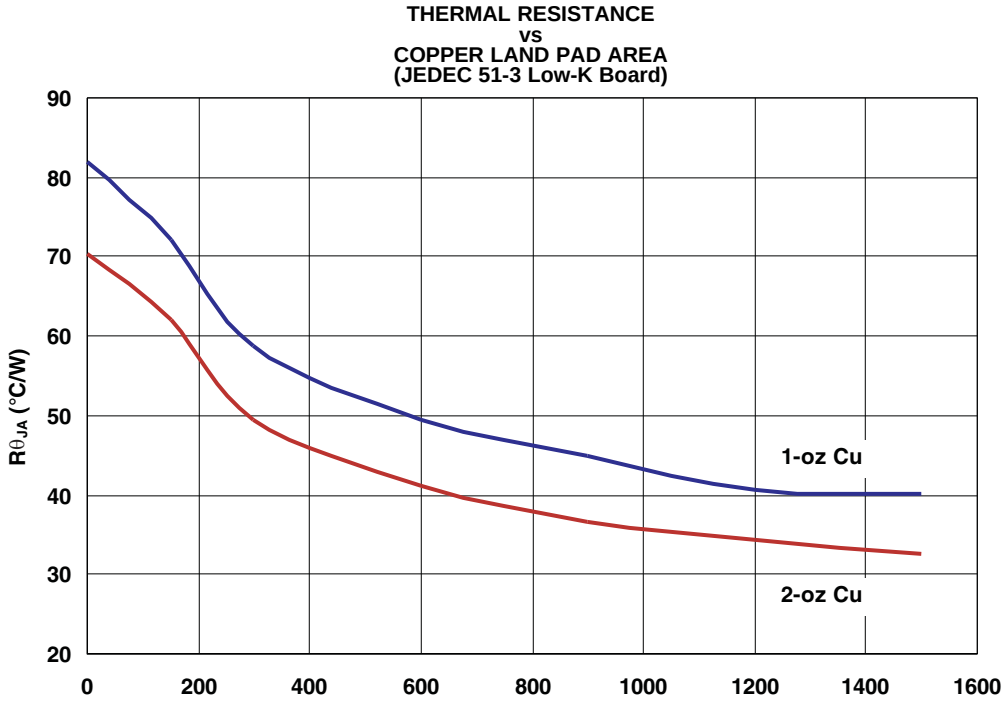


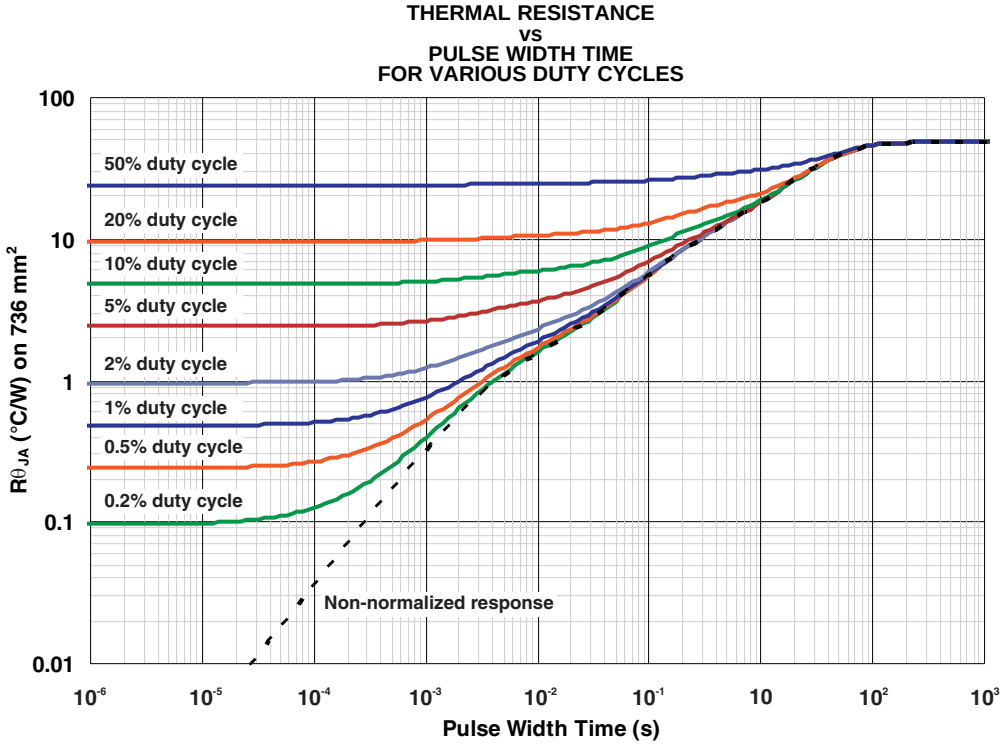
POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY



TYPICAL CHARACTERISTICS (continued)

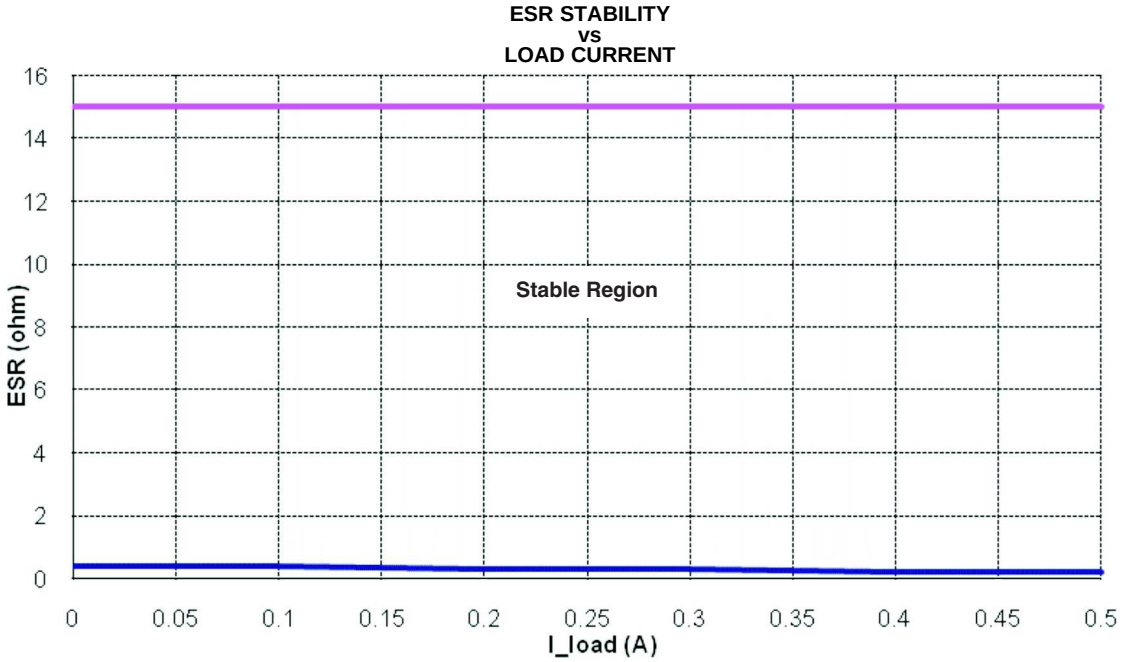
At T_A = 25ºC

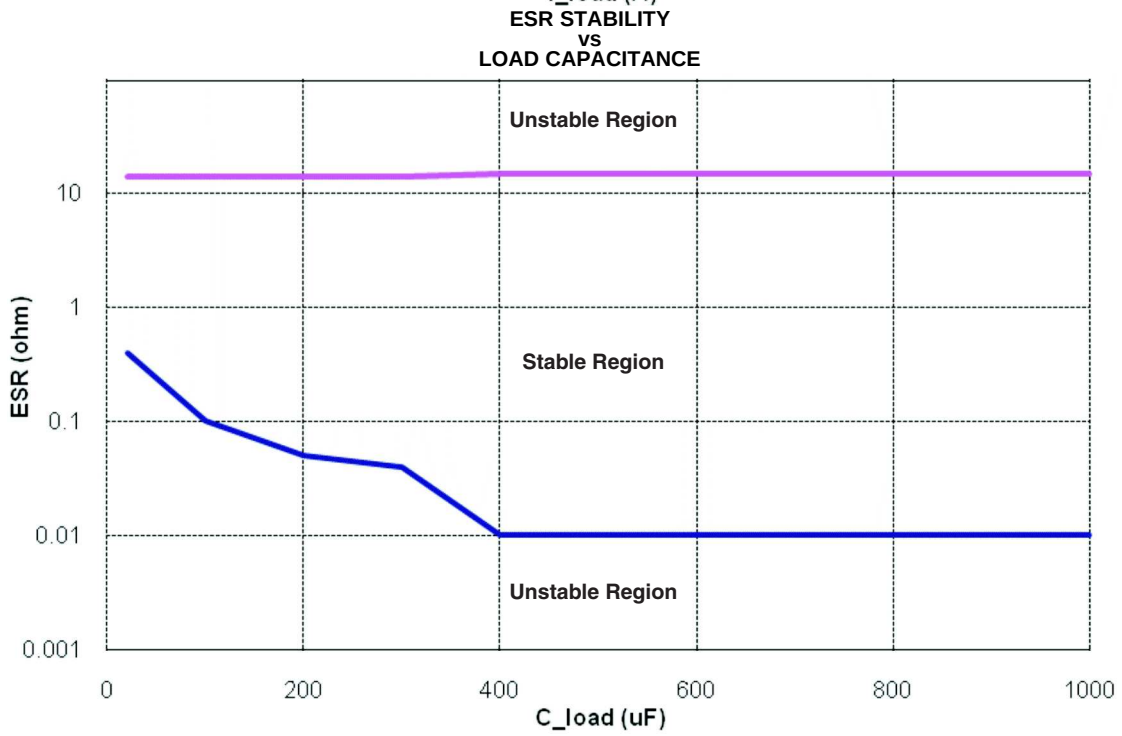




TYPICAL CHARACTERISTICS (continued)

At T_A = 25ºC





PARAMETER MEASUREMENT INFORMATION

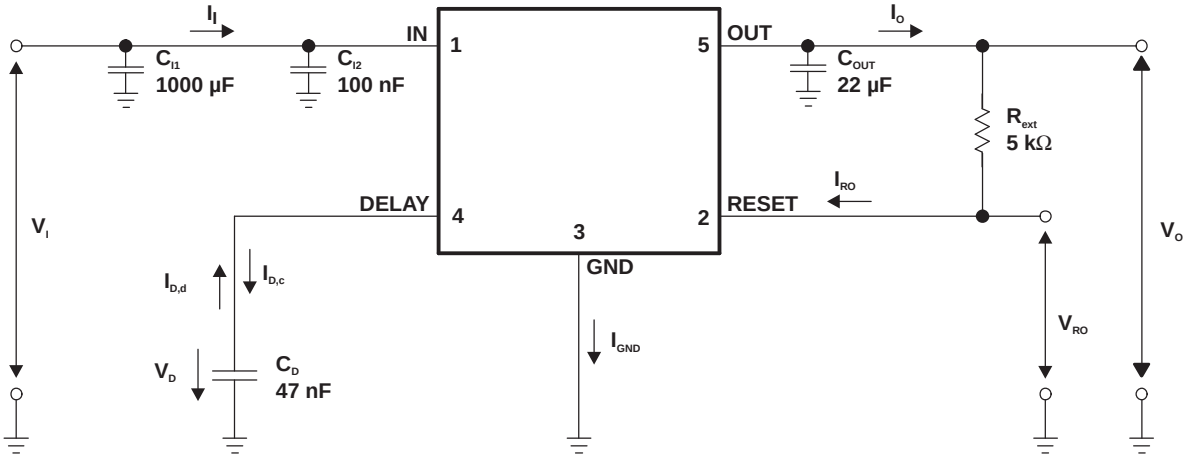


Figure 1. Test Circuit

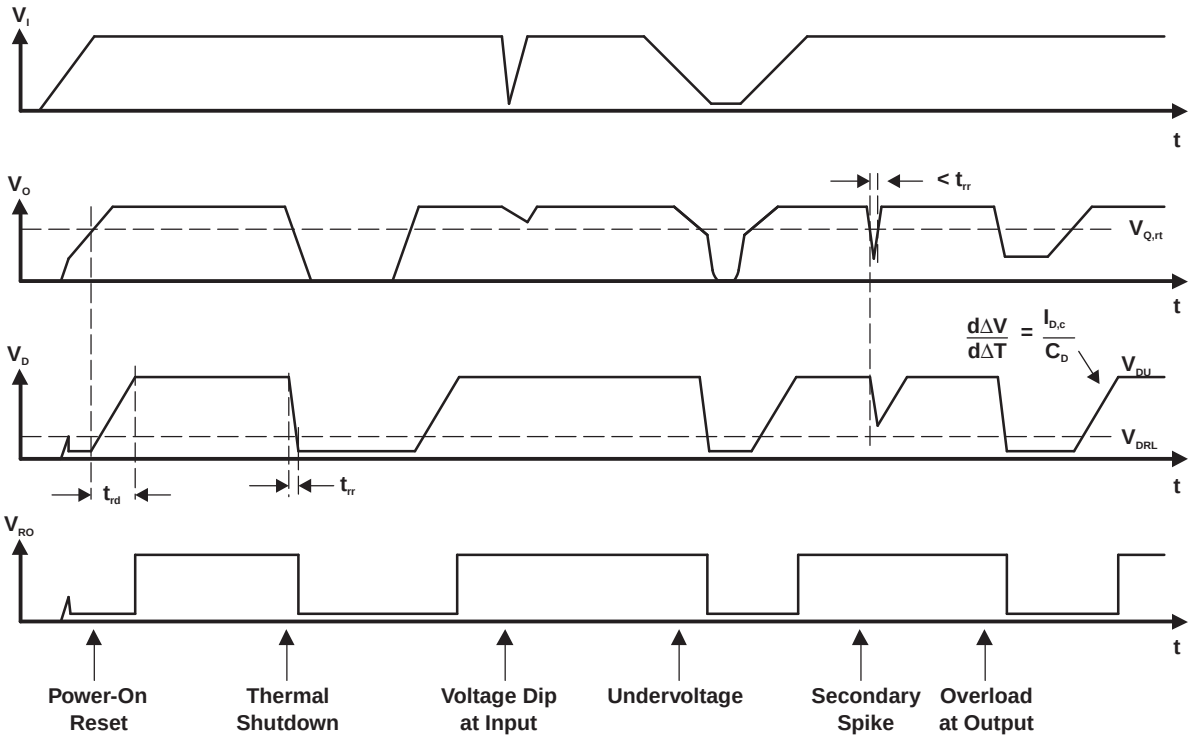


Figure 2. Reset Timing

REVISION HISTORY

Changes from Revision F (May 2011) to Revision G	Page
• Added pin out image for PWP package.	1
• Deleted package column from ordering information table, added orderable part number for PWP package and changed top-side marking to preview.	1
• Updated pin functions table with PWP package pin information.	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLE4275QKTTRQ1	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TLE4275Q	Samples
TLE4275QKVURQ1	ACTIVE	PFM	KVU	5	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	TLE4275Q	Samples

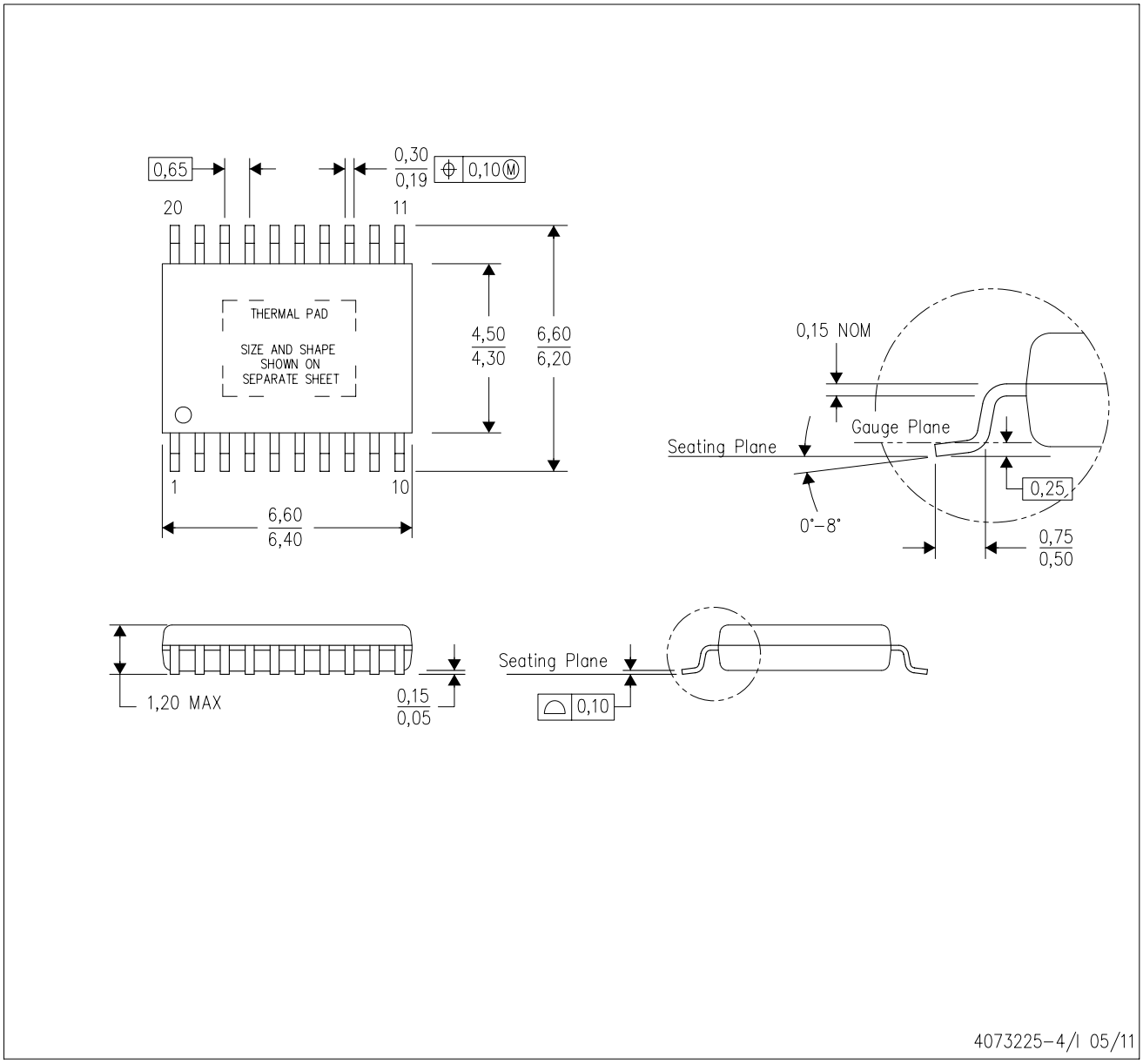
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

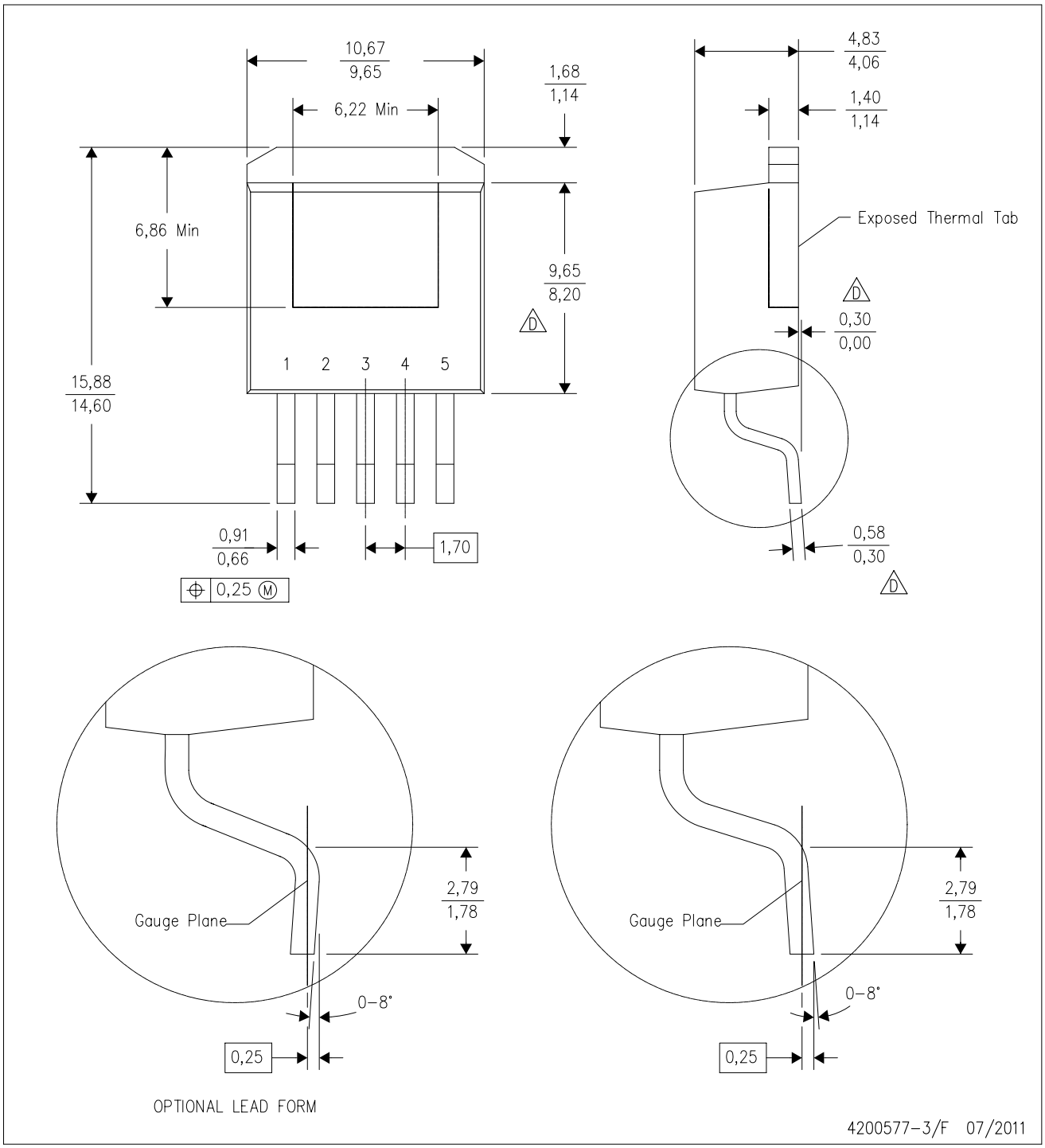
(4) Only one of markings shown within the brackets will appear on the physical device.

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



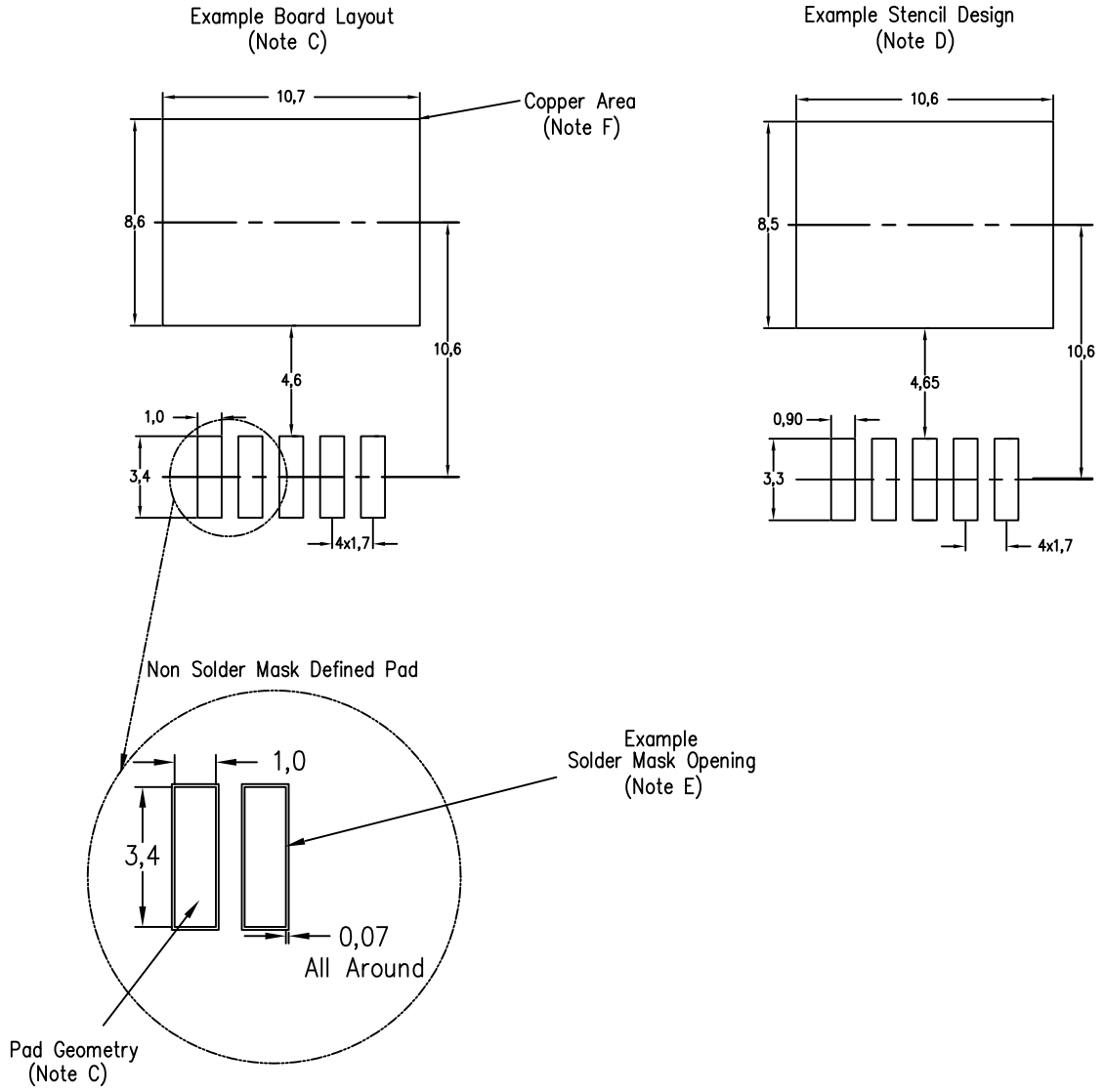
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



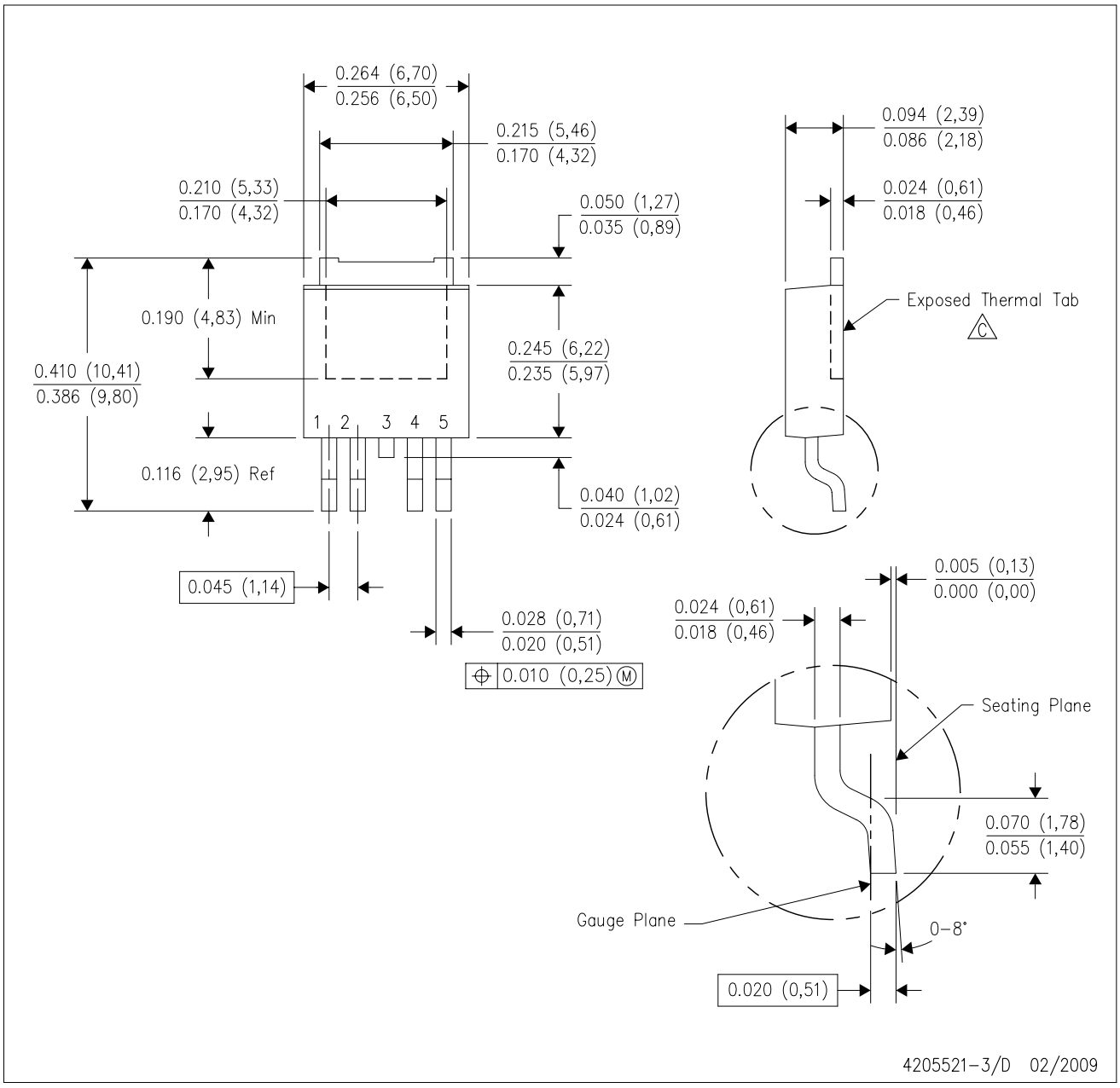
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

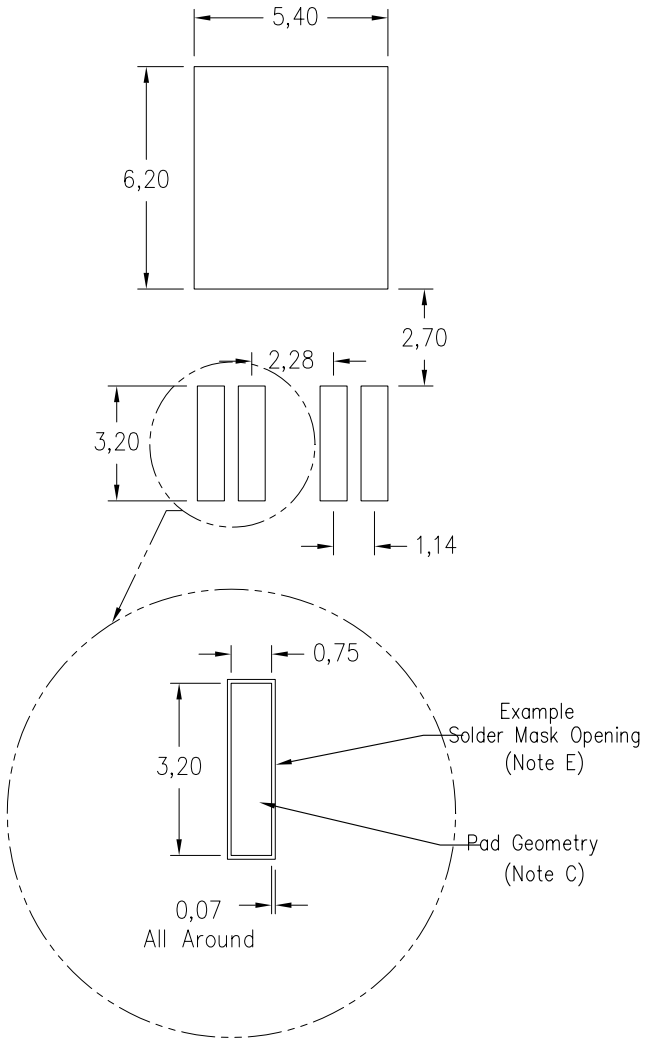
KVU (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



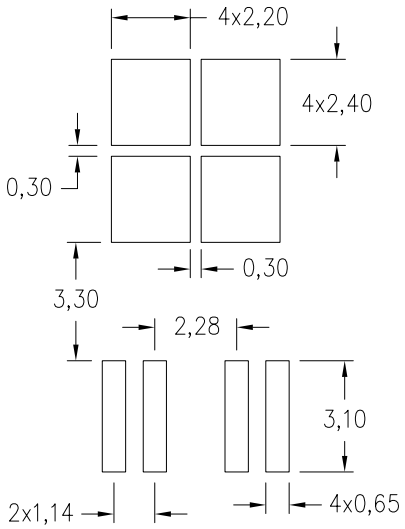
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the exposed thermal tab.
D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
E. Falls within JEDEC TO–252 variation AD.

KVU (R–PSFM–G5) PLASTIC FLANGE MOUNT PACKAGE

Example Board Layout



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



63% solder coverage on center pad

4211592–3/B 03/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is an alternate information source for PCB land pattern designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265