- **Excellent Output Drive Capability**
  V_O = ±2.5 V Min at R_L = 100 Ω,
  $V_{CC\pm}$ = ±5 V
  V_O = ±12.5 V Min at R_L = 600 Ω,
  V_{CC} = ±15 V
- **Low Supply Current . . . 280 μA Typ**
- **High Unity-Gain Bandwidth**
  1.8 MHz Typ
- **High Slew Rate . . . 3.4 V/μs Typ**
- **Macromodels Included**
- **Wide Operating Supply Voltage Range**
  $V_{CC\pm}$ = ±3.5 V to ±19 V
- **High Open-Loop Gain . . . 230 V/mV Typ**
- **Low Offset Voltage . . . 500 μV Max**
- **Low Offset Voltage Drift With Time**
  0.04 μV/mo Typ
- **Low Input Bias Current . . . 4 pA Typ**

description

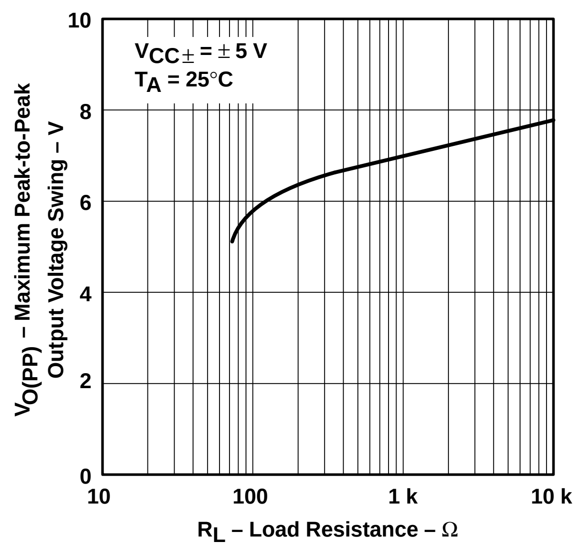
The TLE2061, TLE2061A, TLE2061B, and TLE2061Y are JFET-input, low-power, precision operational amplifiers manufactured using Texas Instruments Excalibur process. These devices combine outstanding output drive capability with low power consumption, excellent dc precision, and wide bandwidth.

In addition to maintaining the traditional JFET advantages of fast slew rates and low input bias and offset currents, the Excalibur process offers outstanding parametric stability over time and temperature. This results in a precision device remaining precise even with changes in temperature and over years of use.

The TLE2061, TLE2061A, and TLE2061B are ideal choices for any application requiring excellent dc precision, high output drive, wide bandwidth, and low power consumption.

A variety of available package options includes small-outline (D) and chip-carrier (FK) versions for high-density system applications.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



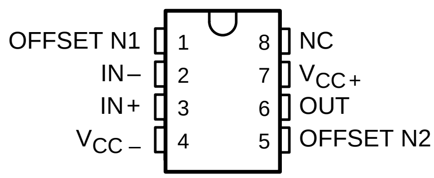
The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

AVAILABLE OPTIONS

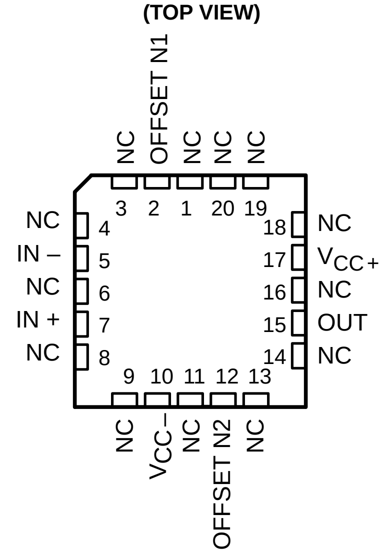
		PACKAGED DEVICES						CHIP FORM (Y)
T_A	V_{IO}max AT 25°C	SMALL OUTLINE (D)	SSOP (DB)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	
0°C to 70°C	500 μV	—	—	—	—	—	—	TLE2061Y
	1.5 mV	TLE2061ACD	—	—	—	TLE2061ACP	—	
	3 mV	TLE2061CD	TLE2061CDBLE	—	—	TLE2061CP	TLE2061CPWLE	
−40°C to 85°C	500 μV	—	—	—	—	—	—	—
	1.5 mV	TLE2061AID	—	—	—	TLE2061AIP	—	
	3 mV	TLE2061ID	—	—	—	TLE2061IP	—	
−55°C to 125°C	500 μV	—	—	—	—	—	—	—
	1.5 mV	TLE2061AMD	—	TLE2061AMFK	TLE2061AMJG	TLE2061AMP	—	
	3 mV	TLE2061MD	—	TLE2061MFK	TLE2061MJG	TLE2061MP	—	

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLE2061ACDR). The DB and PW packages are available left-end taped and reeled (indicated by the LE suffix on the device type (e.g., TLE2061CDBLE). Chips are tested at 25°C.

D, DB, JG, P, OR PW PACKAGE
(TOP VIEW)



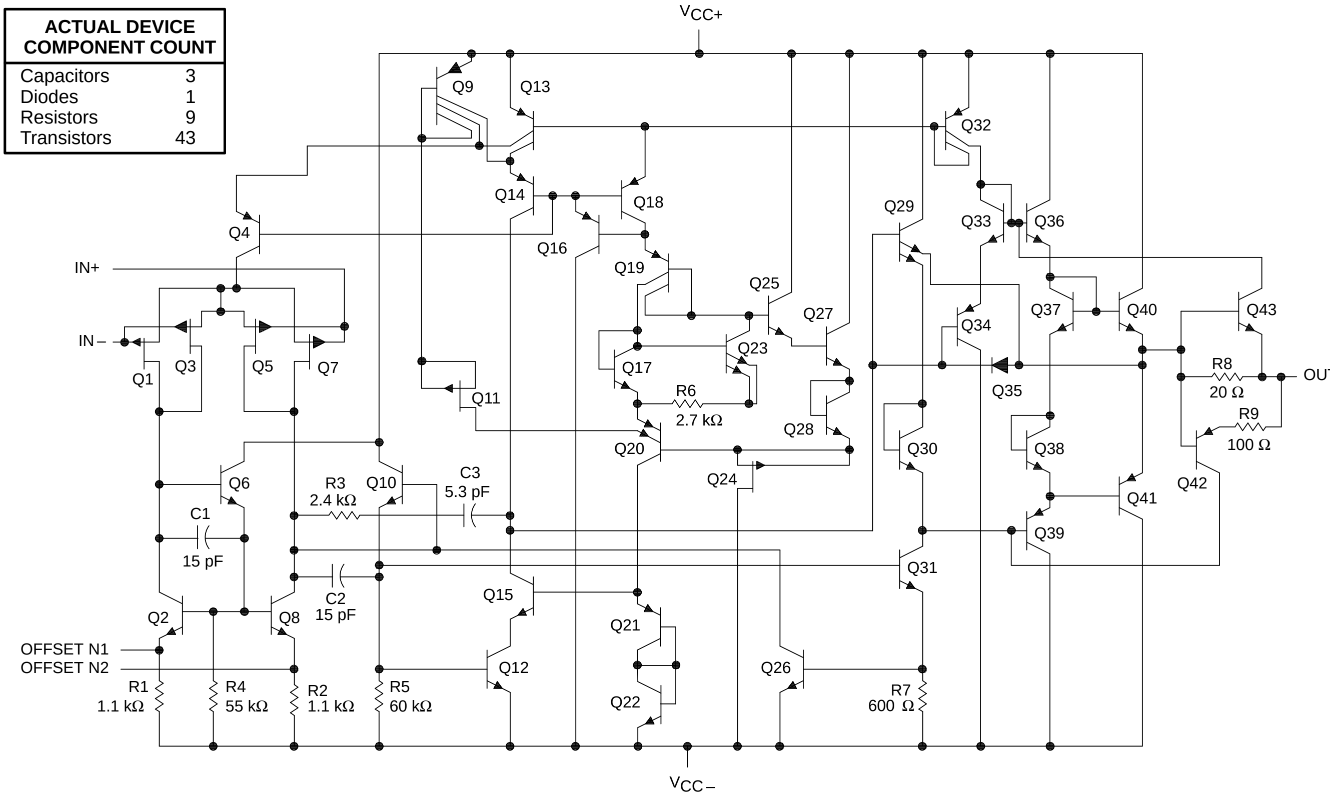
FK PACKAGE
(TOP VIEW)



NC – No internal connection

equivalent schematic

ACTUAL DEVICE COMPONENT COUNT	
Capacitors	3
Diodes	1
Resistors	9
Transistors	43

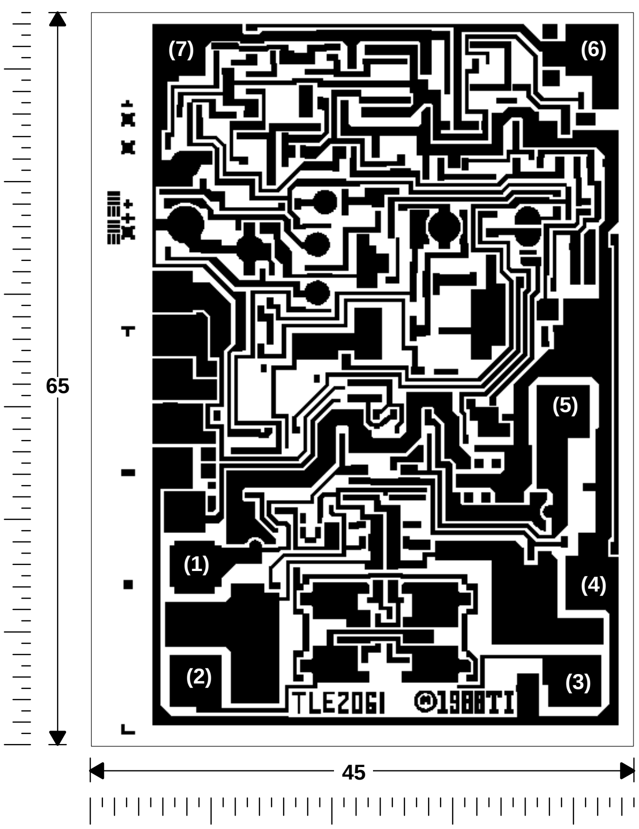


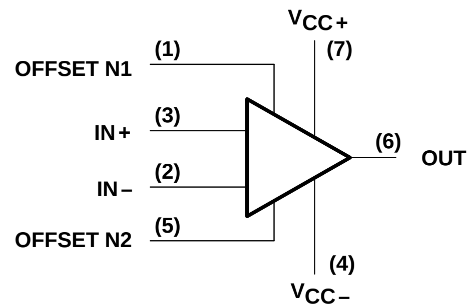
All component values are nominal.

TLE2061Y chip information

This chip, when properly assembled, displays characteristics similar to the TLE2061. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 X 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ± 10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1)	19 V
Supply voltage, V_{CC-}	–19 V
Differential input voltage, V_{ID} (see Note 2)	±38 V
Input voltage range, V_I (any input)	$\pm V_{CC}$
Input current, I_I (each input)	±1 mA
Output current, I_O	±80 mA
Total current into V_{CC+}	80 mA
Total current out of V_{CC-}	–80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix	0°C to 70°C
I suffix	–40°C to 85°C
M suffix	–55°C to 125°C
Storage temperature range	–65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, DB, P, or PW package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
DB	525 mW	4.2 mW/°C	336 mW	—	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW	525 mW	4.2 mW/°C	336 mW	—	—

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±3.5	±18	±3.5	±18	±3.5	±18	V
Common-mode input voltage, V_{IC}	$V_{CC\pm}$ = ± 5 V	–1.6	4	–1.6	4	–1.6	4	V
	$V_{CC\pm}$ = ± 15 V	–11	13	–11	13	–11	13	
Operating free-air temperature, T_A		0	70	–40	85	–55	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2061C TLE2061AC TLE2061BC MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.8	3.1	mV
			Full range			4	
			25°C		0.6	2.6	
			Full range			3.5	
			25°C		0.5	1.9	
			Full range			2.4	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.04		μV/mo
I_{IO}	Input offset current		25°C		1		pA
			Full range			0.8	nA
I_{IB}	Input bias current		25°C		3		pA
			Full range			2	nA
V_{ICR}	Common-mode input voltage range		25°C	–1.6 to 4	–2 to 6		V
			Full range	–1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	3.5	3.7		V
			Full range	3.3			
		$R_L = 100\ \Omega$	25°C	2.5	3.1		
			Full range	2			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$	25°C	–3.7	–3.9		V
			Full range	–3.3			
		$R_L = 100\ \Omega$	25°C	–2.5	–2.7		
			Full range	–2			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm2.8$ V, $R_L = 10\ k\Omega$	25°C	15	80		V/mV
			Full range	2			
		$V_O = 0$ to 2 V, $R_L = 100\ \Omega$	25°C	0.75	45		
			Full range	0.5			
		$V_O = 0$ to –2 V, $R_L = 100\ \Omega$	25°C	0.5	3		
			Full range	0.25			
r_i	Input resistance		25°C		10^{12}		Ω
c_i	Input capacitance		25°C		4		pF
z_o	Open-loop output impedance	$I_O = 0$	25°C		280		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $R_S = 50\ \Omega$	25°C	65	82		dB
			Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm5$ V to ±15 V, $R_S = 50\ \Omega$	25°C	75	93		dB
			Full range	75			

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm5$ V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLE2061C TLE2061AC TLE2061BC			UNIT
				MIN	TYP	MAX	
I_{CC}	Supply current	$V_O = 0$, No load	25°C		280	325	μA
			Full range			350	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		29		μA

† Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLE2061C TLE2061AC TLE2061BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	$R_L = 10$ kΩ,	$C_L = 100$ pF	25°C	2.2	3.4		V/μs
				Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	$R_S = 20$ Ω	25°C		59	100	nV/√Hz
		f = 1 kHz,	$R_S = 20$ Ω			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	$A_{VD} = 1$, $V_{O(PP)} = 2$ V,	f = 10 kHz, $R_L = 10$ kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	$R_L = 10$ kΩ,	$C_L = 100$ pF	25°C		1.8		MHz
		$R_L = 100$ Ω,	$C_L = 100$ pF			1.3		
t_s	Settling time	0.1%		25°C		5		μs
		0.01%				10		
B_{OM}	Maximum output-swing bandwidth	$A_{VD} = 1$,	$R_L = 10$ kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	$R_L = 10$ kΩ,	$C_L = 100$ pF	25°C		58°		
		$R_L = 100$ Ω,	$C_L = 100$ pF			75°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2061C, TLE2061AC, TLE2061BC MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2061C	$V_{IC} = 0$, $R_S = 50$ kΩ	25°C		0.6	3	mV
				Full range			3.9	
		TLE2061AC		25°C		0.5	1.5	
				Full range			2.5	
		TLE2061BC		25°C		0.3	0.5	
				Full range			1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			1	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			3	nA
V_{ICR}	Common-mode input voltage range			25°C	–11 to 13	–12 to 16		V
				Full range	–11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10$ kΩ	25°C	13.2	13.7		V
				Full range	13			
			$R_L = 600$ Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10$ kΩ	25°C	–13.2	–13.7		V
				Full range	–13			
			$R_L = 600$ Ω	25°C	–12.5	–13		
				Full range	–12			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 10$ V, $R_L = 10$ kΩ	25°C	30	230		V/mV
				Full range	20			
			$V_O = 0$ to 8 V, $R_L = 600$ Ω	25°C	25	100		
				Full range	10			
			$V_O = 0$ to –8 V, $R_L = 600$ Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		280		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min, $R_S = 50$ Ω	25°C	72	90		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 15 V, $R_S = 50$ kΩ	25°C	75	93		dB
				Full range	75			

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLE2061C TLE2061AC TLE2061BC MIN	TYP	MAX	UNIT
I_{CC}	Supply current	$V_O = 0$, No load	25°C		290	350	μA
			Full range			375	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		34		μA

† Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V

PARAMETER		TEST CONDITIONS		T_A†	TLE2061C TLE2061AC TLE2061BC MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	$R_L = 10$ kΩ,	$C_L = 100$ pF	25°C	2.6	3.4		V/μs
				Full range	2.5			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	$R_S = 20$ Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	$R_S = 20$ Ω			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	$A_{VD} = 2$, $V_{O(PP)} = 2$ V,	f = 10 kHz, $R_L = 10$ kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	$R_L = 10$ kΩ,	$C_L = 100$ pF	25°C		2		MHz
		$R_L = 600$ Ω,	$C_L = 100$ pF			1.5		
t_s	Settling time	0.1%		25°C		5		μs
		0.01%				10		
B_{OM}	Maximum output-swing bandwidth	$A_{VD} = 1$,	$R_L = 10$ kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	$R_L = 10$ kΩ,	$C_L = 100$ pF	25°C		60°		
		$R_L = 600$ Ω,	$C_L = 100$ pF			70°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm5$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2061I, TLE2061AI TLE2061BI MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2061I	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.8	3.1	mV
				Full range			4.4	
		TLE2061AI		25°C		0.6	2.6	
				Full range			3.9	
		TLE2061BI		25°C		0.5	1.9	
				Full range			2.7	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			2	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			4	nA
V_{ICR}	Common-mode input voltage range			25°C	–1.6 to 4	–2 to 6		V
				Full range	–1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	3.5	3.7		V
				Full range	3.1			
			$R_L = 100\ \Omega$	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	–3.7	–3.9		V
				Full range	–3.1			
			$R_L = 100\ \Omega$	25°C	–2.5	–2.7		
				Full range	–2			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm2.8$ V, $R_L = 10\ k\Omega$	25°C	15	80		V/mV
				Full range	2			
			$V_O = 0$ to 2 V, $R_L = 100\ \Omega$	25°C	0.75	45		
				Full range	0.5			
			$V_O = 0$ to –2 V, $R_L = 100\ \Omega$	25°C	0.5	3		
				Full range	0.25			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		280		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min, $R_S = 50\ \Omega$	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm} = \pm5$ V to ±15 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current		$V_O = 0$, No load	25°C		280	325	μA
				Full range			350	
ΔI_{CC}	Supply-current change over operating temperature range			Full range		29		μA

† Full range is –40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLE2061I TLE2061AI TLE2061BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.2	3.4		V/μs
				Full range	1.7			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz,	R_S = 20 Ω			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		1.8		MHz
		R_L = 100 Ω,	C_L = 100 pF			1.3		
t_s	Settling time	0.1%		25°C		5		μs
		0.01%				10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		58°		
		R_L = 100 Ω,	C_L = 100 pF			75°		

† Full range is –40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2061I, TLE2061AI TLE2061BI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2061I	V_{IC} = 0, R_S = 50 Ω	25°C		0.6	3	mV
				Full range			4.3	
		TLE2061AI		25°C		0.5	1.5	
				Full range			2.9	
		TLE2061BI		25°C		0.3	0.5	
				Full range			1.3	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			3	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			5	nA
V_{ICR}	Common-mode input voltage range			25°C	–11 to 13	–12 to 16		V
				Full range	–11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	13.7		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	–13.2	–13.7		V
				Full range	–13			
			R_L = 600 Ω	25°C	–12.5	–13		
				Full range	–12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	10			
			V_O = 0 to –8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current		V_O = 0, No load	25°C		290	350	μA
				Full range			375	
ΔI_{CC}	Supply-current change over operating temperature range			Full range		34		μA

† Full range is –40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS		T_A†	TLE2061I TLE2061AI TLE2061BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.6	3.4		V/μs
				Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	R_S = 20 Ω			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF			1.5		
t_s	Settling time	0.1%		25°C		5		μs
		0.01%				10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF			70°		

† Full range is –40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2061M TLE2061AM TLE2061BM MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2061M	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.8	3.1	mV
				Full range			6	
		TLE2061AM		25°C		0.6	2.6	
				Full range			4.6	
		TLE2061BM		25°C		0.5	1.9	
				Full range			3.1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			15	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			30	nA
V_{ICR}	Common-mode input voltage range			25°C	–1.6 to 4	–2 to 6		V
				Full range	–1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	3.5	3.7		V
				Full range	3			
			$R_L = 600\ \Omega$	25°C	2.5	3.6		
				Full range	2			
			$R_L = 100\ \Omega$	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	–3.5	–3.9		V
				Full range	–3			
		FK and JG packages	$R_L = 600\ \Omega$	25°C	–2.5	–3.5		
				Full range	–2			
		D and P packages	$R_L = 100\ \Omega$	25°C	–2.5	–2.7		
				Full range	–2			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 2.8$ V, $R_L = 10\ k\Omega$	25°C	15	80		V/mV
				Full range	2			
		FK and JG packages	$V_O = 0$ to 2.5 V, $R_L = 600\ \Omega$	25°C	1	65		
				Full range	0.5			
			$V_O = 0$ to –2.5 V, $R_L = 600\ \Omega$	25°C	1	16		
				Full range	0.5			
		D and P packages	$V_O = 0$ to 2 V, $R_L = 100\ \Omega$	25°C	0.75	45		
				Full range	0.5			
			$V_O = 0$ to –2 V, $R_L = 100\ \Omega$	25°C	0.5	3		
				Full range	0.25			

† Full range is –55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm5$ V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLE2061M TLE2061AM TLE2061BM MIN	TYP	MAX	UNIT
r_i	Input resistance		25°C		10^{12}		Ω
c_i	Input capacitance		25°C		4		pF
z_o	Open-loop output impedance	$I_O = 0$	25°C		280		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $R_S = 50\ \Omega$	25°C	65	82		dB
			Full range	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm5$ V to ±15 V, $R_S = 50\ \Omega$	25°C	75	93		dB
			Full range	65			
I_{CC}	Supply current	$V_O = 0$, No load	25°C		280	325	μA
			Full range			350	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		39		μA

† Full range is –55°C to 125°C.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TLE2061M TLE2061AM TLE2061BM MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	$R_L = 10\ k\Omega$,	$C_L = 100$ pF		3.4		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	$R_S = 20\ \Omega$		59		nV/√Hz
		f = 1 kHz,	$R_S = 20\ \Omega$		43		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		μV
I_n	Equivalent input noise current	f = 1 kHz			1		fA/√Hz
THD	Total harmonic distortion	$A_{VD} = 2$, $V_{O(PP)} = 2$ V,	f = 10 kHz, $R_L = 10\ k\Omega$		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	$R_L = 10\ k\Omega$,	$C_L = 100$ pF		1.8		MHz
		$R_L = 600\ \Omega$,	$C_L = 100$ pF		1.3		
t_s	Settling time	0.1%			5		μs
		0.01%			10		
B_{OM}	Maximum output-swing bandwidth	$A_{VD} = 1$,	$R_L = 10\ k\Omega$		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	$R_L = 10\ k\Omega$,	$C_L = 100$ pF		58°		
		$R_L = 600\ \Omega$,	$C_L = 100$ pF		75°		

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2061M, TLE2061AM TLE2061BM MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2061M	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.6	3	mV
				Full range			6	
		TLE2061AM		25°C		0.5	1.5	
				Full range			3.6	
		TLE2061BM		25°C		0.3	0.5	
				Full range			1.7	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			20	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			40	nA
V_{ICR}	Common-mode input voltage range			25°C	–11 to 13	–12 to 16		V
				Full range	–11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	13	13.7		V
				Full range	12.5			
			$R_L = 600\ \Omega$	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	–13	–13.7		V
				Full range	–12.5			
			$R_L = 600\ \Omega$	25°C	–12.5	–13		
				Full range	–12			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 10$ V, $R_L = 10\ k\Omega$	25°C	30	230		V/mV
				Full range	20			
			$V_O = 0$ to 8 V, $R_L = 600\ \Omega$	25°C	25	100		
				Full range	7			
			$V_O = 0$ to – 8 V, $R_L = 600\ \Omega$	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		280		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\min$, $R_S = 50\ \Omega$	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 15 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current		$V_O = 0$, No load	25°C		290	350	μA
				Full range			375	
ΔI_{CC}	Supply-current change over operating temperature range			Full range		46		μA

† Full range is –55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS		T_A†	TLE2061M TLE2061AM TLE2061BM MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2	3.4		V/μs
				Full range	1.8			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		70		nV/√Hz
		f = 1 kHz,	R_S = 20 Ω	25°C		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF	25°C		1.5		
t_s	Settling time	0.1%		25°C		5		μs
		0.01%		25°C		10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF	25°C		70°		

† Full range is –55°C to 125°C.

electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

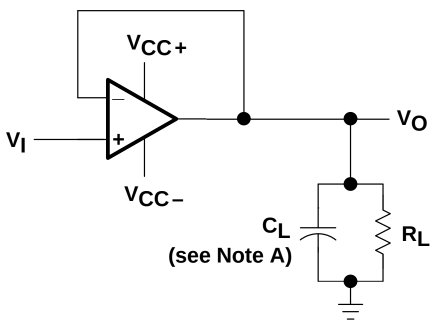
PARAMETER		TEST CONDITIONS		TLE2061Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 50 Ω		0.6	3	mV
α_{VIO}	Input offset voltage long-term drift (see Note 4)	V_{IC} = 0,	R_S = 50 Ω		0.04		μV/mo
I_{IO}	Input offset current	V_{IC} = 0,	R_S = 50 Ω		2		pA
I_{IB}	Input bias current	V_{IC} = 0,	R_S = 50 Ω		4		pA
V_{ICR}	Common-mode input voltage range			–11 to 13	–12 to 16		V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		13.2	13.7		V
		R_L = 600 Ω		12.5	13.2		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		–13.2	–13.7		V
		R_L = 600 Ω		–12.5	– 13		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L = 10 kΩ	30	230		V/mV
		V_O = 0 to 8 V,	R_L = 600 Ω	25	100		
		V_O = 0 to – 8 V,	R_L = 600 Ω	3	25		
r_i	Input resistance				10^{12}		Ω
c_i	Input capacitance				4		pF
z_o	Open-loop output impedance	I_O = 0			280		Ω
CMRR	Common-mode rejection ratio	R_S = 50 Ω,	$V_{IC} = V_{ICR}$min	72	90		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω		75	93		dB
I_{CC}	Supply current	V_O = 0,	No load		290	350	μA

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2061Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ,	C_L = 100 pF	2.6	3.4		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω		70		nV/√Hz
		f = 1 kHz,	R_S = 20 Ω		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		μV
I_n	Equivalent input noise current	f = 1 Hz			1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		2		MHz
		R_L = 600 Ω,	C_L = 100 pF		1.5		
t_s	Settling time	0.1%			5		μs
		0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		60°		
		R_L = 600 Ω,	C_L = 100 pF		70°		

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

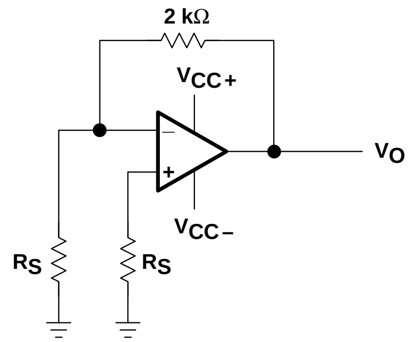
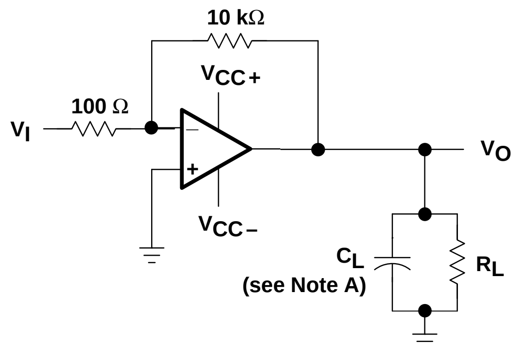


Figure 2. Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Unity-Gain Bandwidth and Phase-Margin Test Circuit

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoampere bias-current level typical of the TLE2061, TLE2061A, and TLE2061B, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted mathematically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	4
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	5 6
I_{IO}	Input offset current	vs Free-air temperature	6
V_{ICR}	Common-mode input voltage range limits	vs Free-air temperature	7
V_{OM}	Maximum peak output voltage	vs Output current vs Supply voltage	8, 9 10, 11, 12
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	13, 14
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	15 16
I_{OS}	Short-circuit output current	vs Time vs Free-air temperature	17 18
z_o	Output impedance	vs Frequency	19
CMRR	Common-mode rejection ratio	vs Frequency	20
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	21 22
	Pulse response	Small signal Large signal	23, 24 25, 26
	Noise voltage (referred to input)	0.1 to 10 Hz	27
V_n	Equivalent input noise voltage	vs Frequency	28
THD	Total harmonic distortion	vs Frequency	29, 30
B_1	Unity-gain bandwidth	vs Supply voltage vs Free-air temperature	31 32
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance vs Free-air temperature	33 34 35
	Phase shift	vs Frequency	15

TYPICAL CHARACTERISTICS†

**TLE2061
DISTRIBUTION OF
INPUT OFFSET VOLTAGE**

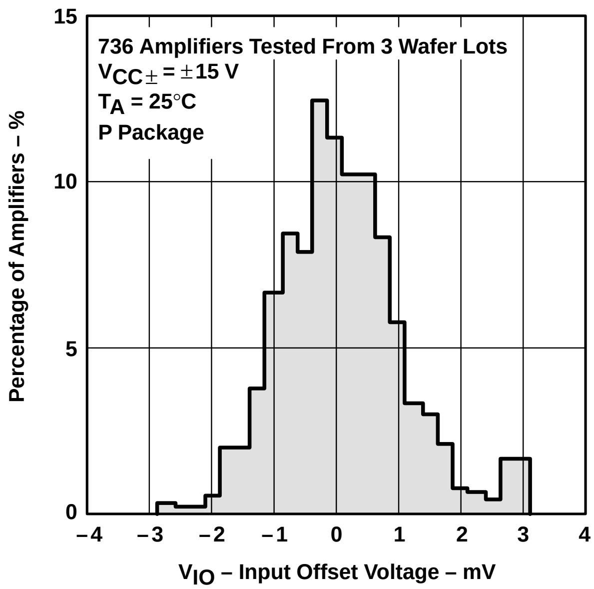


Figure 4

**INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE**

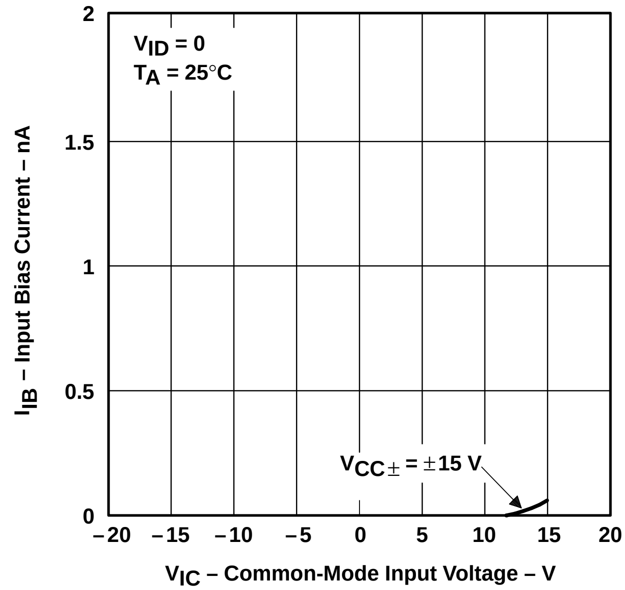


Figure 5

**INPUT BIAS CURRENT
AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE**

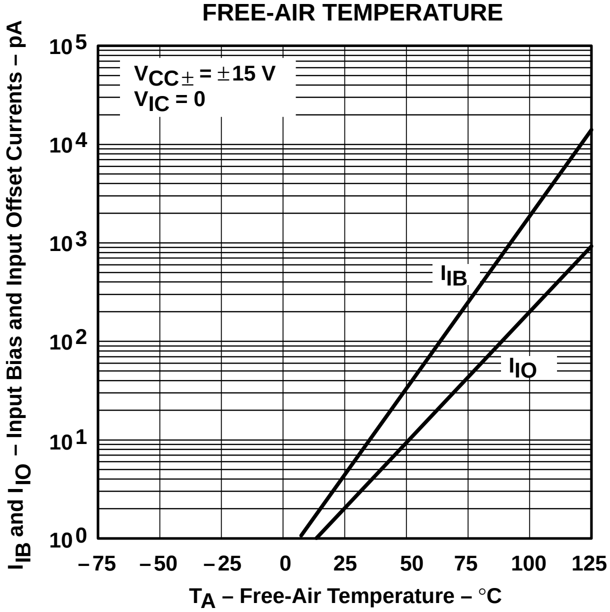


Figure 6

**COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE**

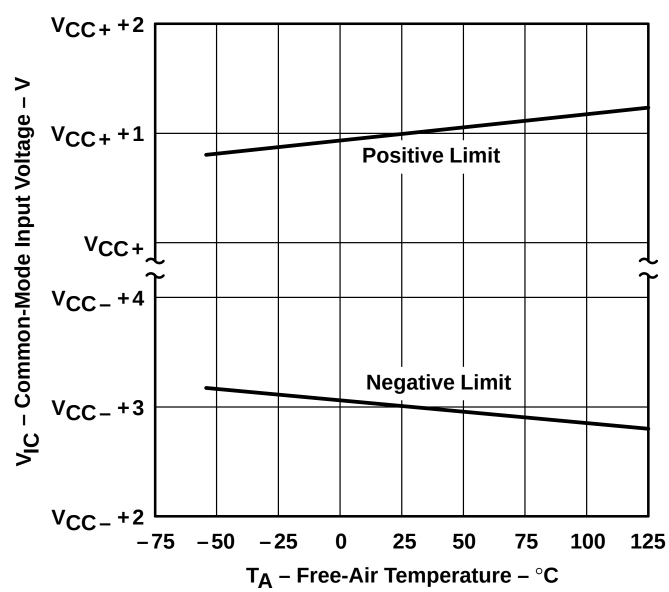


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

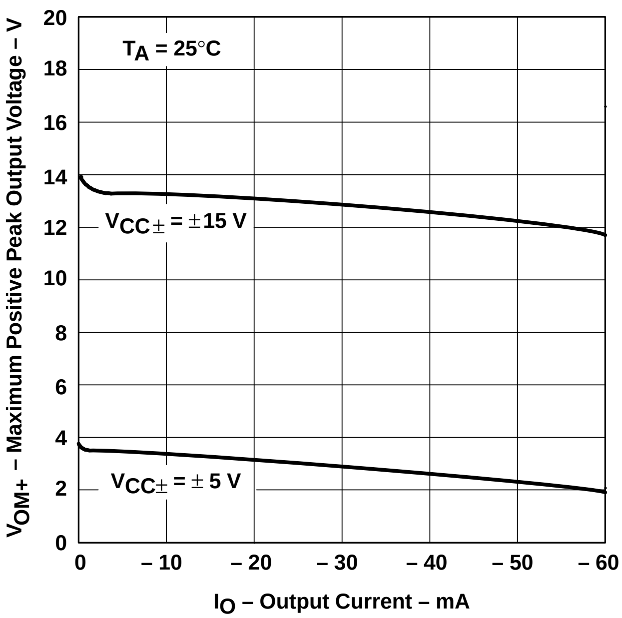


Figure 8

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

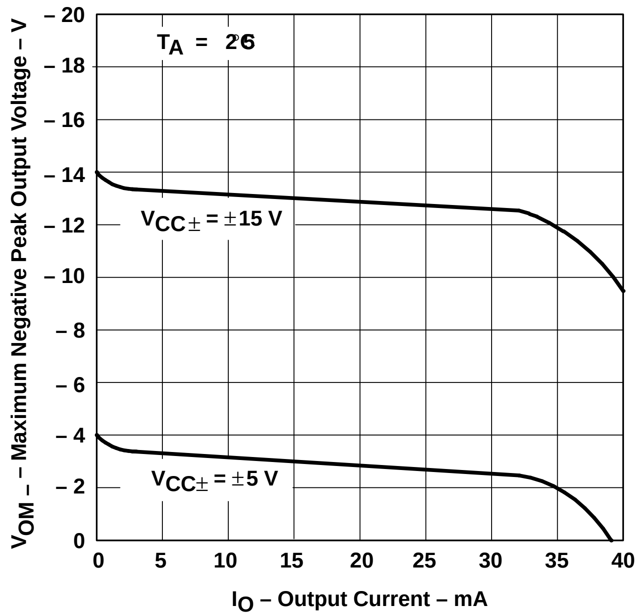


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

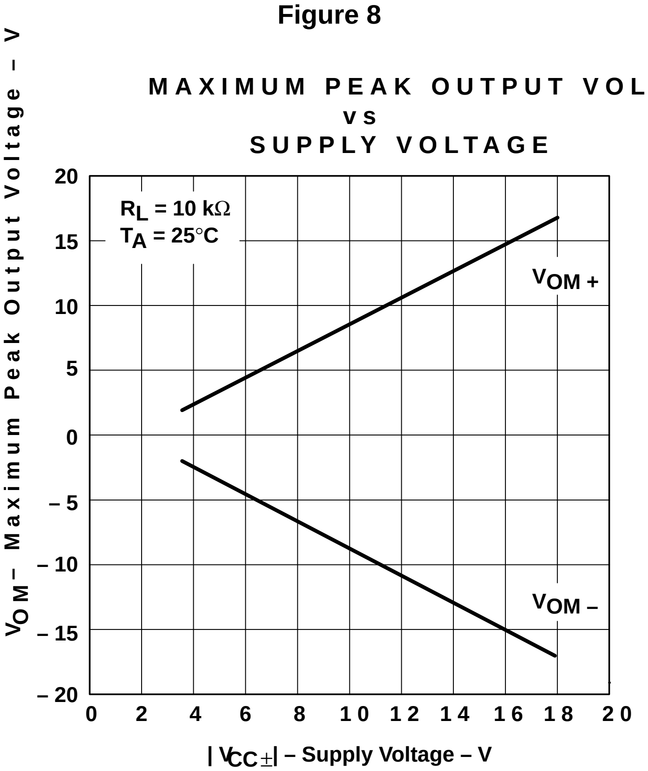


Figure 10

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

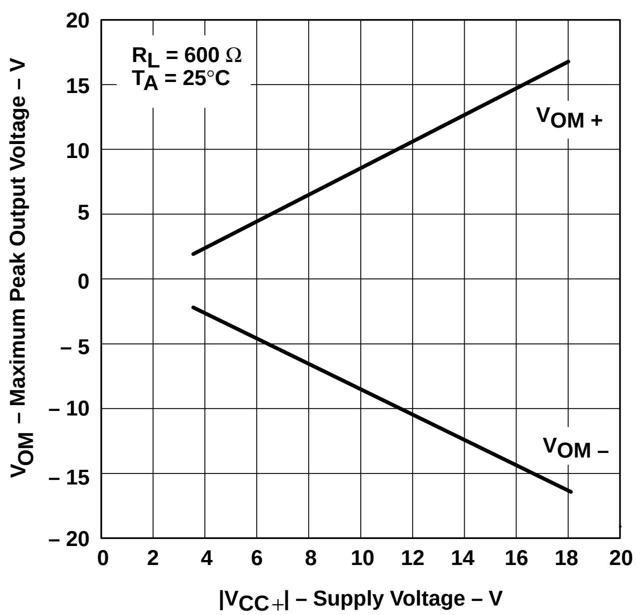


Figure 11

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

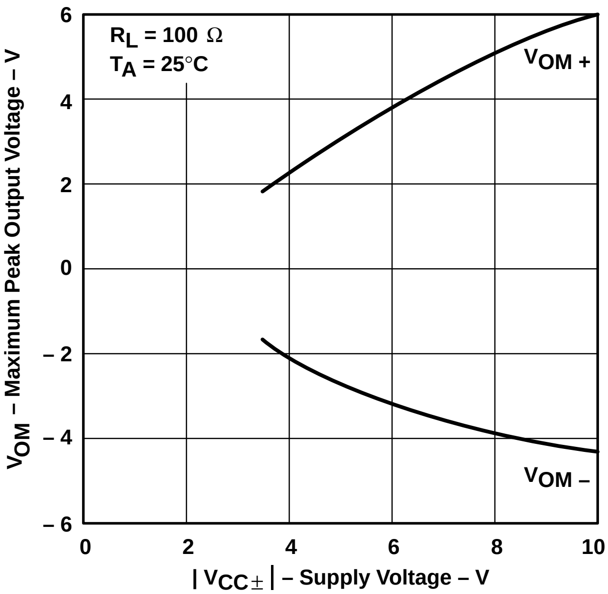


Figure 12

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

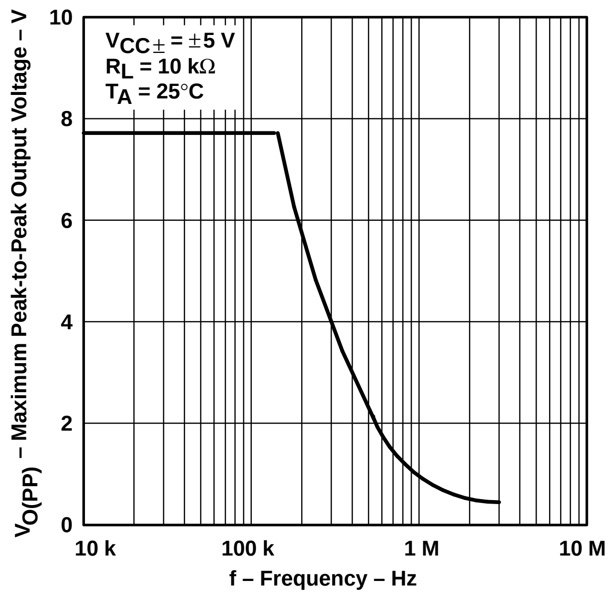


Figure 13

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

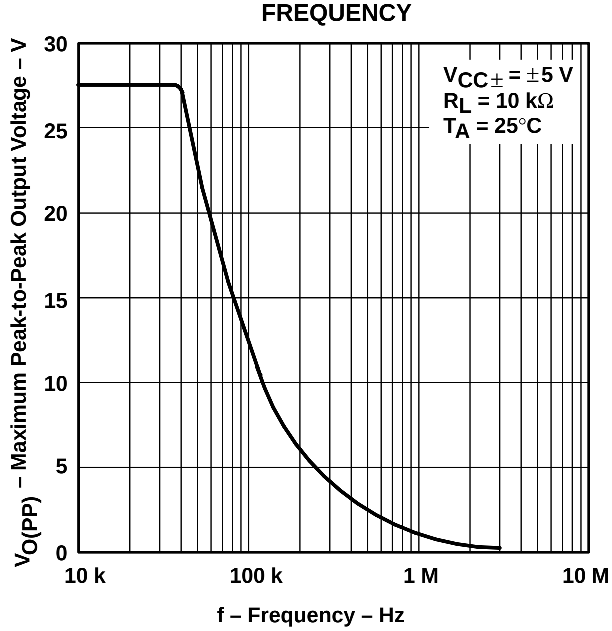


Figure 14

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

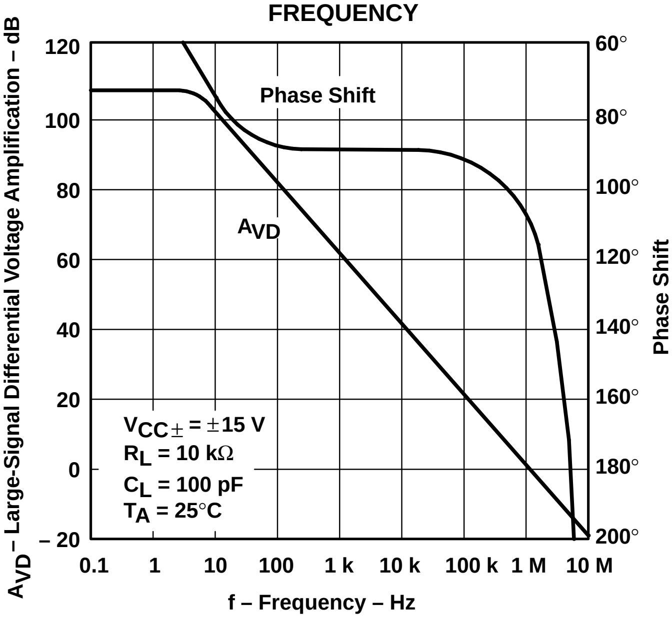


Figure 15

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

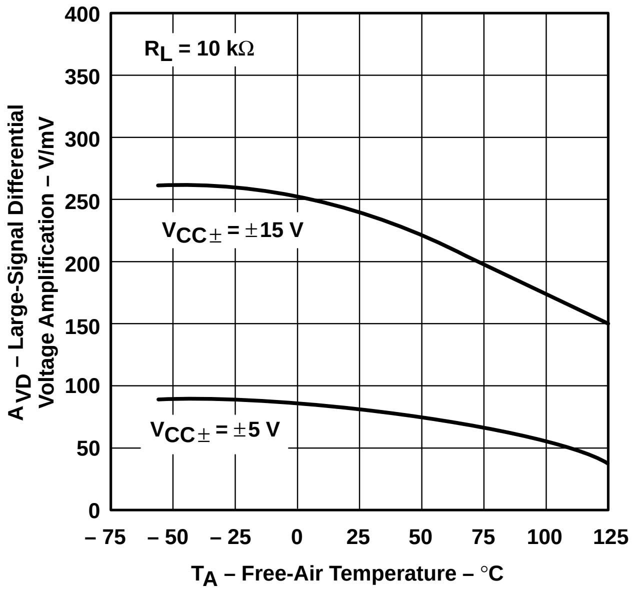


Figure 16

SHORT-CIRCUIT OUTPUT CURRENT vs ELAPSED TIME

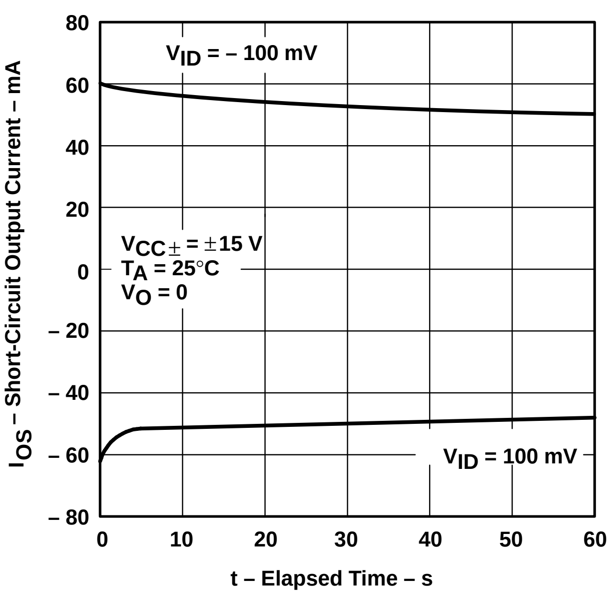


Figure 17

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

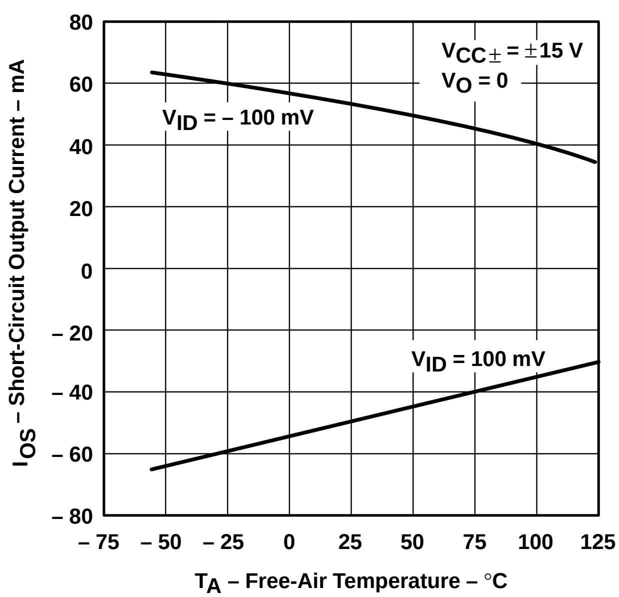


Figure 18

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

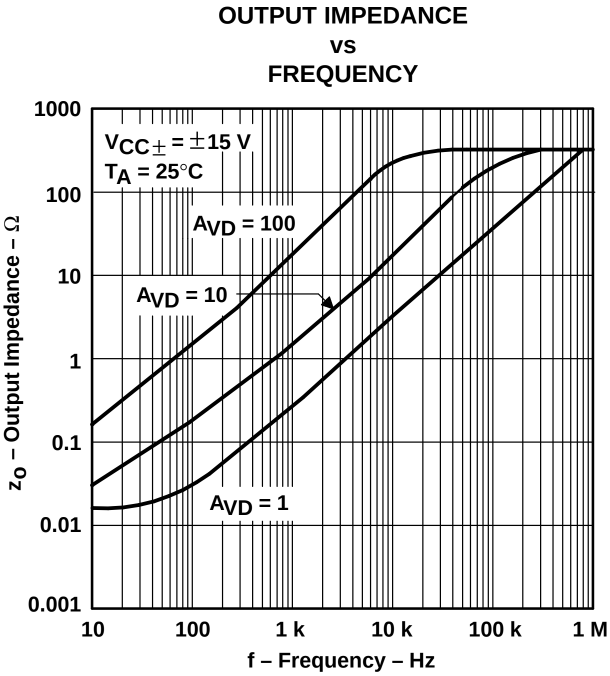


Figure 19

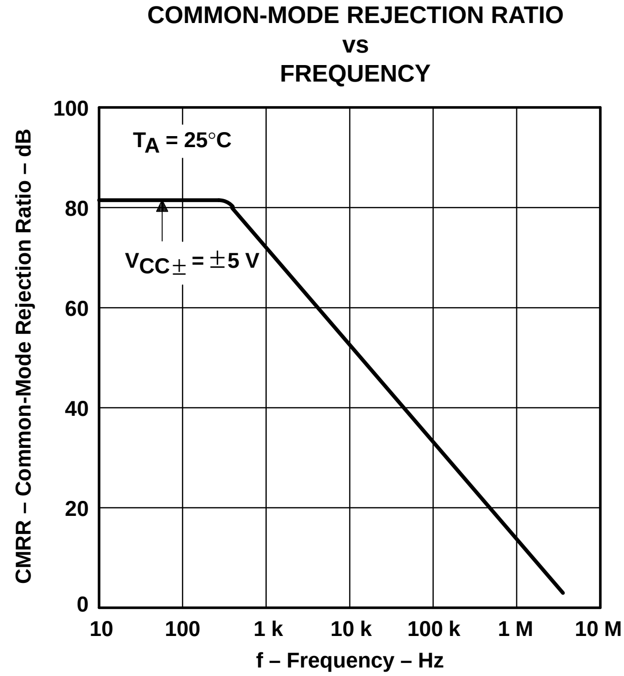


Figure 20

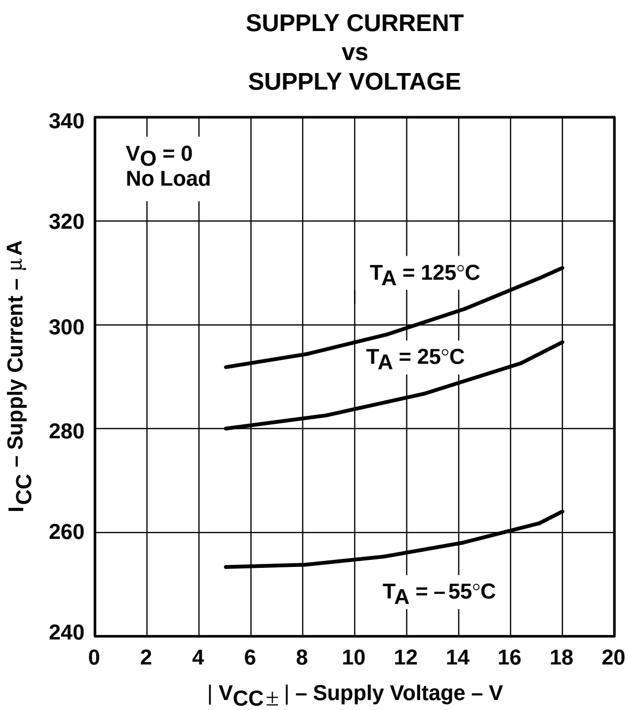


Figure 21

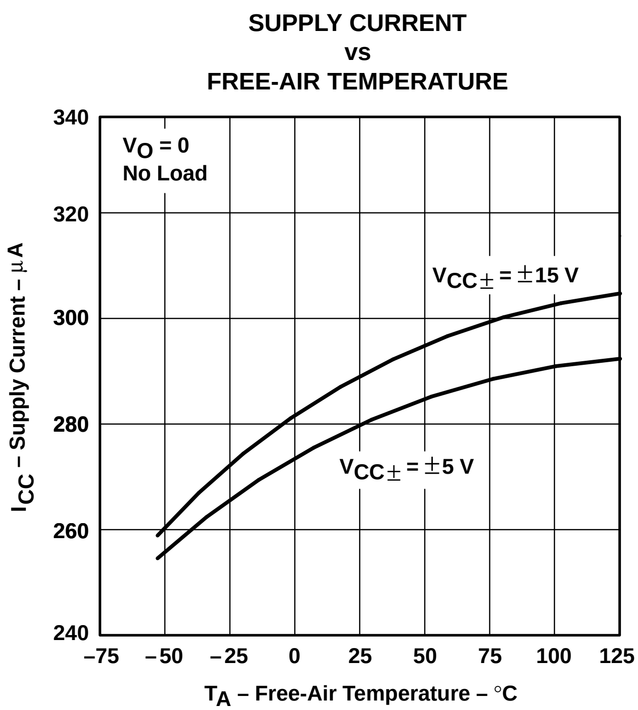


Figure 22

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

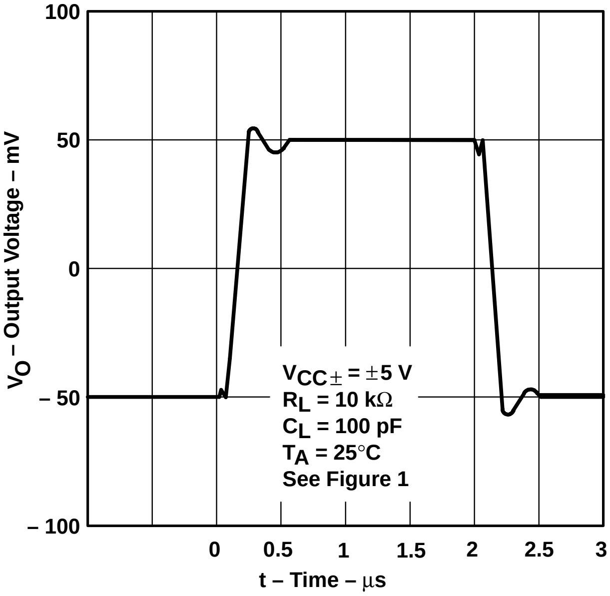


Figure 23

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

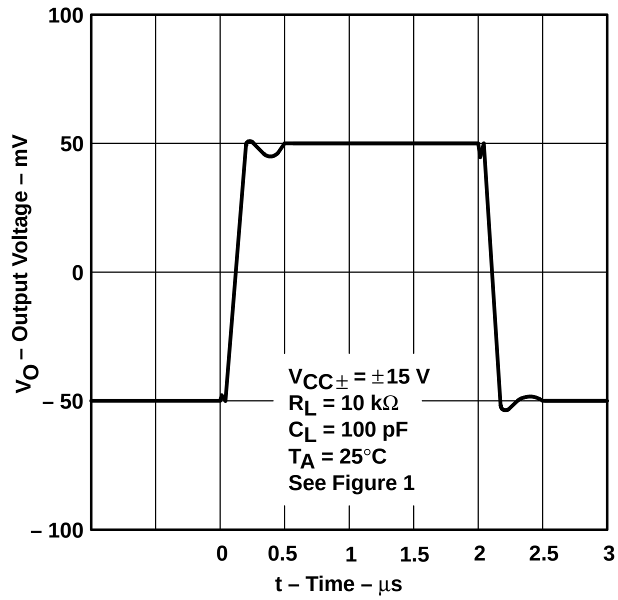


Figure 24

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

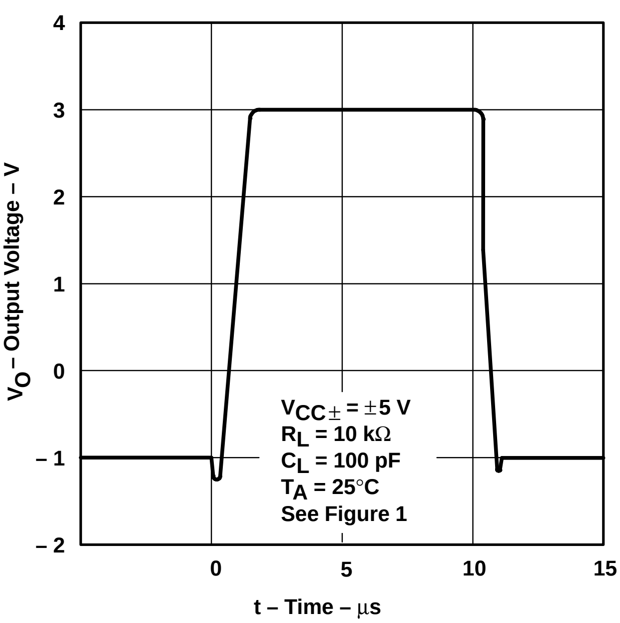


Figure 25

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

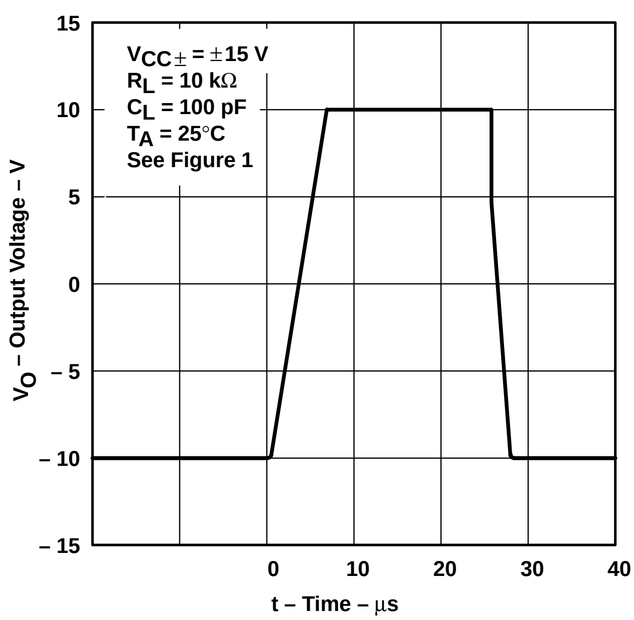


Figure 26

TYPICAL CHARACTERISTICS

NOISE VOLTAGE (REFERRED TO INPUT) OVER A 10-SECOND INTERVAL

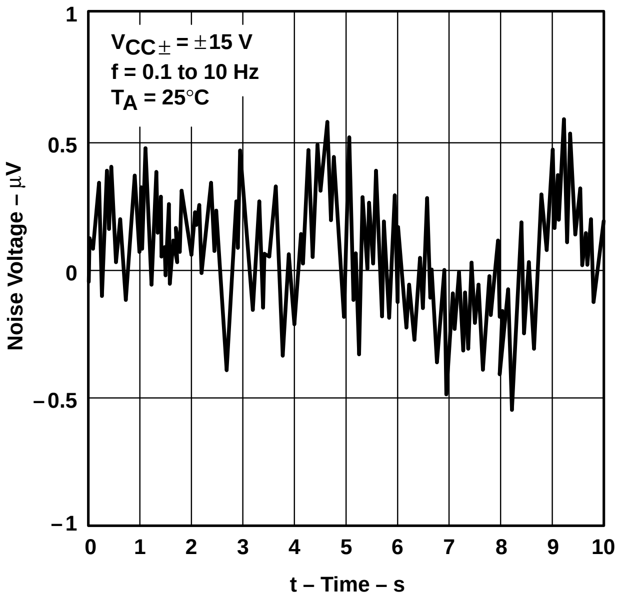


Figure 27

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

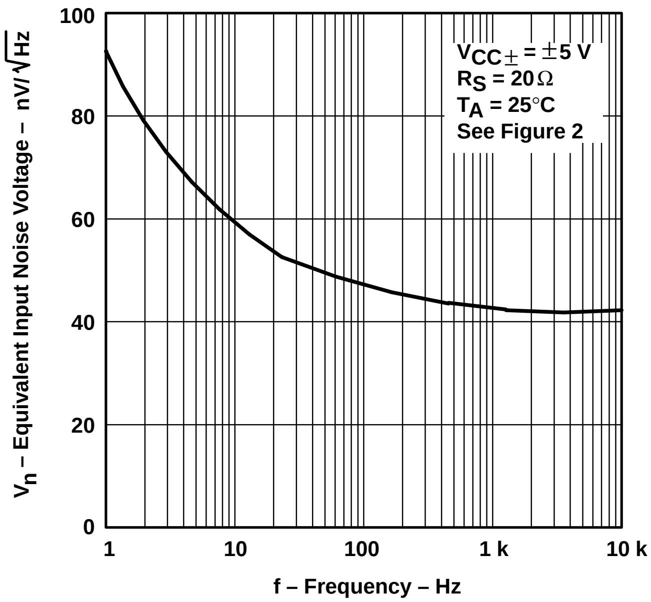


Figure 28

TOTAL HARMONIC DISTORTION vs FREQUENCY

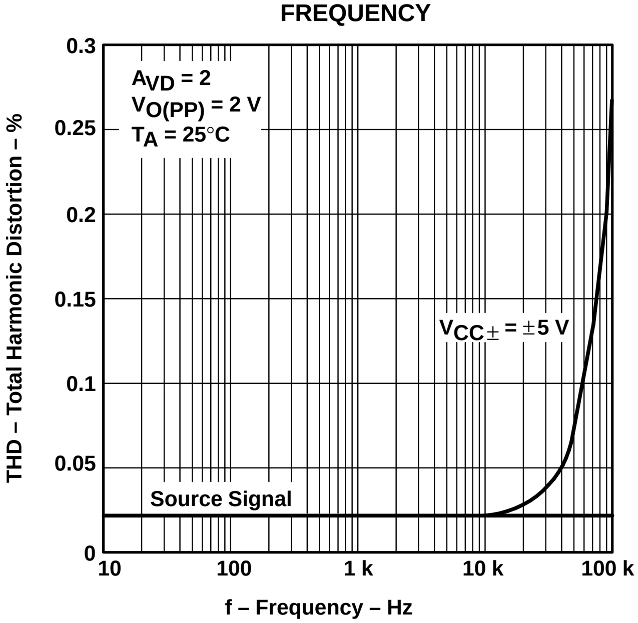


Figure 29

TOTAL HARMONIC DISTORTION vs FREQUENCY

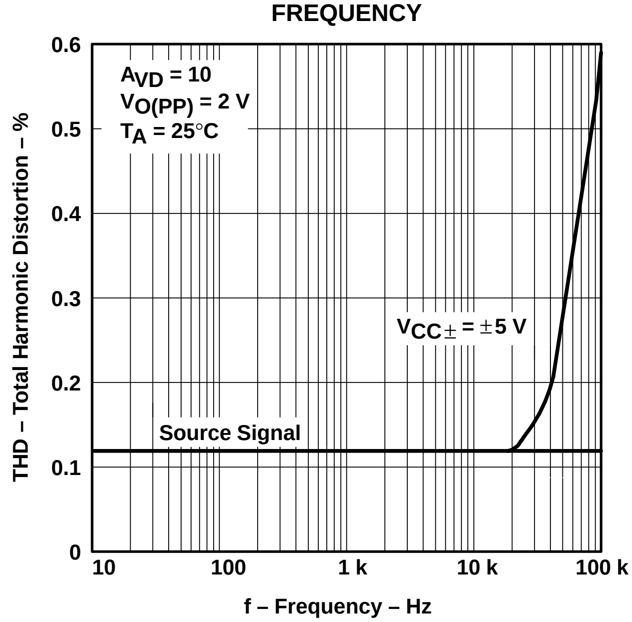


Figure 30

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

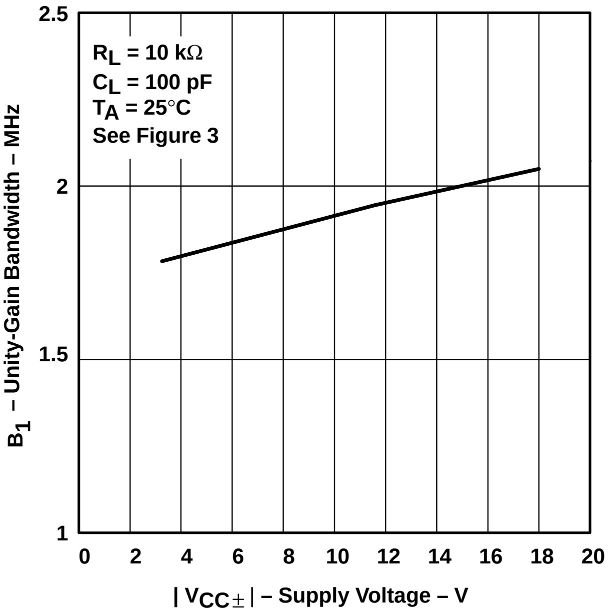


Figure 31

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

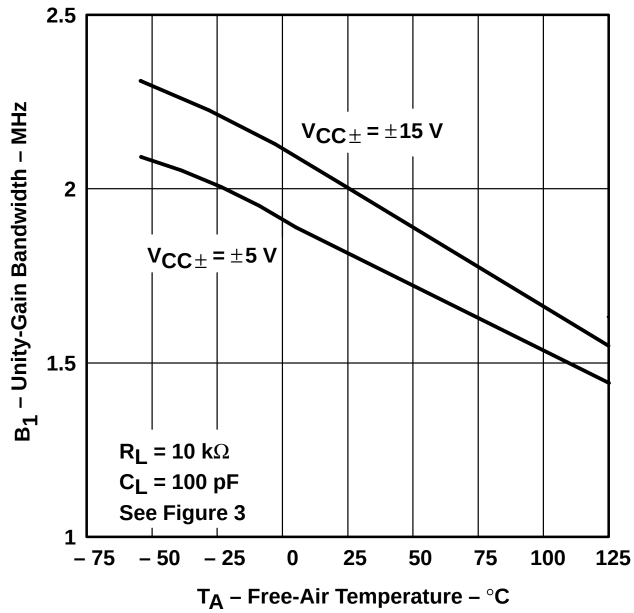


Figure 32

PHASE MARGIN
vs
SUPPLY VOLTAGE

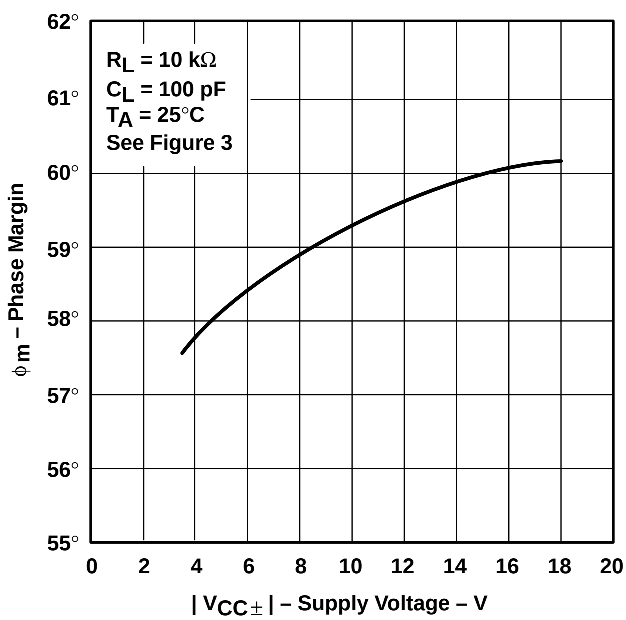


Figure 33

PHASE MARGIN
vs
LOAD CAPACITANCE

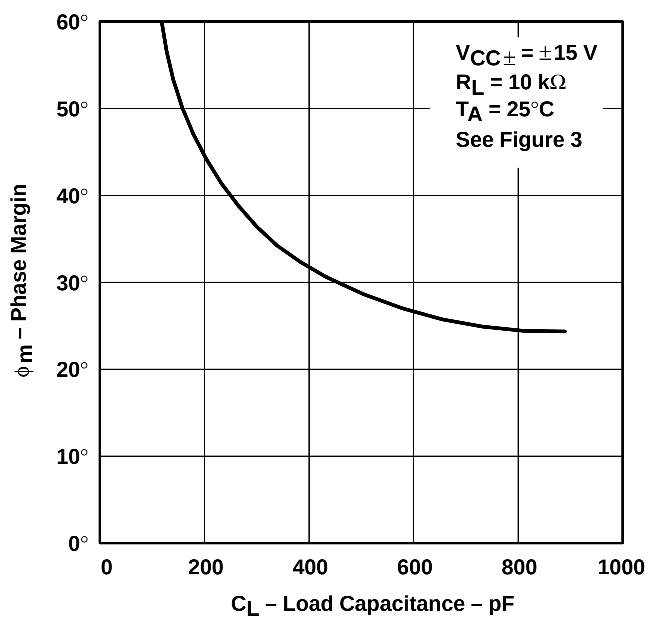
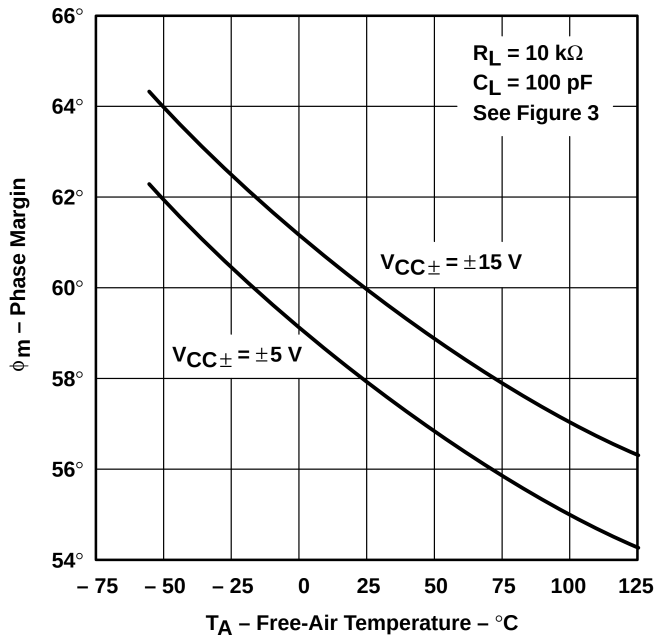


Figure 34

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
FREE-AIR TEMPERATURE†



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 35

APPLICATION INFORMATION

macromodel information

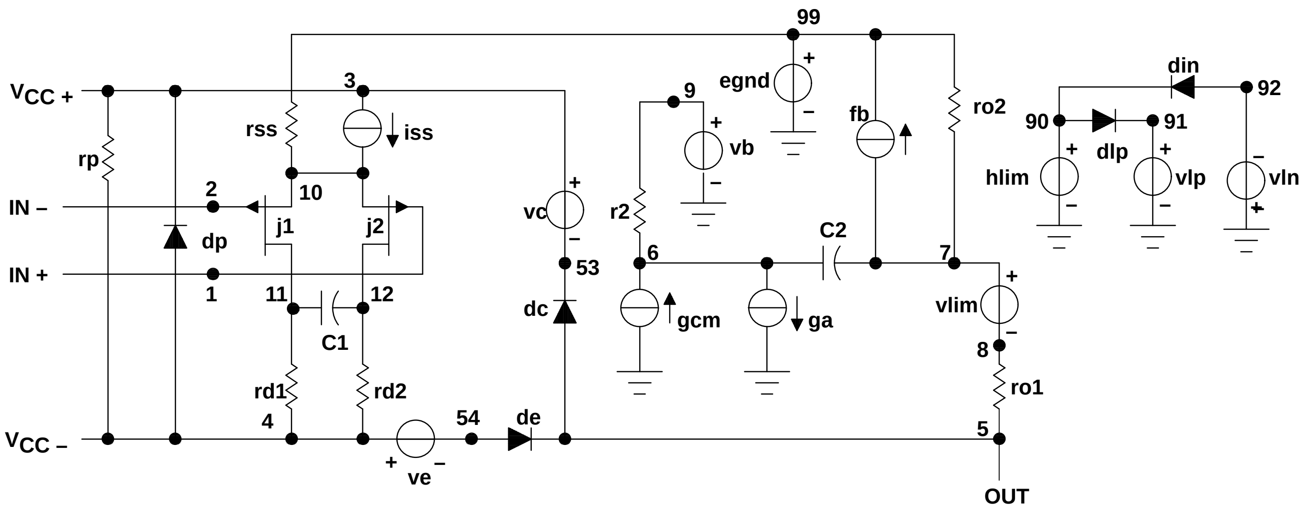
Macromodel information provided is derived using Microsim *PSpice*™ and Microsim *Parts*™ model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figure 36 are generated using the TLE2061 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers”, *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

APPLICATION INFORMATION

macromodel information (continued)




```
.subckt TLE2061 1 2 3 4 5
  c1   11   12  1.457E–12
  c2    6   7   15.00E–12
  dc    5   53  dx
  de   54   5   dx
  dlp  90   91  dx
  dln  92   90  dx
  dp    4   3   dx
  egnd 99   0   poly(2) (3,0) (4,0) 0 .5 .5
  fb    7   99  poly(5) vb vc ve vlp vln 0 4.357E6  –4E6 4E6 4E6 –4E6
  ga    6   0   11 12 188.5E–6
  gcm   0   6   10 99 3.352E–9
  iss   3   10  dc 51.00E–6
  hlim 90   0   vlim 1K
  j1   11   2   10 jx
  j2   12   1   10 jx
  r2    6   9   100.0E3
  rd1   4  11   5.305E3
  rd2   4  12   5.305E3
  ro1   8   5   280
  ro2   7  99   280
  rp    3   4   113.2E3
  rss  10  99   3.922E6
  vb    9   0   dc 0
  vc    3  53   dc 2
  ve   54   4   dc 2
  vlim  7   8   dc 0
  vlp  91   0   dc 50
  vln   0  92   dc 50
.model dx D(Is=800.0E–18)
.model jx PJF(Is=2.000E–12 Beta=423E–6 Vto=–1)
.ends
```

Figure 36. Boyle Macromodel and Subcircuit

APPLICATION INFORMATION

input characteristics

The TLE2061, TLE2061A, and TLE2061B are specified with a minimum and a maximum input voltage that if exceeded at either input could cause the device to malfunction. Because of the extremely high input impedance and resulting low bias current requirements, the TLE2061, TLE2061A, and TLE2061B are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 37). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

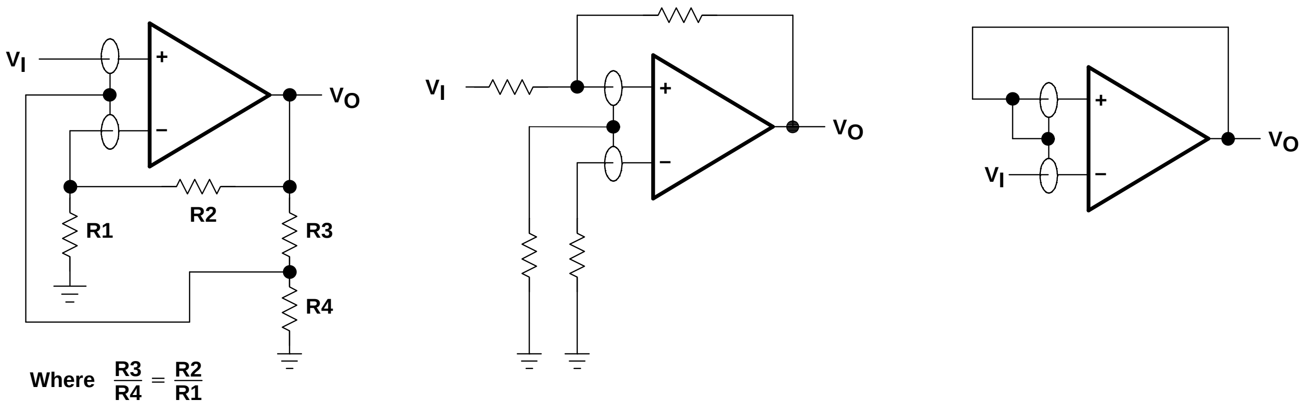


Figure 37. Use of Guard Rings

input offset voltage nulling

The TLE2061 series offers external null pins that can be used to further reduce the input offset voltage. The circuit of Figure 38 can be connected as shown if the feature is desired. When external nulling is not needed, the null pins may be left unconnected.

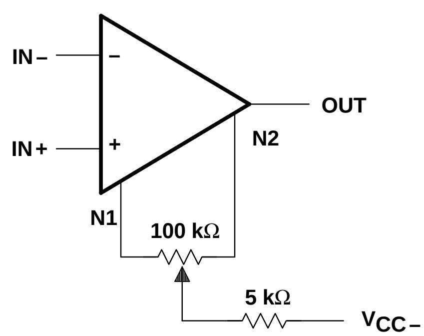


Figure 38. Input Offset Voltage Nulling

IMPORTANT NOTICE