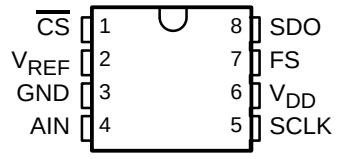
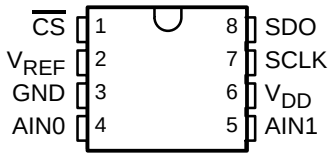
- **Maximum Throughput . . . 175/360 KSPS**
- **INL/DNL: ±1 LSB Max, SINAD: 72 dB, SFDR: 85 dB, f_i = 20 kHz**
- **SPI/DSP-Compatible Serial Interface**
- **Single 5-V Supply**
- **Rail-to-Rail Analog Input With 500 kHz BW**
- **Three Options Available:**
  - **TLC2551: Single Channel Input**
  - **TLC2552: Dual Channels With Autosweep**
  - **TLC2555: Single Channel With Pseudo-Differential Input**
- **Low Power With Autopower Down**
  - **Operating Current: 3.5 mA**
  - **Autopower Down: 8 μA**
- **Small 8-Pin MSOP and SOIC Packages**

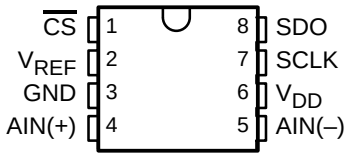
TOP VIEW
TLC2551



TOP VIEW
TLC2552



TOP VIEW
TLC2555



description

The TLC2551, TLC2552, and TLC2555 are a family of high performance, 12-bit, low-power, miniature, CMOS analog-to-digital converters (ADC). The TLC255x family uses a 5-V supply. Devices are available with single, dual, or single pseudo-differential inputs. Each device has a chip select ($\overline{CS}$), serial clock (SCLK), and serial data output (SDO) that provides a direct 3-wire interface to the serial port of most popular host microprocessors (SPI interface). When interfaced with a TMS320™ DSP, a frame sync signal (FS) can be used to indicate the start of a serial data frame on $\overline{CS}$ for all devices or on FS for the TLC2551.

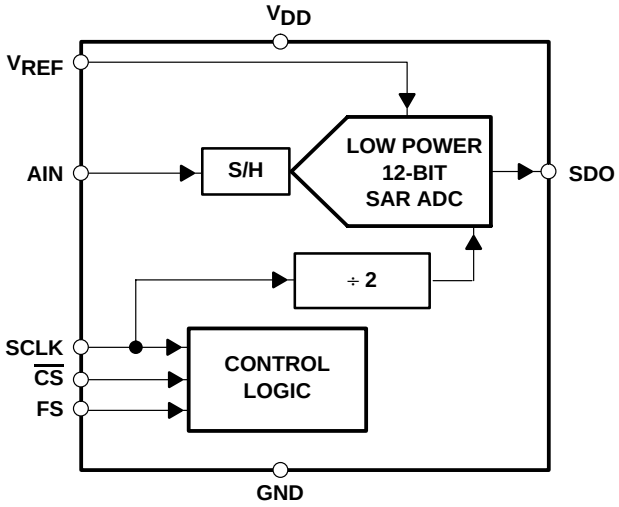
The TLC2551, TLC2552, and TLC2555 are designed to operate with very low power consumption. The power saving feature is further enhanced with an autopower-down mode. This product family features a high-speed serial link to modern host processors with SCLK up to 20 MHz. The maximum SCLK frequency is dependent upon the mode of operation (see Table 1). The TLC255x family uses SCLK as the conversion clock, which provides synchronous operation and a minimum conversion time of 1.5 μs using a 20-MHz SCLK.

AVAILABLE OPTIONS

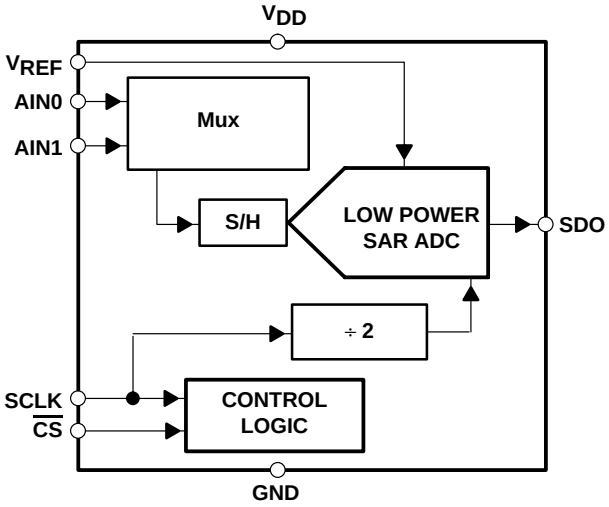
T_A	PACKAGED DEVICES	
	8-MSOP (DGK)	8-SOIC (D)
0°C to 70°C	TLC2551CDGK (AHF)	
	TLC2552CDGK (AHH)	
	TLC2555CDGK (AHJ)	
–40°C to 85°C	TLC2551IDGK (AHG)	TLC2551ID
	TLC2552IDGK (AHI)	TLC2552ID
	TLC2555IDGK (AHK)	TLC2555ID

functional block diagram

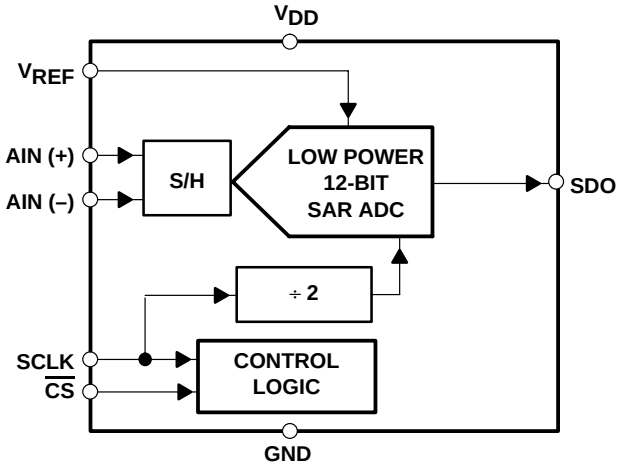
TLC2551



TLC2552



TLC2555



Terminal Functions

TLC2551

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AIN	4	I	Analog input channel
$\overline{CS}$	1	I	Chip select. A high-to-low transition on the $\overline{CS}$ input removes SDO from 3-state within a maximum setup time. $\overline{CS}$ can be used as the FS pin when a dedicated DSP serial port is used.
FS	7	I	DSP frame sync input. Indication of the start of a serial data frame. Tie this terminal to V_{DD} if not used.
GND	3	I	Ground return for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
SCLK	5	I	Output serial clock. This terminal receives the serial SCLK from the host processor.
SDO	8	O	The 3-state serial output for the A/D conversion result. SDO is kept in the high-impedance state until $\overline{CS}$ falling edge or FS rising edge, whichever occurs first. The output format is MSB first. When FS is not used (FS = 1 at the falling edge of $\overline{CS}$), the MSB is presented to the SDO pin after $\overline{CS}$ falling edge and output data is valid on the first falling edge of SCLK. When $\overline{CS}$ and FS are both used (FS = 0 at the falling edge of $\overline{CS}$), the MSB is presented to the SDO pin after the falling edge of $\overline{CS}$. When $\overline{CS}$ is tied/held low, the MSB is presented on SDO after rising FS. Output data is valid on the first falling edge of SCLK. (This is typically used with an active FS from a DSP.)
V_{DD}	6	I	Positive supply voltage
V_{REF}	2	I	External reference input

TLC2552/55

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AIN0 /AIN(+)	4	I	Analog input channel 0 for TLC2552—Positive input for TLC2555
AIN1/AIN (–)	5	I	Analog input channel 1 for TLC2552—Inverted input for TLC2555
$\overline{CS}$	1	I	Chip select. A high-to-low transition on $\overline{CS}$ removes SDO from 3-state within a maximum delay time. This pin can be connected to the FS output from a DSP on a dedicated serial port.
GND	3	I	Ground return for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
SCLK	7	I	Output serial clock. This terminal receives the serial SCLK from the host processor.
SDO	8	O	The 3-state serial output for the A/D conversion result. SDO is kept in the high-impedance state when $\overline{CS}$ is high and presents output data after the $\overline{CS}$ falling edge until the LSB is presented. The output format is MSB first. SDO returns to the Hi-Z state after the 16th SCLK. Output data is valid on the falling SCLK edge.
V_{DD}	6	I	Positive supply voltage
V_{REF}	2	I	External reference input

detailed description

The TLC2551, TLC2552, and TLC2555 are successive approximation (SAR) ADCs utilizing a charge redistribution DAC. Figure 1 shows a simplified version of the ADC.

The sampling capacitor acquires the signal on AIN during the sampling period. When the conversion process starts, the SAR control logic and charge redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator into a balanced condition. When the comparator is balanced, the conversion is complete and the ADC output code is generated.

detailed description (continued)

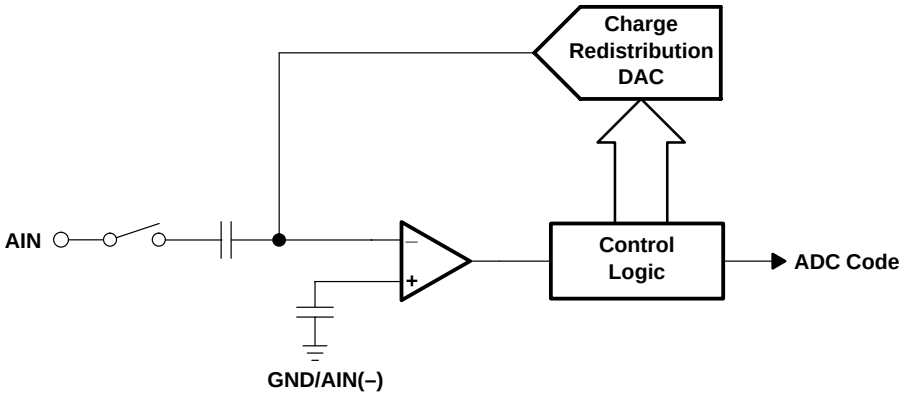


Figure 1. Simplified SAR Circuit

serial interface

OUTPUT DATA FORMAT	
MSB	**LSB**
D15–D4	D3–D0
Conversion result (OD11–OD0)	Don't care

The output data format is binary (unipolar straight binary).

binary

Zero-scale code = 000h, Vcode = GND
Full-scale code = FFFh, Vcode = V_{REF} – 1 LSB

pseudo-differential inputs

The TLC2555 operates in pseudo-differential mode. The inverted input is available on pin 5. It can have a maximum input ripple of ±0.2 V. This is normally used for ground noise rejection.

control and timing

start of the cycle

Each cycle may be started by either $\overline{CS}$, FS, or a combination of both. The internal state machine requires one SCLK high-to-low transition to determine the state of these control signals so internal blocks can be powered up in an active cycle. Special care to SPI mode is necessary. Make sure there is at least one SCLK whenever $\overline{CS}$ (pin 1) is high to assure proper operation.

TLC2551

- Control via $\overline{CS}$ (FS = 1 at the falling edge of $\overline{CS}$)—The falling edge of $\overline{CS}$ is the start of the cycle. The MSB may be read on the first falling SCLK edge after $\overline{CS}$ is low. Output data changes on the rising edge of SCLK. This is typically used for a microcontroller with an SPI interface, although it can also be used for a DSP. The microcontroller SPI interface may be programmed for CPOL = 0 (serial clock referenced to ground) and CPHA = 1 (data is valid on the falling edge of serial clock). At least one falling edge transition on SCLK is needed whenever $\overline{CS}$ is brought high.
- Control via FS—The MSB is presented after the rising edge of FS. The falling edge of FS starts the cycle. The MSB may be read on the first falling edge of SCLK after FS is low. This is the typical configuration when the ADC is the only device on the DSP serial port.

control and timing (continued)

- Control via both $\overline{CS}$ and FS—The MSB is presented after the falling edge of $\overline{CS}$. The falling edge of FS starts the sampling cycle. The MSB may be read on the first falling SCLK edge after FS is low. Output data changes on the rising edge of SCLK. This control via $\overline{CS}$ and FS is typically used for multiple devices connected to a TMS320 DSP.

TLC2552 and TLC2555

All control is provided using $\overline{CS}$ (pin 1) on the TLC2552 and TLC2555. The cycle starts on the falling edge transition provided by either a $\overline{CS}$ signal from an SPI microcontroller or FS signal from a TMS320 DSP. Timing is similar to the TLC2551, with control via $\overline{CS}$ only.

TLC2552 channel MUX reset cycle

The TLC2552 uses $\overline{CS}$ to reset the analog input multiplexer (MUX). A short active $\overline{CS}$ cycle (4 to 7 SCLKs) resets the MUX to AIN0. When the $\overline{CS}$ cycle time is greater than 7 SCLKs in duration, as is the case for a complete conversion cycle, ($\overline{CS}$ is low for 16 SCLKs plus maximum conversion time), the MUX toggles to the next channel (see Figure 4 for timing).

sampling

The converter sample time is 12 SCLKs in duration, beginning on the fifth SCLK received after the converter has received a high-to-low $\overline{CS}$ transition (or a high-to-low FS transition for the TLC2551).

conversion

The TLC2551, TLC2552, and TLC2555 completes conversion in the following manner. The conversion starts after the 16th SCLK falling edge during the cycle and requires 28 SCLKs to complete. Enough time for conversion should be allowed before a rising $\overline{CS}$ or FS edge so that no conversion is terminated prematurely.

TLC2552 input channel selection is toggled on each rising $\overline{CS}$ edge. The MUX channel can be reset to AIN0 via $\overline{CS}$ as described earlier and in Figure 4. The input is sampled for 12 SCLKs and converted. The result is presented on SDO during the next cycle. Care should also be taken to allow enough time between samples to avoid prematurely terminating the cycle, which occurs on a rising $\overline{CS}$ transition if the conversion is not complete.

The SDO data presented during a cycle is the result of the conversion of the sample taken during the previous cycle.

timing diagrams/conversion cycles

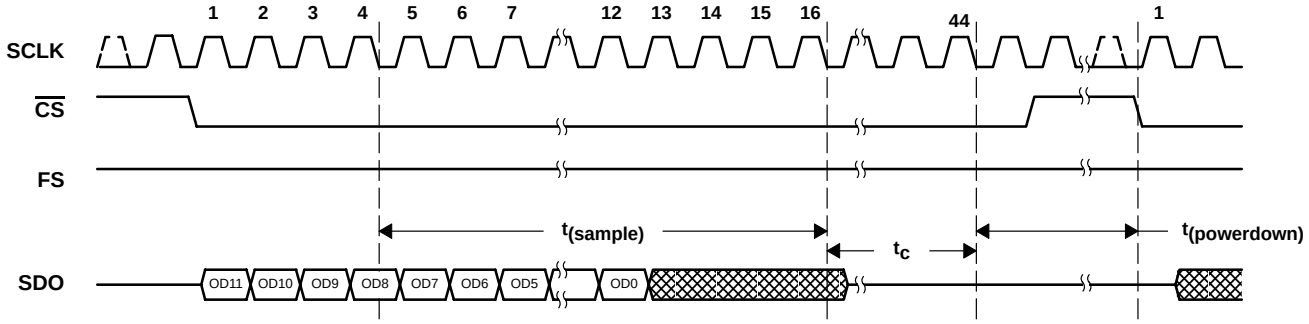


Figure 2. TLC2551 Timing: Control via $\overline{CS}$ (FS = 1)

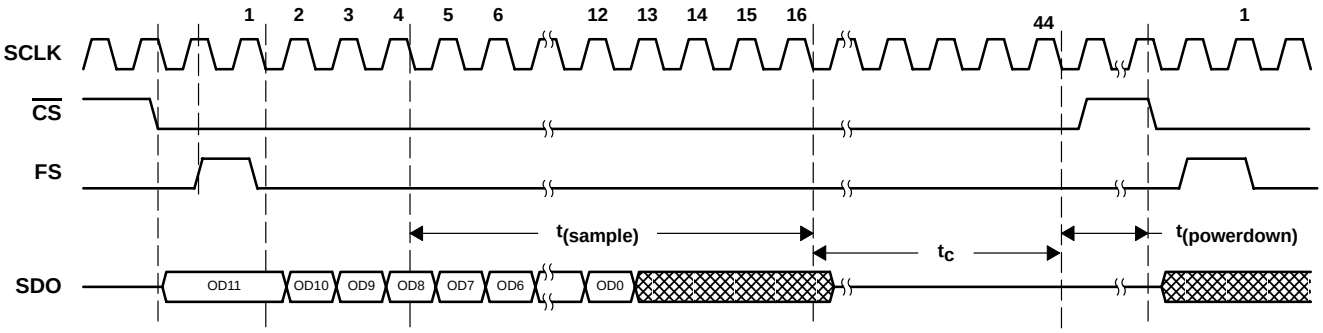


Figure 3. TLC2551 Timing: Control via $\overline{CS}$ and FS or FS Only

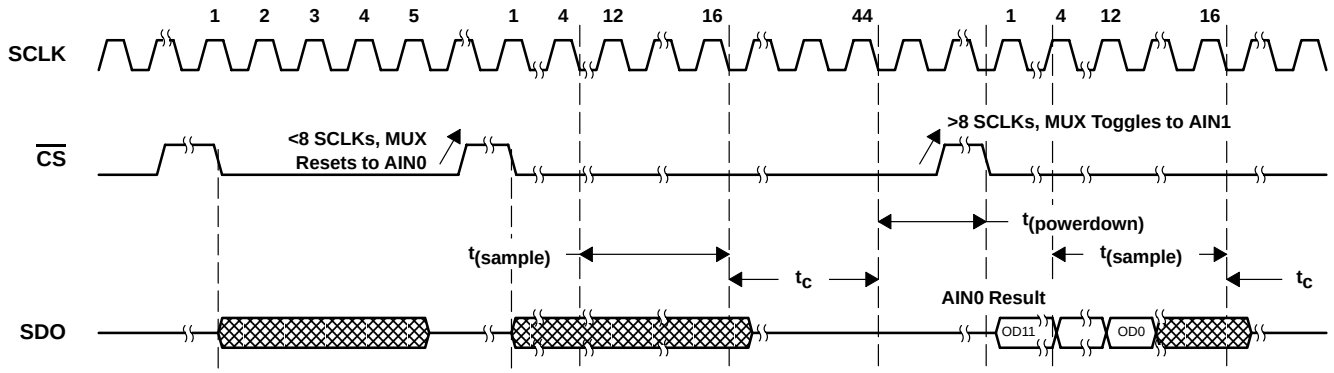


Figure 4. TLC2552 Reset Timing

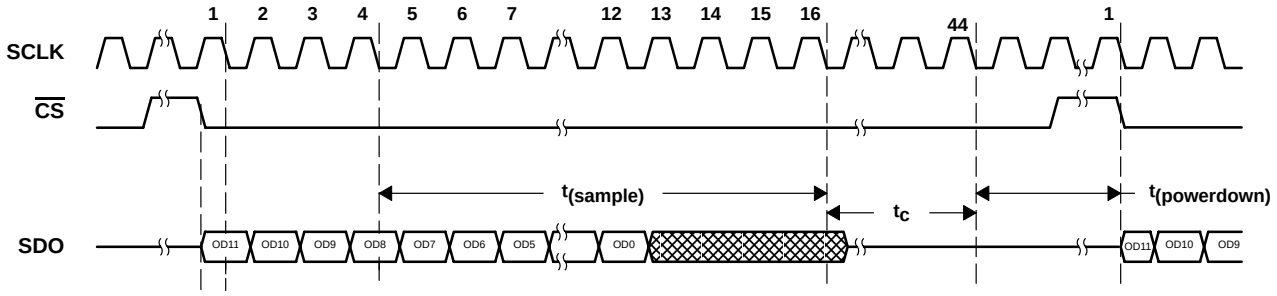


Figure 5. TLC2552 and TLC2555 Timing

using $\overline{CS}$ as the FS input

When interfacing the TLC2551 with the TMS320 DSP, the FSR signal from the DSP may be connected to the $\overline{CS}$ input if this is the only device on the serial port. This connection saves one output terminal from the DSP. (Output data changes on the falling edge of SCLK. This is the default configuration for the TLC2552 and TLC2555).

SCLK and conversion speed

The SCLK input can range in frequency from 100 kHz to 20 MHz. The required number of conversion clocks is 14. The conversion clock for the ADC is SCLK/2 which translates to 28 SCLK cycles to perform a conversion. For a 15-MHz SCLK, the minimum total cycle time is given by: 16x(1/15 M)+14x(1/7.5 M)+1 SCLK = 3.0 μs. An additional SCLK is added to account for the required $\overline{CS}$ or FS high time. These times specify the minimum cycle time for an active $\overline{CS}$ or FS signal. If violated, the conversion terminates, invalidating the next data output cycle. Table 1 gives the maximum SCLK frequency for a given operational mode.

control via pin 1 ($\overline{CS}$, SPI interface)

All devices are compatible with this mode of operation. A falling $\overline{CS}$ initiates the cycle. (For TLC2551, the FS input is tied to V_{DD}.) $\overline{CS}$ remains low for the entire cycle time (sample + convert + 1 SCLK) and can then be released.

NOTE:
IMPORTANT: A single SCLK is required whenever $\overline{CS}$ is high.

control via pin 1 ($\overline{CS}$, DSP interface)

All devices are compatible with this mode of operation. The FS signal from a DSP is connected directly to the $\overline{CS}$ input of the ADC. A falling edge on the $\overline{CS}$ input initiates the cycle. (For TLC2551, the FS input can be tied to V_{DD}, although better performance can be achieved by using the FS input for control. Refer to the *control via pin 1 and pin 7 ($\overline{CS}$ and FS or FS only, DSP interface*) section. The $\overline{CS}$ input should remain low for the entire cycle time (sample + convert + 1 SCLK) and can then be released.

NOTE:
IMPORTANT: A single SCLK is required whenever $\overline{CS}$ is high. This requirement is usually of little consequence since SCLK is normally always present when interfacing with a DSP.

control via pin 1 and pin 7 ($\overline{CS}$ and FS or FS only, DSP interface)

Only the TLC2551 is compatible with this mode of operation. The $\overline{CS}$ input to the ADC can be controlled via a general-purpose I/O pin from the DSP. The FS signal from the DSP is connected directly to the FS input of the ADC. A falling edge on $\overline{CS}$, if used, releases the MSB on the SDO output. When $\overline{CS}$ is not used, the rising FS edge releases the MSB. The falling edge on the FS input while SCLK is high initiates the cycle. The $\overline{CS}$ and FS inputs should remain low for the entire cycle time (sample + convert + 1 SCLK) and can then be released.

reference voltage

An external reference is applied via V_{REF}. The voltage level applied to this pin establishes the upper limit of the analog inputs to produce a full-scale reading. The value of V_{REF} and the analog input must not exceed the positive supply or be less than GND, consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than V_{REF} and at zero when the input signal is equal to or lower than GND.

powerdown and powerup

Autopower down is built into these devices in order to reduce power consumption. The actual power savings depends on the inactive time between cycles and the power supply (loading) decoupling/storage capacitors. *Power-down takes effect immediately after the conversion is complete*. This is fast enough to provide some power savings between cycles with longer than 1 SCLK inactive time. *The device power goes down to 8 μA within 0.5 μs.* To achieve the lowest power-down current *(deep powerdown)* of 1 μA requires 2-ms inactive time between cycles. The power-down state is initiated at the end of conversion. These devices wake up *immediately* at the next falling edge of $\overline{CS}$ or the rising edge of FS.

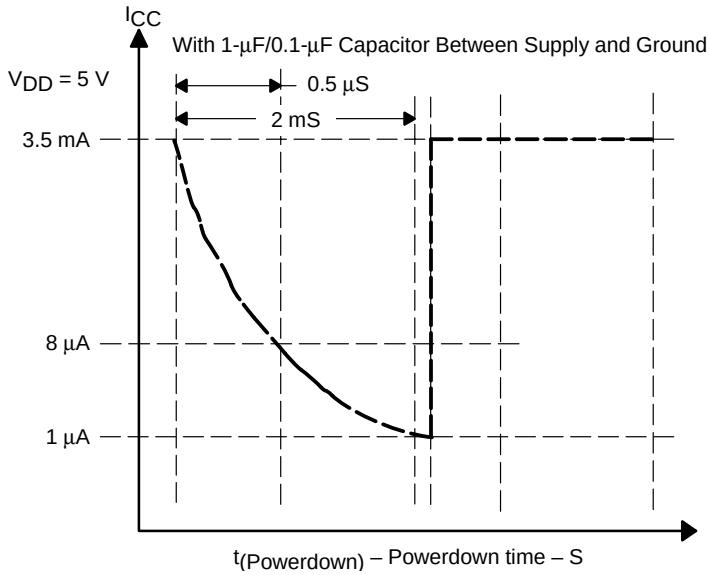


Table 1. Modes of Operation and Data Throughput

CONTROL PIN(s)/DEVICE	MAX SCLK (MHz) (50/50 duty cycle) V_{DD} = 4.5 V	APPROXIMATE CONVERSION THROUGHPUT (ksps) V_{DD} = 4.5 V
$\overline{CS}$ control only (TLC2551 only)		
For SPI†	15	333
DSP interface‡	8	175
$\overline{CS}$ and FS control (TLC2551 only)§		
DSP interface	20	400

† See Figure 21(a).
‡ See Figure 21(b).
§ See Figure 21(c).

absolute maximum ratings over operating free-air temperature (unless otherwise noted)¶

Supply voltage range, GND to V_{DD} . . . . . –0.3 V to 6.5 V
Analog input voltage range . . . . . –0.3 V to V_{DD} + 0.3 V
Reference input voltage . . . . . V_{DD} + 0.3 V
Digital input voltage range . . . . . –0.3 V to V_{DD}+ 0.3 V
Operating virtual junction temperature range, T_J . . . . . –40°C to 150°C
Operating free-air temperature range, T_A: C . . . . . 0°C to 70°C
I . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

¶ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	5	5.5	V
Positive external reference voltage input, V_{REFP} (see Note 1)		2		V_{DD}	V
Analog input voltage (see Note 1)		0		V_{DD}	V
High level control input voltage, V_{IH}		2.1			V
Low-level control input voltage, V_{IL}				0.6	V
Setup time, $\overline{CS}$ falling edge before first SCLK falling edge, $t_{su(CSL-SCLKL)}$	V_{DD} = REF = 4.5 V	40			ns
Hold time, $\overline{CS}$ falling edge after SCLK falling edge, $t_{h(SCLKL-CSL)}$		5			ns
Delay time, delay from $\overline{CS}$ falling edge to FS rising edge $t_{d(CSL-FSH)}$ (TLC2551 only)		0.5		7	SCLKs
Setup time, FS rising edge before SCLK falling edge, $t_{su(FSH-SCLKL)}$ (TLC2551 only)		0.35			SCLKs
Hold time, FS hold high after SCLK falling edge, $t_{h(SCLKL-FSL)}$ (TLC2551 only)				0.65	SCLKs
Pulse width $\overline{CS}$ high time, $t_{w(H\_CS)}$		100			ns
Pulse width FS high time, $t_{w(H\_FS)}$ (TLC2551 only)		0.75			SCLKs
SCLK cycle time, V_{DD} = 5.5 V to 4.5 V, $t_{c(SCLK)}$ (maximum tolerance of 40/60 duty cycle)		50		10000	ns
Pulse width low time, $t_{w(L\_SCLK)}$		0.4		0.6	SCLKs
Pulse width high time, $t_{w(H\_SCLK)}$		0.4		0.6	SCLKs
Hold time, hold from end of conversion to $\overline{CS}$ high, $t_{h(EOC-CSH)}$ (EOC is internal, indicates end of conversion time, t_c)			0.05		µs
Active $\overline{CS}$ cycle time to reset internal MUX to AIN0, $t_{(Reset\ cycle)}$ (TLC2552 only)		4		7	SCLKs
Delay time, delay from $\overline{CS}$ falling edge to SDO valid, $t_{d(CSL-SDOV)}$	V_{DD} = REF = 4.5 V, 25-pF load			40	ns
Delay time, delay from FS falling edge to SDO valid, $t_{d(FSL-SDOV)}$ (TLC2551 only)	V_{DD} = REF = 4.5 V, 25-pF load			1	ns
Delay time, delay from SCLK rising edge to SDO valid, $t_{d(SCLKH-SDOV)}$	V_{DD} = REF = 4.5 V, 25-pF load			11	ns
Delay time, delay from 17th SCLK rising edge to SDO 3-state, $t_{d(SCLK17H-SDOZ)}$	V_{DD} = REF = 4.5 V, 25-pF load			30	ns
Conversion time, t_c			28		SCLKs
Sampling time, $t_{(sample)}$	See Note 2	300			ns
Operating free-air temperature, T_A	TLC2551/2/5C	0		70	°C
	TLC2551/2/5I	–40		85	

NOTES: 1. Analog input voltages greater than that applied to V_{REF} convert as all ones (111111111111), while input voltages less than that applied to GND convert as all zeros(000000000000).
2. Minimal $t_{(sample)}$ is given by $0.9 \times 50\ pF \times (R_S + 0.5\ k\Omega)$, where R_S is the source output impedance.

electrical characteristics over recommended operating free-air temperature range, V_{DD} = V_{REF} = 4.5 V to 5.5 V, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} = 5.5 V, I_{OH} = –0.2 mA at 30-pF load		2.4			V
V_{OL}	Low-level output voltage	V_{DD} = 5.5 V, I_{OL} = 0.8 mA at 30-pF load				0.4	V
I_{OZ}	Off-state output current (high-impedance-state)	V_O = V_{DD}	$\overline{CS}$ = V_{DD}		1	2.5	µA
		V_O = 0			–1	–2.5	
I_{IH}	High-level input current	V_I = V_{DD}			0.005	2.5	µA
I_{IL}	Low-level input current	V_I = 0 V			–0.005	2.5	µA
I_{CC}	Operating supply current	$\overline{CS}$ at 0 V,	V_{DD} = 4.5 V to 5.5 V		3	3.5	mA
$I_{CC(AUTOPWDN)}$	Autopower-down current $t_{(powerdown)} \geq 0.5$ µs	For all digital inputs, 0≤ $V_I \leq 0.3$ V or $V_I \geq V_{DD}$– 0.3 V, SCLK = 0, V_{DD} = 4.5 V to 5.5 V, Ext ref				8	µA
	Deep autopower-down current $t_{(powerdown)} \geq 2$ ms					1	
	Selected analog input channel leakage current	Selected channel at V_{DD}				1	µA
		Selected channel at 0 V				–1	
C_i	Input capacitance	Analog inputs		20	45	50	pF
		Control Inputs			5	25	
	Input on resistance	V_{DD} = 5.5 V				500	Ω

† All typical values are at V_{DD} = 5 V, T_A = 25°C.

ac specifications (f_i = 20 kHz)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise ratio + distortion	400 KSPS, $V_{DD} = V_{REF}$ = 5 V	70	72		dB
THD	Total harmonic distortion	400 KSPS, $V_{DD} = V_{REF}$ = 5 V		–84	–80	dB
ENOB	Effective number of bits	400 KSPS, $V_{DD} = V_{REF}$ = 5 V		11.8		bits
SFDR	Spurious free dynamic range	400 KSPS, $V_{DD} = V_{REF}$ = 5 V		–84	–80	dB
Analog Input						
	Full-power bandwidth, –3 dB			1		MHz
	Full-power bandwidth, –1 dB			500		kHz

external reference specifications

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Reference input voltage	V_{DD} = 4.5 V to 5.5 V		2		V_{DD}	V
	Reference input impedance	V_{DD} = 5.5 V	$\overline{CS}$ = 1, SCLK = 0	100			MΩ
			$\overline{CS}$ = 0, SCLK = 20 MHz	20	25		kΩ
	Reference current	$V_{DD} = V_{REF}$ = 5.5 V			100	400	μA
	Reference input capacitance	$V_{DD} = V_{REF}$ = 5.5 V	$\overline{CS}$ = 1, SCLK = 0	5		15	pF
			$\overline{CS}$ = 0, SCLK = 20 MHz	20	45	50	
V_{REF}	Reference voltage	V_{DD} = 4.5 V to 5.5 V				V_{DD}	V

dc specification, $V_{DD} = V_{REF}$ = 4.5 V to 5.5 V, SCLK frequency = 20 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INL	Integral linearity error (see Note 4)				±0.6	±1	LSB
DNL	Differential linearity error	See Note 3			±0.5	±1	LSB
E_O	Offset error (see Note 5)	See Note 3	TLC2551/52			±1.5	LSB
			TLC2555			±2.5	
E_G	Gain error (see Note 5)	See Note 3	TLC2551/52			±2	LSB
			TLC2555			±5	
E_t	Total unadjusted error (see Note 6)	See Note 3	TLC2551/52			±2	LSB
			TLC2555			±5	

NOTES: 3. Analog input voltages greater than that applied to V_{REF} convert as all ones (111111111111).
4. Linear error is the maximum deviation from the best straight line through the A/D transfer characteristics.
5. Zero error is the difference between 000000000000 and the converted output for zero input voltage: full-scale error is the difference between 111111111111 and the converted output for full-scale input voltage.
6. Total unadjusted error comprises linearity, zero, and full-scale errors.

PARAMETER MEASUREMENT INFORMATION

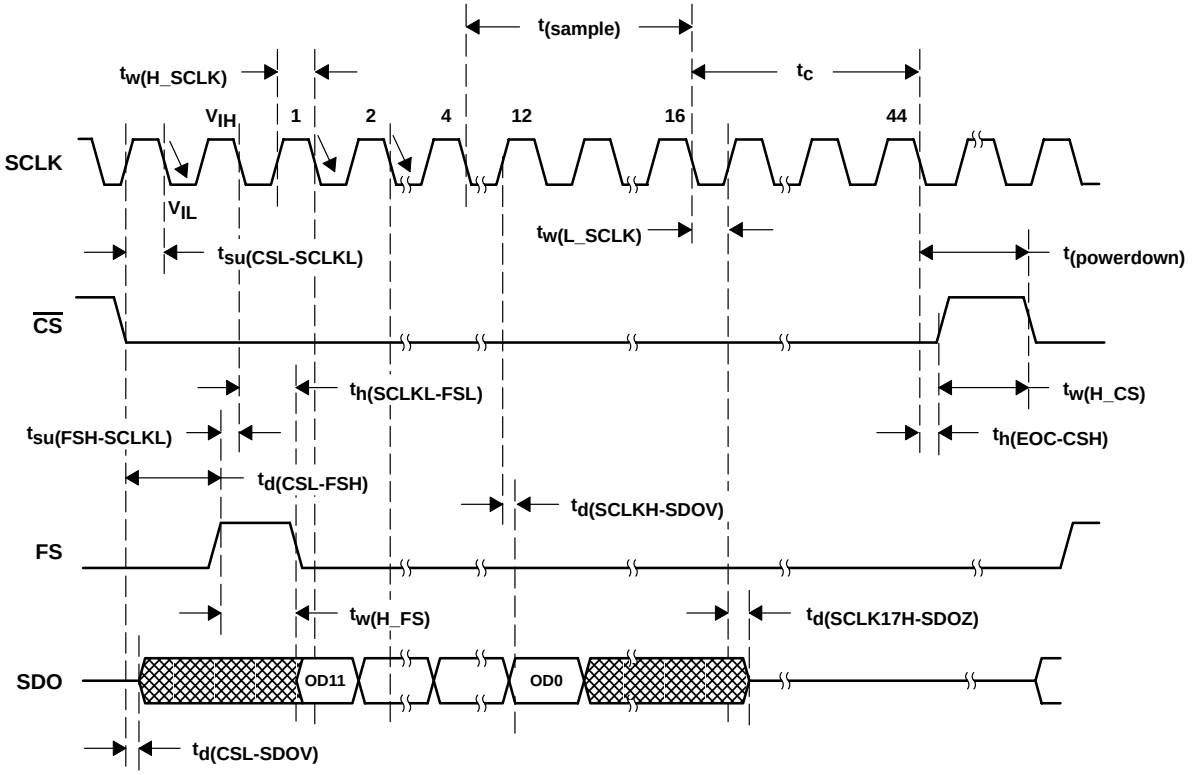


Figure 6. TLC2551 Critical Timing (Control via $\overline{CS}$ and FS or FS only)

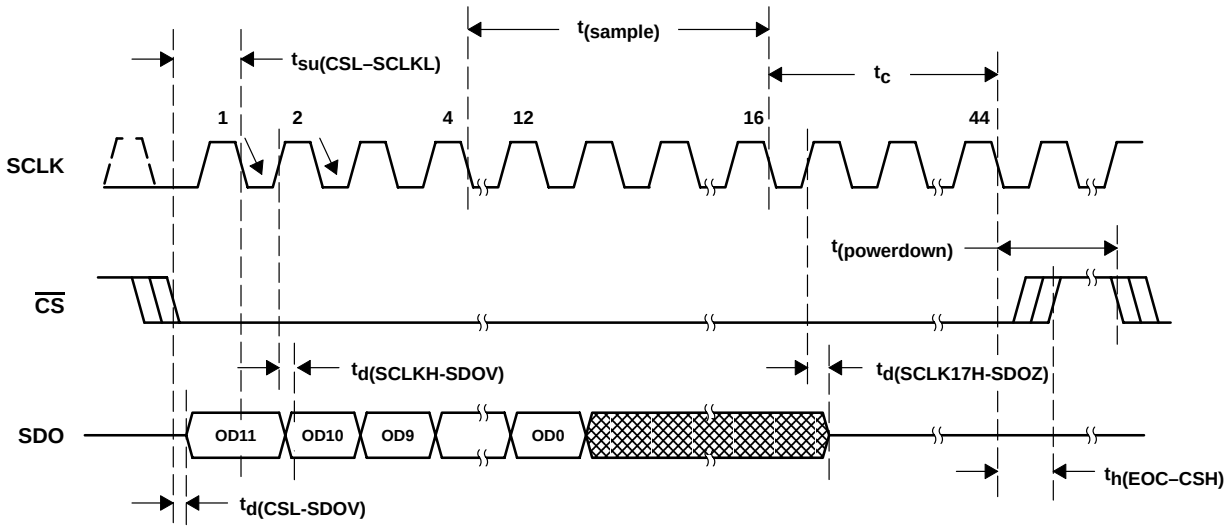


Figure 7. TLC2551 Critical Timing (Control via $\overline{CS}$ only, FS = 1)

PARAMETER MEASUREMENT INFORMATION

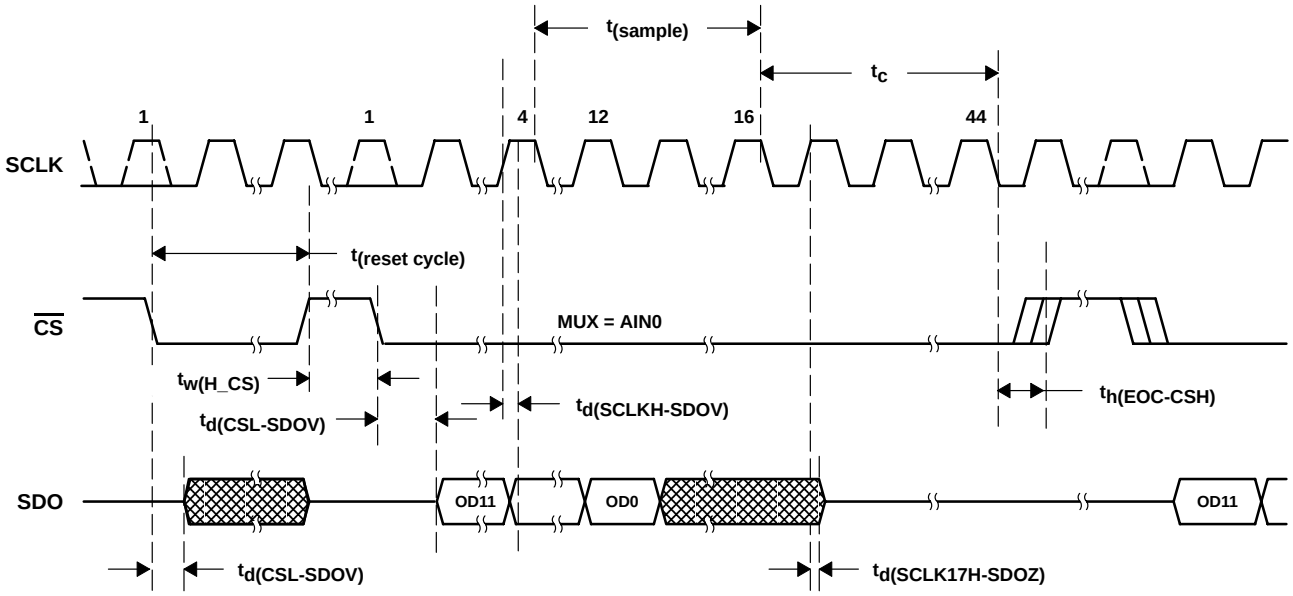


Figure 8. TLC2552 Reset Cycle Critical Timing

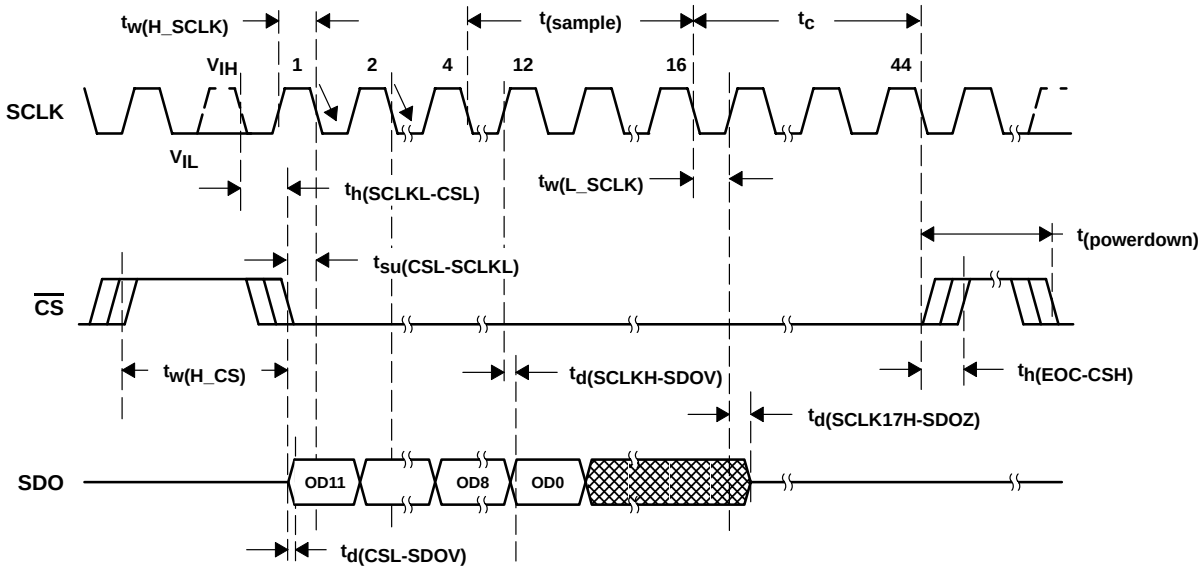


Figure 9. TLC2552 and TLC2555 Conversion Cycle Critical Timing

TYPICAL CHARACTERISTICS

INTEGRAL NONLINEARITY vs FREE-AIR TEMPERATURE

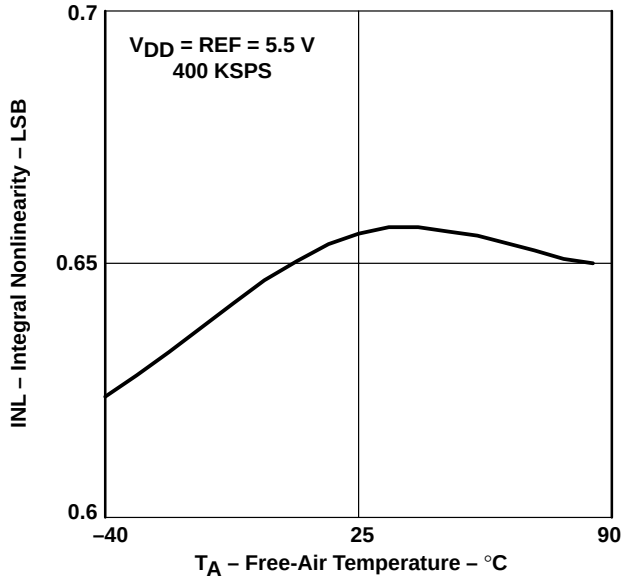


Figure 10

DIFFERENTIAL NONLINEARITY vs FREE-AIR TEMPERATURE

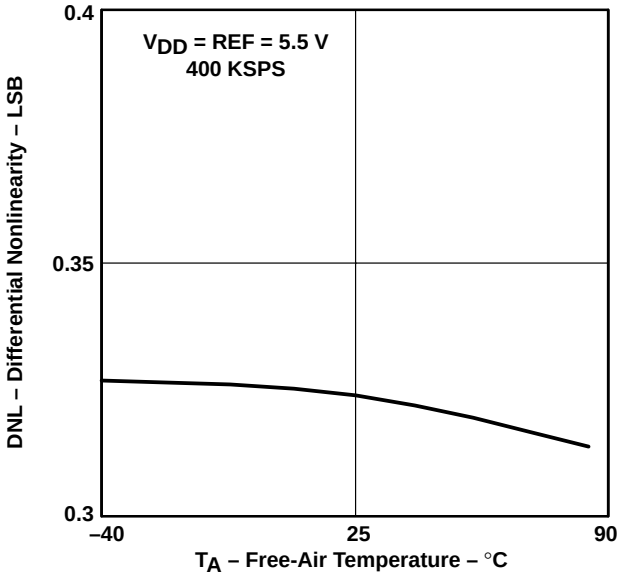


Figure 11

OFFSET ERROR vs FREE-AIR TEMPERATURE

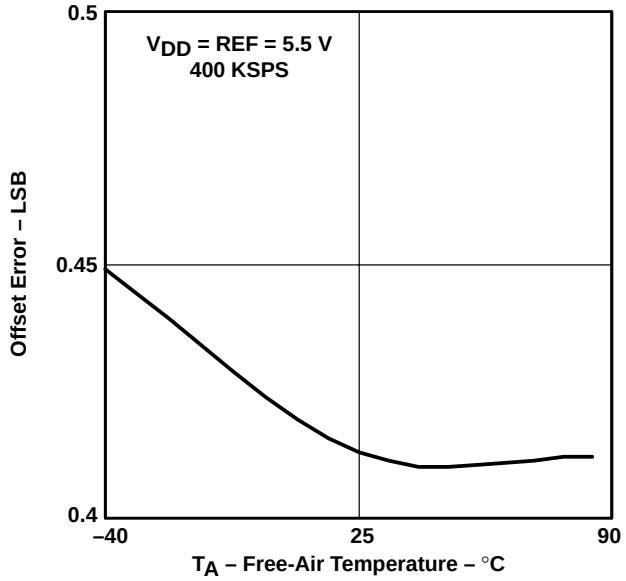


Figure 12

GAIN ERROR vs FREE-AIR TEMPERATURE

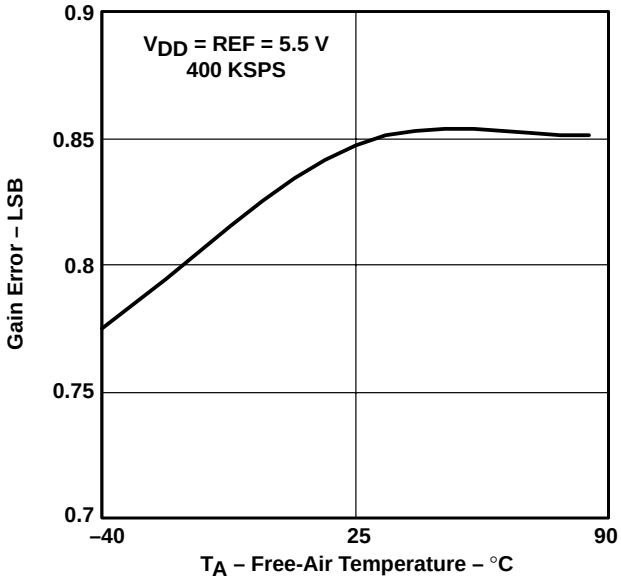


Figure 13

TYPICAL CHARACTERISTICS

**SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE**

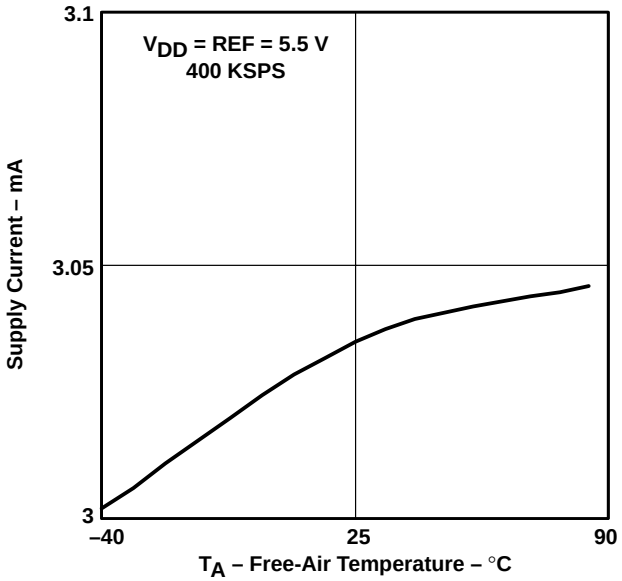


Figure 14

**DIFFERENTIAL NONLINEARITY
vs
DIGITAL OUTPUT CODES**

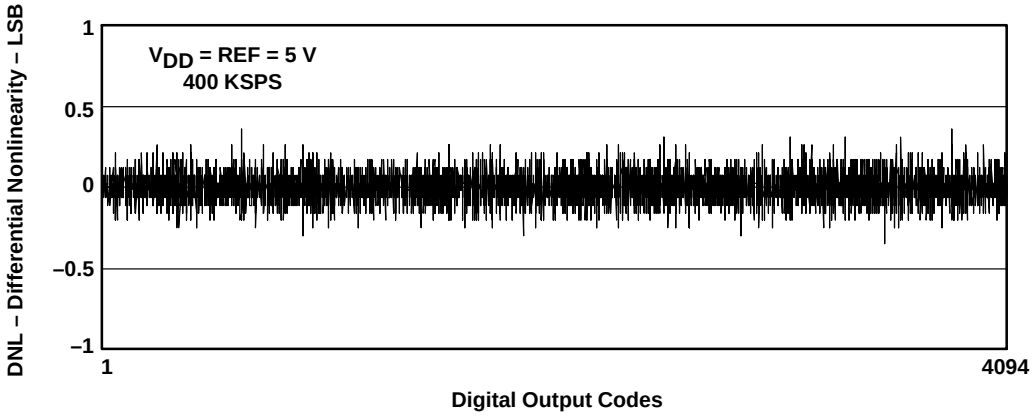


Figure 15

TYPICAL CHARACTERISTICS

INTEGRAL NONLINEARITY vs DIGITAL OUTPUT CODES

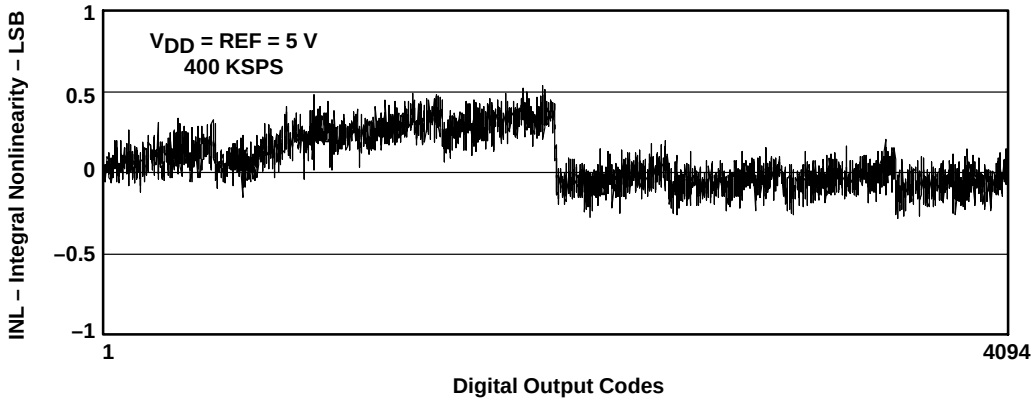


Figure 16

2048 POINTS FAST FOURIER TRANSFORM (FFT)

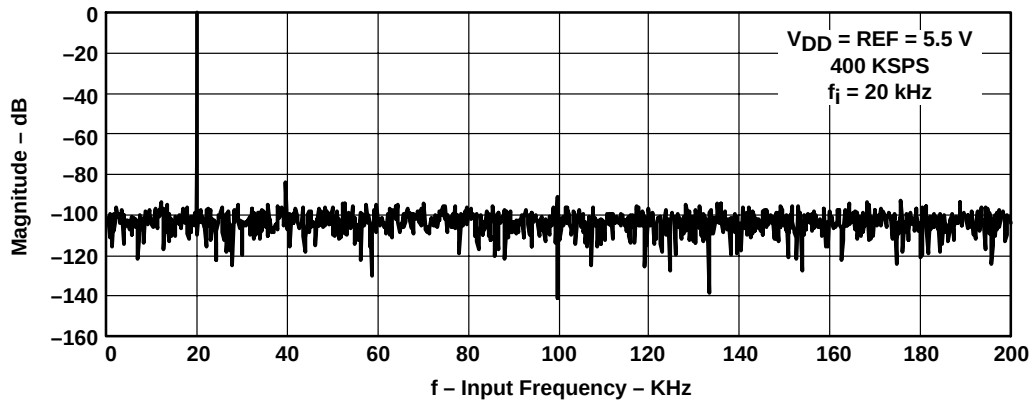


Figure 17

TYPICAL CHARACTERISTICS

SIGNAL-TO-NOISE AND DISTORTION vs INPUT FREQUENCY

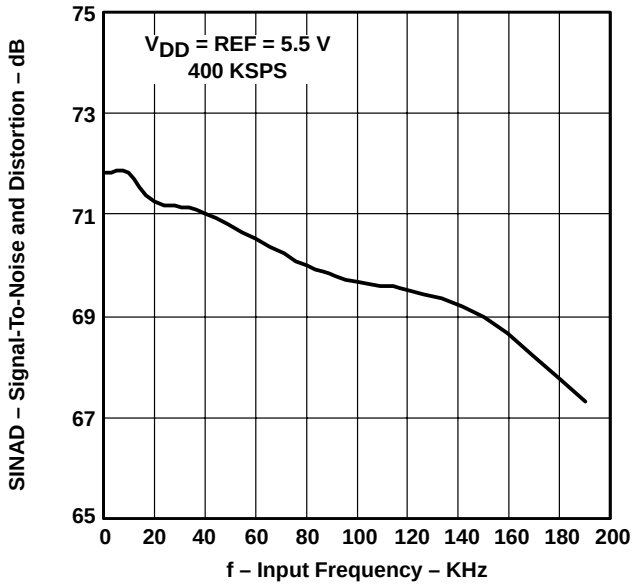


Figure 18

EFFECTIVE NUMBER OF BITS vs INPUT FREQUENCY

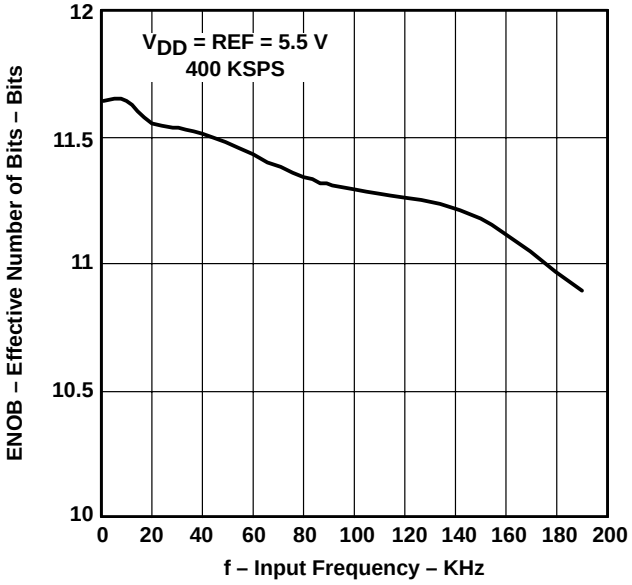


Figure 19

TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

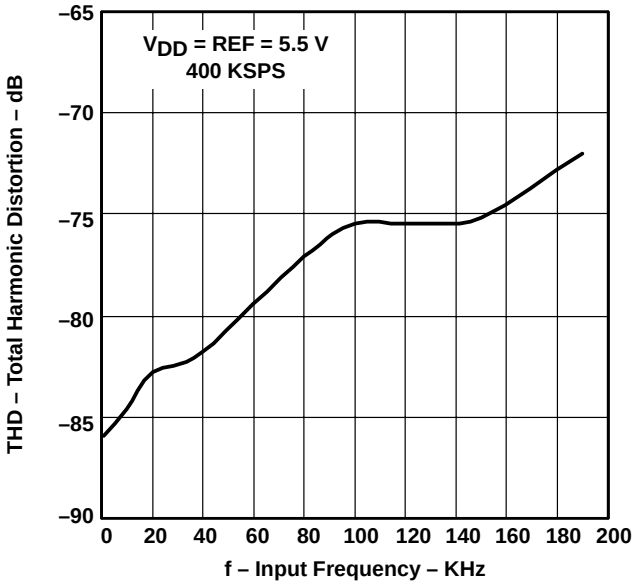
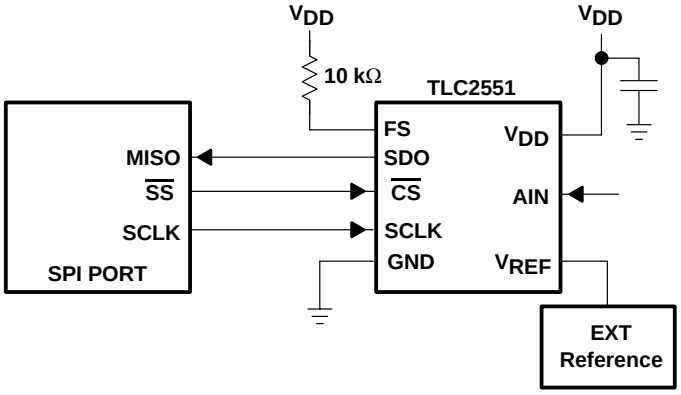
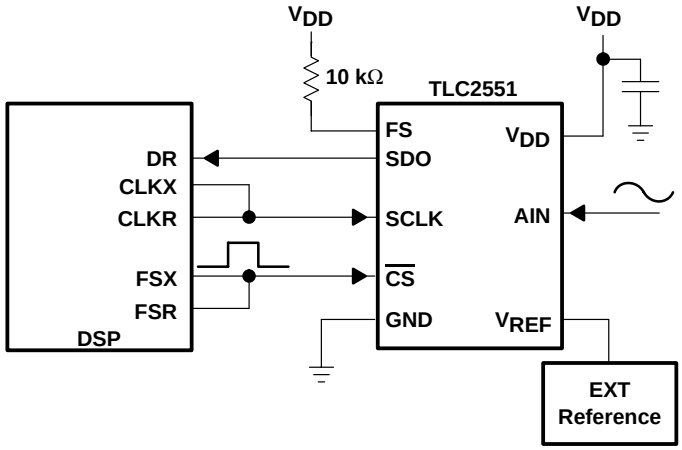


Figure 20

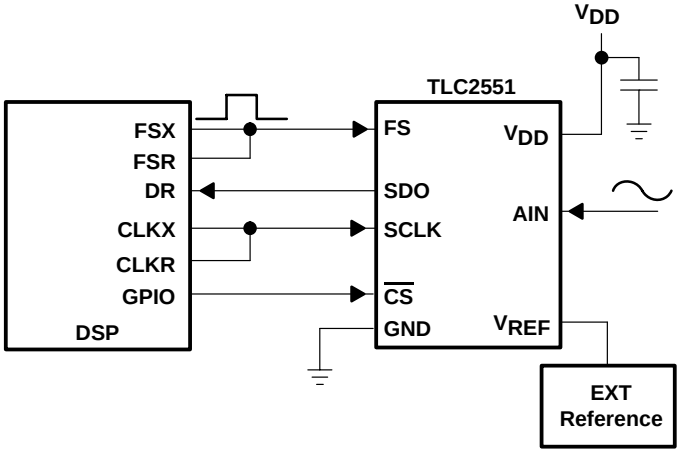
APPLICATION INFORMATION



(a)



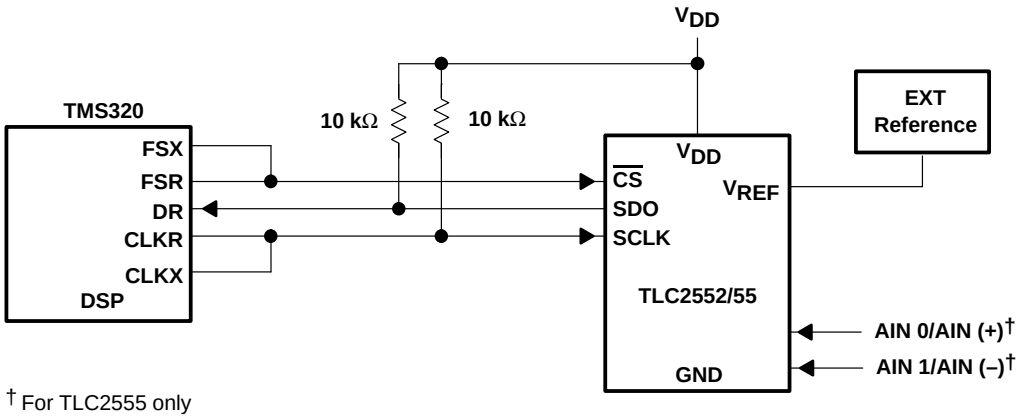
(b)



(c)

Figure 21. Typical TLC2551 Interface to a TMS320 DSP

APPLICATION INFORMATION



† For TLC2555 only

Figure 22. Typical TLC2552/55 Interface to a TMS320 DSP

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLC2551CDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	
TLC2551CDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	
TLC2551CDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	
TLC2551CDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	
TLC2551ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2551IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2551IDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	
TLC2551IDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	
TLC2551IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2551IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2552CDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	
TLC2552CDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	
TLC2552ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2552IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2552IDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	
TLC2552IDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	
TLC2555ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLC2555IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2555IDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	
TLC2555IDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	

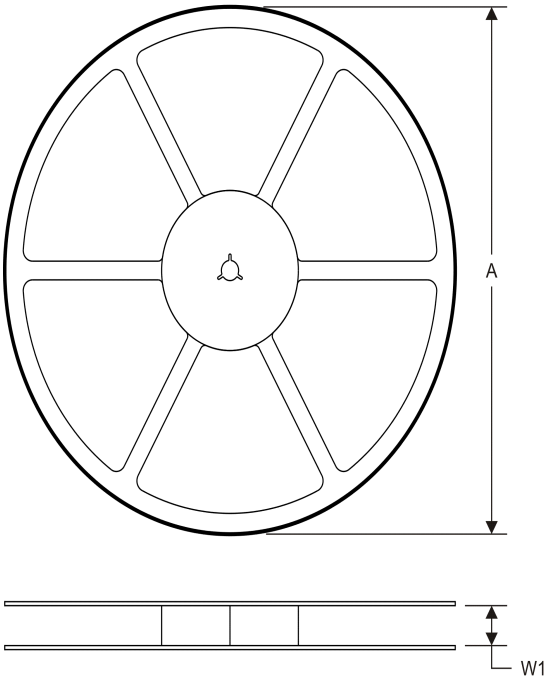
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

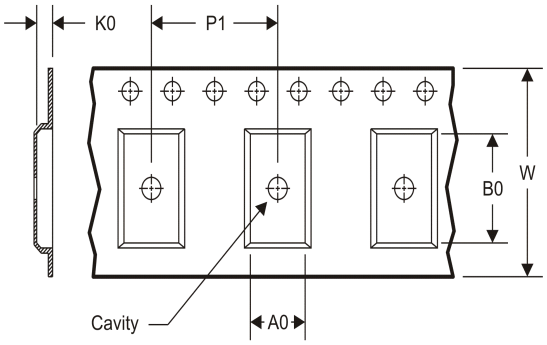
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



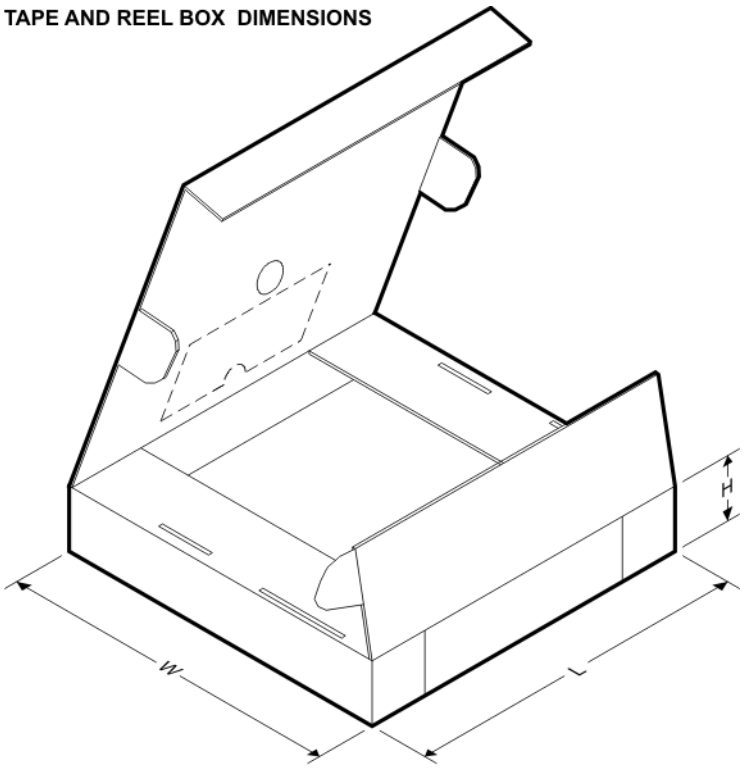
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2551CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLC2551IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

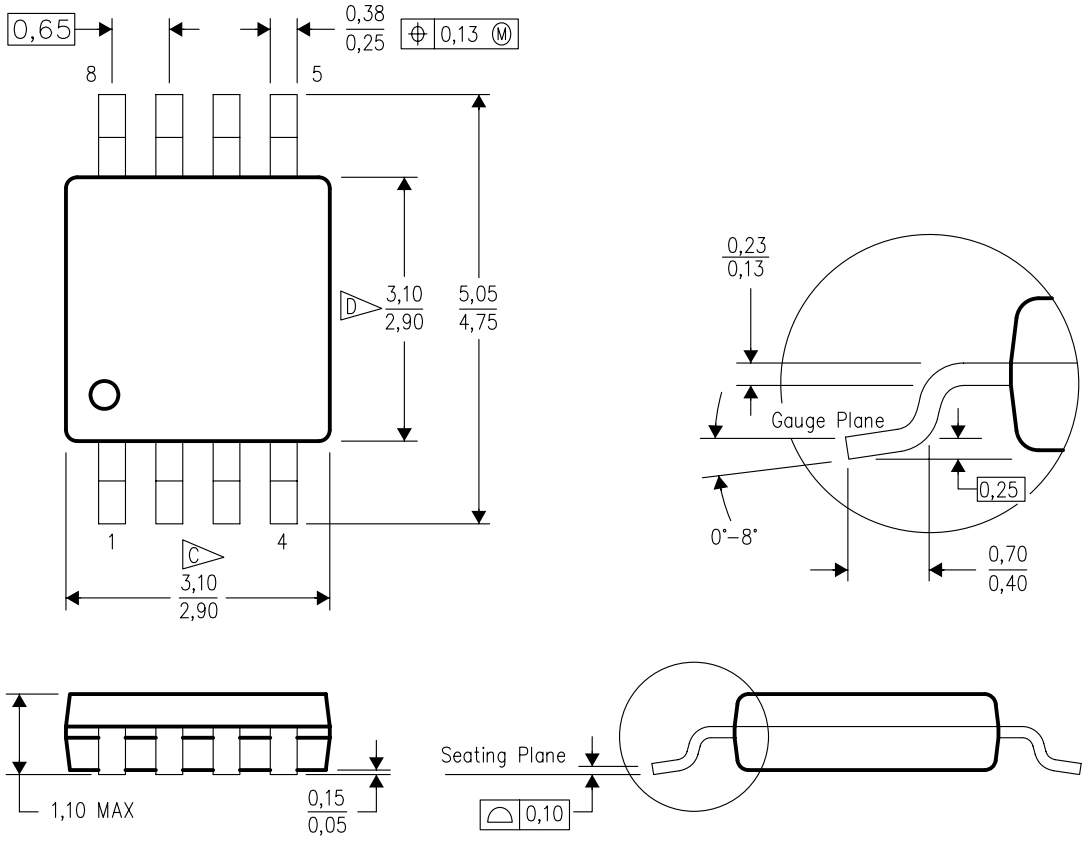
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2551CDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
TLC2551IDR	SOIC	D	8	2500	367.0	367.0	35.0

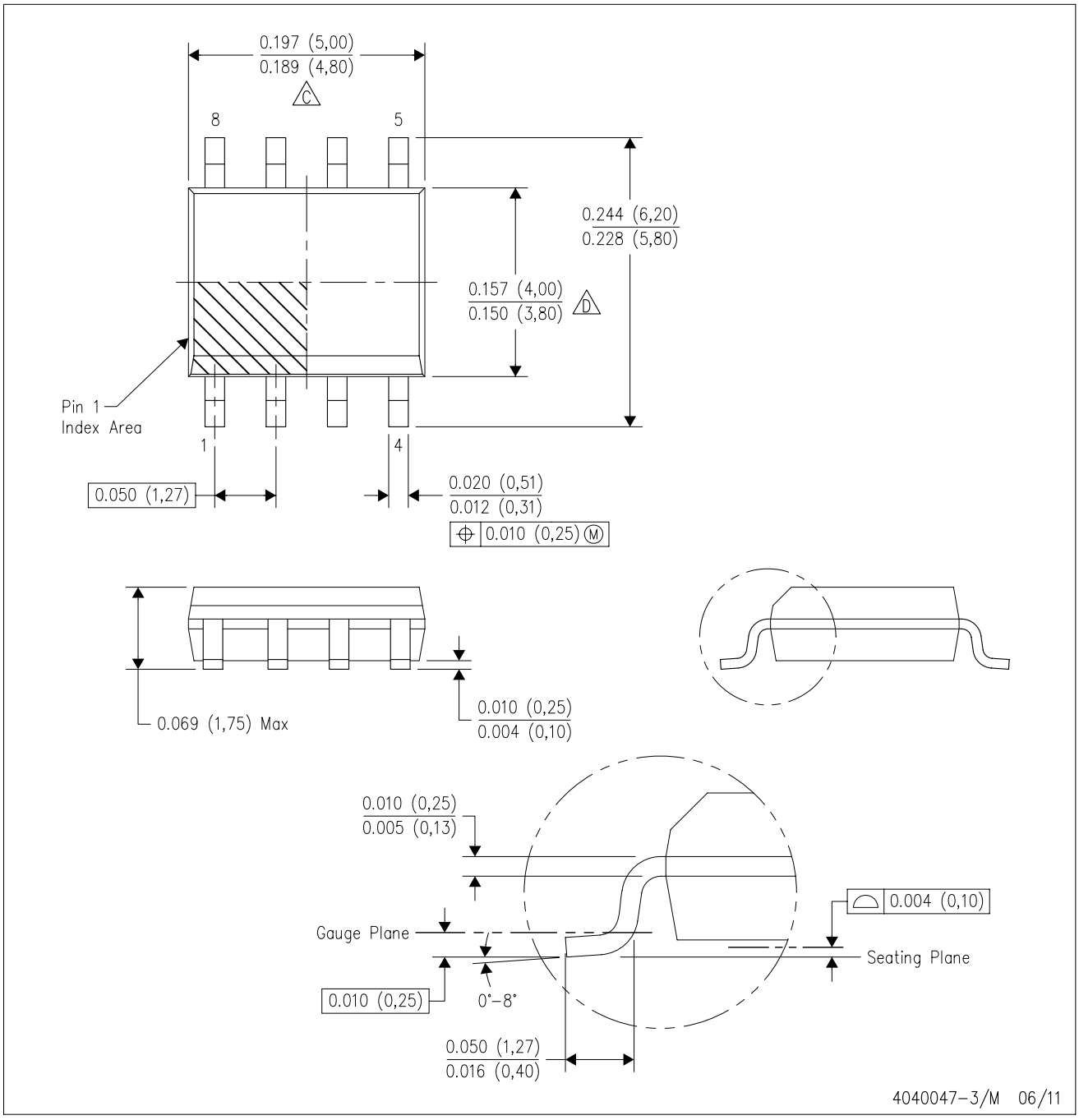
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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