

TL1451A DUAL PULSE-WIDTH-MODULATION CONTROL CIRCUITS

SLVS024E – FEBRUARY 1983 – REVISED NOVEMBER 1999

- Complete PWM Power Control Circuitry
- Completely Synchronized Operation
- Internal Undervoltage Lockout Protection
- Wide Supply Voltage Range
- Internal Short-Circuit Protection
- Oscillator Frequency . . . 500 kHz Max
- Variable Dead Time Provides Control Over Total Range
- Internal Regulator Provides a Stable 2.5-V Reference Supply
- Available in Q-Temp Automotive HighRel Automotive Applications Configuration Control / Print Support Qualification to Automotive Standards

description

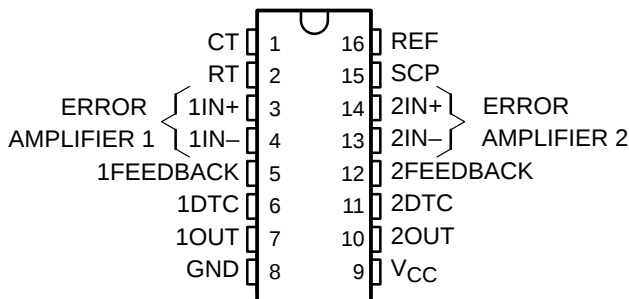
The TL1451A incorporates on a single monolithic chip all the functions required in the construction of two pulse-width-modulation (PWM) control circuits. Designed primarily for power-supply control, the TL1451A contains an on-chip 2.5-V regulator, two error amplifiers, an adjustable oscillator, two dead-time comparators, undervoltage lockout circuitry, and dual common-emitter output transistor circuits.

The uncommitted output transistors provide common-emitter output capability for each

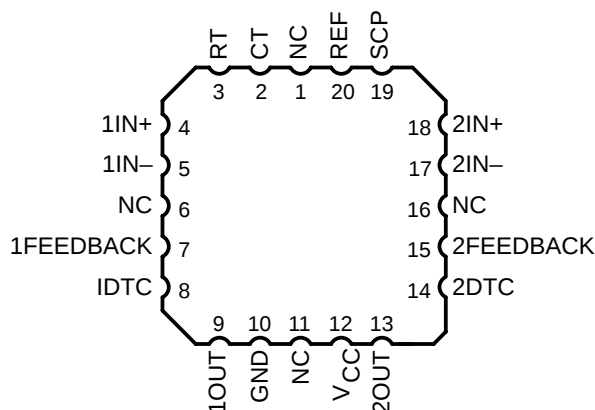
controller. The internal amplifiers exhibit a common-mode voltage range from 1.04 V to 1.45 V. The dead-time control (DTC) comparator has no offset unless externally altered and can provide 0% to 100% dead time. The on-chip oscillator can be operated by terminating RT and CT. During low V_{CC} conditions, the undervoltage lockout control circuit feature locks the outputs off until the internal circuitry is operational.

The TL1451AC is characterized for operation from -20°C to 85°C . The TL1451AQ is characterized for operation from -40°C to 125°C . The TL1451AM is characterized for operation from -55°C to 125°C .

D, DB, N, NS, PW, OR J PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T _A	PACKAGED DEVICES						
	SMALL OUTLINE (D)	SMALL OUTLINE (DB) [†]	PLASTIC DIP (N)	SMALL OUTLINE (NS)	TSSOP (PW) [†]	CHIP CARRIER (FK)	CERAMIC DIP (J)
-20°C to 85°C	TL1451ACD	TL1451ACDB	TL1451ACN	TL1451ACNS	TL1451ACPW	—	—
-40°C to 125°C	TL1451AQD	—	—	—	—	—	—
-55°C to 125°C	—	—	—	—	—	TL1451AMFK	TL1451AMJ

[†] The DB and PW packages are only available left-end taped and reeled (add LE suffix, i.e., TL1451ACPWLE).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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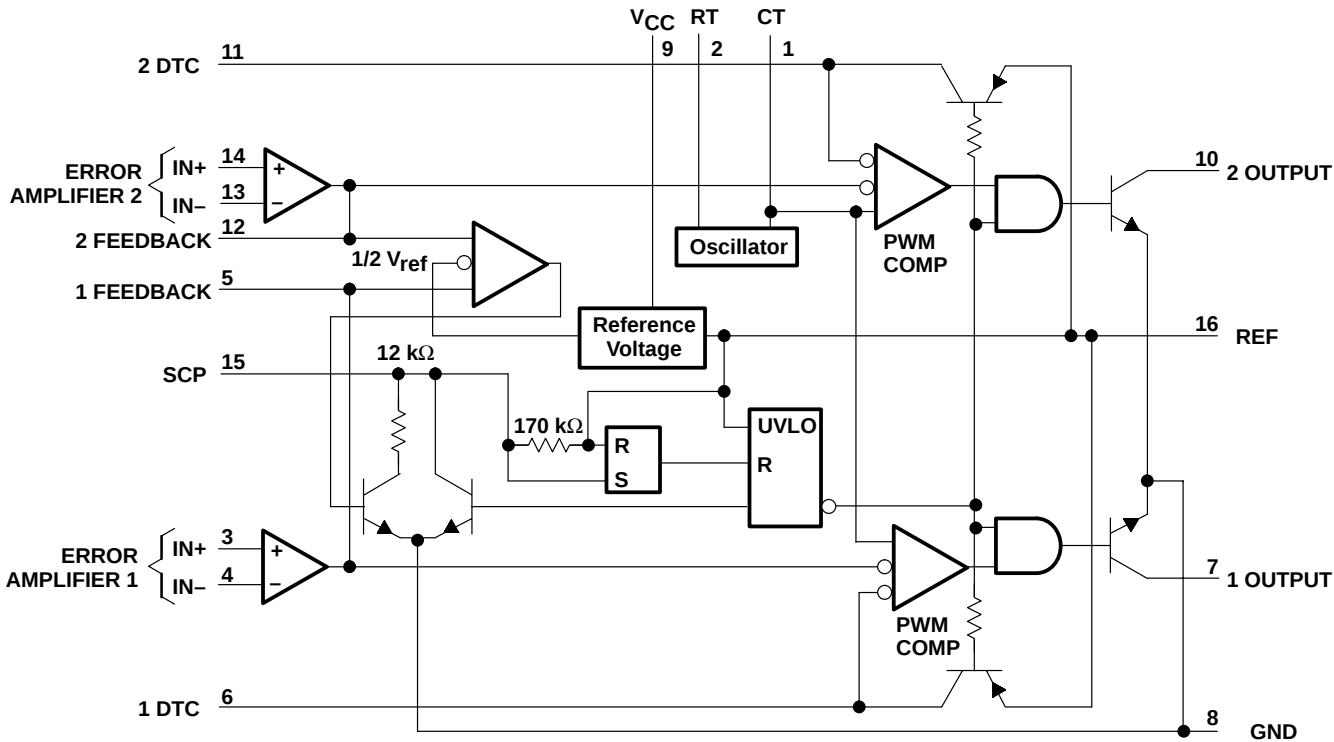
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

TL1451A

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functional block diagram



COMPONENT COUNT	
Resistors	65
Capacitors	8
Transistors	105
JFETs	18

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absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	51 V
Amplifier input voltage, V_I	20 V
Collector output voltage, V_O	51 V
Collector output current, I_O	21 mA
Continuous power total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A C suffix	–20°C to 85°C
Q suffix	–40°C to 125°C
M suffix	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	1088 mW	8.7 mW/°C	696 mW	566 mW	218 mW
DB	775 mW	6.2 mW/°C	496 mW	403 mW	—
N	1000 mW	8.0 mW/°C	640 mW	520 mW	—
NS	500 mW	4.0 mW/°C	320 mW	260 mW	—
PW	838 mW	6.7 mW/°C	536 mW	436 mW	168 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	3.6	50	V
Amplifier input voltage, V_I	1.05	1.45	V
Collector output voltage, V_O		50	V
Collector output current, I_O		20	mA
Current into feedback terminal		45	μA
Feedback resistor, R_F	100		kΩ
Timing capacitor, C_T	150	15000	pF
Timing resistor, R_T	5.1	100	kΩ
Oscillator frequency	1	500	kHz
Operating free-air temperature, T_A	C suffix	–20	85
	Q suffix	–40	125
	M suffix	–55	125

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electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 6\text{ V}$, $f = 200\text{ kHz}$ (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS	TL1451AC			UNIT
		MIN	TYP†	MAX	
Output voltage (pin 16)	$I_O = 1\text{ mA}$	2.4	2.5	2.6	V
Output voltage change with temperature	$T_A = -20^\circ\text{C}$ to 25°C		-0.1%	$\pm 1\%$	
	$T_A = 25^\circ\text{C}$ to 85°C		-0.2%	$\pm 1\%$	
Input voltage regulation	$V_{CC} = 3.6\text{ V}$ to 40 V		2	12.5	mV
Output voltage regulation	$I_O = 0.1\text{ mA}$ to 1 mA		1	7.5	mV
Short-circuit output current	$V_O = 0$	3	10	30	mA

† All typical values are at $T_A = 25^\circ\text{C}$.

undervoltage lockout section

PARAMETER	TEST CONDITIONS	TL1451AC			UNIT
		MIN	TYP†	MAX	
Upper threshold voltage (V_{CC})	$I_{O(\text{ref})} = 0.1\text{ mA}$, $T_A = 25^\circ\text{C}$		2.72		V
Lower threshold voltage (V_{CC})			2.6		V
Hysteresis (V_{CC})		80	120		mV
Reset threshold voltage (V_{CC})		1.5	1.9		V

† All typical values are at $T_A = 25^\circ\text{C}$.

short-circuit protection control section

PARAMETER	TEST CONDITIONS	TL1451AC			UNIT
		MIN	TYP†	MAX	
Input threshold voltage (SCP)	$T_A = 25^\circ\text{C}$	0.65	0.7	0.75	V
Standby voltage (SCP)	No pullup	140	185	230	mV
Latched input voltage (SCP)	No pullup		60	120	mV
Input (source) current	$V_I = 0.7\text{ V}$, $T_A = 25^\circ\text{C}$	-10	-15	-20	μA
Comparator threshold voltage (FEEDBACK)			1.18		V

† All typical values are at $T_A = 25^\circ\text{C}$.

oscillator section

PARAMETER	TEST CONDITIONS	TL1451C			UNIT
		MIN	TYP†	MAX	
Frequency	$C_T = 330\text{ pF}$, $R_T = 10\text{ k}\Omega$		200		kHz
Standard deviation of frequency	$C_T = 330\text{ pF}$, $R_T = 10\text{ k}\Omega$		10%		
Frequency change with voltage	$V_{CC} = 3.6\text{ V}$ to 40 V		1%		
Frequency change with temperature	$T_A = -20^\circ\text{C}$ to 25°C		-0.4%	$\pm 2\%$	
	$T_A = 25^\circ\text{C}$ to 85°C		-0.2%	$\pm 2\%$	

† All typical values are at $T_A = 25^\circ\text{C}$.

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dead-time control section

PARAMETER	TEST CONDITIONS	TL1451AC			UNIT
		MIN	TYP†	MAX	
Input bias current (DTC)				1	μA
Latch mode (source) current (DTC)	$T_A = 25^\circ\text{C}$	-80	-145		μA
Latched input voltage (DTC)	$I_O = 40\ \mu\text{A}$	2.3			V
Input threshold voltage at $f = 10\ \text{kHz}$ (DTC)	Zero duty cycle		2.05	2.25	V
	Maximum duty cycle	1.2	1.45		

† All typical values are at $T_A = 25^\circ\text{C}$.

error-amplifier section

PARAMETER	TEST CONDITIONS	TL1451AC			UNIT
		MIN	TYP†	MAX	
Input offset voltage	V_O (FEEDBACK) = 1.25 V			±6	mV
Input offset current	V_O (FEEDBACK) = 1.25 V			±100	nA
Input bias current	V_O (FEEDBACK) = 1.25 V			160 500	nA
Common-mode input voltage range	$V_{CC} = 3.6\ \text{V to } 40\ \text{V}$	1.05 to 1.45			V
Open-loop voltage amplification	$R_F = 200\ \text{k}\Omega$	70	80		dB
Unity-gain bandwidth			1.5		MHz
Common-mode rejection ratio		60	80		dB
Positive output voltage swing		$V_{ref}-0.1$			V
Negative output voltage swing				1	V
Output (sink) current (FEEDBACK)	$V_{ID} = -0.1\ \text{V}, V_O = 1.25\ \text{V}$	0.5	1.6		mA
Output (source) current (FEEDBACK)	$V_{ID} = 0.1\ \text{V}, V_O = 1.25\ \text{V}$	-45	-70		μA

† All typical values are at $T_A = 25^\circ\text{C}$.

output section

PARAMETER	TEST CONDITIONS	TL1451AC			UNIT
		MIN	TYP†	MAX	
Collector off-state current	$V_O = 50\ \text{V}$			10	μA
Output saturation voltage	$I_O = 10\ \text{mA}$		1.2	2	V
Short-circuit output current	$V_O = 6\ \text{V}$		90		mA

† All typical values are at $T_A = 25^\circ\text{C}$.

pwm comparator section

PARAMETER	TEST CONDITIONS	TL1451AC			UNIT
		MIN	TYP†	MAX	
Input threshold voltage at $f = 10\ \text{kHz}$ (FEEDBACK)	Zero duty cycle		2.05	2.25	V
	Maximum duty cycle	1.2	1.45		

† All typical values are at $T_A = 25^\circ\text{C}$.

total device

PARAMETER	TEST CONDITIONS	TL1451AC			UNIT
		MIN	TYP†	MAX	
Standby supply current	Off-state		1.3	1.8	mA
Average supply current	$R_T = 10\ \text{k}\Omega$		1.7	2.4	mA

† All typical values are at $T_A = 25^\circ\text{C}$.

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electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 6\text{ V}$, $f = 200\text{ kHz}$ (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS		TL1451AQ, TL1451AM			UNIT
			MIN	TYP†	MAX	
Output voltage (pin 16)	I _O = 1 mA	T _A = 25°C	2.40	2.50	2.60	V
		T _A = MIN and 125°C	2.35	2.46	2.65	
Output voltage change with temperature			–0.63%		*±4%	
Input voltage regulation	V _{CC} = 3.6 V to 40 V	T _A = 25°C	2.0		12.5	mV
		T _A = 125°C	0.7		15	
		T _A = MIN	0.3		30	
Output voltage regulation	I _O = 0.1 mA to 1 mA	T _A = 25°C	1.0		7.5	mV
		T _A = 125°C	0.3		14	
		T _A = MIN	0.3		20	
Short-circuit output current	V _O = 0		3	10	30	mA

*These parameters are not production tested.

† All typical values are at $T_A = 25^\circ\text{C}$ unless otherwise indicated.

undervoltage lockout section

PARAMETER	TEST CONDITIONS		TL1451AQ, TL1451AM			UNIT
			MIN	TYP†	MAX	
Upper threshold voltage (V _{CC})		T _A = 25°C	2.72			V
		T _A = 125°C	1.70			
		T _A = MIN	3.15			
Lower threshold voltage (V _{CC})		T _A = 25°C	2.60			V
		T _A = 125°C	1.65			
		T _A = MIN	3.09			
Hysteresis (V _{CC})		T _A = 25°C	80	120	mV	
		T _A = 125°C	10	50		
		T _A = MIN	10	60		
Reset threshold voltage (V _{CC})		T _A = 25°C	1.50			V
		T _A = 125°C	0.95			
		T _A = MIN	1.50			

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short-circuit protection control section

PARAMETER	TEST CONDITIONS	TL1451AQ, TL1451AM			UNIT
		MIN	TYP†	MAX	
Input threshold voltage (SCP)	$T_A = 25^\circ\text{C}$	650	700	750	mV
	$T_A = 125^\circ\text{C}$	400	478	550	
	$T_A = \text{MIN}$	800	880	950	
Standby voltage (SCP)		140	185	230	mV
Latched input voltage (SCP)	$T_A = 25^\circ\text{C}$		60	120	mV
	$T_A = 125^\circ\text{C}$		70	120	
	$T_A = \text{MIN}$		60	120	
Equivalent timing resistance			170		k Ω
Comparator threshold voltage (FEEDBACK)			1.18		V

† All typical values are at $T_A = 25^\circ\text{C}$ unless otherwise indicated.

oscillator section

PARAMETER	TEST CONDITIONS		TL1451AQ, TL1451AM			UNIT
			MIN	TYP†	MAX	
Frequency	$C_T = 330\text{ pF}$, $R_T = 10\text{ k}\Omega$	$T_A = 25^\circ\text{C}$		200		kHz
		$T_A = 125^\circ\text{C}$		195		
		$T_A = \text{MIN}$		193		
Standard deviation of frequency	$C_T = 330\text{ pF}$, $R_T = 10\text{ k}\Omega$			2%		
Frequency change with voltage	$V_{CC} = 3.6\text{ V to }40\text{ V}$	$T_A = 25^\circ\text{C}$		1%		
		$T_A = 125^\circ\text{C}$		1%		
		$T_A = \text{MIN}$		3%		
Frequency change with temperature				1.37%	$\pm 10\%$	

*These parameters are not production tested.

† All typical values are at $T_A = 25^\circ\text{C}$ unless otherwise indicated.

dead-time control section

PARAMETER	TEST CONDITIONS	TL1451AQ, TL1451AM			UNIT
		MIN	TYP†	MAX	
Input bias current (DTC)	$T_A = 25^\circ\text{C}$			1	μA
	$T_A = \text{MIN and } 125^\circ\text{C}$			3	
Latch mode (source) current (DTC)		-80	-145		μA
Latched input voltage (DTC)	$T_A = 25^\circ\text{C}$	2.30			V
	$T_A = 125^\circ\text{C}$	2.22	2.32		
	$T_A = \text{MIN}$	2.28	2.40		
Input threshold voltage at $f = 10\text{ kHz}$ (DTC)	Zero duty cycle		2.05	*2.25	V
	Maximum duty cycle	*1.20	1.45		

*These parameters are not production tested.

† All typical values are at $T_A = 25^\circ\text{C}$ unless otherwise indicated.

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error-amplifier section

PARAMETER	TEST CONDITIONS	TL1451AQ, TL1451AM			UNIT
		MIN	TYP [†]	MAX	
Input offset voltage	V_O (FEEDBACK) = 1.25 V	$T_A = 25^\circ\text{C}$		±6	mV
		$T_A = 125^\circ\text{C}$		±10	
		$T_A = \text{MIN}$		±12	
Input offset current	V_O (FEEDBACK) = 1.25 V	$T_A = 25^\circ\text{C}$		±100	nA
		$T_A = 125^\circ\text{C}$		±100	
		$T_A = \text{MIN}$		±200	
Input bias current	V_O (FEEDBACK) = 1.25 V	$T_A = 25^\circ\text{C}$	160	500	nA
		$T_A = 125^\circ\text{C}$	100	500	
		$T_A = \text{MIN}$	142	700	
Common-mode input voltage range	$V_{CC} = 3.6 \text{ V to } 40 \text{ V}$	1.05 to 1.45			V
Open-loop voltage amplification	$R_F = 200 \text{ k}\Omega$	$T_A = 25^\circ\text{C}$	70	80	dB
		$T_A = 125^\circ\text{C}$	70	80	
		$T_A = \text{MIN}$	64	80	
Unity-gain bandwidth			1.5		MHz
Common-mode rejection ratio		60	80		dB
Positive output voltage swing		2			V
Negative output voltage swing				1	V
Output (sink) current (FEEDBACK)	$V_{ID} = -0.1 \text{ V}, V_O = 1.25 \text{ V}$	$T_A = 25^\circ\text{C}$	0.5	1.6	mA
		$T_A = 125^\circ\text{C}$	0.4	1.8	
		$T_A = \text{MIN}$	0.3	1.7	
Output (source) current (FEEDBACK)	$V_{ID} = 0.1 \text{ V}, V_O = 1.25 \text{ V}$	$T_A = 25^\circ\text{C}$	-45	-70	μA
		$T_A = 125^\circ\text{C}$	-25	-50	
		$T_A = \text{MIN}$	-15	-70	

[†] All typical values are at $T_A = 25^\circ\text{C}$ unless otherwise indicated.

output section

PARAMETER	TEST CONDITIONS	TL1451AQ, TL1451AM			UNIT
		MIN	TYP [†]	MAX	
Collector off-state current	$V_O = 50 \text{ V}$			10	μA
Output saturation voltage	$T_A = 25^\circ\text{C}$		1.20	2.0	V
	$T_A = 125^\circ\text{C}$		1.60	2.4	
	$T_A = \text{MIN}$		1.36	2.2	
Short-circuit output current	$V_O = 6 \text{ V}$		90		mA

[†] All typical values are at $T_A = 25^\circ\text{C}$ unless otherwise indicated.

pwm comparator section

PARAMETER	TEST CONDITIONS	TL1451AQ, TL1451AM			UNIT
		MIN	TYP [†]	MAX	
Input threshold voltage at $f = 10 \text{ kHz}$ (FEEDBACK)	Zero duty cycle		2.05	*2.25	V
	Maximum duty cycle	*1.20	1.45		

*These parameters are not production tested.

[†] All typical values are at $T_A = 25^\circ\text{C}$ unless otherwise indicated.

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total device

PARAMETER	TEST CONDITIONS	TL1451AQ, TL1451AM			UNIT
		MIN	TYP [†]	MAX	
Standby supply current	Off-state		1.3	1.8	mA
Average supply current	$R_T = 10\text{ k}\Omega$		1.7	2.4	mA

[†] All typical values are at $T_A = 25^\circ\text{C}$ unless otherwise indicated.

PARAMETER MEASUREMENT INFORMATION

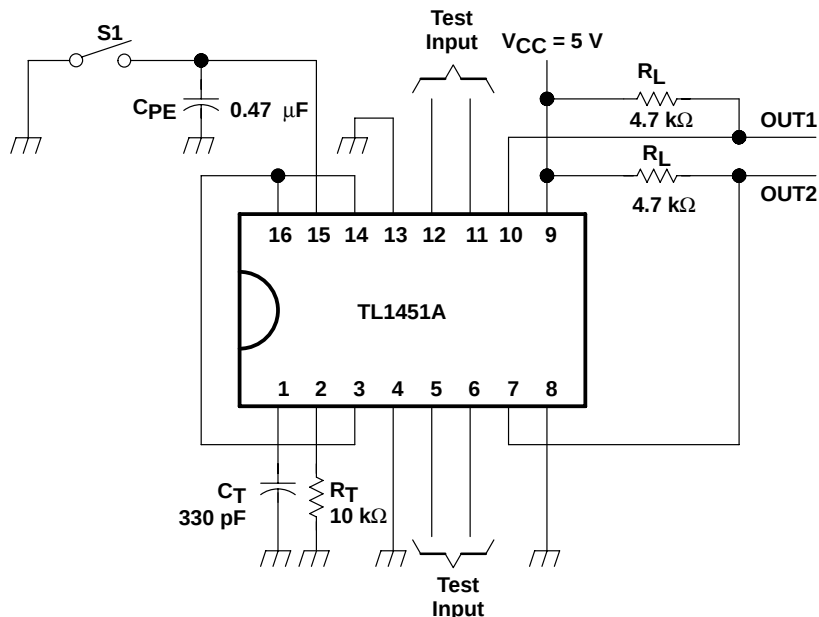
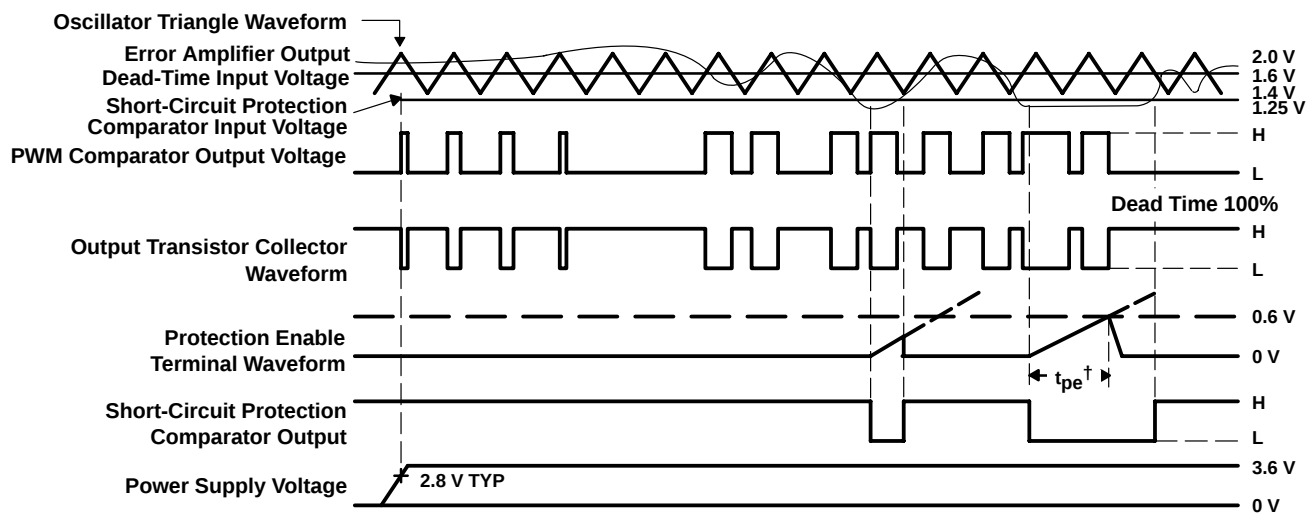


Figure 1. Test Circuit



[†] Protection Enable Time, $t_{pe} = (0.051 \times 10^6 \times C_{pe})$ in seconds

Figure 2. TL1451A Timing Diagram

TL1451A

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TYPICAL CHARACTERISTICS

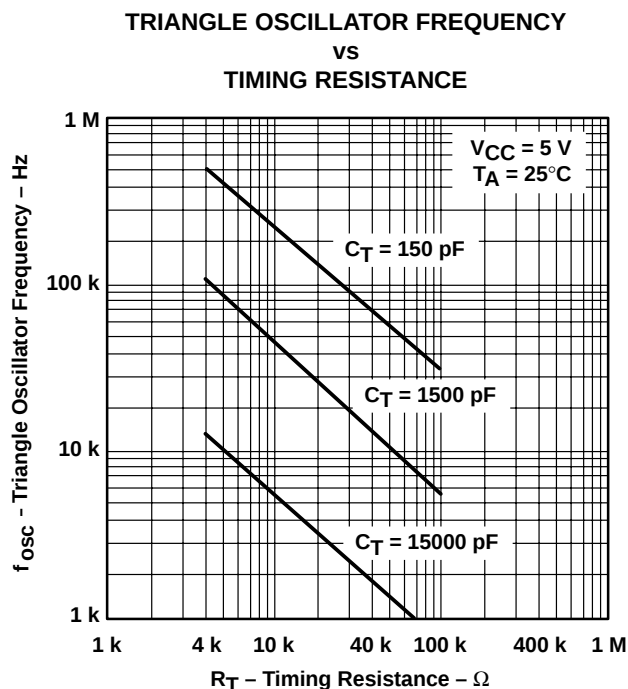


Figure 3

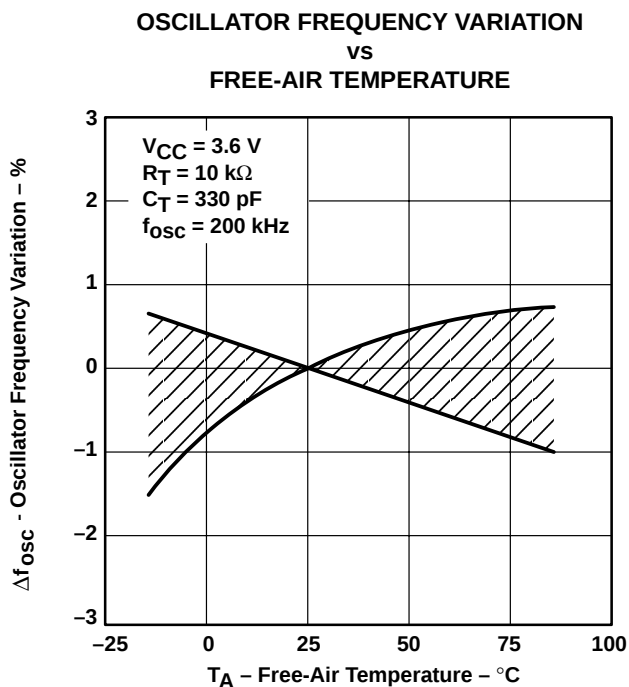


Figure 4

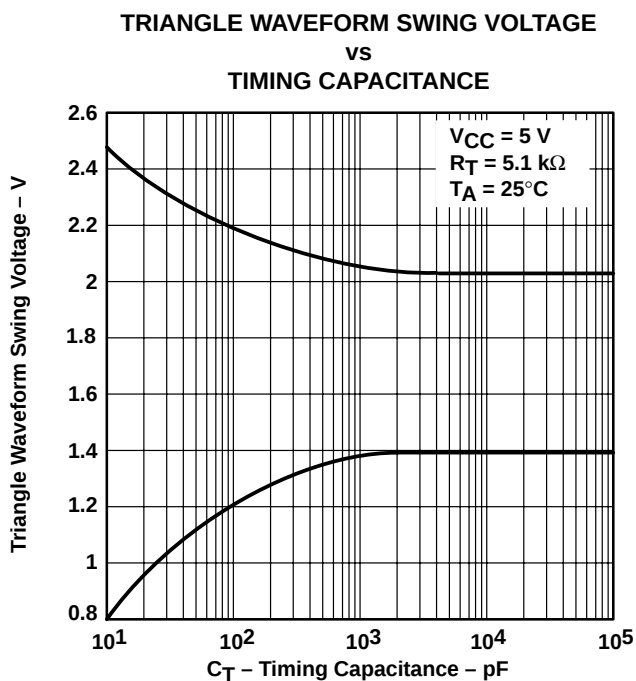


Figure 5

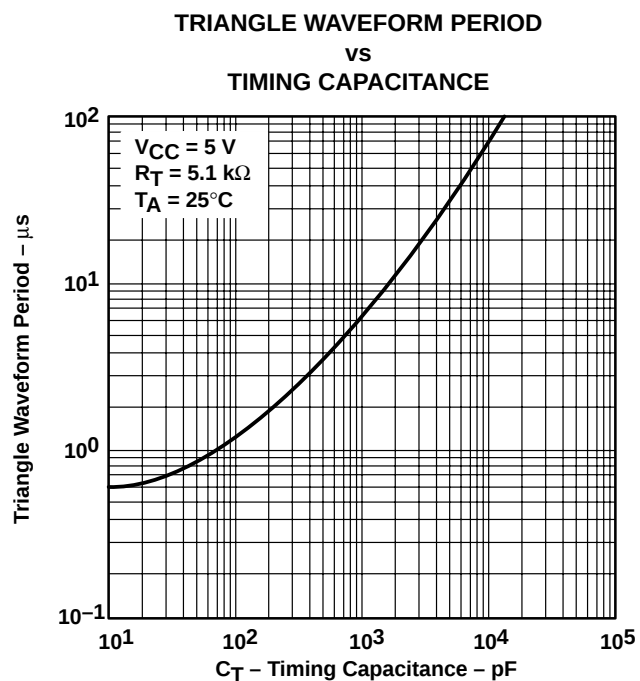


Figure 6

TYPICAL CHARACTERISTICS

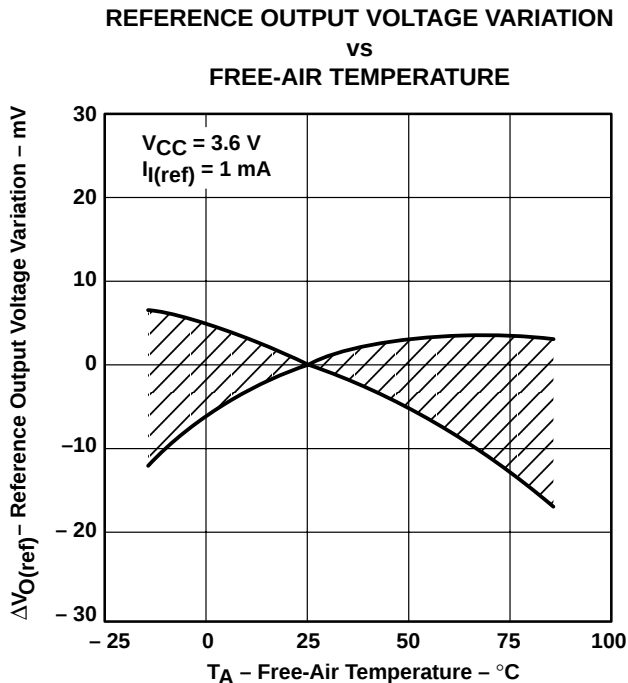


Figure 7

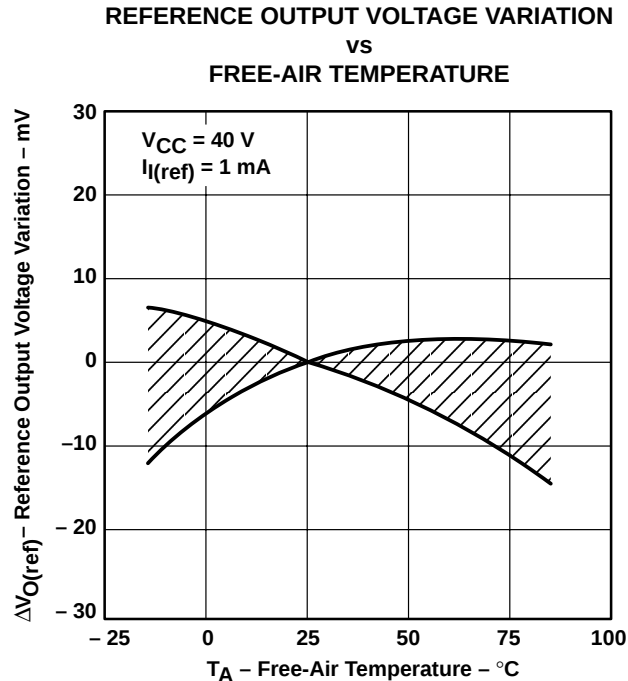


Figure 8

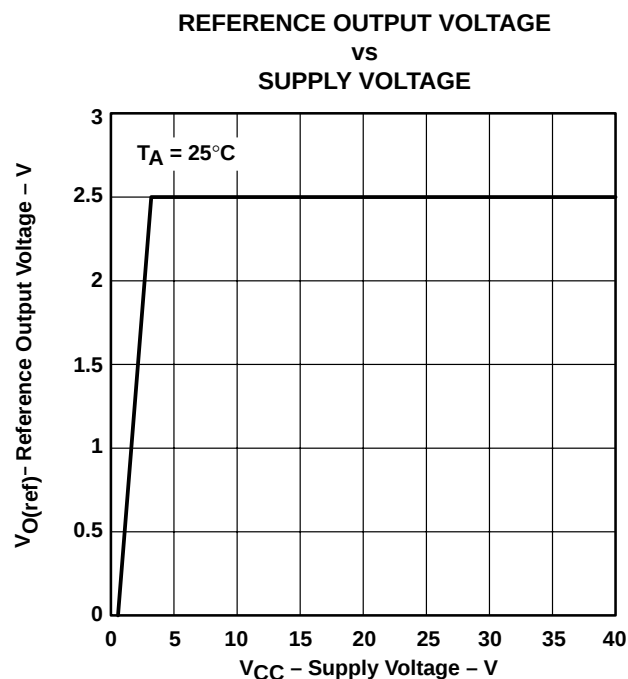


Figure 9

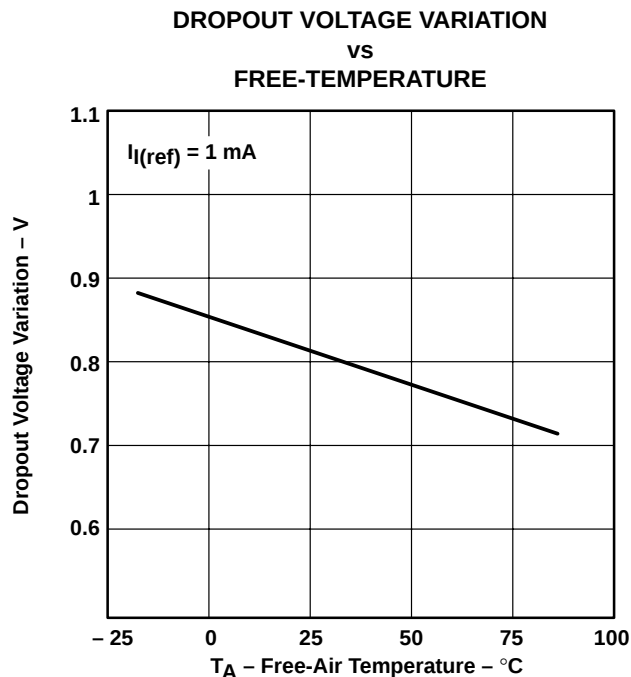


Figure 10

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TYPICAL CHARACTERISTICS

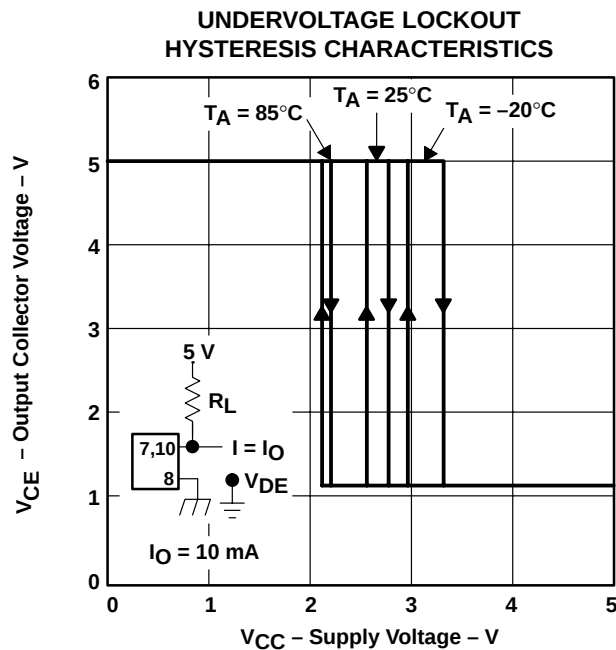


Figure 11

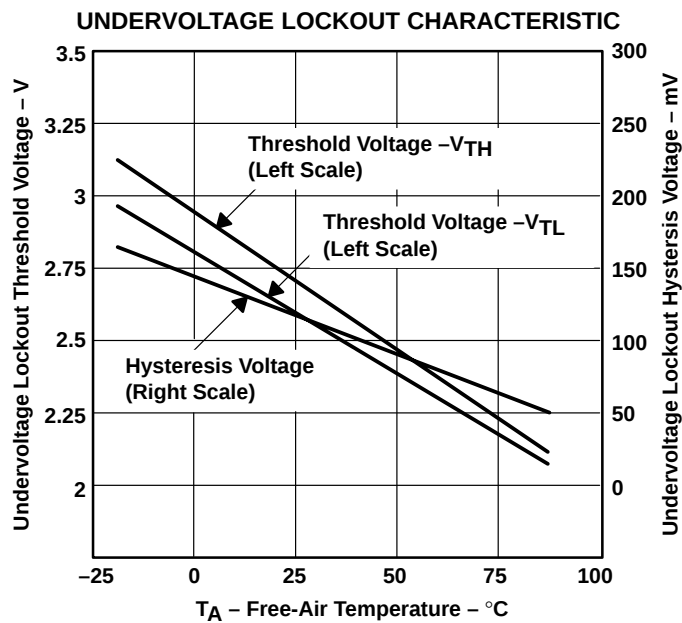


Figure 12

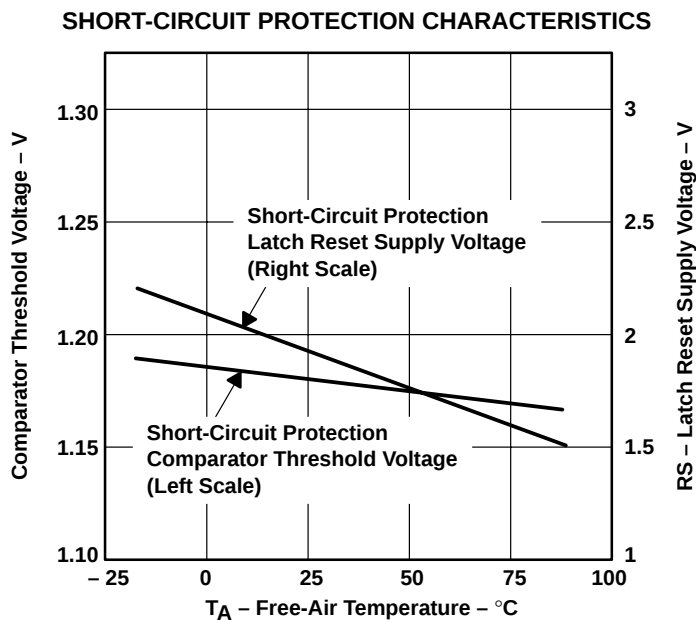


Figure 13

TYPICAL CHARACTERISTICS

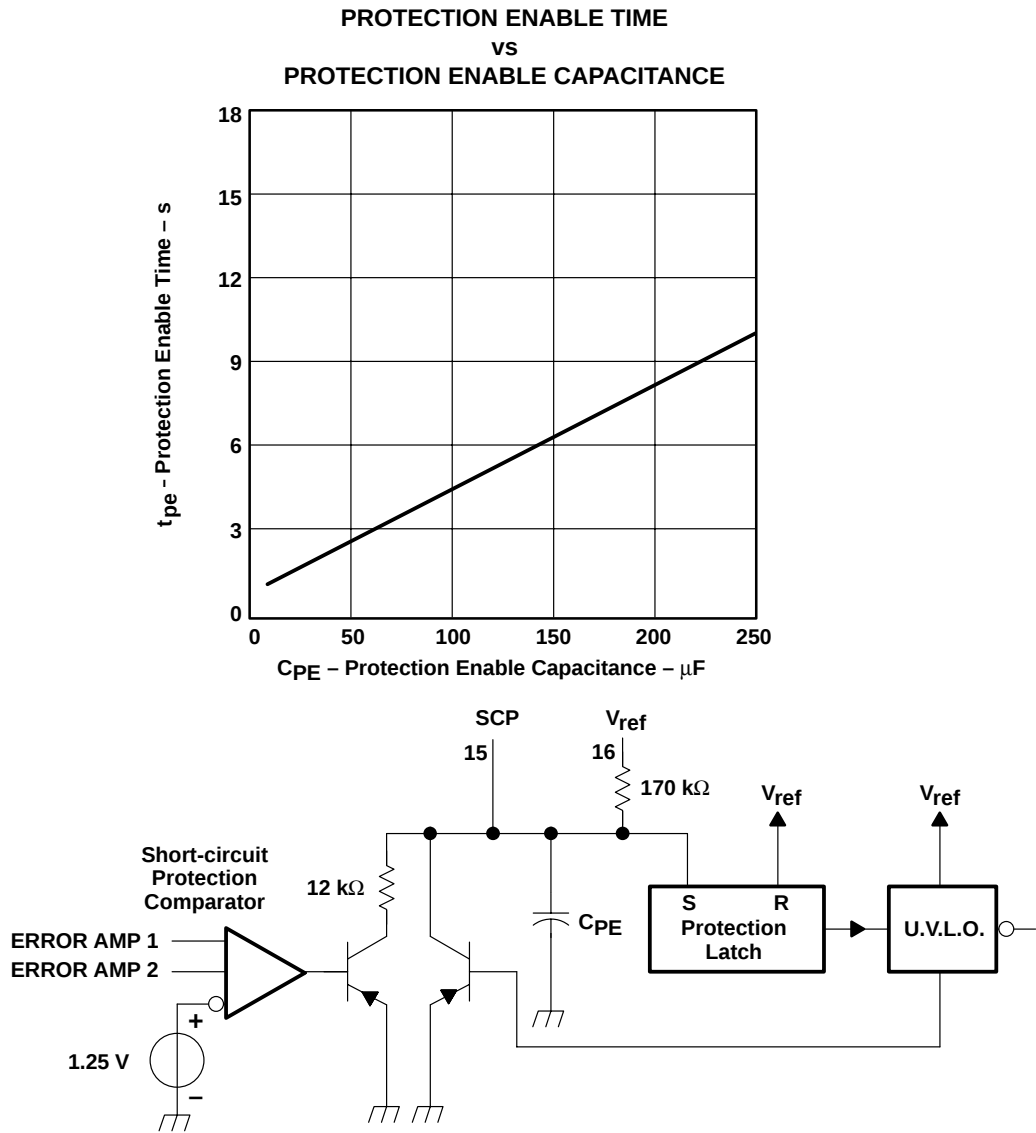


Figure 14

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DUAL PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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TYPICAL CHARACTERISTICS

ERROR AMP MAXIMUM OUTPUT VOLTAGE SWING

VS
FREQUENCY

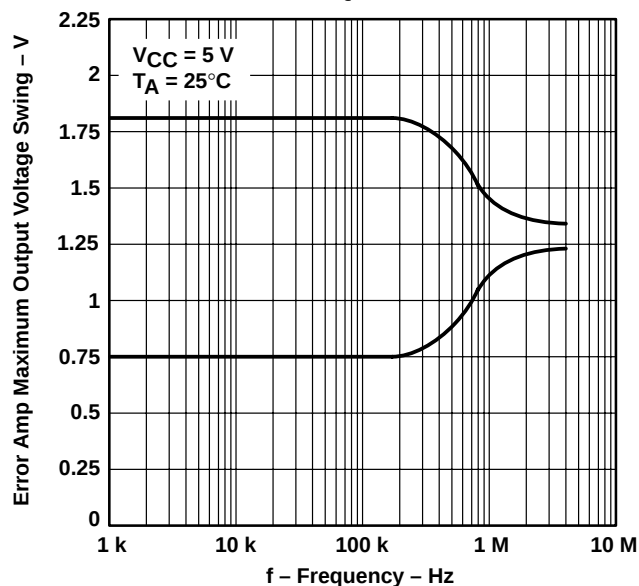


Figure 15

OPEN-LOOP VOLTAGE AMPLIFICATION

VS
FREQUENCY

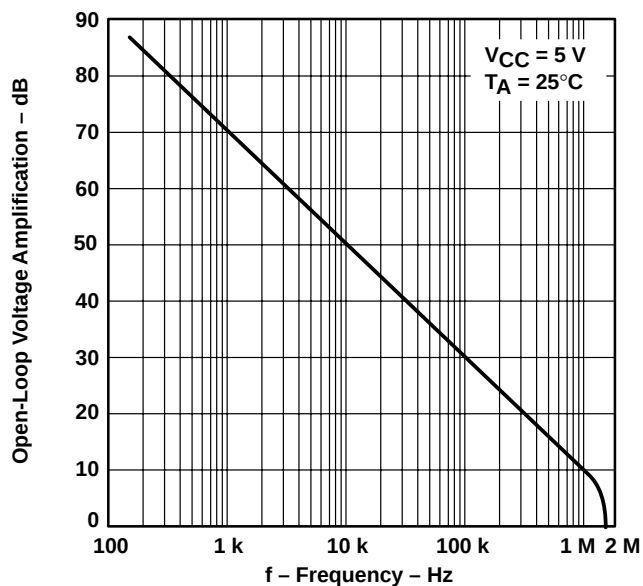


Figure 16

GAIN (AMPLIFIER IN
UNITY-GAIN CONFIGURATION)

VS
FREQUENCY

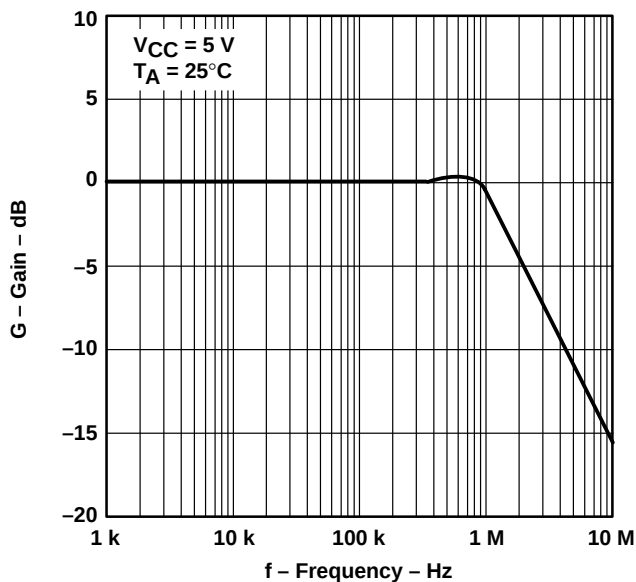
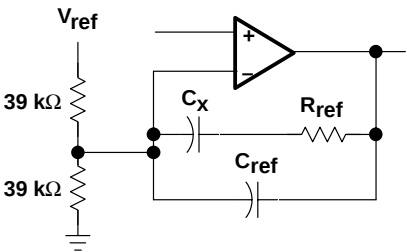
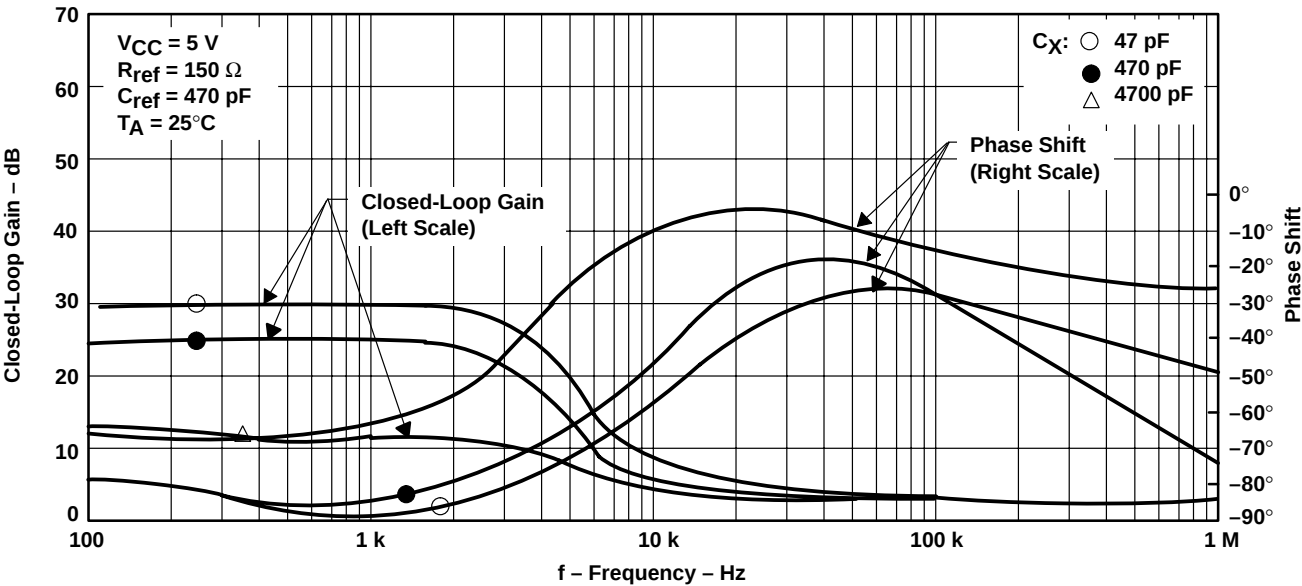


Figure 17

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE SHIFT
VS
FREQUENCY



Test Circuit

Figure 18

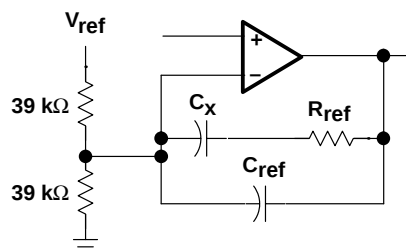
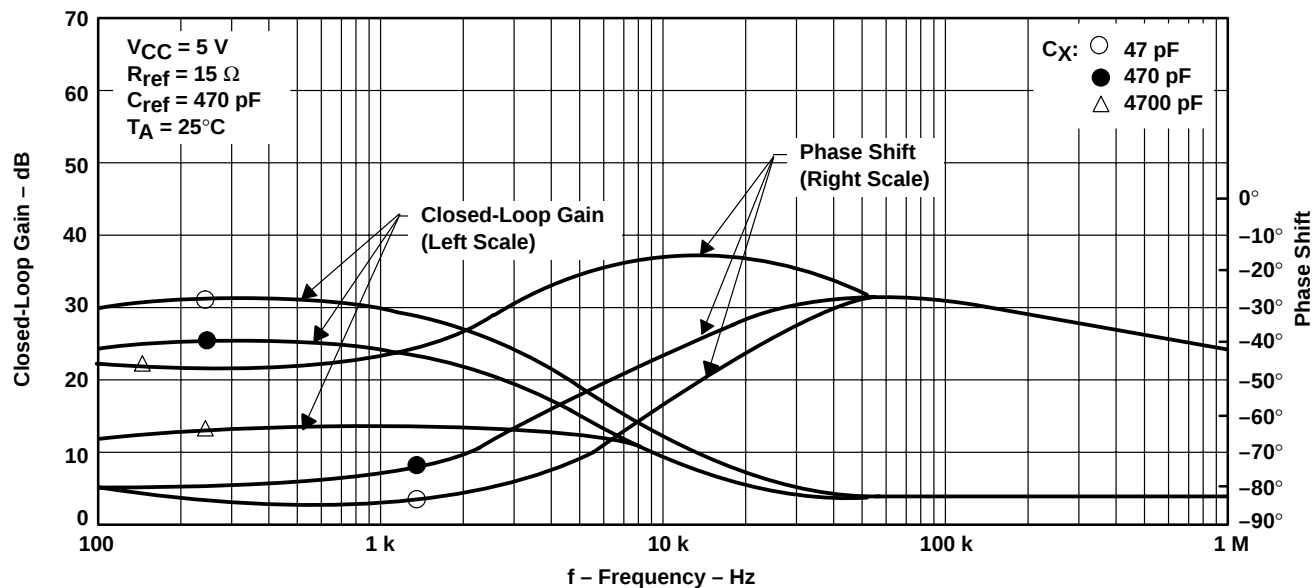
TL1451A

DUAL PULSE-WIDTH-MODULATION CONTROL CIRCUITS

SLVS024E – FEBRUARY 1983 – REVISED NOVEMBER 1999

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE SHIFT vs FREQUENCY

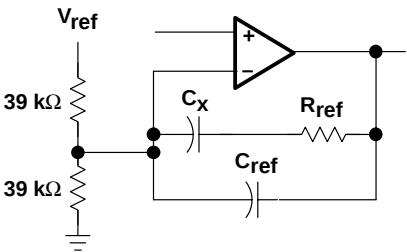
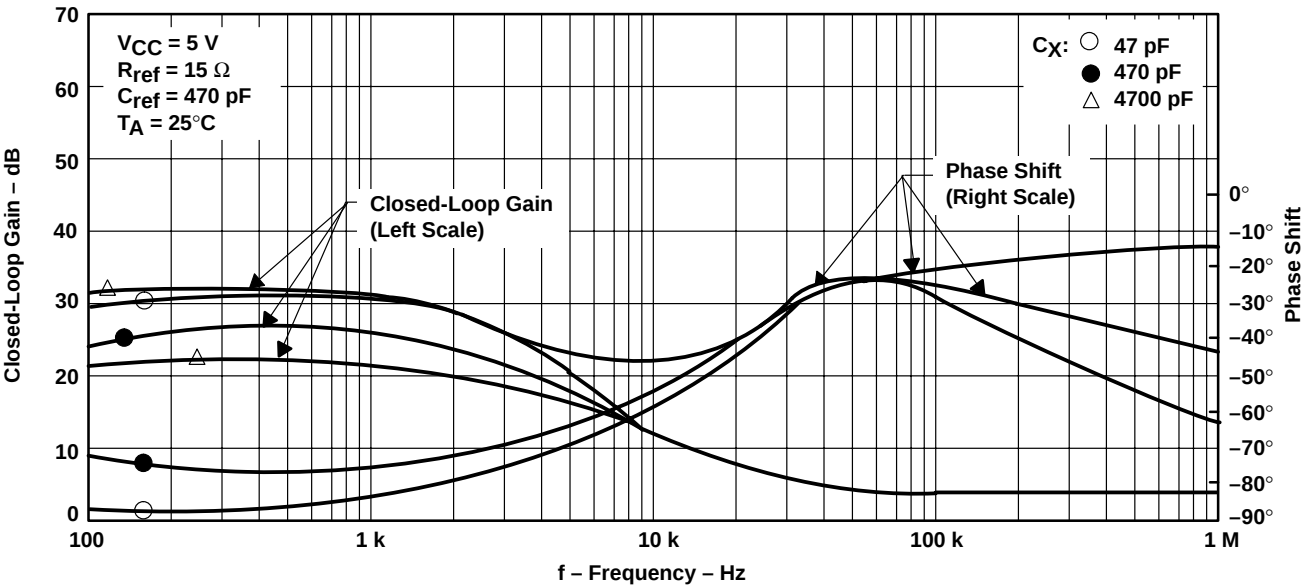


Test Circuit

Figure 19

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE SHIFT
VS
FREQUENCY



Test Circuit

Figure 20

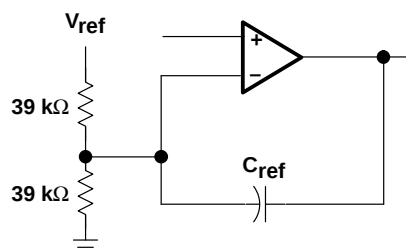
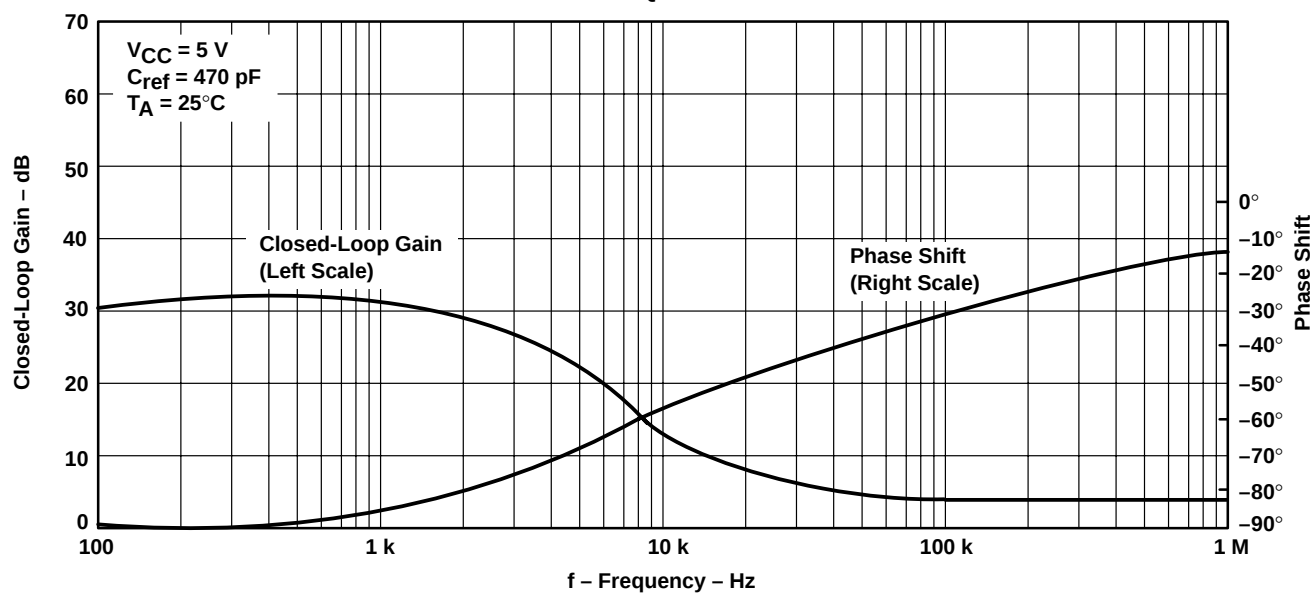
TL1451A

DUAL PULSE-WIDTH-MODULATION CONTROL CIRCUITS

SLVS024E – FEBRUARY 1983 – REVISED NOVEMBER 1999

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE SHIFT vs FREQUENCY



Test Circuit

Figure 21

TYPICAL CHARACTERISTICS

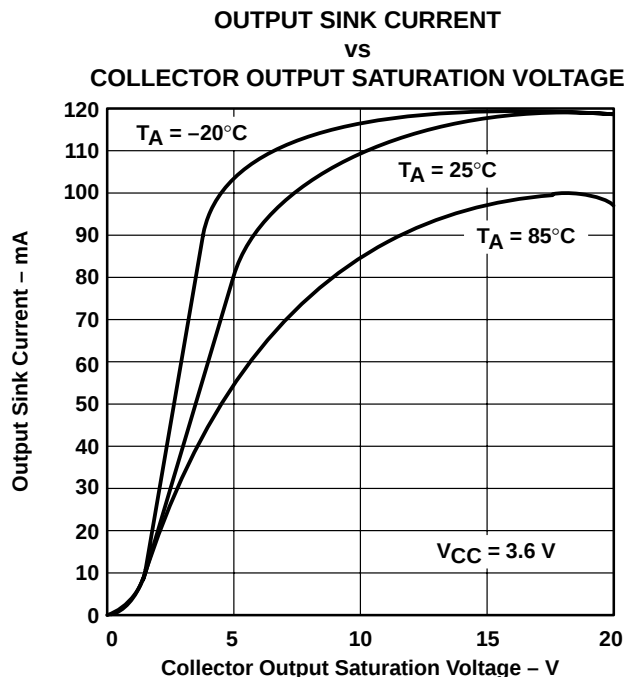


Figure 22

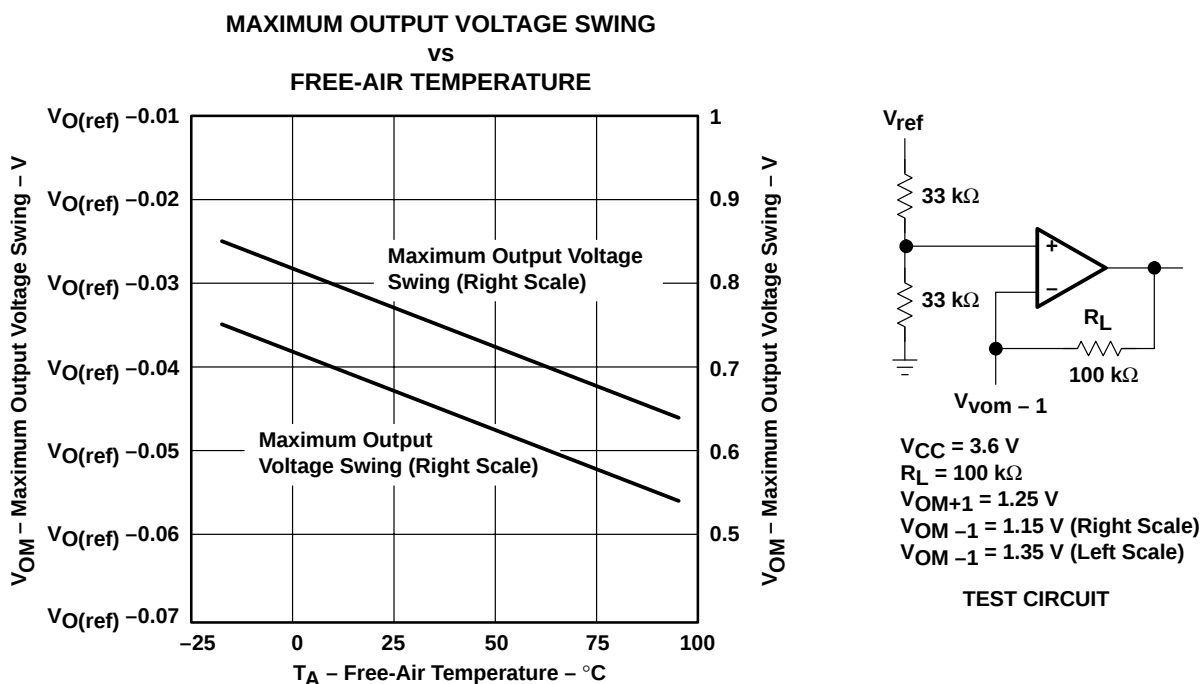


Figure 23

TL1451A

DUAL PULSE-WIDTH-MODULATION CONTROL CIRCUITS

SLVS024E – FEBRUARY 1983 – REVISED NOVEMBER 1999

TYPICAL CHARACTERISTICS

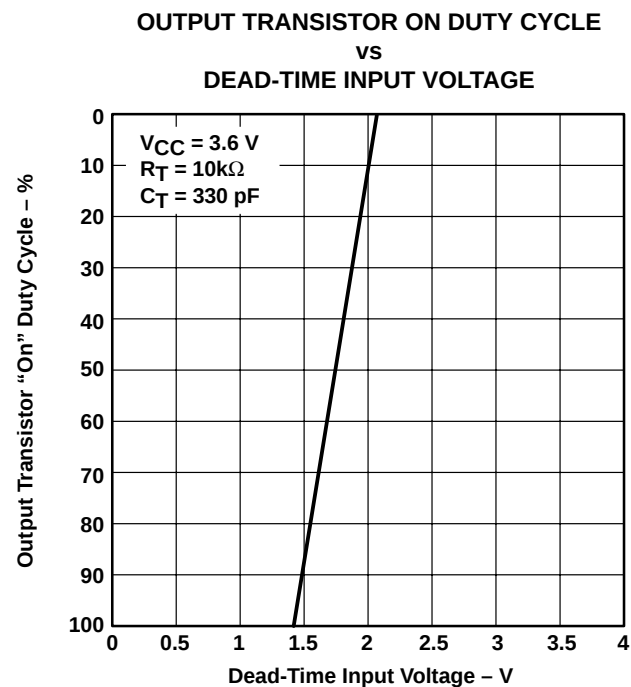


Figure 24

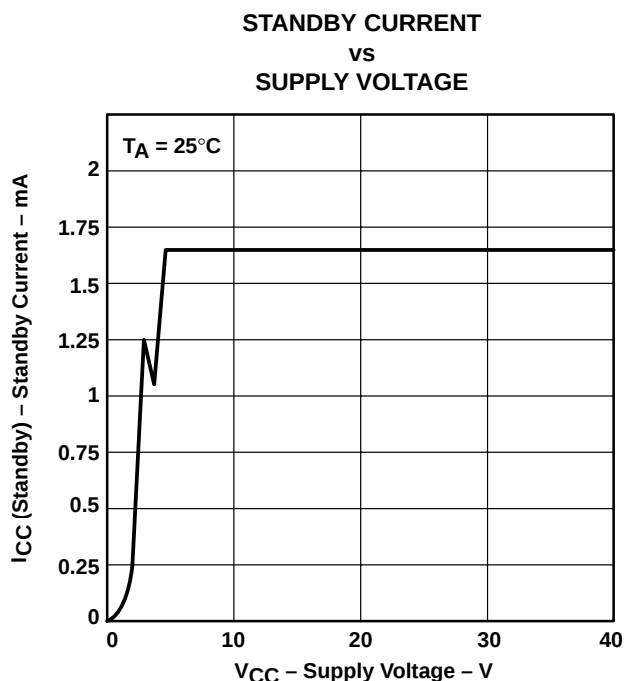


Figure 25

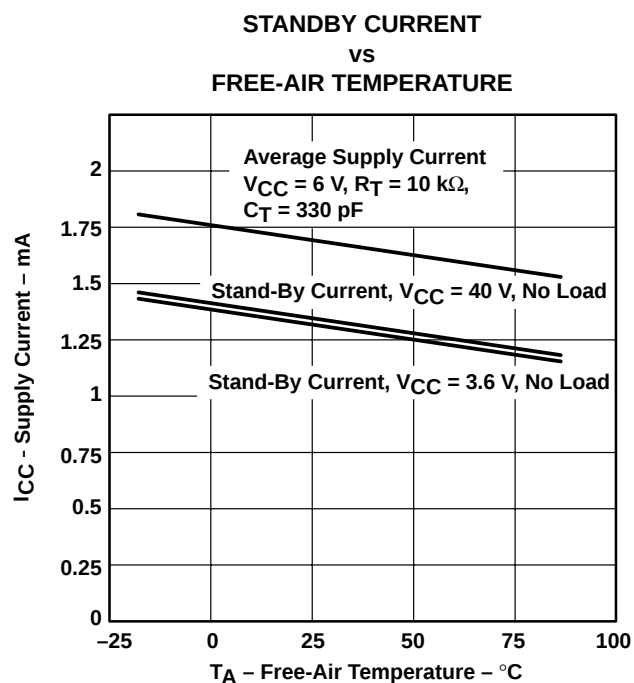


Figure 26

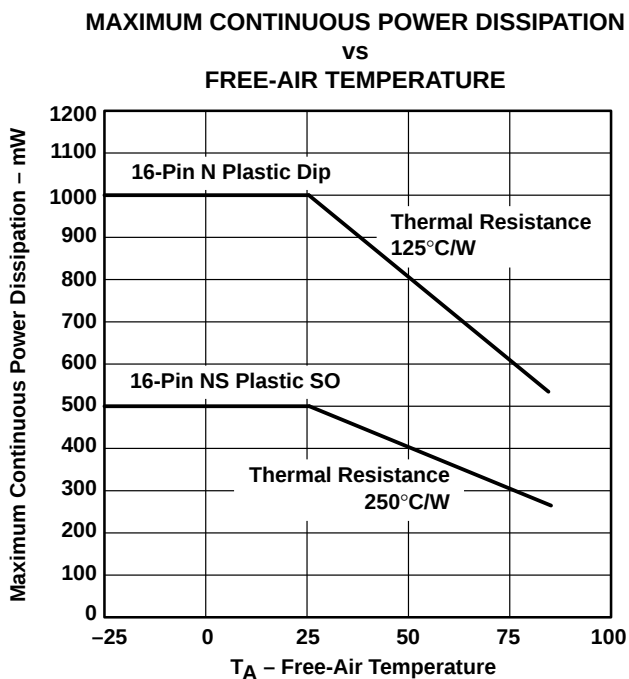
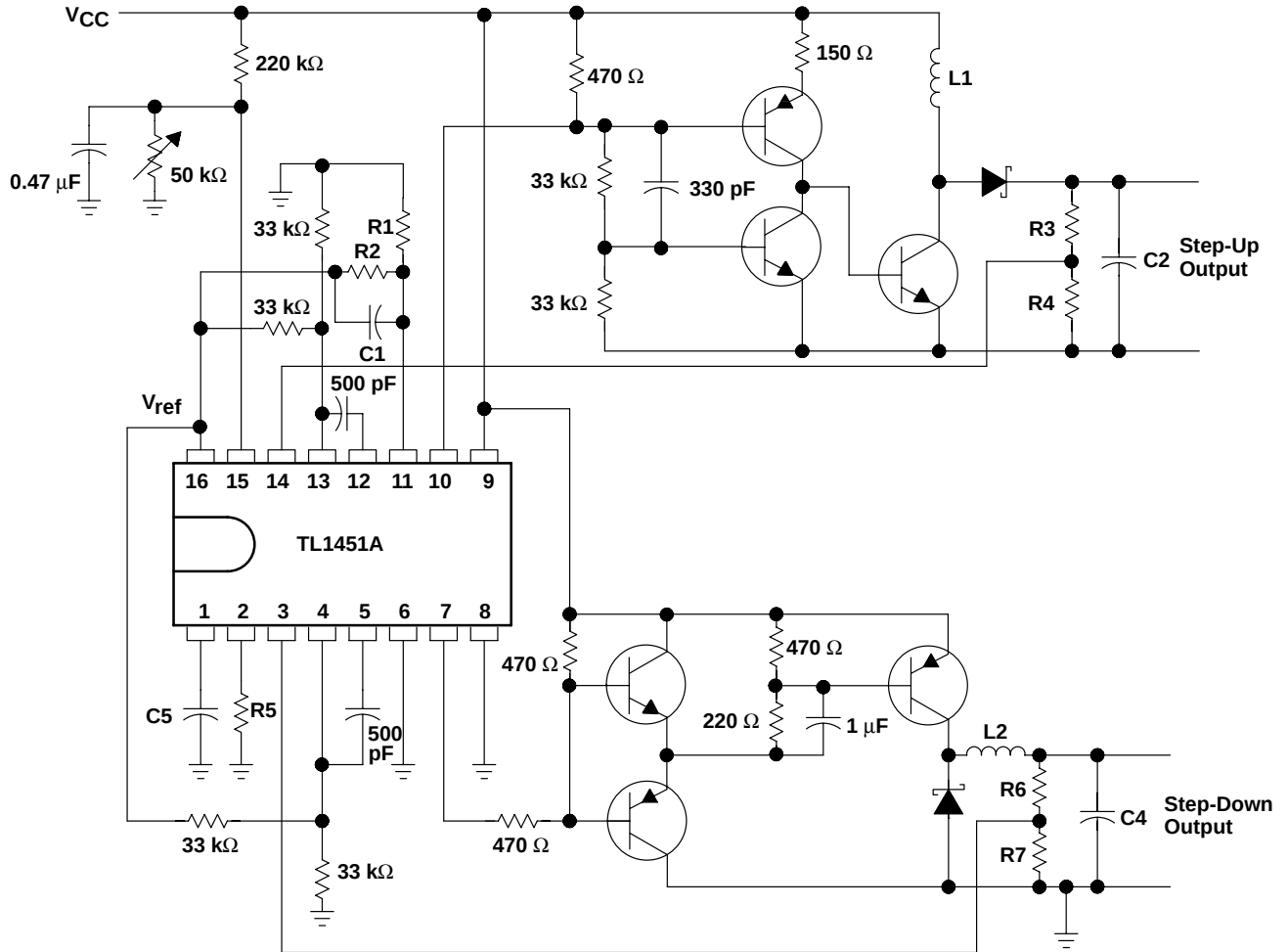


Figure 27

APPLICATION INFORMATION



NOTE A: Values for R1 through R7, C1 through C4, and L1 and L2 depend upon individual application.

Figure 28. High-Speed Dual Switching Regulator

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-9958401Q2A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	
5962-9958401QEA	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	
TL1451ACD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451ACDBLE	NRND	SSOP	DB	16		TBD	Call TI	Call TI	
TL1451ACDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451ACDBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451ACDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451ACDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451ACDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451ACN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL1451ACNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL1451ACNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451ACNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451ACPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451ACPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451ACPWLE	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	
TL1451ACPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451ACPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451AMFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	
TL1451AMJB	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TL1451AQD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451AQDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451AQDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451AQDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451CDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451CDBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451CN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL1451CNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL1451CNS	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451CNSG4	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451CNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451CNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451INSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL1451INSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

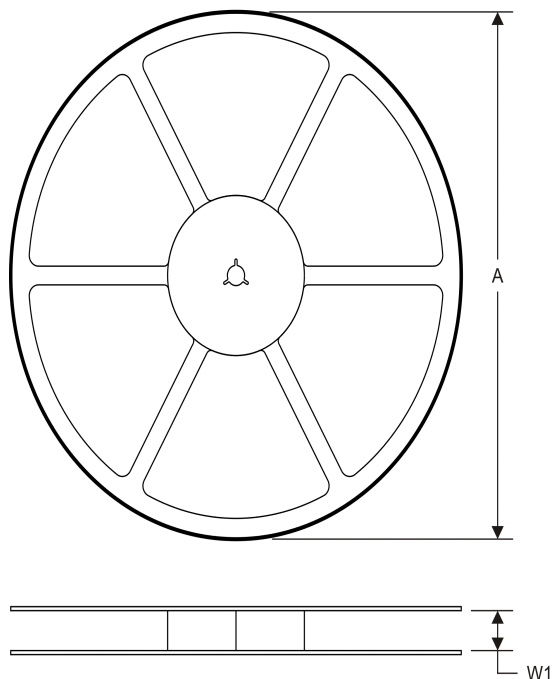
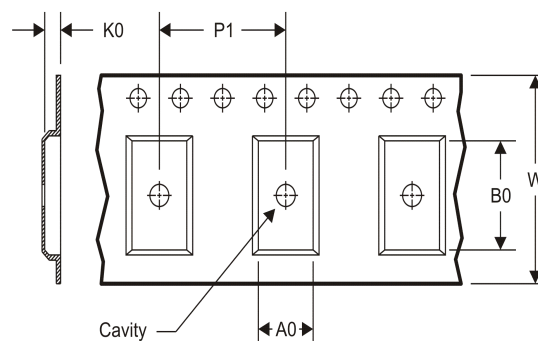
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL1451A, TL1451AM :

- Catalog: [TL1451A](#)
- Automotive: [TL1451A-Q1](#), [TL1451A-Q1](#)
- Enhanced Product: [TL1451A-EP](#), [TL1451A-EP](#)
- Military: [TL1451AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


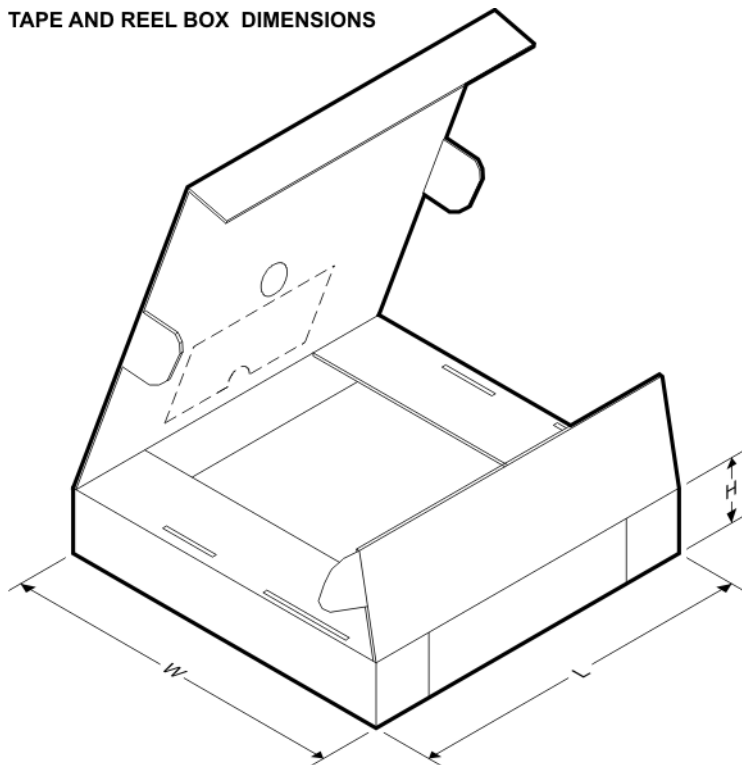
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL1451ACDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL1451ACDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TL1451ACDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TL1451ACNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL1451ACPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL1451AQDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TL1451CDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL1451CNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL1451INSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



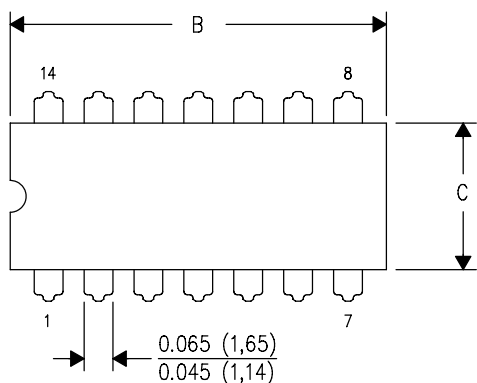
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL1451ACDBR	SSOP	DB	16	2000	367.0	367.0	38.0
TL1451ACDR	SOIC	D	16	2500	367.0	367.0	38.0
TL1451ACDR	SOIC	D	16	2500	333.2	345.9	28.6
TL1451ACNSR	SO	NS	16	2000	367.0	367.0	38.0
TL1451ACPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TL1451AQDR	SOIC	D	16	2500	367.0	367.0	38.0
TL1451CDBR	SSOP	DB	16	2000	367.0	367.0	38.0
TL1451CNSR	SO	NS	16	2000	367.0	367.0	38.0
TL1451INSR	SO	NS	16	2000	367.0	367.0	38.0

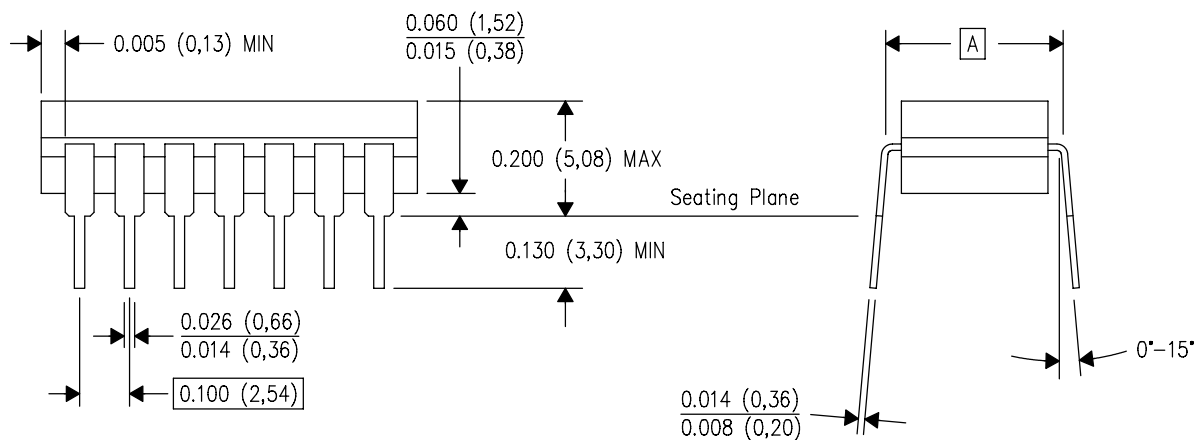
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



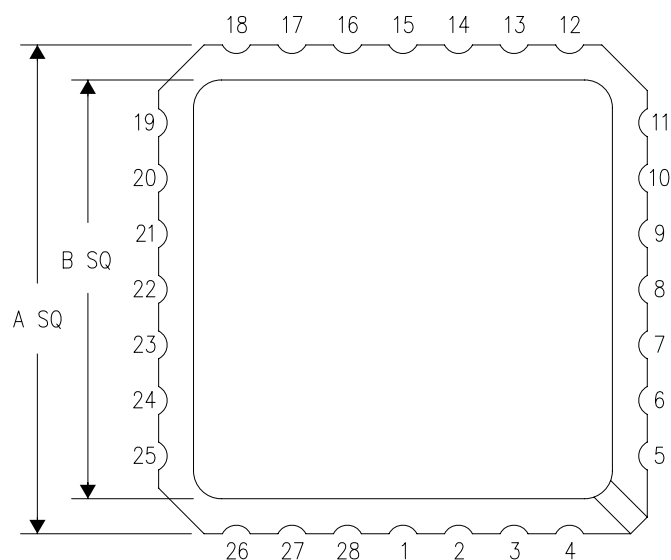
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

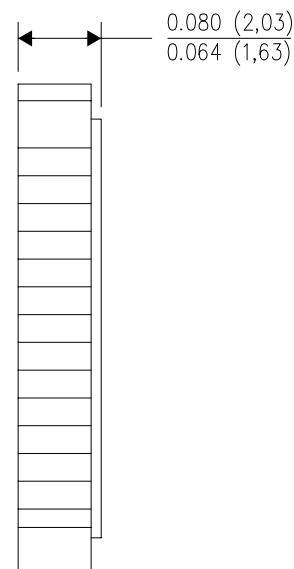
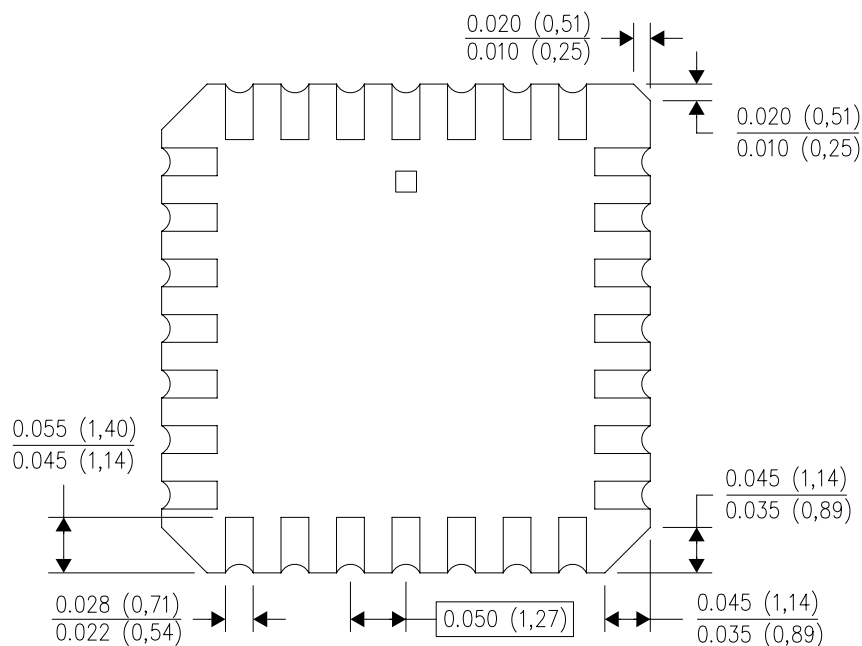
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



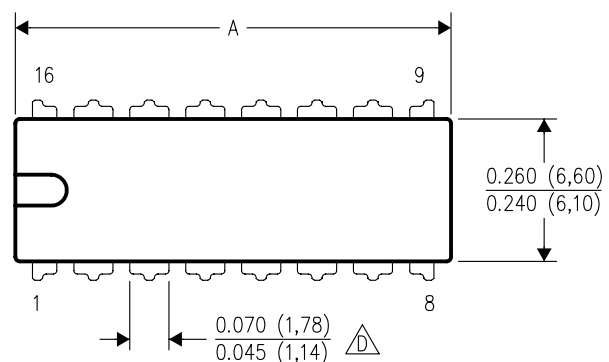
4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

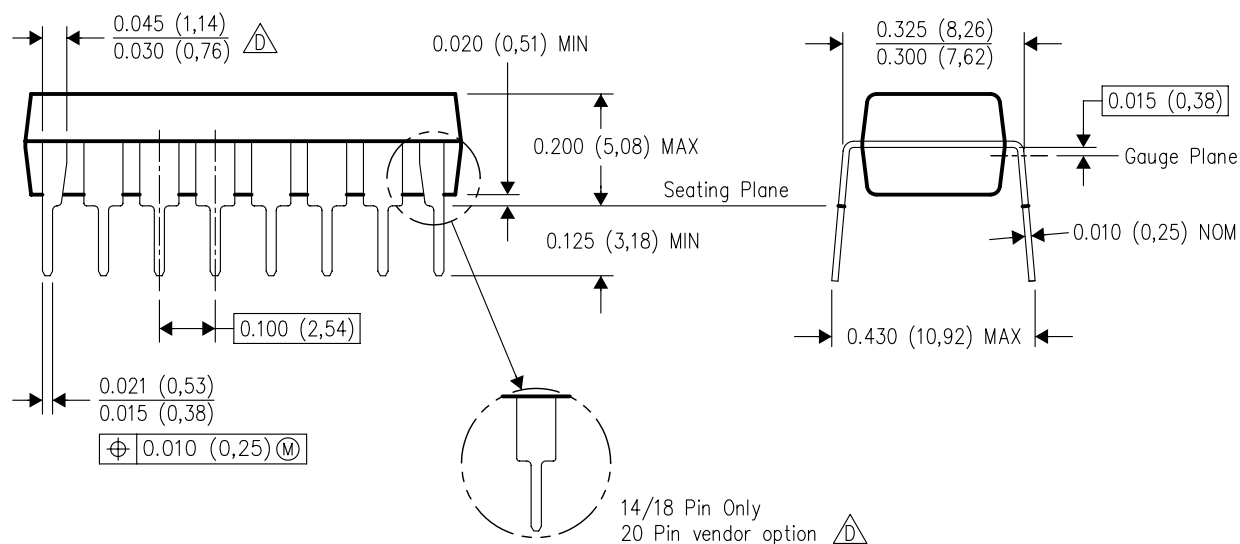
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

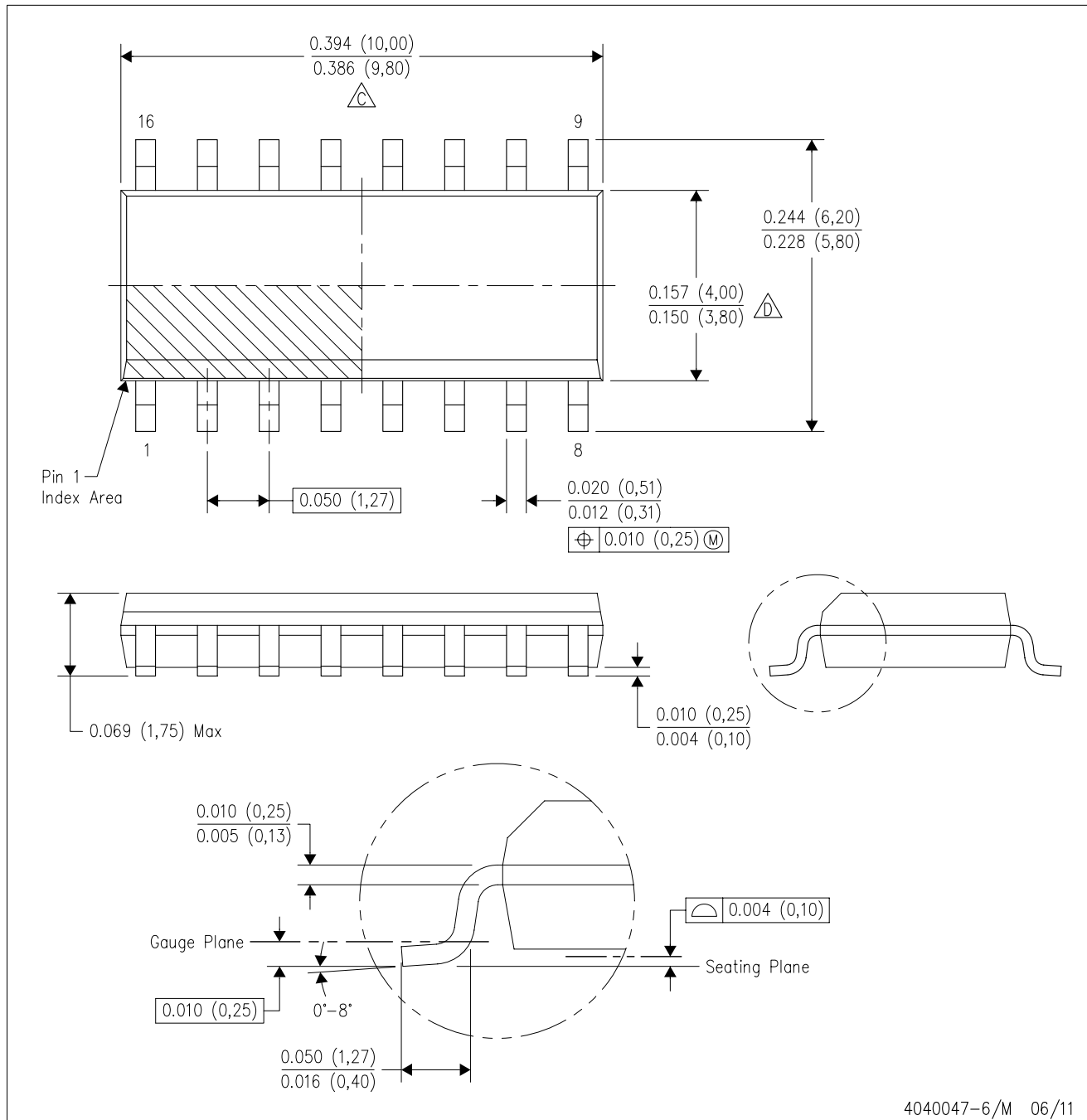


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

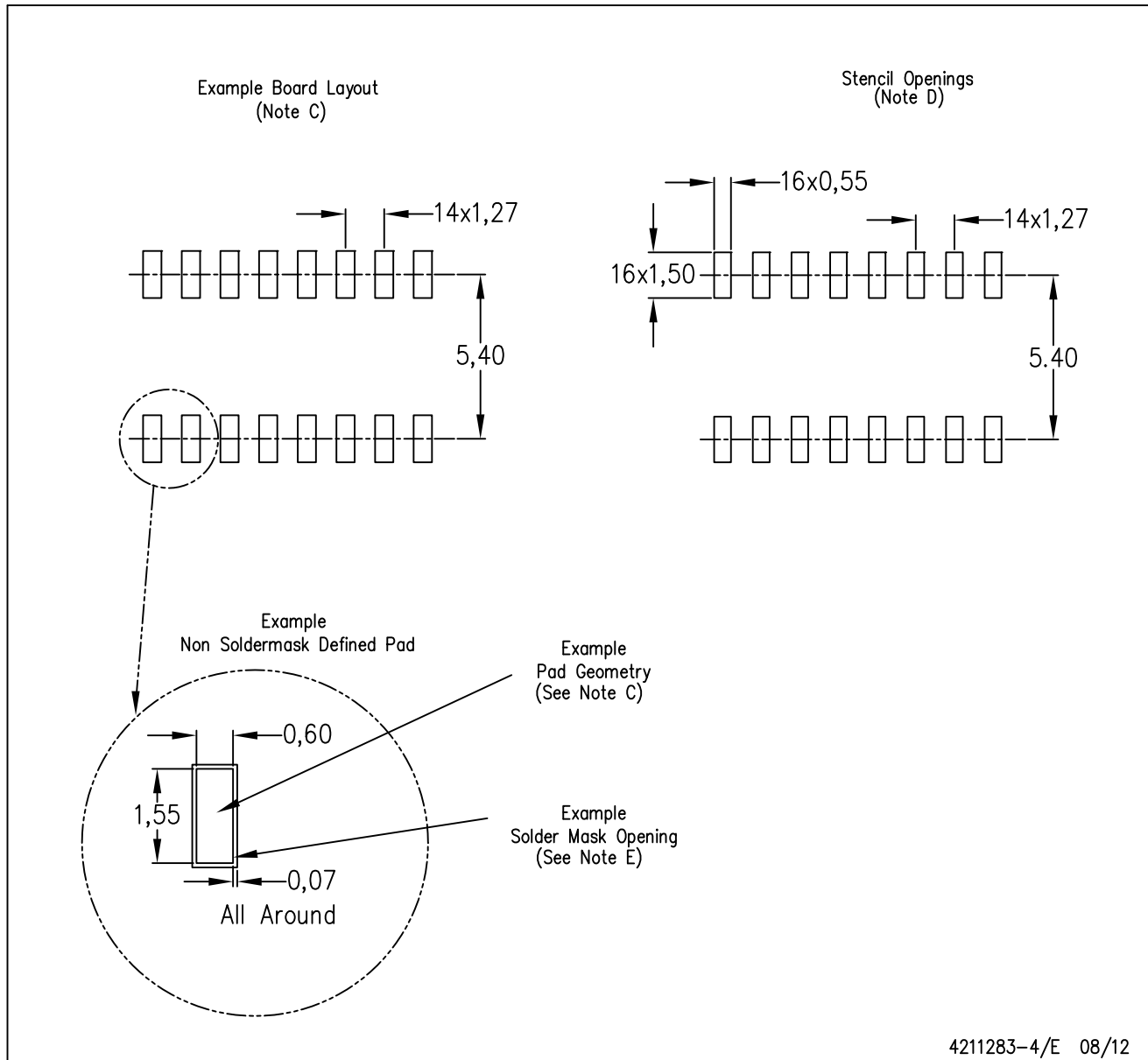


4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

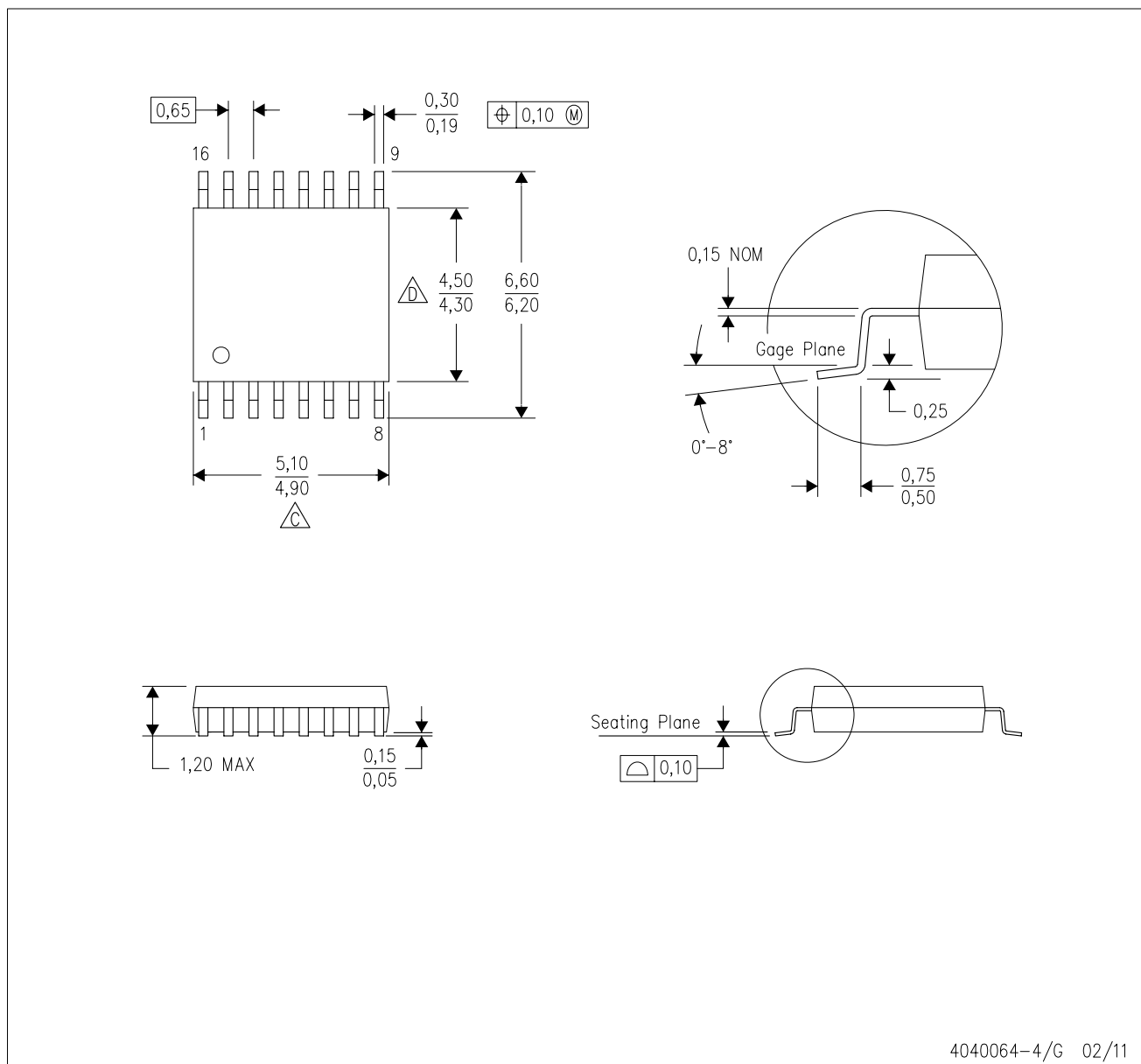
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

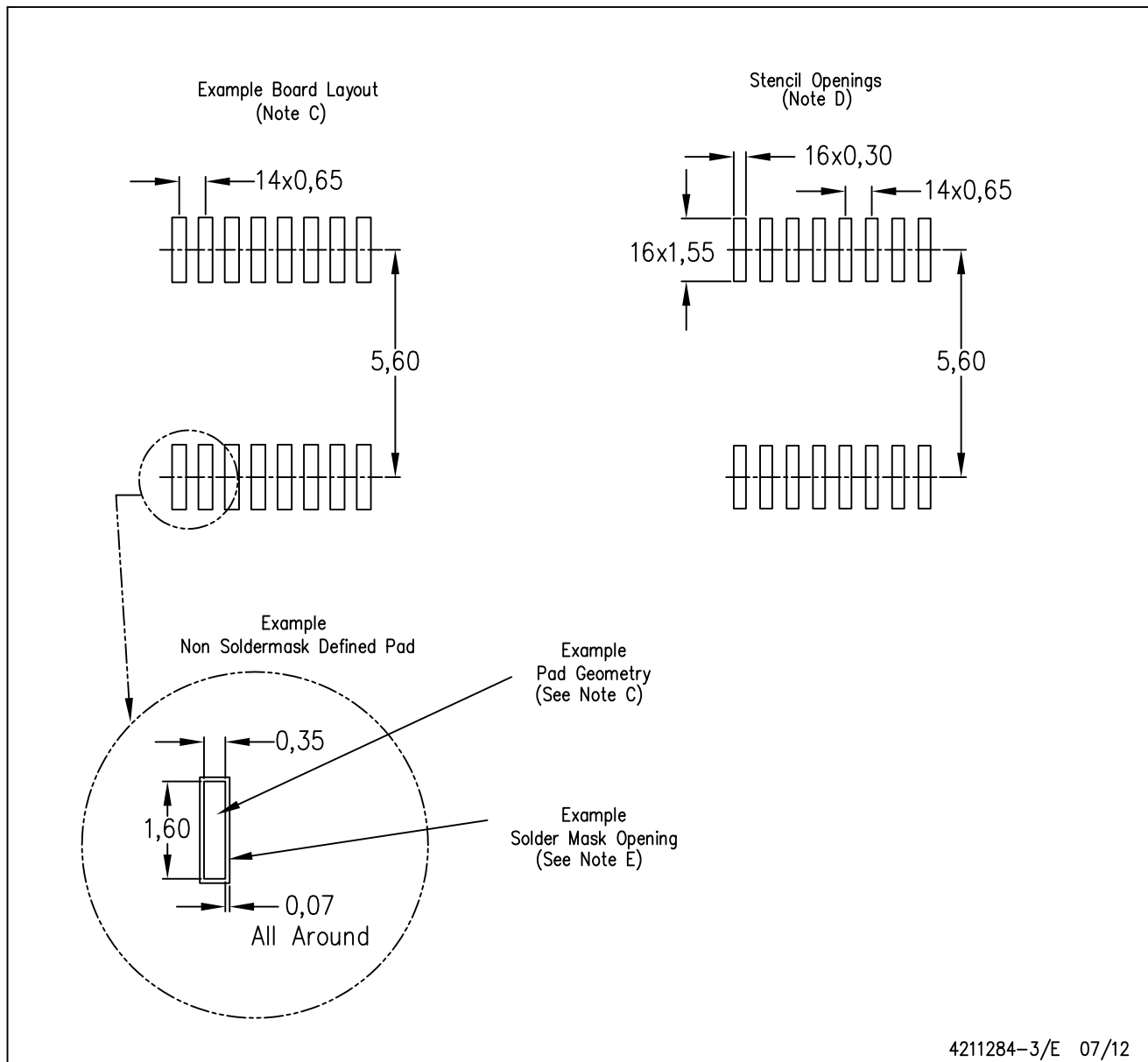


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



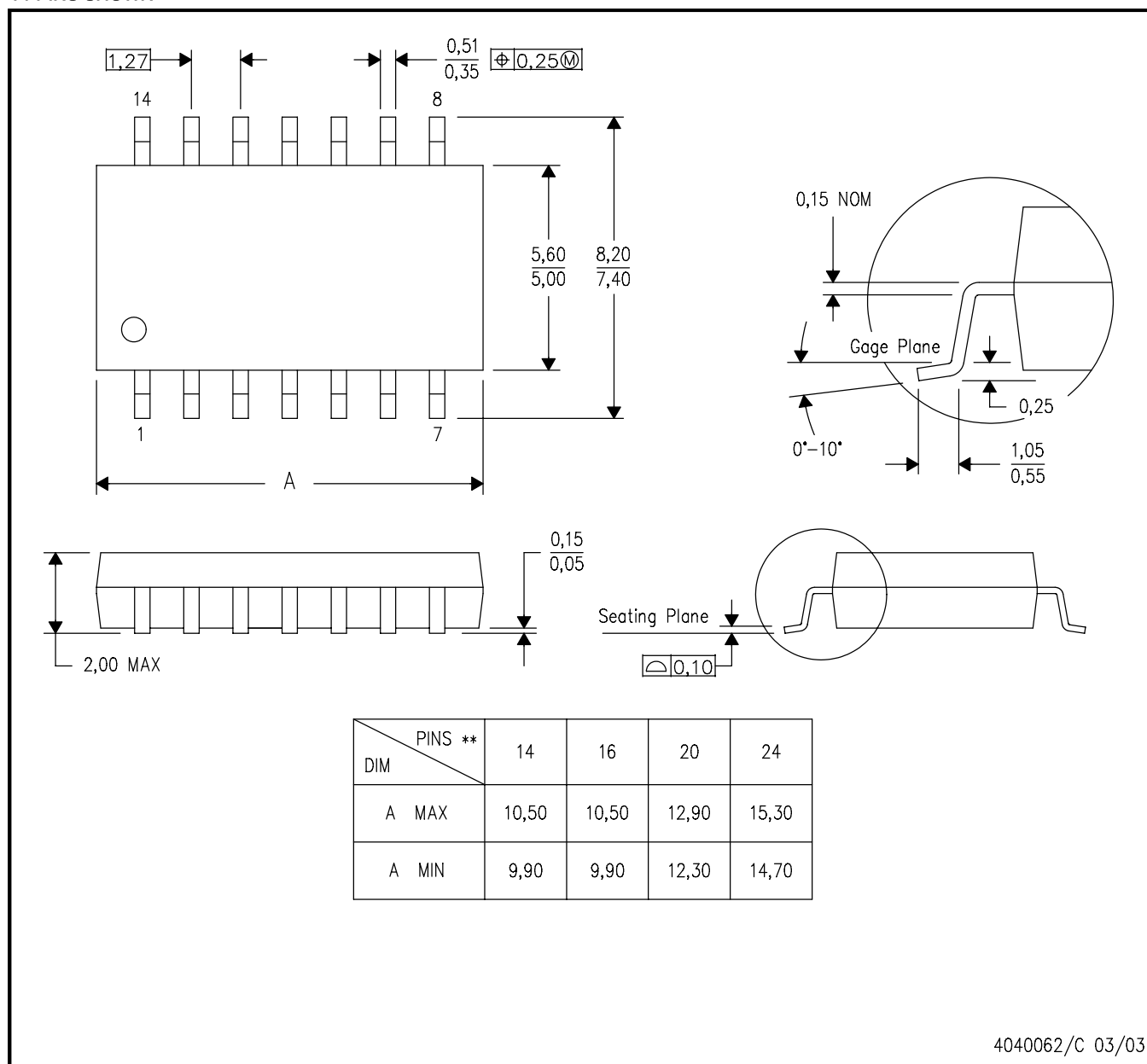
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

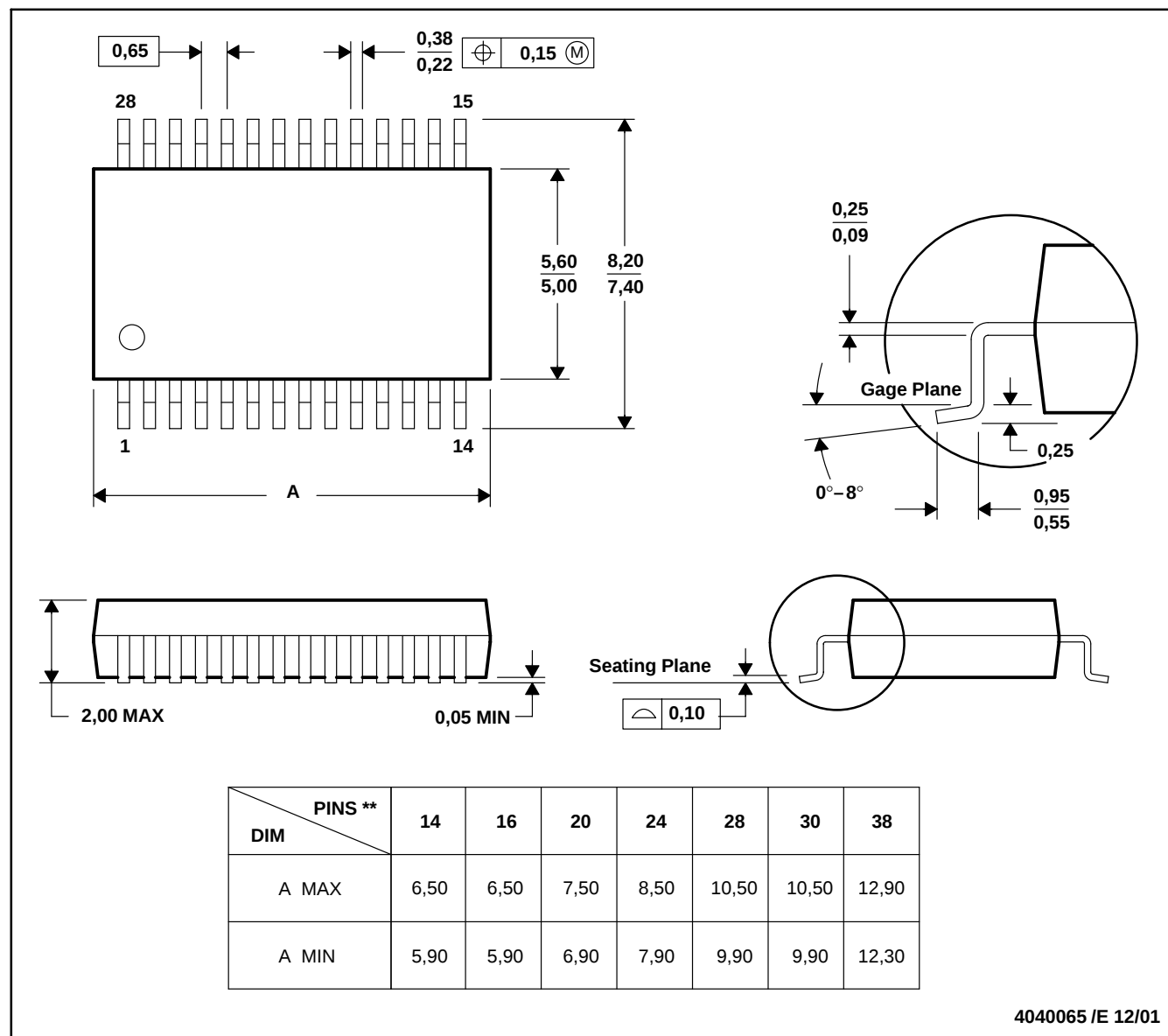


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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