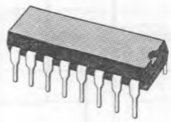
VOLTAGE REGULATOR FOR CMOS MICROPROCESSOR BASED SYSTEMS

- OUTPUT CURRENT : 100 mA
- ON-CHIP CURRENT LIMIT AND THERMAL PROTECTION
- RESET GENERATOR WITH EXTERNALLY ADJUSTABLE DELAY
- REGULATOR INPUT VOLTAGE LEVEL DETECTION SYSTEM (level adjusted externally)
- WATCH DOG TIMER
- INPUT VOLTAGE FAILURE DETECTION SYSTEM DELIVERS A STORE SIGNAL IN CASE OF INPUT VOLTAGE DISCONTINUITY
- REGULATOR ON/OFF CONTROL SIGNAL ALSO SETS THE OUTPUT TO HIGH IMPEDANCE STATE



TEA7105
BATWING DIP-16
(Plastic Package)

DESCRIPTION

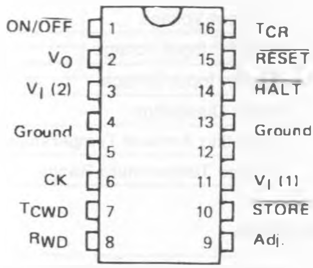
The TEA7105 is a voltage regulator especially suited to all microprocessor-based digital systems. Upon initial power on, the circuit delivers a RESET signal with programmable delay. This signal is disabled under three conditions :

- When supply voltage falls below a certain threshold level adjusted externally
- When output voltage falls below a preset level
- In the absence of trigger pulses on WATCH DOG input

The regulator features a WATCH DOG function with timing requirements met by a wide range of frequencies. The device detects the occurance of input voltage DROP and delivers a STORE signal whitebeing powered by the energy stored in the input capacitor.

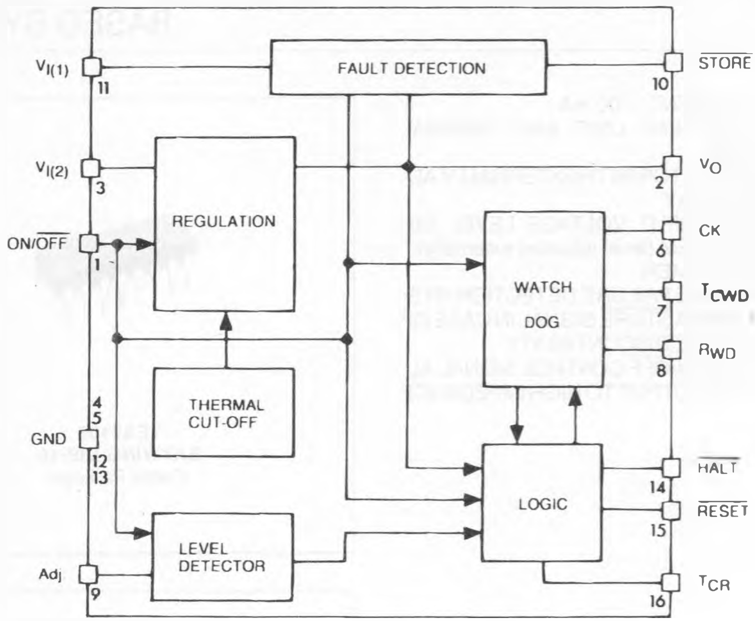
An ON/OFF function is provided enabling the circuit to be put in standby mode and also to set the regulated output to high impedance state. In this mode, the power consumption is extremely low.

PIN CONNECTIONS



E88TEA7105-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{I(1)}$, $V_{I(2)}$	Supply Voltage	+ 40	V
	CK Input Voltage	– 0.3 to V_O	V
	ON/$\overline{OFF}$ Input Voltage	– 0.3 to $V_{I(2)}$	V
	Adj. Pin Input Voltage	– 0.3 to $V_{I(2)}$	V
P_{tot}	Power Dissipation	Internally Limited	–
T_{oper}	Operating Ambient Temperature Range	– 40 to + 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

THERMAL DATA

$R_{th\ (j-a)}$	Maximum Junction-ambient Thermal Resistance	45	°C/W
$R_{th\ (j-c)}$	Maximum Junction-case Thermal Resistance	11	°C/W

$R_{th(j-a)}$ is measured on packages soldered on a printed circuit board with a copper area of 20 cm^2.

ELECTRICAL CHARACTERISTICS T_{amb} = + 25 °C, $V_{I(1)} = V_{I(2)}$ = + 12 V
(unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VOLTAGE REGULATOR					
V_O	Output Voltage (+ 7 V ≤ V_I ≤ + 36 V, 1 ≤ I_O ≤ 100 mA)	4.85	–	5.15	V
K_{VI}	Line Regulation (+ 7 V ≤ V_I ≤ + 36 V, I_O = 50 mA)	–	30	100	mV
K_{VO}	Load Regulation (V_I = + 10 V, 5 mA < I_O < 100 mA)	–	10	75	mV
I_{SC}	Short-circuit Current (V_I = + 10 V, 0 ≤ V_O ≤ + 5 V)	–	200	–	mA
$\overline{RESET}$ FUNCTION					
	Minimum Output Voltage to Activate $\overline{RESET}$	4.5	–	4.8	V
	Output Voltage Hysteresis to Disable $\overline{RESET}$	–	50	–	mV
$V_{(ref)}$	Internal Reference for the Adj. Detection	–	2.5	–	V
$I_{(adj)}$	Maximum Adj. Pin Current ($V_{(adj)}$ = 0 V)	–	–	1	µA
$V_{L(\overline{reset})}$	Low Level $\overline{RESET}$ Output (I_O = 2 mA)	–	–	0.4	V
$V_{H(\overline{reset})}$	High Level $\overline{RESET}$ Output (I_{OH} = – 100 µA)	V_O – 1	–	V_O	V
CK AND ON/$\overline{OFF}$ INPUTS					
V_{IL}	Maximum Low Level Input Voltage	–	–	0.8	V
I_{IL}	Maximum Low Level Input Current (V_{IL} = 0 V)	– 120	– 60	–	µA
V_{IH}	Minimum High Level Input Voltage	2.4	–	–	V
I_{IH}	Maximum High Level Input Current (V_{IH} = + 2.4 V)	–	–	100	µA
ALARM /$\overline{STORE}$ FUNCTION					
$V_{H(min)}$	Minimum Input Voltage to Activate $\overline{STORE}$ Signal	5	5.7	6.4	V
$V_{L(\overline{store})}$	Low Level $\overline{STORE}$ Output (I_O = 2 mA)	–	–	0.4	V
$V_{H(\overline{store})}$	High Level $\overline{STORE}$ Output (I_{OH} = – 100 µA)	V_O – 1	–	V_O	V
ON/$\overline{OFF}$ FUNCTION					
$I_{(sb)}$	Standby Current $V_{(ON/\overline{OFF})}$ = 2.4 V $V_{(ON/\overline{OFF})}$ = 0 V	 – –	 4 0.5	 8 –	mA
$I_{O(dis)}$	V_O Pin Discharge Current ($V_{ON/\overline{OFF}}$ = 0, V_O = + 5 V)	–	–	2	µA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
TIMING (see timing diagrams)					
	CWD	–	–	33	nF
	C_R	–	–	220	nF
t_{init}	t_{init} (C_R = 100 nF) Note 1	–	30	–	ms
t_d	t_d (CWD = 33 nF) Note 2	–	7	–	ms
t_{reset}	t_{reset} (CWD = 33 nF, C_R = 100 nF) Note 3	–	6	–	ms
t_{cycle}	t_{cycle} (CWD = 33 nF, C_R = 100 nF) Note 4	–	13	–	ms
T_{CK}	Pulse Width at Input CK	20	–	t_d	µs

Notes : 1. This is the period at the end of which RESET signal appears after V_{OUT} rises up and when switch S1 has been closed, this is given by the following relationship.

$$t_{init} = 0.3 \cdot CR \cdot 10^6$$

2. This is the maximal clock period determined by the value of CWD.

$$t_d = \frac{2.7}{11.6} \cdot CWD \cdot 10^6.$$

3. This is the time required for micorcomputer reinitialisation.

$$t_{reset} = \frac{1}{11.6} \cdot CWD \cdot 10^6 + \frac{5}{125} \cdot CR \cdot 10^6$$

4. This is the time required by the microcomputer during a restart to generate at least one clock pulse.

$$t_{cycle} = t_d + t_{reset}.$$

Remark : For more important clock period see specifiic application figure 10.

PIN DESCRIPTION

$V_{I(1)}$

Input connected directly to power supply to detect any supply failure.

$V_{I(2)}$

Regulator's power input. This input is separated from power supply through a diode.

A decoupling capacitor is connected to this input.

An inadequate supply voltage level is detected at this input.

Adj

In order to detect the level of $V_{I(2)}$ a resistance inserted between Adj pin and $V_{I(2)}$ and another between Adj pin and GND are necessary.

ON/$\overline{OFF}$

Logic input. A logic 1 applied to this input will cause the TEA7105 to become fully operational ; whereas a logic O will set the circuit to standby mode.

V_O

Power cutput to microprocessor and digital systems.

Two different output voltage levels are detected according to whether the transition is from low voltage to high voltage or the inverse (Refer to timing diagram - figure 4).

High impedance output when the circuit is in standby mode.

T_{CR}

Combination of a grounded capacitor and the internal current generator will implement the $\overline{RESET}$ signal delay upon the initial power on.

T_{CWD}

A relaxation oscillator is implemented by combining a grounded capacitor and the internal current generator

R_{WD}

A resistance inserted between this pin and ground will cause the flow of additional charging current to capacitor C_{WD} thereby modifying the slope of the local oscillator and improving the choice of C_{WD} values.

C_K

This is the WATCH DOG function input. The clock signal resets the ramp of the relaxation oscillator. The circuit is triggerred on rising edge of the clock.

$\overline{\text{RESET}}$

During the initialization, TEA7105 detects at the output V_O a voltage level V_{C1} and generates a $\overline{\text{RESET}}$ signal (see timing diagrams - figure 5).

The following three conditions cause $\overline{\text{RESET}}$ signal to be forced to zero level :

- If the output voltage level falls below V_{C1} by a hysteresis of ΔV_{C1} (see timing diagrams - figure 5).
- If no signal arrives at input CK for a minimal period to 20 µs and maximal period equal to td (see timing diagrams - figure 6).
- If the input voltage falls below the adjustable threshold level (see timing diagrams - figure 4).

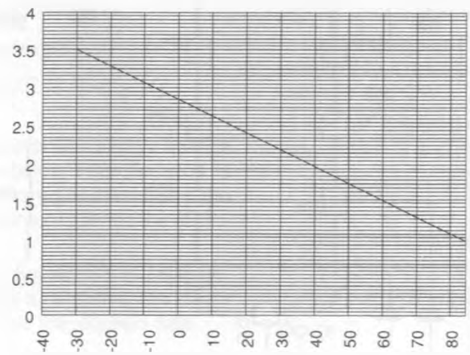
$\overline{\text{HALT}}$

Fonction and electrical characteristics are the same as the $\overline{\text{RESET}}$ pin.

$\overline{\text{STORE}}$

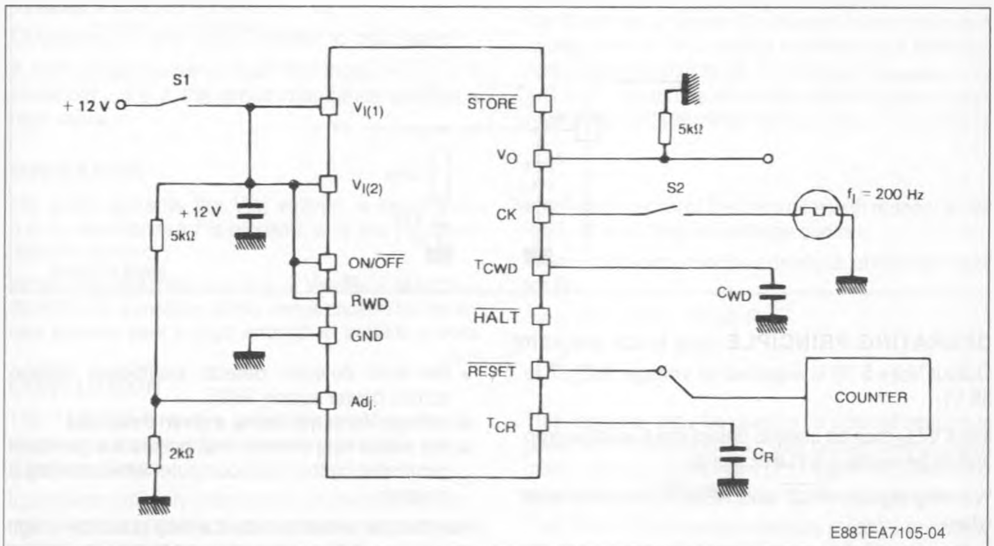
If input voltage $V_{I(1)}$ falls below V_{C2} level, TEA7105 will use the energy stored in the input capacitor to generate the $\overline{\text{STORE}}$ signal for the microprocessor data protection (see timing diagrams - figure 4).

Figure 1 : Maximum Power Dissipation Versus Junction-ambient Temperature.



E88TEA7105-03

Figure 2 : Test Circuit.

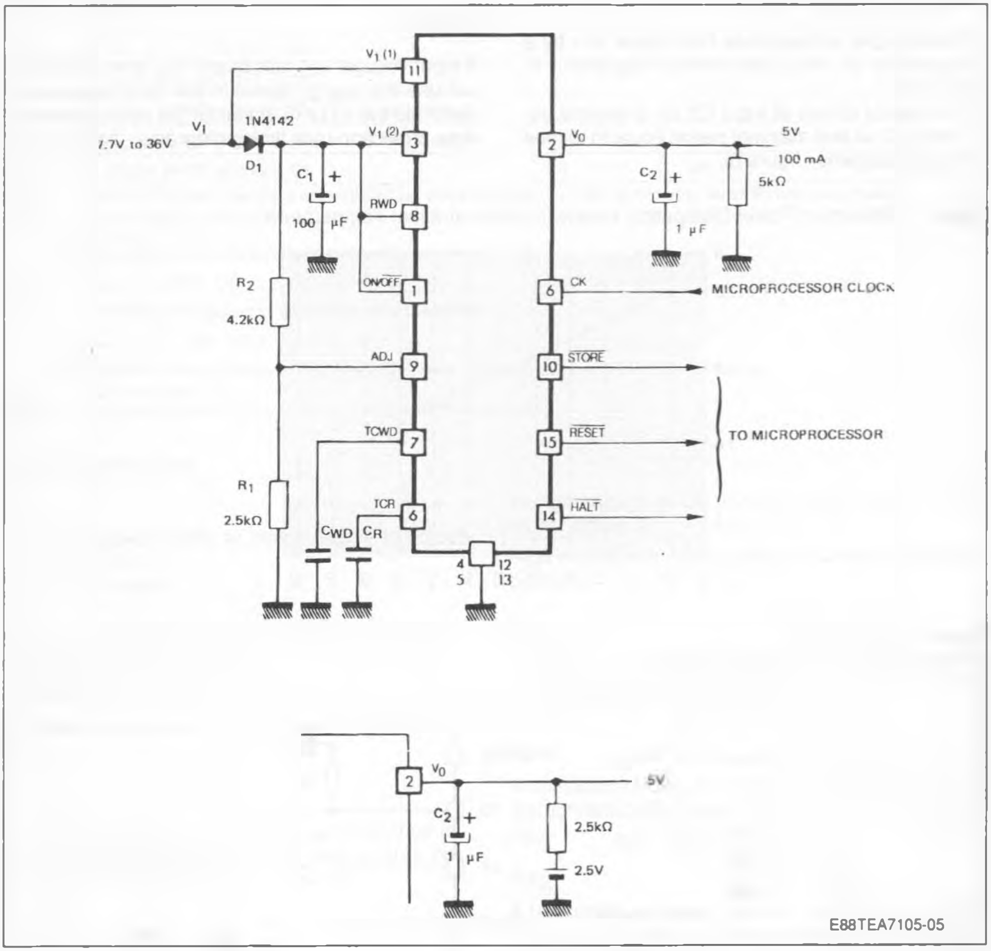


E88TEA7105-04

TYPICAL APPLICATION

A minimum current of 1 mA should be delivered by the TEA7105 for effective voltage control. This is why a 5 KΩ resistor (or an equivalent load if a backup battery is used) shall be connected between V_O and the ground.

Figure 3 : Typical Application.



OPERATING PRINCIPLE (see block diagram)

Output V_O(+ 5 V) is supplied by voltage $V_I(2)$ (7 to 36 V).

Input $V_I(1)$ may be used to detect input voltage drop and to generate a STORE signal.

Warning signals $\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ are generated when :

- the circuit is being powered, for a time t_{init},
- the level detector detects insufficient voltage across power supply $V_I(2)$,
- voltage V_O drops below a given threshold,
- the watch dog detects that pulses are no more generated by the microcomputer when running a program.

The thermal protection device may produce a high impedance at the voltage regulator output.

The impedance of the complete circuit becomes high when $V_I(2)$ drops below a fixed threshold, 4.5 V < V threshold < 4.8 V or by acting on the ON/OFF input.

External capacitors allow inputs t_{CWD} and t_{CR} to define the t_{init}, t_{reset}, t_{cycle}, td times (figures 5 and 7) which are characteristic of the HALT and RESET signals.

It's possible to inhibit the watch dog function by grounding the pin 7 (CWD).

If store function is not used the diode D1 is not accessary.

WHEN POWERING (figures 4,5,6)

Outputs $\overline{HALT}$ and $\overline{RESET}$ are (at logic level O) during a time t_{init} following voltage V_O build up, which is used for microcomputer initialization.

t_{init} (ms) = 0.3 CR (nF).

WHEN NO INPUT VOLTAGE IS PRESENT (figure 4)

The TEA7105 regulates the power supply voltage $V_I(1)$. As soon as it drops below $V_I(2)$ diode D1 is blocked. The energy is delivered by capacitor C1 to supply the internal logics of the circuit and the microcomputer.

If $V_I(1)$ drops below a fixed threshold, 5 V < V threshold < 6.4 V, a $\overline{STORE}$ signal is generated to indicate to the supplied system to save the required data.

If $V_I(2)$ drops below an externally programmed threshold (7 V < V threshold < 36 V).

$V_{threshold} = (2.5\ (R1 + R2)/R1) + V_d$.

Outputs $\overline{HALT}$ and $\overline{RESET}$ switch to logic state 0.

If $V_I(2)$ drops below a fixed threshold, 4.5 V < V threshold < 4.8 V, the circuit impedance reaches a high value.

WHEN THE OUTPUT VOLTAGE DROPS (figure 4)

When voltage V_O drops below a fixed threshold, 4.5 V < V $_{threshold}$ < 4.8 V outputs $\overline{HALT}$ and $\overline{RESET}$ switch to logic state 0.

WHEN NO CLOCK SIGNAL IS PRESENT (figure 6)

The microcomputer when in operation will generate a clock signal whose period t will be between t min = 20 µs and t max = td

When this signal is not generated, or if the clock period is larger than td, this means that the microcomputer does not operate correctly.

The TEA7105 thus generates the $\overline{HALT}$ and $\overline{RESET}$ signals after a time td from the last rising edge.

In this case signals HALT and RESET are activated periodically, t reset and t cycle being fixed by capacitors Cr and CWD.

td may be adjusted by a resistor RWD connected between pin 8 and the ground (figure 9).

In normal condition the maximal clock period is to 7 ms.

It's possible to increase this value in adding some external components (figure 10).

INCREASE OF THE OUTPUT CURRENT (figure 7)

The TEA7105 can deliver a 100 mA current which can be increased by using an external transistor, which maintains the circuit characteristics. The setup illustrated in figure 10 an used in our laboratory circuit gives a 7 mV output variation for a load current varying from 0 to 1A. In this case $V_{threshold} \approx V_S + 3\ V_D + R_S.I_S$. The maximum value of power supply voltage is determined by $V_{min} \approx V_S + 3\ V_D + R_S.I_S$.

OPERATION

For small currents the V_{BE} voltage is lower than 0.6 V ; the transistor is blocked, only the regulator delivers current.

When V_{BE} reaches 0.6 V ($I = V_{BE}/R_b = 0.6/33 = 20$ mA) the transistor starts conduction. The transistor current gain is high enough to provide a very small current drift of the controller with respect to the load, which improves voltage control.

When short-circuited the current is limited by resistor R_S.

$I_{SC} = (V_I - 2.V_d - Vsat)\ R_S$

CONCLUSION

The TEA7105 is a new generation voltage regulator giving a simple answer to microcomputer power supply problems.

It prevents untimely interruption of microcomputers and makes it possible to return to current program without any trouble.

This regulator may be used in its original version to power a microcomputer or any system with a maximum current requirement of 100 mA. A current extension is available for more powerful systems.

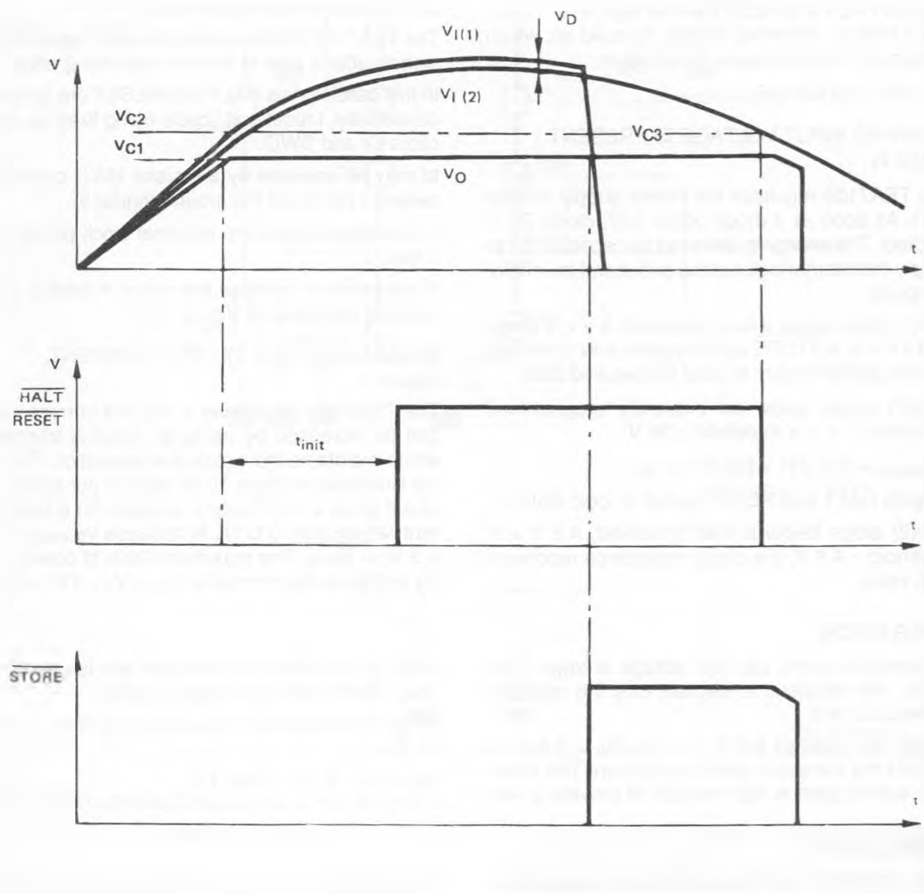
The TEA7105 provides a simple, reliable, economical and high performance power supply.

When V_I (1) becomes lower than a fixed threshold 5V < VC3 < 6.4 the $\overline{\text{STORE}}$ output switches to logic state 1. This threshold may be modified by using an external potential divider.

When V_I (2) becomes lower than an externally adjustable threshold signals $\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ switch to logic state O ($V_C2 = 2.5$ (R1 + R2) / R1).

When V_I (2) becomes lower than a fixed threshold 4.5 V < V threshold < 5.5 V the circuit impedance becomes high.

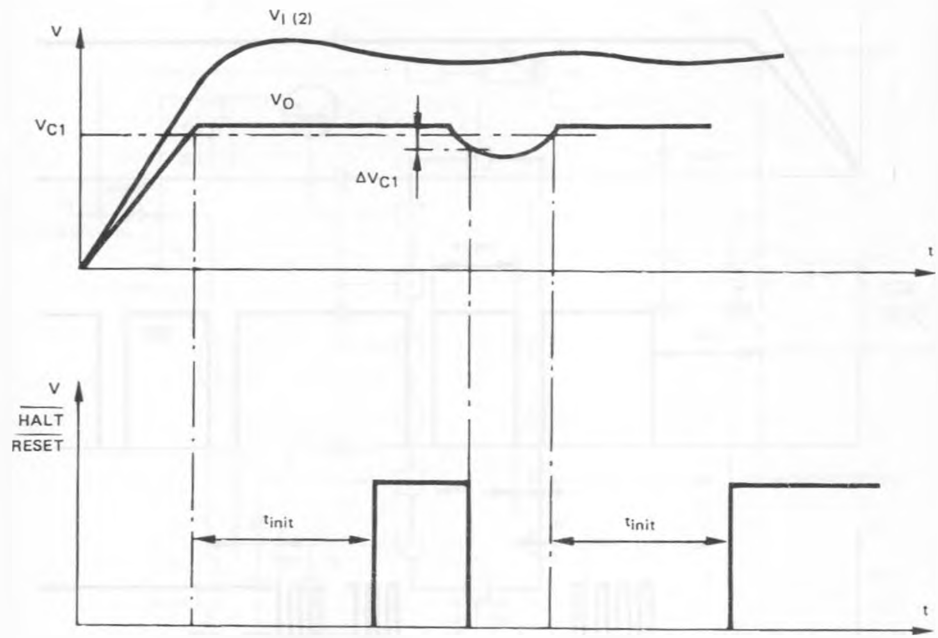
Figure 4 : Detection of Input Voltage Drop.



When the output voltage becomes lower than V threshold (4.5 < threshold < 4.8 V) the warning signals HALT and RESET switch to logic state O.

These signals become active as soon as V_O reaches the threshold to reinitialize and block the microcomputer during t_{init}.

Figure 5 : Detection of Output Voltage Drop.

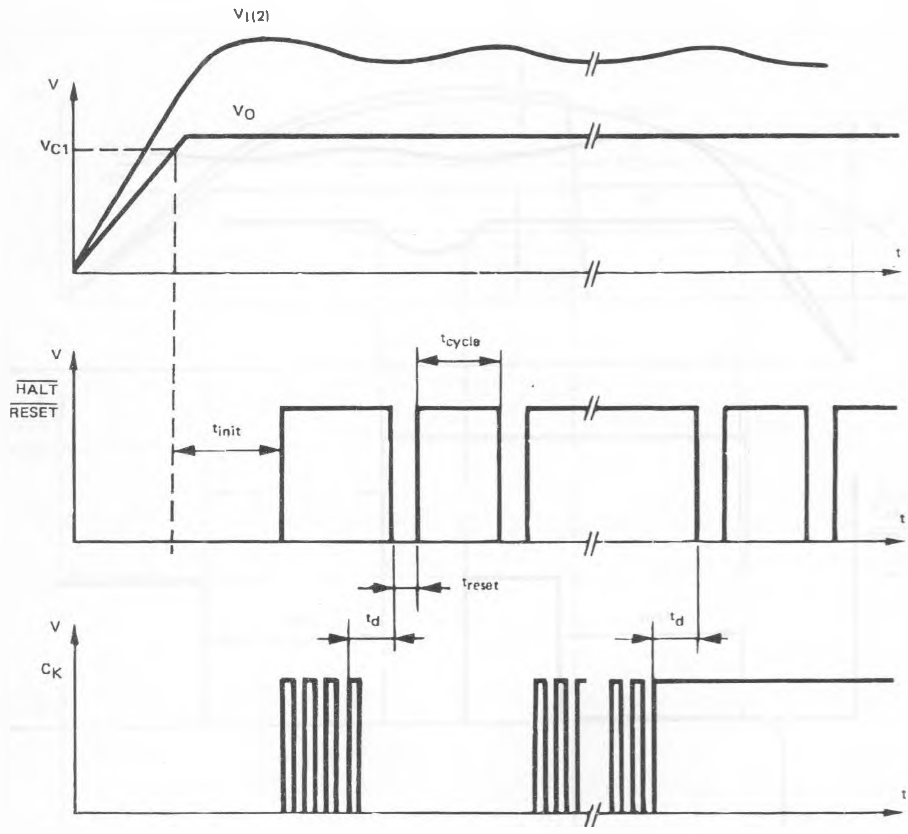


E88TEA7105-07

Signals $\overline{HALT}$ and $\overline{RESET}$ become active after a time t_d from the last clock signal rising edge.

t_d and t_{reset} depend on capacitors C_{WD} and C_R, pre-set curves are given in figure 8.

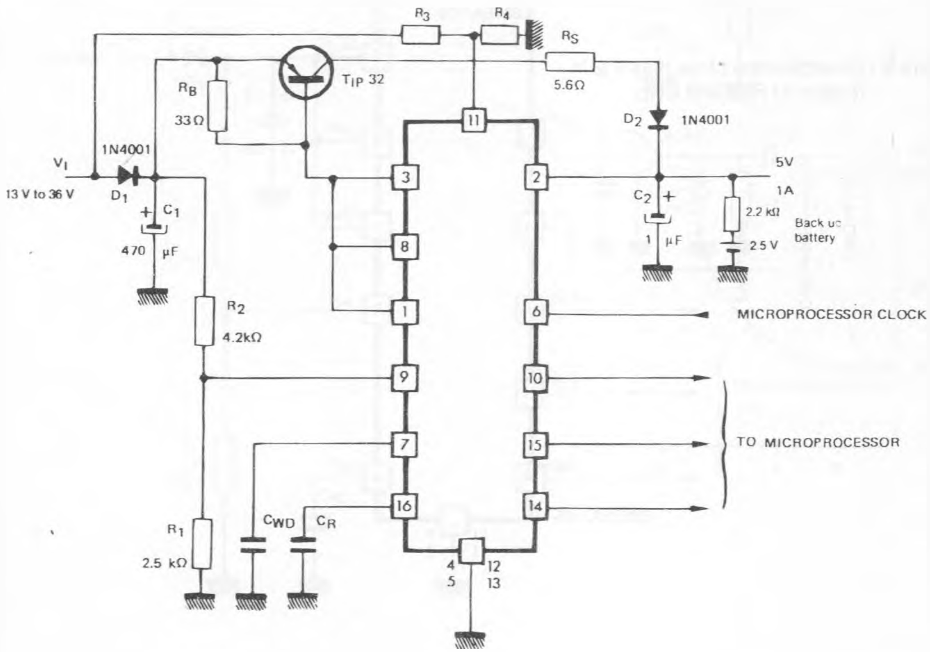
Figure 6 : Interruption of Clock Pulses.



This application is used to deliver a 1 A current with excellent voltage control. The D2 diode avoids the discharge of the back up battery in the TEA7105 when it' s in hight impedance output in stand by mode.

The value of $V_{I(1)}$ activing $\overline{STORE}$ signal is determined by ($V_{I(1)}$ store = (5.7 (R3 + R4)/ R4).

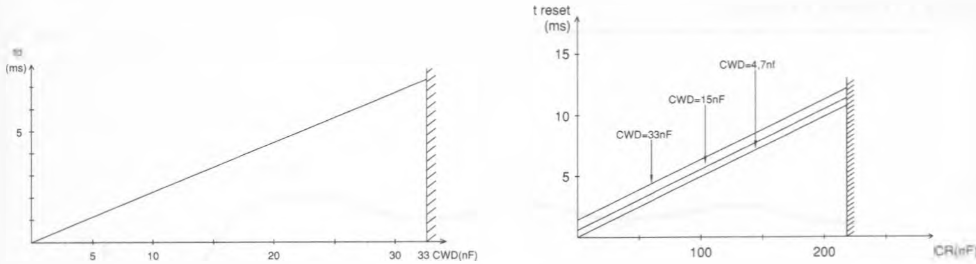
Figure 7 : Current Extension.



E88TEA7105-09

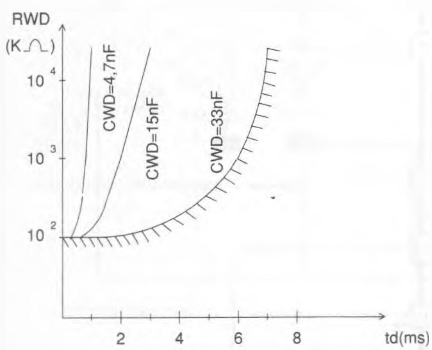
We see that C_r and C_{WD} actions are not fully independent. It is possible to adjust td more finely by using an external resistor connected between pin R_{WD} and the ground (figure 9).

Figure 8 : Determination of t_d and t_{reset} in relation to C_{WD} and C_R.



E88TEA7105-10

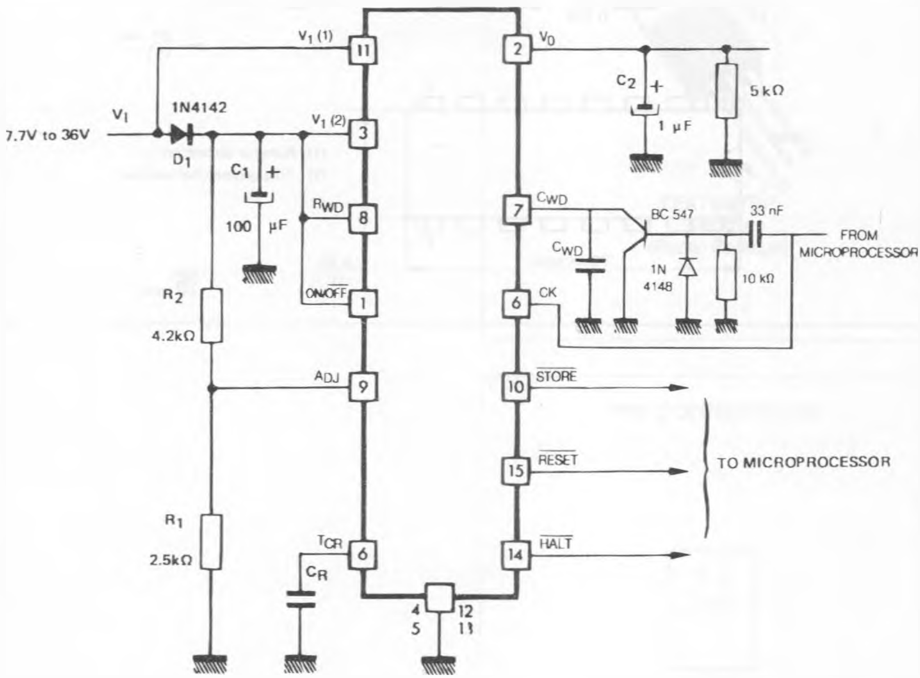
Figure 9 : Determination of t_{CK} max = t_d in relation to R_{WD} and C_{WD}.



E88TEA7105-11

For applications using very long clock period it's possible to use an external transistor. In this case the maximal clock period, in relation to C_{WD}, may be longer than 500 ms. The relationship to define t_{init}, t_d, t_{reset} are same that in typical application.

Figure 10 : Very Long Clock Period.



E88TEA7105-12

PACKAGE MECHANICAL DATA

16 PINS – PLASTIC DIP