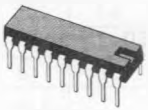
SPEECH CIRCUIT WITH POWER MANAGEMENT

- 2/4 WIRES INTERFACE WITH
  - double antisidetone network
  - Rx gain and AC impedance externally programmable
  - AGC attack/disconnect points programmable
- DTMF INTERFACE
- 3.3 VOLTS SUPPLY FOR MICROPROCESSOR OR DIALER
- CURRENT SUPPLY FOR LOUDSPEAKER



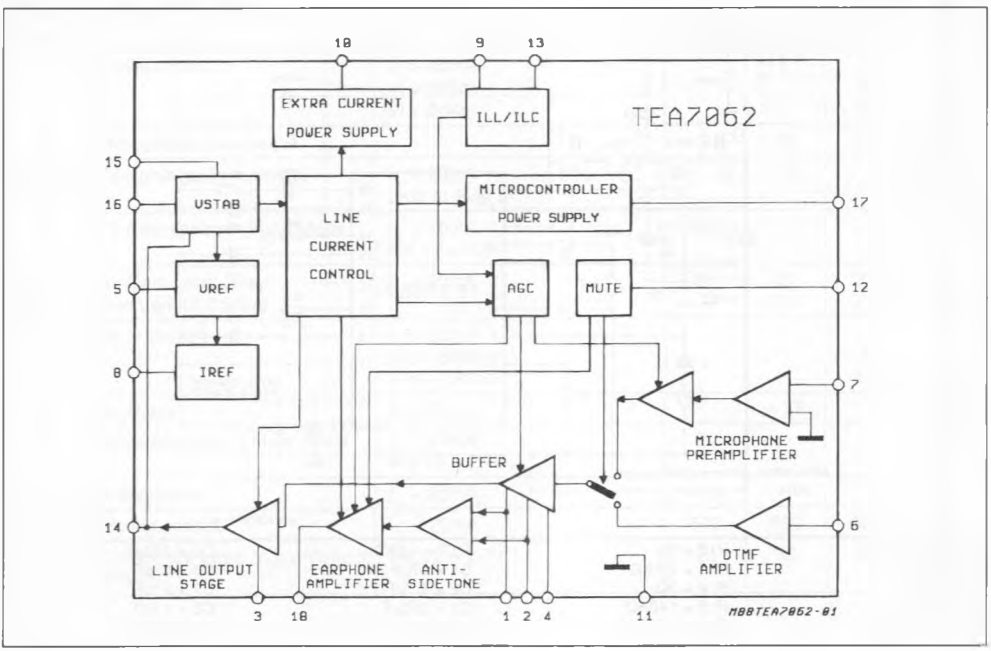
DIP18

ORDER CODE : TEA7062DP

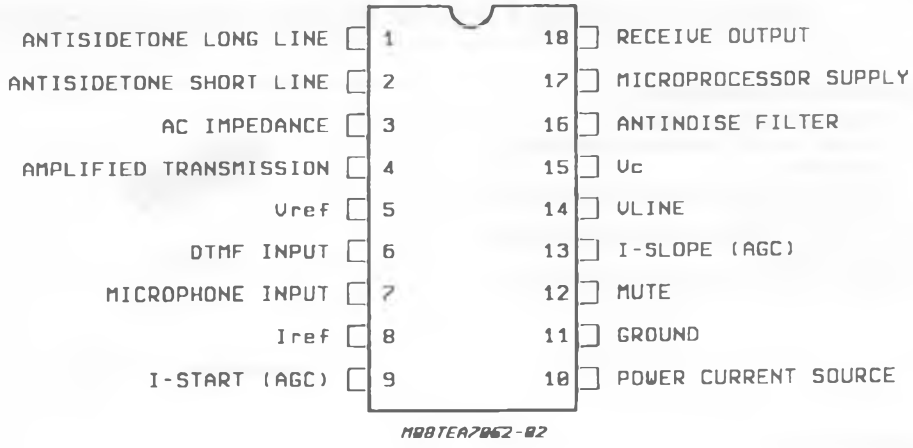
DESCRIPTION

The TEA7062 is designed to meet the different european specifications for telephone set in medium and high range equipments.

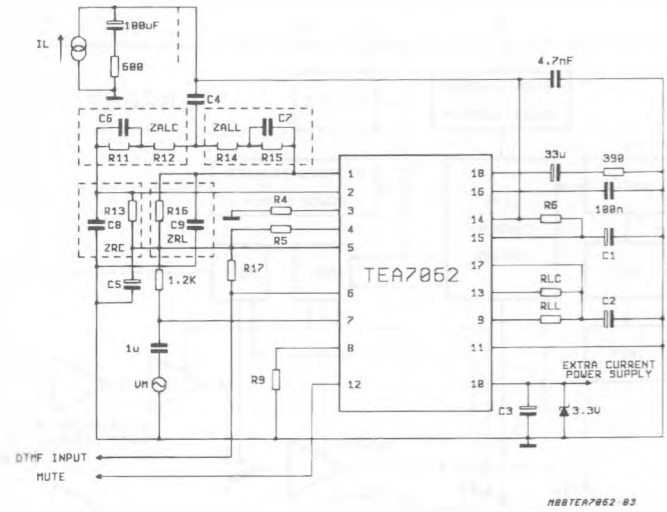
BLOCK DIAGRAM



PIN CONNECTIONS (top view)



TEST CIRCUIT



R4 = 75Ω	R12 = 0Ω	R17 = 1.2KΩ	C5 = 100µF
R5 = 5.1KΩ	R13 = 2.7KΩ	C1 = 47µF	C6 = 27pF
R6 = 18KΩ	R14 = 0Ω	C2 = 4.7µF	C7 = 27pF
R9 = 100KΩ	R15 = 140KΩ	C3 = 220µF	C8 = 1.5nF
R11 = 140 KΩ	R16 = 2.7KΩ	C4 = 1µF	C9 = 1.5nF

ELECTRICAL CHARACTERISTICS

(R_9 = 100KΩ ; T_a = 25°C ; identification of the pins related to DIP-18 unless otherwise noted)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
VC	Stabilized Voltage (pin 15)	I_L = 25mA	2.3	2.5	2.7	V
Iint	Internal Bias Current (pin 15)	I_L = 25mA I_L = 6mA (V14 = R6*Iint + VC)		210 145		µA
Vref	Reference Voltage	I_L = 25mA	1.05	1.2	1.35	V
Iref	Current at Vref		– 10		100	µA
Vmp	Stabilized Supply at Pin 17		3.1	3.3	3.5	V
Icmp mA	Charging Current at Pin 17	Pin 15 = GND	0.6 X I_{line}			mA
Ispm	Static Current at Pin 17	I_L = 6mA I_L > 25 mA	0.5 1.4	1.6		mA
		I_L > 25mA ; R9 = 68K		2.8		mA
Iimp	Internal Consumption		90	120	160	µA
Iea	Supply Current for Parallel Circuits (pin 10)	I_L = 16mA I_L = 30mA I_L = 60mA		5.0 13.0 40.0		mA mA mA
Vmh Vmb	Mute Microphone (pin 12)	ON OFF	1.6		 0.8	V V
Vmh Vmb	Mute Earphone (pin 12)	ON OFF	2.7		 2.1	V V
Gs AGCs	Tx Gain Long Line Line Lenght Control	I_L = 20mA	50 – 7	51 – 6	52 – 5	dB dB
Gmf	DTMF Gain	Pin 12 > 1.6V	34.5	35.5	36.5	dB
THDs	Tx Distortion	I_L > 25mA Vl = 0dBm Vl = 3dBm			 3 10	 % %
Ze	Microphone Impedance		9	12	15	KΩ
Nep	Tx Noise (psophometric)	I_L > 25mA 2KΩ at Pins 5-7		– 70		dBmp
Rs	Tx Attenuation in Mute Mode	I_L > 25mA Pin 12 > 1.6V	60			dB
Gr AGCr	Rx Gain Long Line Line Lenght Control	I_L = 20mA	29 – 7	30 – 6	31 – 5	dB dB
THDr	Rx Distortion	I_L > 25mA Vro = 500mV Vro = 630mV			 3 10	 % %
Nrp	Rx Noise	I_L > 25mA		– 72		dBmp
Rr	Rx Attenuation in Mute Mode	I_L = 25mA Pin 12 > 2.7V	60			dB
Gas	Antisidetone	I_L = 20mA	– 22			dB
Zac	AC Impedance	I_L > 25mA	500	650	800	Ω
Grs	Confidence Level V_{LINE}/V_{REC} in DTMF	Pin 12 > 2.7V	29	32	35	dB

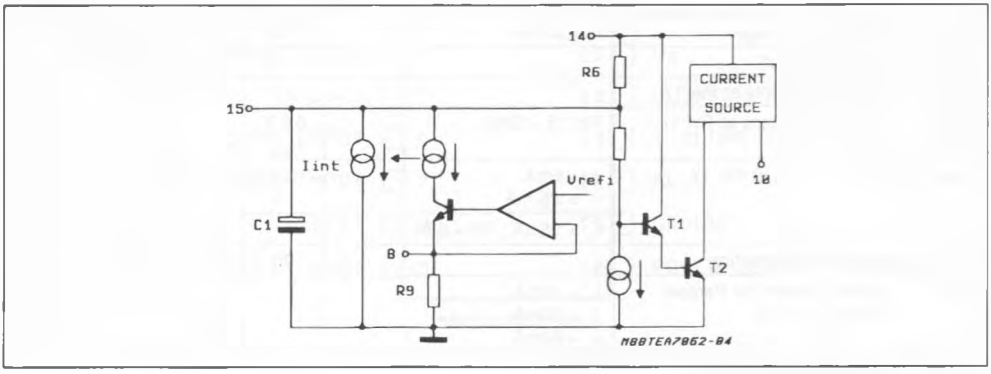
CIRCUIT DESCRIPTION

1. DC Characteristics

1.1 Vc (pin 15). The stabilized voltage Vc is connected to Vline (pin 14) througth an internal shunt regulator T1, T2, which presents to the line a high AC impedance at frequencies higher than 200Hz. At this purpose the value of C1 (at pin 15) must be not lower than 47 microFarad (suggested value is 100μF).

The shunt regulator, T1 and T2, also controls the extra current source, or power management, at pin 10 (see also paragraph 6).

Figure 1.



1.2 V_{LINE} (pin 14). The line voltage (pin 14) is determined by the value of the external resistor R6 and by the internal current, I_{int}, flowing between Vc (pin 15) and Ground (see also paragr. 1.1) :

$V_{LINE} = Vc + R6 \times I_{Int}$.

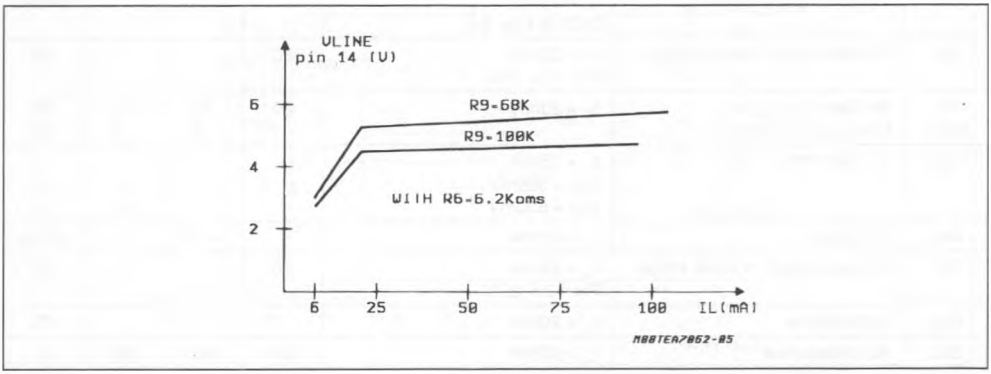
Vc is fixed by design at about 2.5V.

I_{int} is reversely related to R9 (I_{int} = 16V/R9 + 60μA at I_{LINE} > 25mA).

V_{LINE} must be externally adjusted (with R6) to guarantee both DC and AC characteristic in accordance to the specific standard of the different administrations.

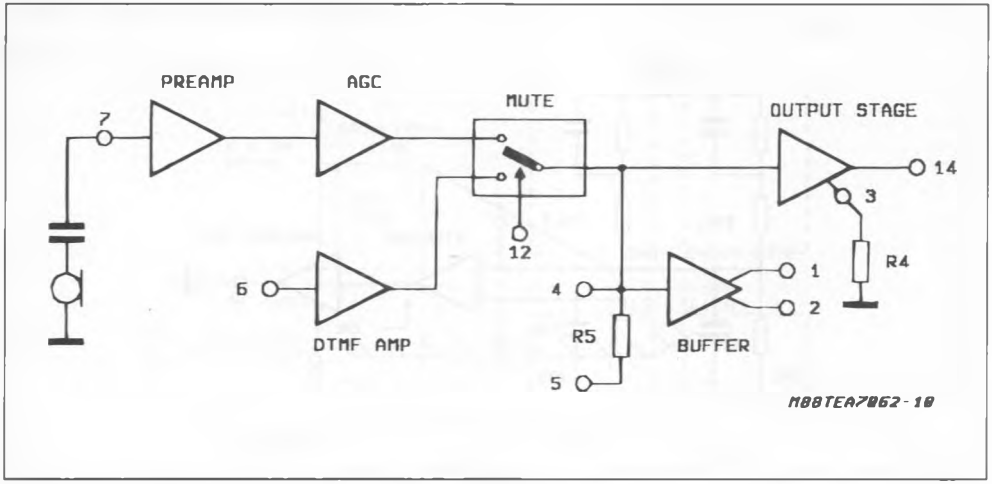
Another adjustment of the DC characteristic is possible with R9. Increasing the value of R9 causes a decrease of I_{int} and consequently a reduction of the product I_{int} x R9.

Figure 2.



2. Transmission Chain

Figure 3.



2.1 A.G.C. IN TRANSMISSION. The transmission gain between Microphone Input (pin 7) and Vline (pin 14) is internally decreased of 6dB when the line current varies from ILL to ILS with a constant AC load of 600Ω.

The values of ILL (long line current) and ILS (short line current) are programmable through I-start (pin 9) and I-slope (pin 13) (see also paragr. 4).

2.2 SENDING IMPEDANCE. The impedance of the Output Stage Amplifier, Zout, is determined by the impedance Z4 (at pin 3).

$$Zout = 10.65 \times Z4.$$

The total AC impedance shown to the line is the parallel

$$Zpar = Zout//Zint//Zext$$

where :

- Zint = 10kΩ//8.5nF (internal)
- Zext = R6//C4 (at pin 14)

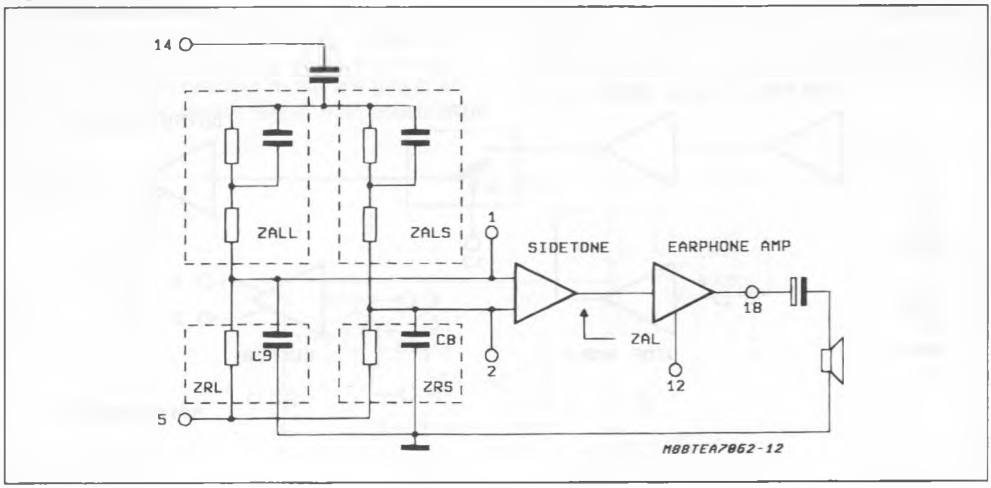
2.3 SENDING MUTE. In normal speech operation (Vmute at pin 12 < 0.8V), the signal at Microphone Input (pin 7) is amplified to Vline (pin 14) with the gain Gs (long line) or up to 6dB lower (shorter lines) depending on AGC control (see paragr. 4).

In sending mute condition (V12 > 1.6V) these gains are reduced of at least 60dB. In the same condition, DTMF input (pin 6) is activated, with gain Gmf to the line independent from Iline.

2.4 ANTISIDETONE BUFFER. The signal coming from the sending preamplifier is internally presented at pin 4 and than buffered to pins 1 and 2 for sidetone cancellation (see paragraph 3.2).

3.Receive Chain

Figure 4.



3.1 A.G.C. IN RECEIVE. As described for the transmission chain, also the receiving gains Gr, from pins 1 and 2 to pin 24, have a reduction of 6dB when Iline moves from ILL to ILS (see also paragr. 4).

3.2 SIDETONE COMPENSATION. The circuit is provided with a double anti-sidetone network to optimize both at long and short lines.

In case double antisidetone network is not requested by the application needs, pins 1 and 2 can be connected to each other and 5 external passive components can be saved (ZALL and ZRL).

Before entering pins 1 and 2, the received signal is areduced by the two attenuating networks :

-ZALL/ZRL to pin 1 for long lines sidetone compensation,

-ZALS/ZALS to pin 2 for short lines sidetone compensation.

ZRL and ZRC define the total receive gains :

a) $\frac{V18}{V14} = Gr \times \frac{ZRL}{ZRL+ZALL}$ for long lines

b) $\frac{V18}{V14} = (Gr - 6dB) \times \frac{ZRS}{ZRS+ZALS}$ for short lines

ZALL and ZALS define the sidetone compenstaion of the circuit.

The equivalent balancing impedance is given by the formula :

ZAL = K x ZALS + (1 - K) x ZALL

where :
-K = 0 at Iline = ILL or lower (long line)
-K varies from 0 to 1 with Iline between ILL and ILS
-K = 1 at Iline = ILS or higher (short line).

Calculations to define ZALL and ZALS are :

a)
$$ZALL = 70 \times R5 \times \frac{Zline\ (long)//Zext//Zint//Zout}{Zout}$$

b)
$$ZALS = 70 \times R5 \times \frac{Zline\ (short)//Zext//Zint//Zout}{Zout}$$

where :

- Zext = R6//C4//(Zelectret) (at pin 11)
- Zint = 10Kohms//8.5nF (internal impedance)
- Zout = 10.65 * Z4 (at pin 3 ; see paragr. 2.2)
- Zline (short) and (long) are the impedances of the line at minimum and maximum line length
- R5 = 5.1Kohm ± 1%

3.3 AC IMPEDANCE. The total AC impedance of the circuit to the line is :

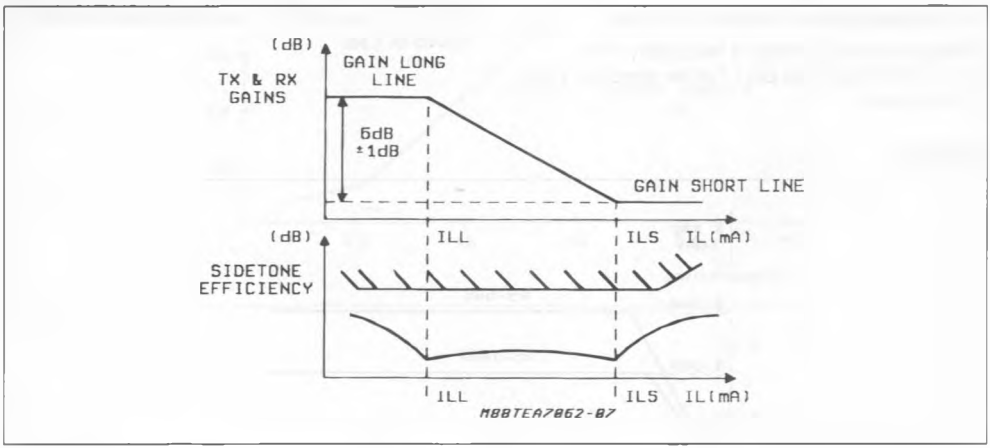
ZAC = Zout//Zint//Zext//ZALS//ZALL (see par. 2.2 and 3.2)
ZAC = Zout//Zint//Zext (ZALS, ZALL>>ZAC)

3.4 RECEIVE MUTE (and confidence level). When the receive channel is muted (Vpin 12 > 2.7V) the receive gain is reduced of 60dB minimum.

In this condition an internal connection is activated from line DTMF output (pin 16) to Receive Output (pin 18) with a gain Gmf = 32dBto provide acoustic feedback of the DTMF transmission.

4. A.G.C. and Sidetone Programming

Figure 5.



4.1 PROGRAMMABLE CONTROLS. AGC and sidetone attack and disonnect points (or currents) are programmable externally through two indepentents pins, I-start (pin 19) and I-slope (pin 13).

4.2 I-START (pin 9). An external resistor RLL connected between I-start (pin 9) and Microprocessor Supply (pin 17) controls the attack point of AGC and ZAL (antisedetone Z).

ILL is the line current at which the control starts. Formulas for ILL and RLL with R9 = 100K are :

$$ILL \frac{2880}{RLL} + 11mA$$

$$RLL \frac{2880}{(ILL - 11mA)}$$

4.3 I-SLOPE (pin 13)

An external resistor RLS connected between I-slope (pin 13) and Microprocessor Supply (pin 17) controls the disconnect point of AGC and ZAL (antisidetone Z). ILS is the line current at which the control stops. Formulas for ILS and RLS with R9 = 100K are :

$$ILS = \frac{4680}{RLS} + ILL;$$

$$RLS = \frac{4680}{(ILS - ILL)}$$

4.4 A.G.C. OFF (pin 9 and 13). Programming ILL and ILS respectively higher than 70mA and 450mA is forcing the IC in AGC OFF Condition.

Suggested external components are : RLL = 51kohm and RLS = 10Kohm.

Sending, receiving gain and sidetone compensation are so independent of the line lenght. Pins 1 and 2 can be connected to each other saving 5 passive external components at pin 2.

4.5 SECRET FUNCTION FOR PRIVATE (pin 12). The two separate thresholds for sending and Receiving Mute (pin 12) allow "Secret Function" (only microphone muted).

Pin 12 can be set :

a) between 0V and 0.8V for speech mode,

b) between 1.6V and 2.1V for "secret" mode (micro phone muted),

c) between 2.7V and 3.3V for "all muted" mode

5. Microprocessor Interface

5.1 MICROPROCESSOR SUPPLY (pin 17). At "off-hook" the first priority of the circuit is to make some current available at the Microprocessor Supply (pin 17) to charge quicly the external capacitor C2.

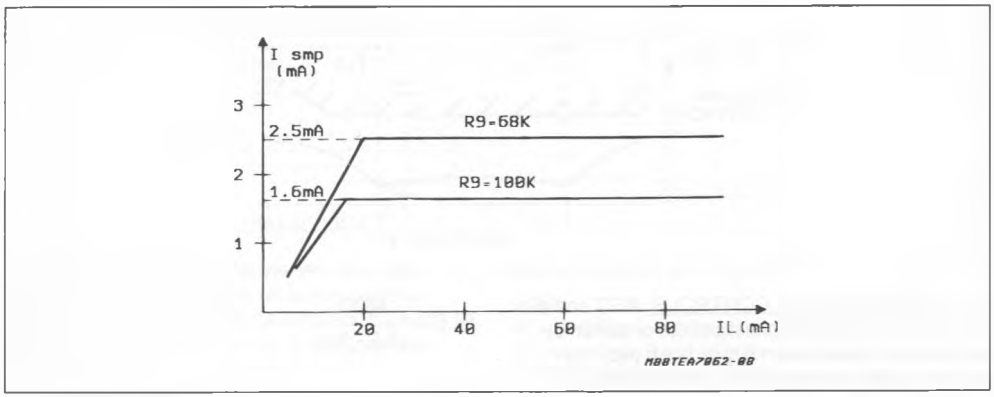
This charging current is Icpm = 0.6 x I_{LINE}.

T-charge of about 1 msec is necessary, with C2 = 4.7/µF, to charge pin 17 at the specified value of 3.3V typical :

$$T\text{-charge} = \frac{3.3V \times C2}{0.6 \times I_{LINE}} \text{ typically.}$$

Vmp = 3.3V in normal operation and current increases linearly from 0.5 mA min, at I_{LINE} = 6mA, to 2.5mA, at I_{LINE} = 25mA, remaining stable for higher values of I_{LINE}.

Figure 6.



6. Power Management

6.1 POWER MANAGEMENT(pin 10). Most of the DC current available from the line be delivered by the speech circuit at the output Isource (pin 10) through an internal current generator.

Typical values of this current, Iea with R9 = 100K, are :

Iea = (0.3 xI_{LINE}) for I_{LINE} < 16.5mA

Iea = (0.9 x I_{LINE} - 10mA) for I_{LINE} >16.5mA

(ex : I_{LINE} = 16mA then I_{ea} = 5mA

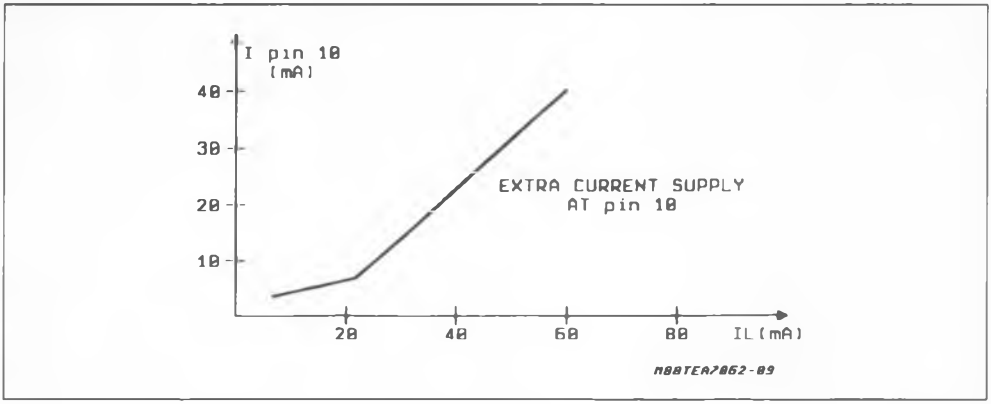
I_{LINE} = 30mA then Iea = 17mA

I_{LINE} = 60mA then Iea = 11mA).

The voltage level at pin 10 must be defined by an external regulator (i.e. : zener) and, if necessary, filtered with a capacitor (47 to 220 microF).

In case V_{LINE} (at pin 14) approaches voltage at pin 10, then the internal current source switches off and its DC current is shunt to ground through an internal complmentary generator, thus avoiding any negative effect on the AC and DC impedances of the telephone set application.

Figure 7.


I pin 10
(mA)
40
30
20
10
EXTRA CURRENT SUPPLY
AT pin 10
20
40
60
80
IL(mA)
MBBTEA7062-09