SGS-THOMSON
MICROELECTRONICS

TEA7050

# HIGH RANGE SPEECH CIRCUIT WITH SQUELCH FUNCTION

- 2/4 WIRES INTERFACE WITH
  - DOUBLE ANTISIDETONE NETWORK
  - MICROPHONE NOISE THRESHOLD (squelch)
  - RX GAIN AND AC IMPEDANCE EXTERNALLY PROGRAMMABLE
- DTMF INTERFACE
- PULSE DIAL INTERFACE
- 3.25 VOLTS SUPPLY FOR MICROPROCESSOR OR DIALER
- RESET TO MICROPROCESSOR
- CURRENT SUPPLY FOR LOUDSPEAKER
- HANDS-FREE INTERFACE
- DC CHARACTERISTIC AND ON/OFF HOOK FOR FRANCE
- CONTROL AGAINST HIGH VOLTAGE TRANSIENTS

DIP28   **SO-28**

ORDER CODES : TEA7050DP (DIP28)
TEA7050D (SO-28)
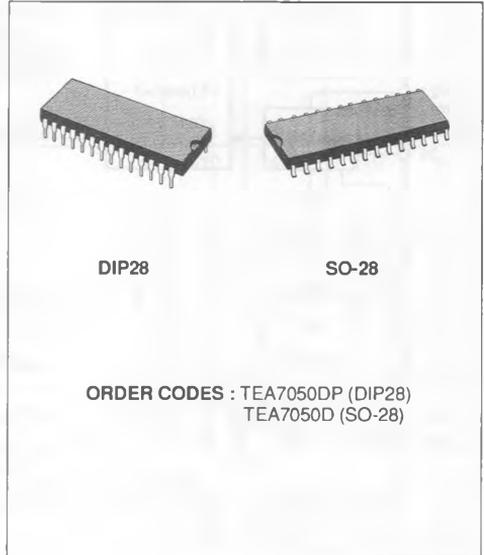
DESCRIPTION

The TEA7050 is expressly designed to meet the french specification for telephone set in high range equipments.

PIN CONNECTION (top view)

ANTISIDETONE LONG LINE	1	28 RECEIVE OUTPUT
ANTISIDETONE SHORT LINE	2	27 MICROPROCESSOR SUPPLY
AC IMPEDANCE	3	26 ANTINOISE FILTER
EXTRA RECEIVE OUTPUT	4	25 UC
AMPLIFIED TRANSMISSION	5	24 ULINE
Vref	6	23 SURCHARGE FILTER
DTMF INPUT	7	22 PULSE DIAL INPUT
MICROPHONE INPUT	8	21 HU STAGE CONTROL
Iref	9	20 MICROPROCESSOR RESET
PRIVATE/PUBLIC	10	19 HOOK DETECTION
MICROPHONE MUTE	11	18 RECEIVE MUTE
POWER CURRENT SOURCE	12	17 GROUND
THRESHOLD 1	13	16 THRESHOLD 4
THRESHOLD 2	14	15 THRESHOLD 3

M88TEA7050-02

BLOCK DIAGRAM

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ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
Vc	Stabilized Voltage (pin 25)	Il = 27mA	2.6	2.8	2.95	V
Idem	Charging Current (pin 25)	Il = 27mA		2.6		mA
Ir	Line Current Regulation for HV Control (pin 21)	Pin 19 = Pin 25 = GND Il = 150mA Il = 100mA	150		5	µA
		Pin 19 ON ; Pin 25 = GND Il = 75mA	150			µA
		Pins 19 and 25 ON Il = 60mA Il = 16mA	150		100	µA nA
Ir/Il		27mA < Il < 50mA	0.8	0.9	1.0	µA/mA
Iint	Internal Bias Current (pin 25)	Il = 27mA ; R9 = 26.7 Kohms ; (V24 = R6*Iint + Vc)	410	460	510	µA
Vref	Reference Voltage	Il = 27mA	1.32	1.38	1.47	V
Iref	Current at Vref		– 10		100	µA
Vmp	Stabilized Supply at Pin 27		3.1	3.3	3.5	V
Icmp	Charging Current at Pin 27	Pin 19 = Pin 25 = GND IL1 = Il – Idem	0.7 x x IL1			mA
Ispm	Static Current at Pin 27	Il = 6mA Il > 25mA	0.5 2.5	2.8		mA
Iimp	Internal Consumption		90	120	160	µA
Iea	Supply Current for Parallel Circuits (pin 12)	R9 = 26.7Kohm Il = 10mA Il = 27mA Il = 42mA	8 21	3 9.5 23.5	11 26	mA mA mA
Vrh Vrb Vrsh Vrsb	Microprocessor Reset High Treshold Low Treshold Output High Output Low	Reset = 1 Reset = 0	0.845 0.76 0.9	0.89 0.8	0.84 0.1	Vmp (pin 27)

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
Vmh Vmb	Mute Microphone (pin 11)	ON OFF	1.6		0.8	V V
Vmh Vmb	Mute Earphone (pin 18)	ON OFF	2.7		2.1	V V
Gel Gec	Tx Gain Long Line Tx Gain Short Line	Il = 27mA Il = 42mA	48.5 41.5	49.5 43.5	50.5 45.5	dB
DGe	Squelch Attenuation			– 9		dB
Vse	Squelch Switch-off Level on the Line	Il = 27mA	– 44	– 39	– 34	dBm
Gmf	DTMF Gain	Il = 27mA Pin 11 > 1.6V	33.5	34.5	35.5	dB
De	Tx Distortion	Il = 27 to 42mA Vl = 0dBm Vl = 3dBm			3 10	% %
Ze	Microphone Impedance		9.6	12	14.5	Kohm
Bep	Tx Noise (psophometric)	Il > 27mA 2K at Pins 6-8		– 71		dBmp
Re	Tx Attenuation in Mute Mode	Il = 27mA Pin 11 > 1.6V	60			dB
Grl Grc	Rx Gain Long Line Rx Gain Short Line	Il = 27mA Il = 42mA	29 22	30 24	31 26	dB
Dr	Rx Distortion	Il = 27 to 42mA Vec = 500mV Vec = 700mV			3 10	% %
Brp	Rx Noise	Il > 27mA		– 74		dBmp
Rc	Rx Attenuation in Mute Mode	Il = 27mA Pin 18 > 2.7V	60			dB
Gal	Antisidetone	Il = 27 to 42mA	– 22			dB
Zac	AC Impedance	Il > 27mA	500	650	800	ohm
Grs	Confidence Level Vrec/Vmf	Pin 11 > 1.6V ; Pin 14 > 2.7V	28	31	34	dB

TEST CIRCUIT

M88TEA7050-03

R1 = 920KΩ	R12 = 8Ω	C1 = 188µF	C6 = 27pF
R2 = 820KΩ	R13 = 2.7KΩ	C2 = 4.7µF	C7 = 27pF
R3 = 1.5MΩ	R14 = 8Ω	C3 = 10µF	C8 = 2.2nF
R4 = 75Ω	R15 = 140KΩ	C4 = 1µF	C9 = 2.2nF
R5 = 5.1KΩ	R16 = 2.7KΩ	C5 = 100µF	C10 = 2.2µF
R8 = 13KΩ	R17 = 1.2 KΩ		C11 = 220µF
R9 = 26.7KΩ	R18 = 680KΩ for private complex		
R11 = 140KΩ			

CIRCUIT DESCRIPTION

1. DC-CHARACTERISTICS

1.1. VC (PIN 25). The stabilized voltage Vc is connected to Vline (pin 24) through an internal shunt regulator which presents to the line a high AC impe-

dance at frequencies higher than 200Hz. At this purpose the value of C1 (at pin 25) must be not lower than 47 microFarad.

Figure 1.

M88TEA7050-04
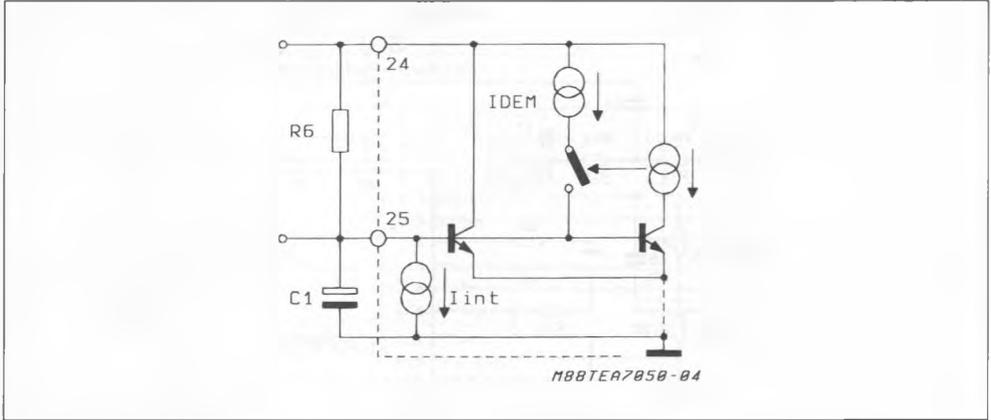
At "Off-hook", with only DC voltage applied to the line terminals, C1 fixes the timing of the line current profile at :
- 150mA max for a time shorter than 400msec (T-charge)
- 60mA max in steady state (conversation)

T-charge of 240msec (typ) is obtained with C1 = 220µF.

$$T\text{-charge} = \frac{Vc \times C1}{Idem} \text{ typically.}$$

Figure 2.

M88TEA7050-05

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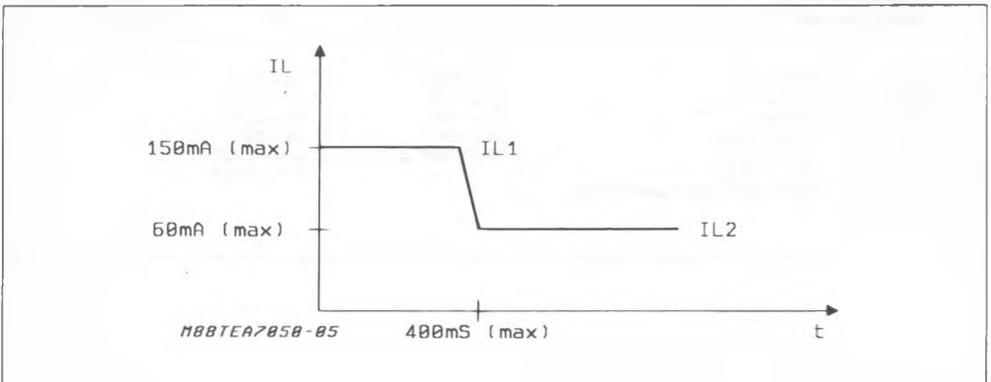
1.2. HOOK DETECTION (in ring mode) (pin 19).
The DC-characteristic requested to allow off-hook
detection by the exchange during ring call may be
accomplished :

a) through an analog control (R-C) or
b) by a microprocessor.

a) Application with standard dialer (analog control)
The components R1, R2 and C2 define the timing

of the DC characteristic and also limit at 75mA-peak
the line current during decadic dialing.

Optimum values are : - R1 x C2 = 1.8sec ;
R2 x C2 = 0.8sec.

To reduce the minimum time between a "on-hook /
off-hook" sequence, R2 may be replaced by a switch
to ground.

Figure 3.
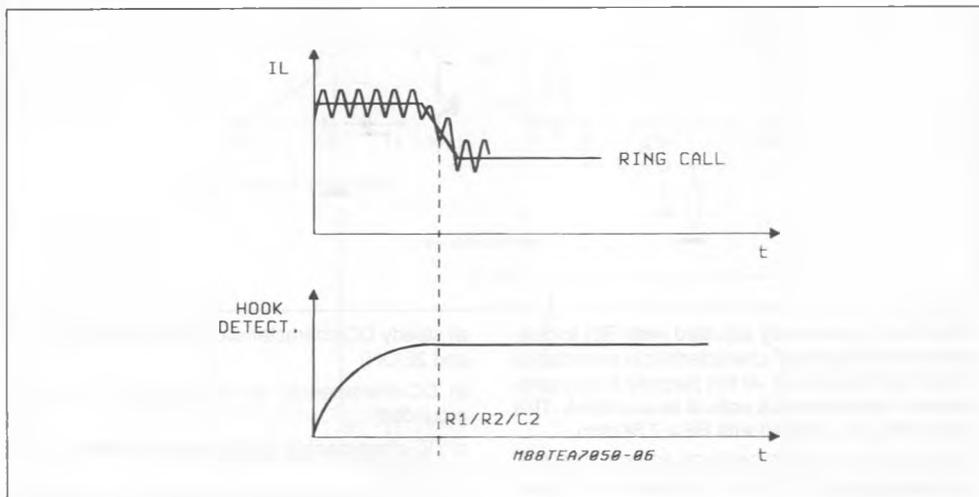
b) Application with a microprocessor

Pin 19 may be controlled directly by the micro-controller, through a resistor R1b which replaces R1, R2 and C2.

Figure 4.
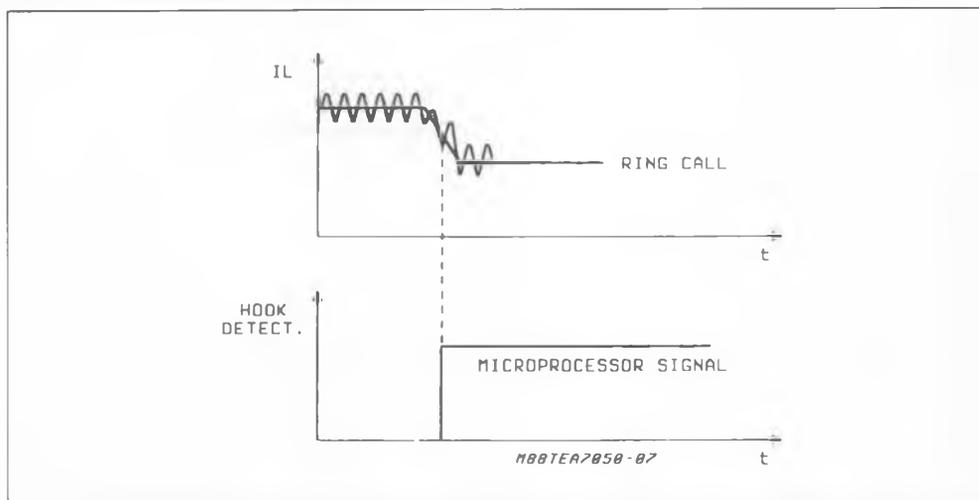
1.3. VLINE (PIN 24). The line voltage (pin 24) is determined by the value of the external resistor R6 and by the internal current, Iint, flowing between Vc (pin 25) and Ground (see also paragr. 1.1.) :

$$Vline = Vc + R6 \times Iint.$$

Vc is fixed by design at about 2.8 volts.

Iint is reversely related to R9 (Iint = 12V / R9 at Iline = 27mA).

Figure 5.

M88TEA7050-08
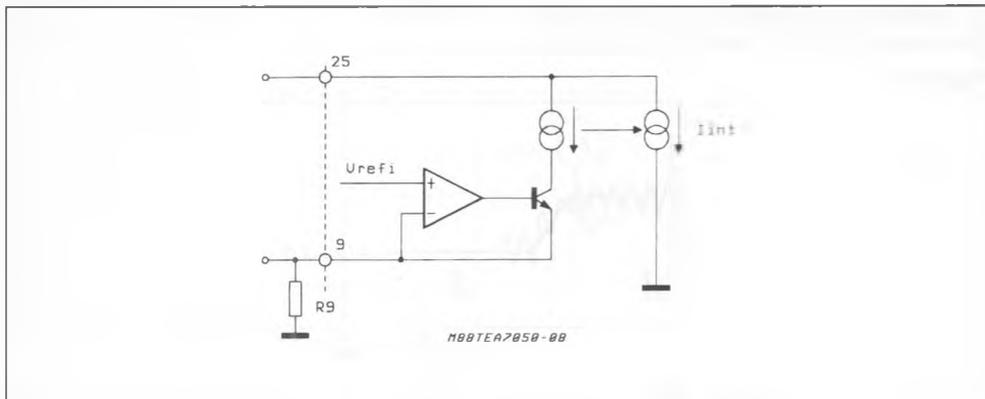
Vline must be externally adjusted (with R6) to guarantee both DC and AC characteristic in accordance to the french standards. At this purpose it is suggested that Vline equals 5.6 volts at Iline = 16mA. This typical value is obtained with R6 = 7.5Kohm.

1.4. HIGH VOLTAGE CONTROL STAGE (PIN 21). The behaviour of "HV control" is determined by several conditions, both internal (Iline sensor) and external (pins 19 and 25) with the purpose to accomplish the different DC characteristics and transitory conditions imposed by the French specification :

a) steady DC-characteristic and lightnings (pins 19 and 25 ON)

b) DC-characteristic at off-hook (pin 19 and 25 grounded)

c) DC-characteristic during decadic dialing (pin 25 grounded)

d) DC-characteristic after off-hook in ringing (pin 19 grounded)

To do that, HV control pin regulates the current injected into the external high voltage transistor stage, requested by the French specification.

Figure 6.

a) pin 19 and 25 ON

b) pin 19 and 25 grounded

c) pin 19 ON ; PIN 25 grounded

d) pin 19 grounded ; pin 25 ON

M881EA7050-89
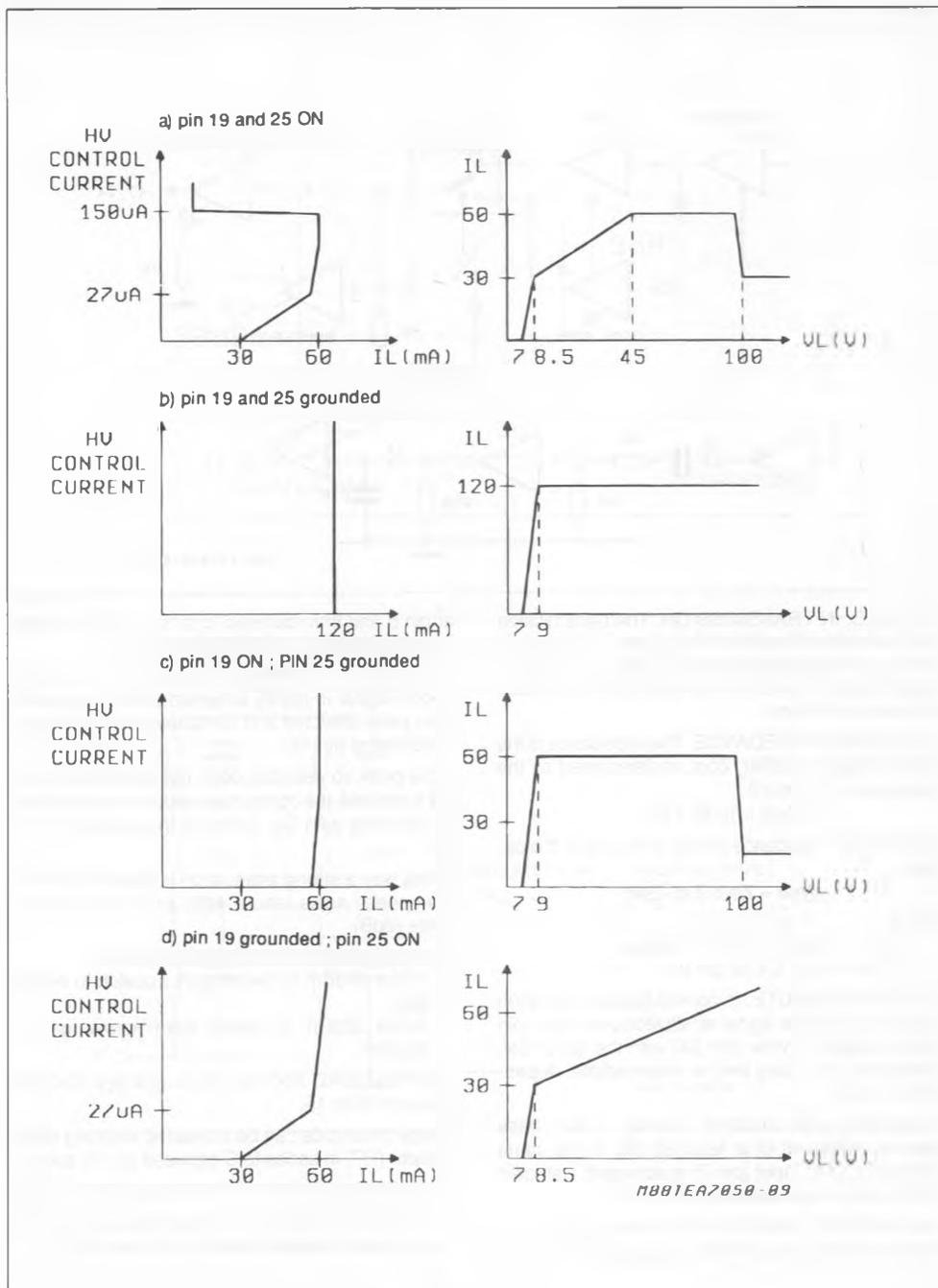
2. TRANSMISSION CHAIN

Figure 7.
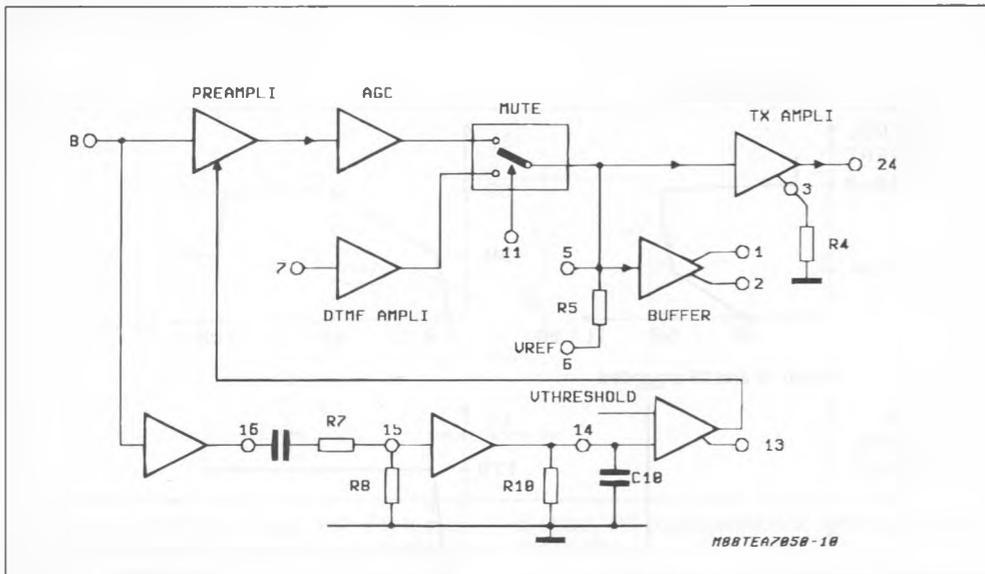
2.1. A.G.C. IN TRANSMISSION. The transmission gain between Microphone Input (pin 8) and Vline (pin 24) is internally decreased of 6dB when the line current varies from 27mA to 42mA with a constant AC load of 600ohms.

2.2. SENDING IMPEDANCE. The impedance of the Output Stage Amplifier, Zout, is determined by the impedance Z4 at pin 3.

$$Zout = 10.65 \times Z4.$$

The total AC impedance shown to the line is the parallel

$$Zpar = Zout//Zint//Zext$$

where :
- Zint = 10kohm // 8.5nF (internal)
- Zext = R6 // C4 (at pin 24)

2.3. SENDING MUTE. In normal speech operation (Vmute 0.8V), the signal at Microphone Input (pin 8) is amplified to Vline (pin 24) with the gains Gec (short line), Gel (long line) or intermediate, depending on Iline.

In sending mute condition (Vmute 1.6V) these gains are reduced of at least 60 dB. In the same condition DTMF input (pin 7) is activated, with gain Gmf to the line independent from Iline.

2.4. ANTISIDETONE BUFFER. The signal coming from the sending preamplifier is internally presented

at pin 5 and than buffered to pins 1 and 2 for side-tone cancellation (see paragraph 3.2.).

2.5. NOISE THRESHOLD (SQUELCH). The microphone signal is highly amplified (46dB) at pin 16, then peak detected and compared with an internal threshold at pin 14.

If the peak so detected does not exceed the internal threshold, the comparator reduces of about 9dB the sending gain Ge, acting at the preamplifier level.

In this way a strong attenuation is obtained, both of the speech noise (about 4dB) and of the ambient noise (9dB).

The equivalent thresholds on the line are :
- minus 39dBm to switch from squelch to normal gain,
- minus 32dBm to switch from normal gain to squelch,

with R8=150KΩ from pin 15 to gnd and C=3.3nF from pin 16 to 15.

These thresholds can be increased inserting also a resistor (R7) in series to C between pin 16 and 15.

The variation is given by the formula : (R8 + R7)/R8.

A hysteresis of about 3dB is defined to avoid continuous switch between squelch and normal gain.

Figure 8.

M88TEA7050-11
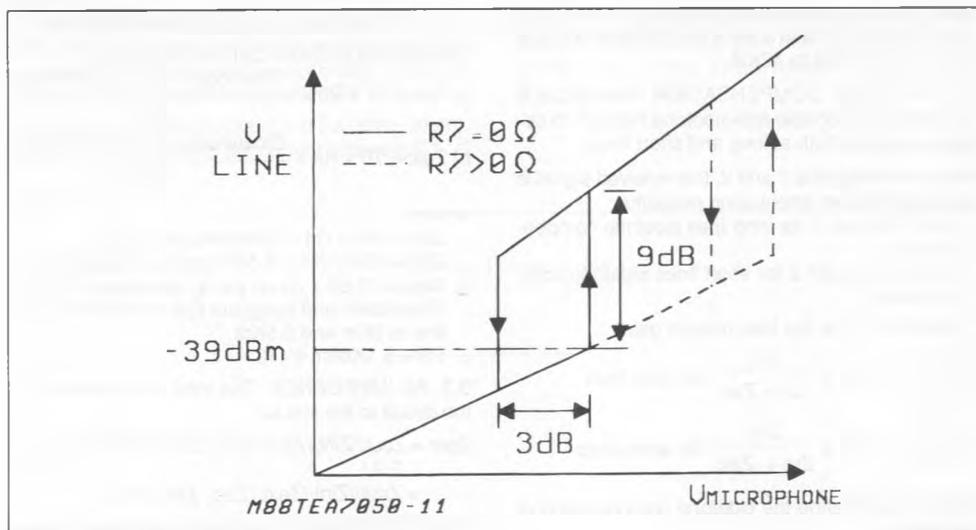
3. RECEIVE CHAIN

Figure 9.

M88TEA7050-12
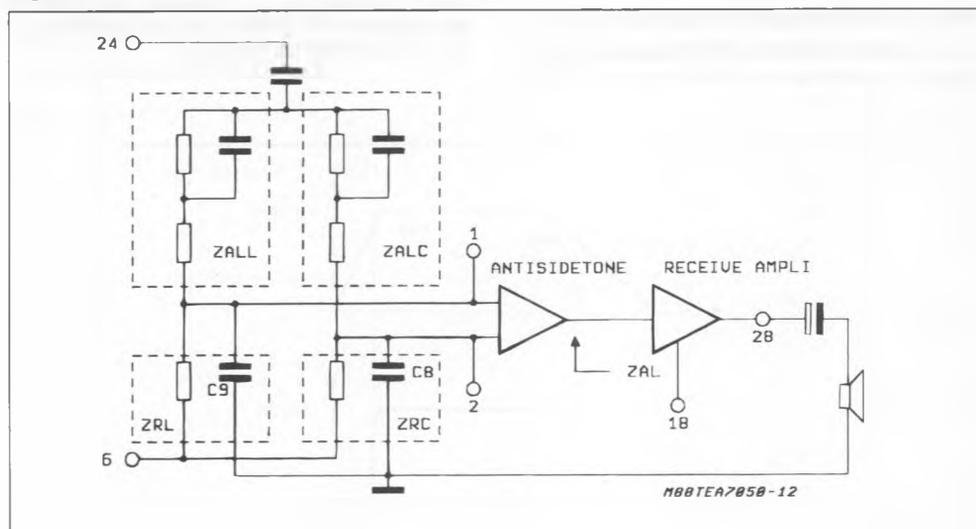
3.1. A.G.C. IN RECEIVE. As described for the transmission chain, also the receiving gains Gr, from pins 1 and 2 to pin 28, have a reduction of 6dB when Iline moves from 27mA to 42mA.

3.2. SIDETONE COMPENSATION. The circuit is provided with a double anti-sidetone network to optimize sidetone both at long and short lines.

Before entering pins 1 and 2, the received signal is attenuated by two attenuating networks :
- Zall / Zrl to pin 1 for long lines sidetone compensation,
- Zalc / Zrc to pin 2 for short lines sidetone compensation.

Zrl and Zrc define the total receive gains :

a) $\dfrac{V28}{V24} = Grl \times \dfrac{Zrl}{Zrl + Zall}$ for long lines

b) $\dfrac{V28}{V24} = Grc \times \dfrac{Zrc}{Zrc + Zalc}$ for short lines

Zall and Zalc define the sidetone compensation of the circuit.

The equivalent balancing impedance is given by the formula :

$$Zal = K \times Zalc + (1\ K) \times Zall$$

where K = 0 at Iline = 27mA or lower (long line)

K varies from 0 to 1 with Iline between 27mA

and 42mA,

K=1 at Iline=42mA or higher (short line).

Calculations to define Zall and Zalc are :

a) $Zall = 70 \times R5 \times \dfrac{Zline(long)\ //\ Zext\ //\ Zint\ //\ Zout}{Zout}$

b) $Zalc = 70 \times R5 \times \dfrac{Zline(short)\ //\ Zext\ //\ Zint\ //\ Zout}{Zout}$

where :
- Zext = R6 // C4 // (Zelectret) (at pin 24)
- Zint = 10Kohms // 8.5nF (internal impedance)
- Zout = 10.65 x Z4 (at pin 3 ; see paragr. 2.2.)
- Zline(short) and (long) are the impedances of the line at 0Km and 3.5Km.
- R5 = 5.1Kohm ± 1%

3.3. AC IMPEDANCE. The total AC impedance of the circuit to the line is :

Zpar = Zout//Zint//Zext//Zalc//Zall (see par. 2.2. and 3.2.)

= Zout//Zint//Zext (Zalc, Zall Zpar)

3.4. RECEIVE MUTE (and confidence level). When the receive channel is muted (Vpin 18 2.7V) the receive gain is reduced of 60dB minimum.

In this condition an internal connection is activated from DTMF input (pin 7) to Receive Output (pin 28) with a gain Gmf = 31dB to provide acoustic feedback of the DTMF transmission.

4. MICROPROCESSOR INTERFACE

4.1. MICROPROCESSOR SUPPLY (PIN 27). At "off-hook" the first priority of the circuit is to make some current available at the Microprocessor Supply (pin 27) to charge quickly the external capacitor C3.

This charging current is : Icpm = 0.7 x (Iline - Idem), where Idem = 2.6mA is the current charging C1.

Vmp = 3.3V in normal operation and current increases linearly from 0.5mA min, at Iline = 6mA, to 2.5mA min, at Iline = 27mA, remaining stable for higher values of Iline.

Figure 10.
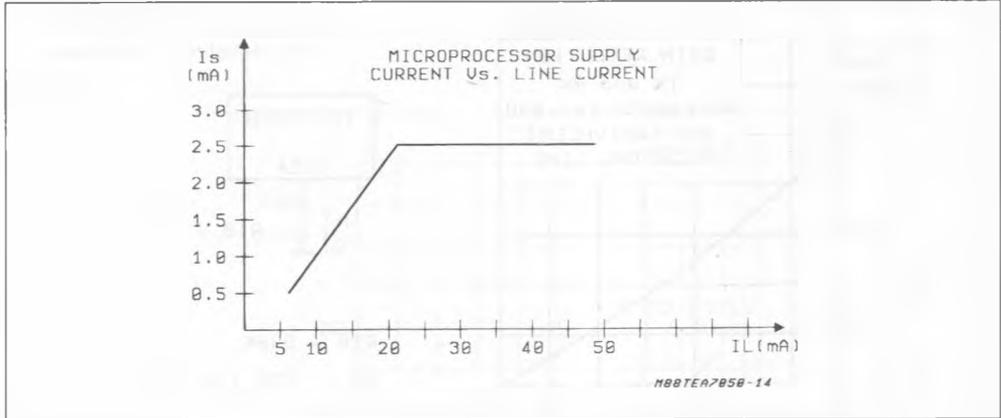

4.2. MICROPROCESSOR RESET (pin 20). The Microprocessor Reset becomes active when Vmp overcomes 85% of its nominal level.

It becomes low when Vmp undergoes 84%.

Slope A is related to C3, Iimp (internal consumption) and to the external load (microprocessor or dialer).

**Figure 11.**

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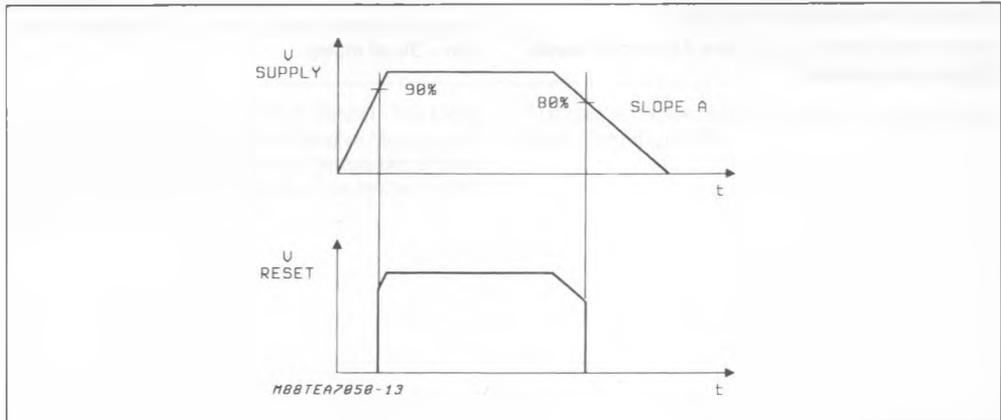
5. PUBLIC / PRIVATE

5.1. A.G.C. OFF (PIN 10). An external resistor, R18, applied between pin 10 and ground disconnects the AGC control.

Sending, receiving gain and sidetone compensation are now independent of the line length and the value of the current Ip, flowing through R18, defines the length of the line for which sidetone is optimized (Ip = 2.7V / R18).

Figure 12.
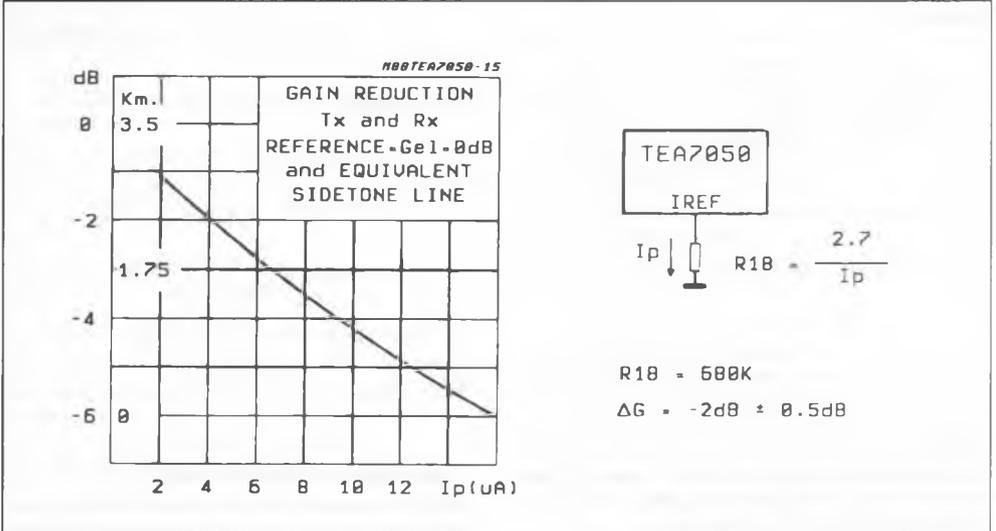
5.2. SECRET FUNCTION FOR PRIVATE (PINS 11 & 18). The two separate Mute pins allow "Secret Function" (only microphone muted).

As the two controls have different threshold levels, they can be operated :

a) separately through two different control logic,

b) connected in short circuit with a three levels logic (Vm = 0V speech mode ; Vm = 1.8V microph mute ; Vm = 3V all mute).

6. POWER MANAGEMEN AND HANDS-FREE INTERFACE

6.1. POWER MANAGEMENT (PIN 12). Most of the DC current available from the line will be delivered by the speech circuit at the output Isource (pin 12) through an internal current generator.

Typical values of this current, Iea, are :
- Iea = (0.3 x Iline) for Iline < 22mA
- Iea = (0.9 x Iline 13mA) for Iline > 22mA

(ex : Iline=16mA then Iea=4.8mA
Iline=30mA then Iea=14.0mA
Iline=60mA then Iea=41.0m)

The voltage level at pin 12 must be defined by an external regulator (i.e. : zener) and, if necessary, filtered with a capacitor (47 to 220 µF).

In case Vline (at pin 24) approaches V at pin 12, then the internal current source switches off and its DC current is shunt to ground through an internal complementary generator, thus avoiding any negative effect on the Ac and DC impedances of the telephone set application.

Figure 13.
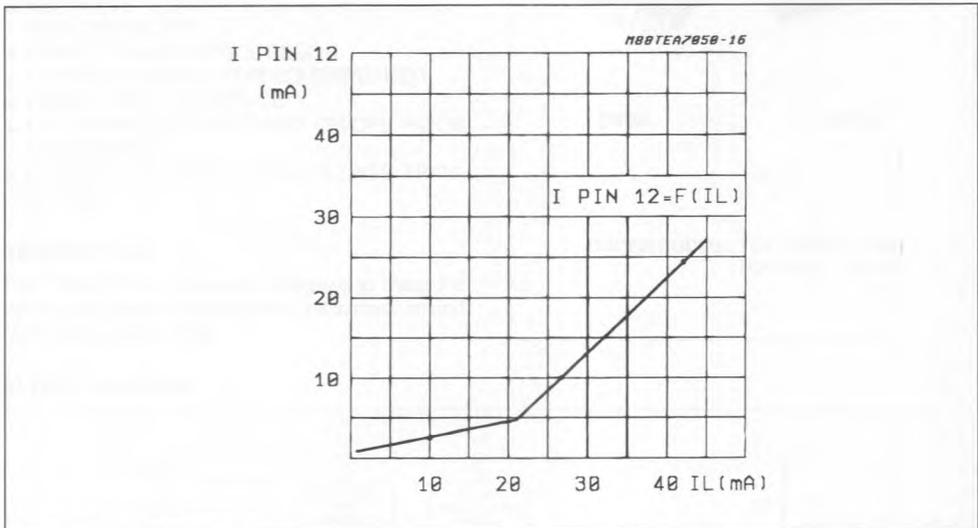
6.2. EXTRA RECEIVE OUTPUT (PIN 4). The Extra Receive Signal is active also in Receive Mute condition, so allowing the transit of the receive signal from the speech circuit to the Hands-Free system even when the earpiece is muted.

The gain at this pin is 30dB lower than standard Receive Output (pin 28).