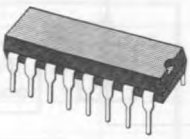
SGS-THOMSON MICROELECTRONICS

TEA2037A

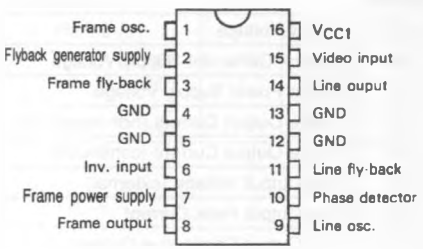
HORIZONTAL AND VERTICAL DEFLECTION MONITOR

- DIRECT LINE DARLINGTON DRIVE
- DIRECT FRAME-YOKE DRIVE (± 1A)
- COMPOSITE VIDEO SIGNAL INPUT CAPABILITY
- FRAME OUTPUT PROTECTION AGAINST SHORT CIRCUITS
- PLL
- VERY FEW EXTERNAL COMPONENT
- VERY LOW COST POWER PACKAGE



TEA2037A
BATWING DIP 16
(Plastic Package)

PIN CONNECTIONS

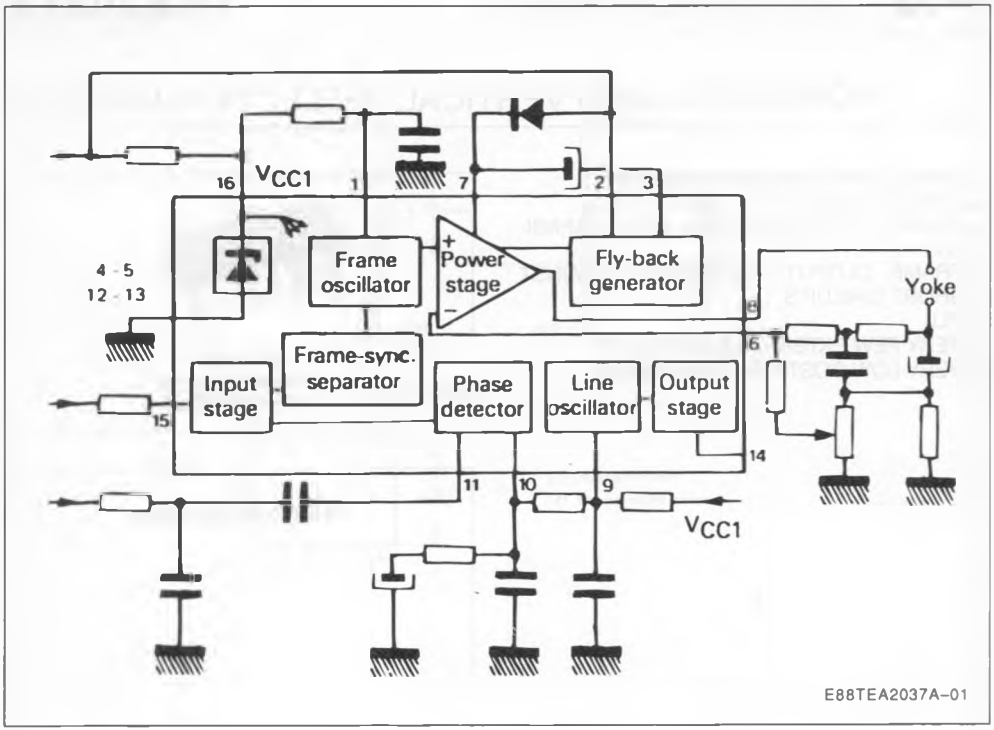


E88TEA2037A-02

DESCRIPTION

The TEA2037A is an horizontal and vertical deflection circuit. It uses the same concept as the TEA2017 but optimised for small screens, for a very low cost solution.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
VCC1	Supply Voltage	30	V
V2	Flyback Generator Supply Voltage	35	V
V7	Frame Power Supply Voltage	60	V
I8nr	Frame Output Current (non repetitive)	± 1.5	A
I8	Frame Output Current (continuous)	± 1	A
V14	Line Output Voltage (external)	60	V
Ip14	Line Output Peak Current	0.8	A
IC14	Line Output Continuous Current	0.4	A
Tstg	Storage Temperature	–40, + 150	°C
Tj	Max Operating Junction Temperature	150	°C

THERMAL DATA

Rth (j-c)	Max Junction-case Thermal Resistance	15	°C/W
Rth (j-a)	Typical Junction-ambient Thermal Resistance (soldered on a 35µm thick 45cm2 PC board copper aera)	45	°C/W
T_J	Max Recommended Junction Temperature	120	°C

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Supply (shunt regulator) Pin 16				
ICC1	Supply Current	10		20	mA
VCC1	Supply Voltage (ICC1 = 15mA)	9	9.8	10.5	V
ΔVCC1	Voltage Variation (ICC1 : 10mA → 20mA)	− 280	50	+ 280	mV
LPS	Starting Threshold for Line Output Pulses			5	V
	Video Input Pin 15				
V15	Reference Voltage (I15 = − 1μA)	1.4	1.75	2	V
MWF	Minimum Width of Frame Pulse (when synchronized with TTL signal)	50			μs
	Line Oscillator Pin 9				
LT9	Low Threshold Voltage	2.8	3.2	3.6	V
HT9	High Threshold Voltage	5.4	6.6	7.8	V
BI9	Bias Current		100		nA
DR9	Discharge Impedance	1.0	1.4	1.8	KΩ
FLP1	Free Running Line Period R = 34.9KΩ Tied to VCC1 C = 2.2nF Tied to Ground	62	64	66	μs
FLP2	Free Running Line Period R = 13.7KΩ C = 2.2nF		27		μs
OT9	Oscillator Threshold for Line Output Pulse Triggering		4.6		V
$\frac{\Delta F}{\Delta \theta}$	Horizontal Frequency Drift with Temperature (see application fig.8)		2		Hz/°C
	Line Output Pin 14				
LV14	Saturation Voltage (I14 = 200mA)		1.1	1.6	V
OPW	Output Pulse Width (line period = 64μs)	20	22	24	μs
	Line Flyback Input Pin 11				
V11	Bias Voltage	1.8	2.4	3.2	V
Z11	Input Impedance	4.5	5.8	8	KΩ
	Phase Detector Pin 10				
I10	Output Current During Synchro Pulse	250	450	800	μA
RI10	Current Ratio (positive/negative)	0.95	1	1.05	
LI10	Leakage Current	− 2		+ 2	μA
CV10	Control Range Voltage	2.60		7.10	V

ELECTRICAL CHARACTERISTICS (continued)

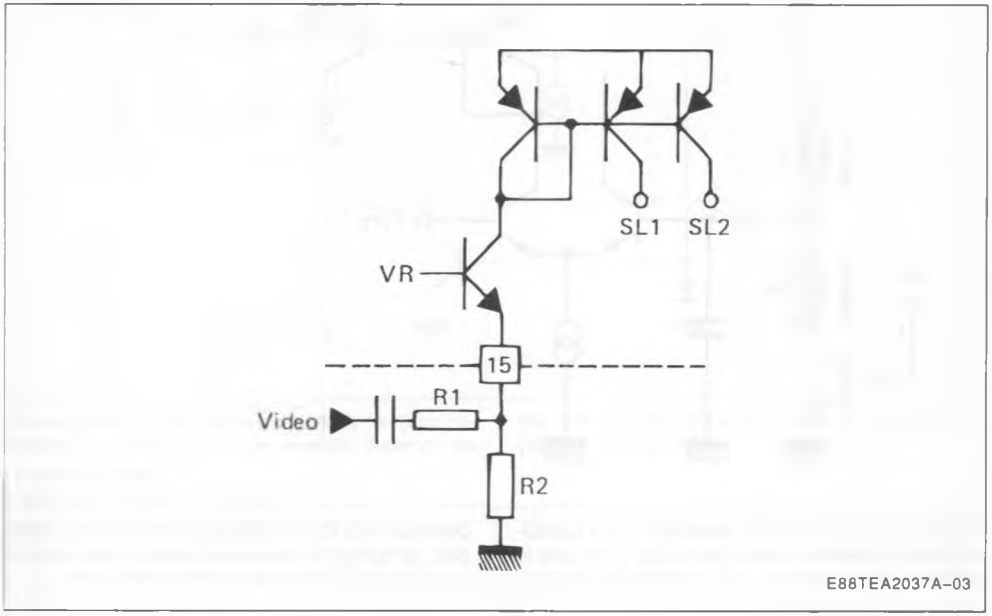
Symbol	Parameter	Min.	Typ.	Max.	Unit
	Frame Oscillator Pin 1				
LT1	Low Threshold Voltage	1.6	2.0	2.3	V
HT1	High Threshold Voltage	2.6	3.1	3.6	V
BI1	Bias Current		30		nA
DR1	Discharge Impedance	300	470	700	Ω
FFP1	Free Running Frame Period R = 845KΩ Tied to VCC1 C = 180nF Tied to Ground	20.5	23	25	ms
MFP	Minimum Frame Period (I15 = – 100µA) With the Same RC		12.8		ms
FFP2	Free Running Frame Period R = 408KΩ C = 220nF		14.3		ms
FPR	Frame Period Ratio = $\frac{FFP}{MFP}$	1.7	1.8	1.9	
FG	Frame Saw-tooth Gain Between Pin 1 and non Inverting Input of the Frame Amplifier		– 0.4		
$\frac{\Delta F}{\Delta \theta}$	Vertical Freq. Drift with Temperature (see application fig.8)		4.10^{-3}		Hz/°C
	Frame Power Supply Pin 7				
V7	Operating Voltage (with flyback Generator)	10		58	V
I7	Supply Current (V7 = 30V)			22	mA
	Flyback Generator Supply Pin 2				
V2	Operating Voltage	10		30	V
	Frame Output Pin 8				
	Saturation Voltage to Ground (V7 = 30V)				
LV8A	I8 = 0.1A		0.06	0.6	V
LV8B	I8 = 1A		0.37	1	V
	Saturation Voltage to V7 (V7 = 30V)				
HV8A	I8 = – 0.1A		1.3	1.6	V
HV8B	I8 = – 1A		1.7	2.4	V
	Saturation Voltage to V7 in Flyback Mode (V8 > V7)				
FV8A	I8 = 0.1A		1.6	2.1	V
FV8B	I8 = 1A		2.5	4.5	V
	Flyback Generator Pin 2 and Pin 3				
	* Flyback Transistor on (output = high state) V2 = 30V				
F2DA	V3/2 with $I_{3 \rightarrow 2}$ = 0.1A		1.5	2.1	V
F2DB	$I_{3 \rightarrow 2}$ = 1A		3.0	4.5	V
FSVA	V2/3 with $I_{2 \rightarrow 3}$ = 0.1A		0.8	1.1	V
FSVB	$I_{2 \rightarrow 3}$ = 1A		2.2	4.5	V
	* Flyback Transistor off (output = V7 – 8V) V7 = V2 = 30V				
FCI	Leakage Current Pin 2			170	µA

The TEA2037A performs all the video and power functions required to provide signals for the direct drive of the line darlington and frame yoke.

It contains :

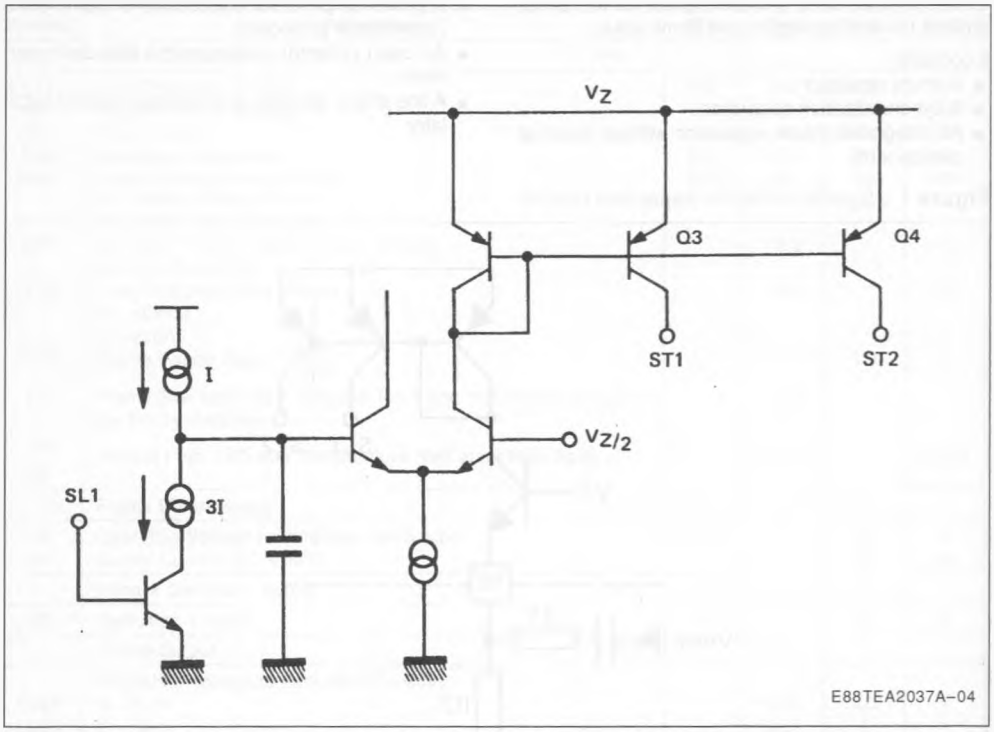
- A shunt regulator
- A synchronization separator
- An integrated frame separator without external components
- A saw-tooth generator for the frame
- A power amplifier for direct drive of frame yoke (short circuit protected)
- An open collector output for the line darlington drive
- A line phase detector and a voltage control oscillator

Figure 1 : Synchronization Separator Circuit.



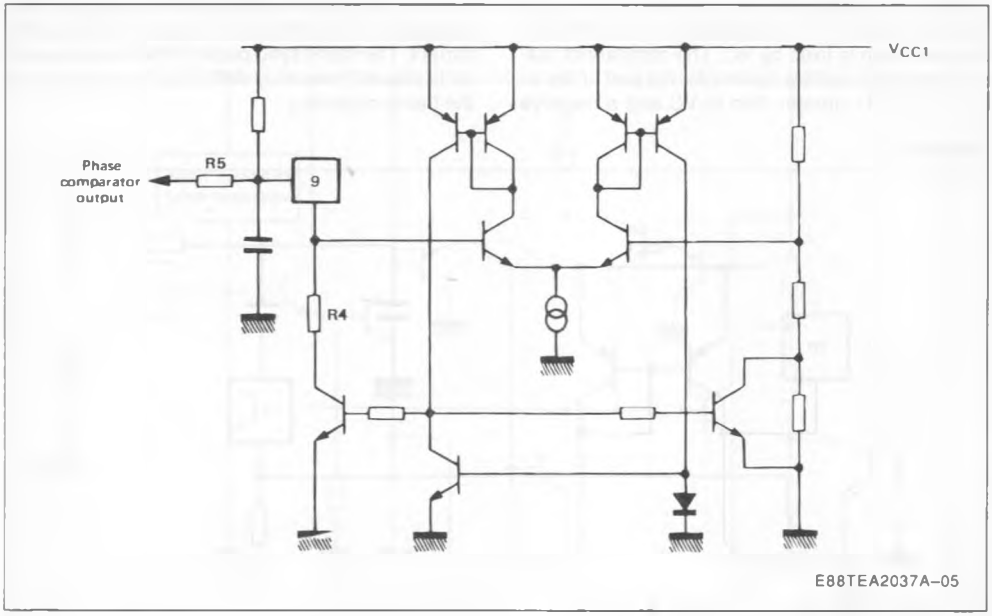
The slice level of sync-separation is fixed by value of the external resistors R_1 and R_2. V_R is an internally fixed voltage.

Figure 2 : Frame Separator.



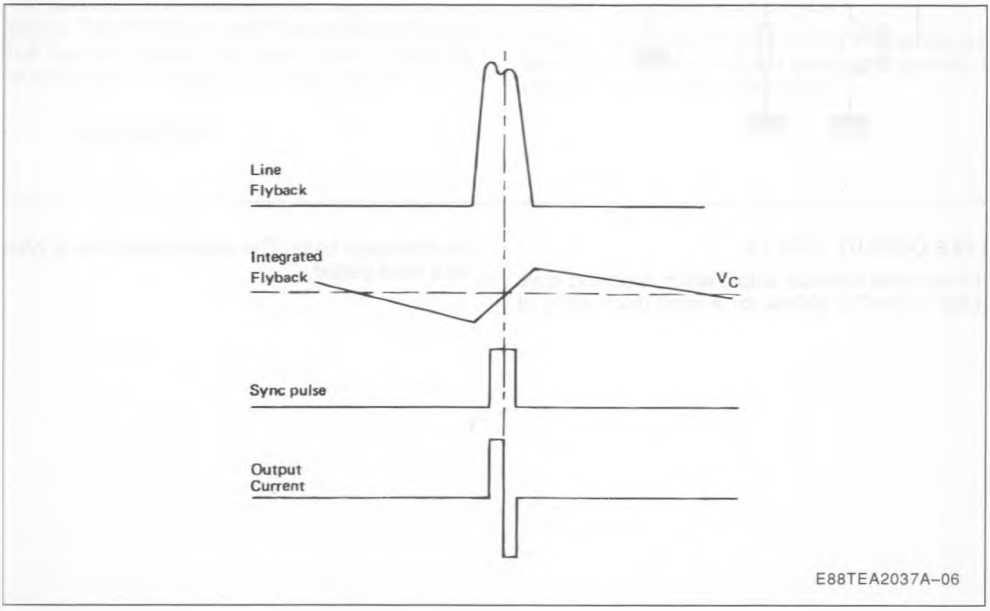
The sync-pulse allows the discharge of the capacitor by a 2 x I current. A line sync-pulse is not able to discharge the capacitor under $V_Z/2$. A frame sync pulse permits the complete discharge of the capacitor, so during the frame sync-pulse Q3 and Q4 provide current for the other parts of the circuit.

Figure 3 : Line Oscillator.



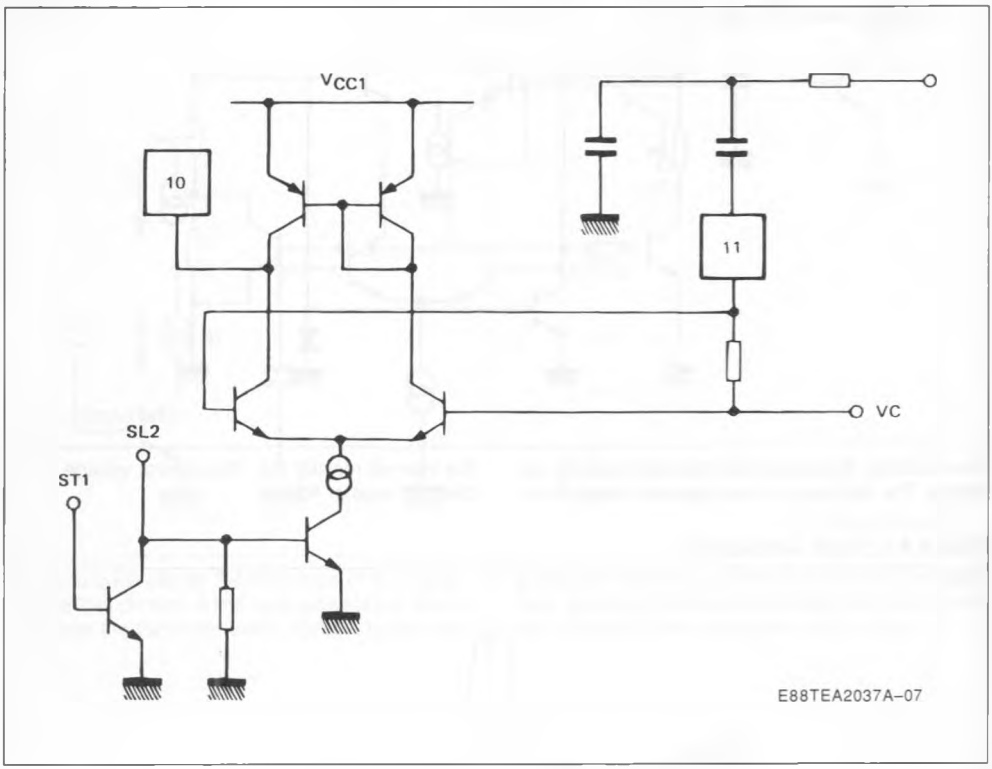
The oscillator thresholds are internally fixed by resistors. The discharge of the capacitor depends on the internal resistor R4. The control voltage is applied on resistor R5.

Figure 4 : Phase Comparator.



The sync-pulse drives the current in the comparator. The line flyback integrated by the external network gives on pin 11 a saw tooth, the DC offset of this saw tooth is fixed by VC. The comparator output provides a positive current for the part of the signal on pin 11 greater than to VC and a negative current for the other part. When the line flyback and the video signal are synchronized, the output of the comparator is an alternatively negative and positive current. The frame sync-pulse inhibits the comparator to prevent frequency drift of the line oscillator on the frame beginning.

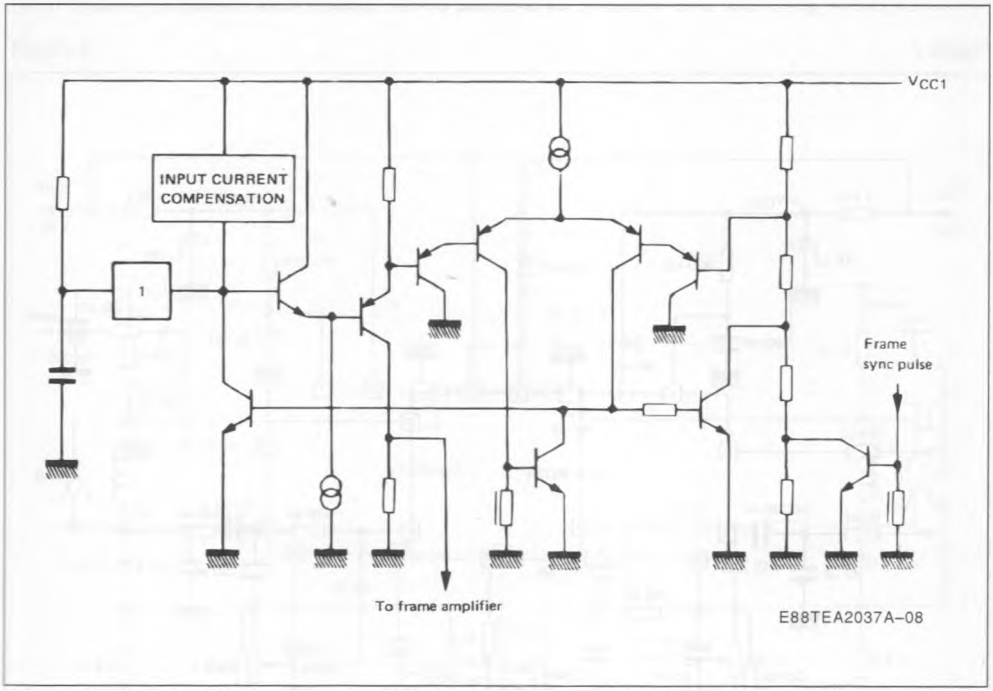
Figure 5.



LINE OUTPUT (PIN 14)

It is an open collector output which is able to drive pulse current of 800mA for a rapid discharging of the darlington base. The output pulse time is 22µs for a 64µs period.

Figure 6 : Frame Oscillator.



The oscillator thresholds are internally fixed by resistors. The oscillator is synchronized during the last half free run period. The input current during the charge of the capacitor is less than 100nA.

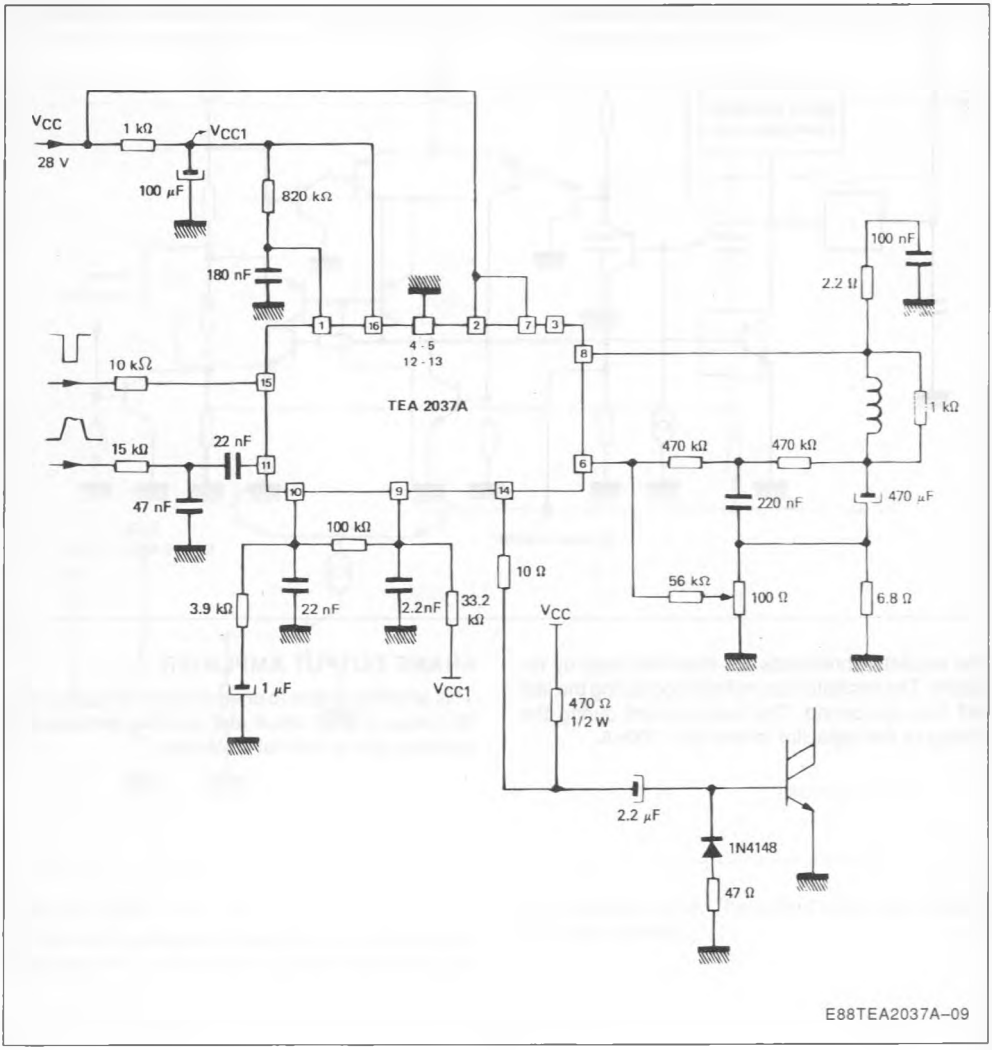
FRAME OUTPUT AMPLIFIER

This amplifier is able to drive directly the frame yoke. Its output is short circuit and overload protected ; it contains also a thermal protection.

TYPICAL APPLICATION FOR DISPLAY UNITS

(without flyback generator and with TTL sync-pulse drive ; yoke : 72mH, 40Ω)

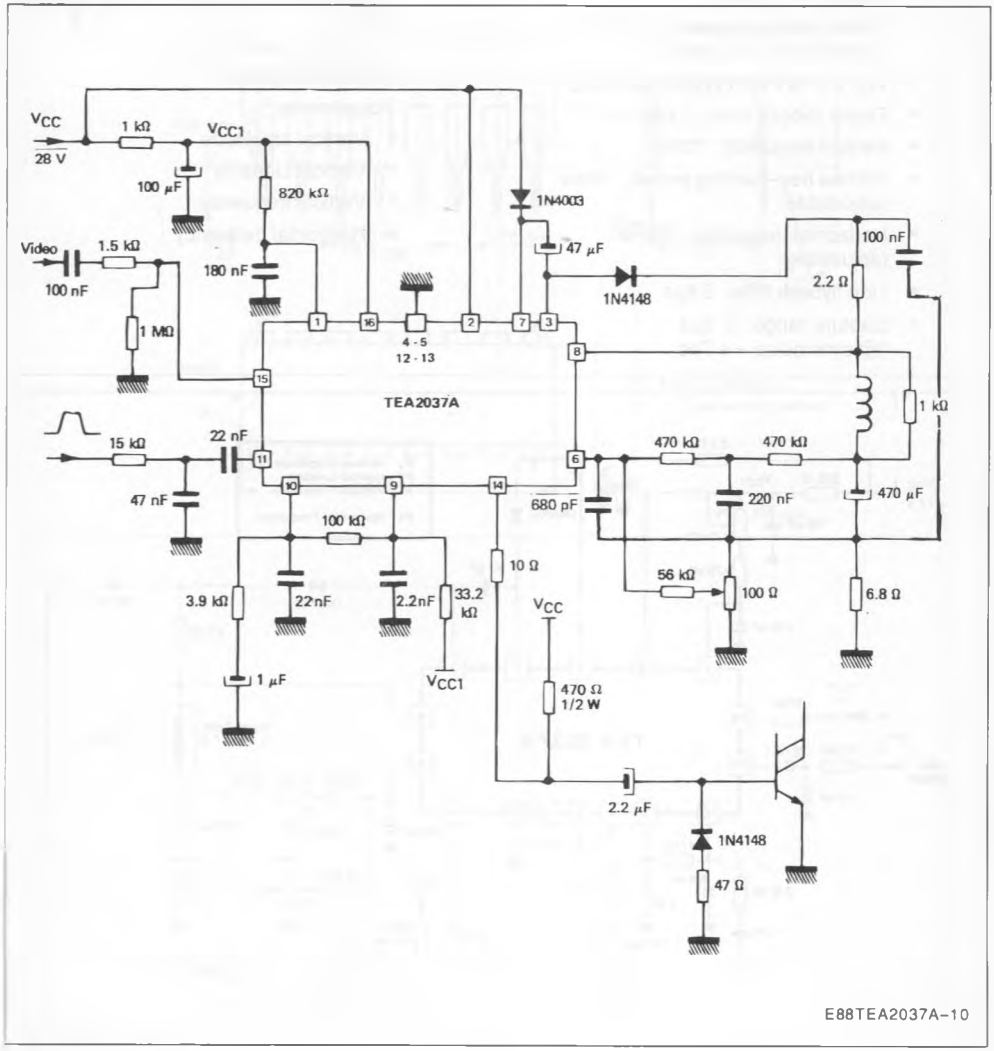
Figure 7.



TYPICAL APPLICATION FOR DISPLAY UNITS

(with flyback generator and video drive ; yoke : 72mH, 40Ω)

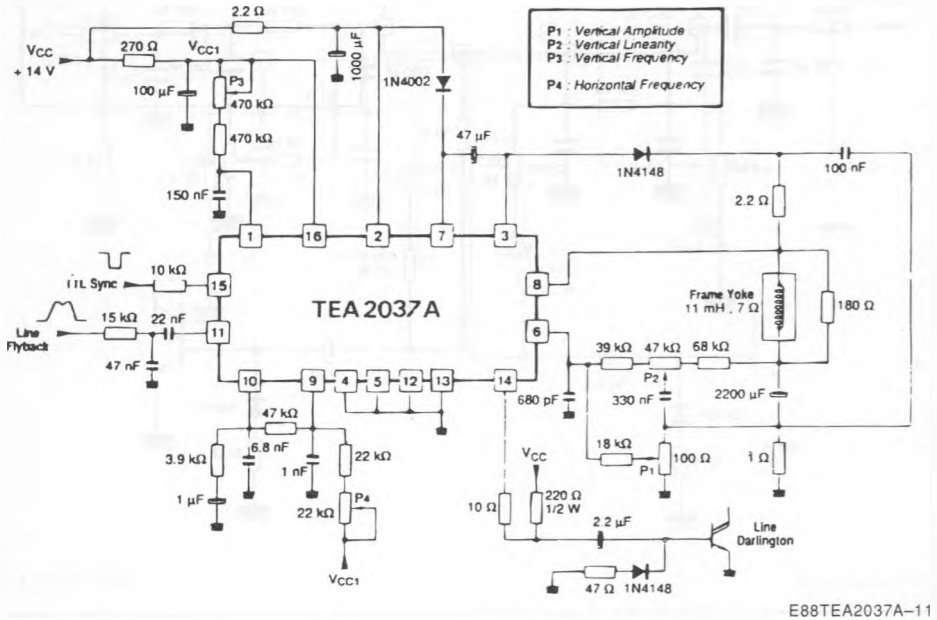
Figure 8.



TYPICAL APPLICATION FOR HIGH FREQUENCY MONITOR

CHARACTERISTICS

- Screen : 14" Colour
- Frame deflection yoke : 11mH, 7Ω, 750mA peak–to–peak
- V_{CC} = + 14V with flyback generator
- Frame flyback time : 0.6ms
- Vertical frequency : 72Hz
- Vertical free–running period : 16ms (adjustable)
- Horizontal frequency : 35kHz (adjustable)
- Line flyback time : 5.5µs
- Capture range : ± 5µs (@ sync pulse = 4.7µs)
- Input signal : negative TTL sync (line + frame)
- Dissipated power : 1.4W (heatsink required)
- Adjustments :
  - Vertical amplitude
  - Vertical Linearity
  - Vertical frequency
  - Horizontal frequency



E88TEA2037A–11

PACKAGE MECHANICAL DATA

16 PINS – PLASTIC DIP