295-760

INTEGRATED CIRCUITS

DATA SHEET

TEA1100; TEA1100T
Battery monitor for NiCd and NiMH chargers

Preliminary specification
File under Integrated Circuits, IC03

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Philips Semiconductors

PHILIPS

Battery monitor for NiCd and NiMH chargers

TEA1100; TEA1100T

FEATURES

- Accurate regulation of charge current settings in co-operation with a switched mode power supply
- Accurate detection of fully charged batteries by currentless battery voltage sensing
- Switch over from fast to normal charging when batteries are fully charged
- Adjustable fast charging level (1 C to 5 C)
- Adjustable normal charging level (0.05 C to 0.25 C)
- Temperature guarding by means of an NTC resistor
- Tracking of maximum fast charging time with fast charging current level
- Protections against short-circuited and open batteries
- Large battery voltage range
- Both DC and PWM outputs with polarity switch

APPLICATIONS

- Charge systems for NICd and NiMH batteries

GENERAL DESCRIPTION

The TEA1100 is manufactured in a BICMOS process intended to be used as a battery monitor circuit in charge systems for NICd and NIMH batteries.

The circuit has to be situated on the secondary side in mains-isolated systems where it monitors the battery voltage and the charge current. The circuit drives, by means of an opto-coupler or a pulse transformer interface, an SMPS circuit, situated on the primary side of the system, thus controlling the charge current of the batteries. The circuit can drive the external power transistor in switched mode systems, which have a DC power source, via a driver stage.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1100	16	DIL	plastic	SOT38G
TEA1100T	16	SO16L	plastic	SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_p	positive supply voltage range		5.65	–	11.5	V
I_o	supply current	outputs off	–	–	4.1	mA
V_{vac}	voltage range of battery-full detection		0.385	–	3.85	V
dV_{vac}/V_{vac}	–dV detection level w.r.t. top value	note 1	–	1	–	%
I_{vac}	input current battery monitor		–	–	1	nA
V_{vac}	voltage protection battery low battery high		 – –	 0.3 4.25	 – –	 V V
 I_{ref} I_o	charging level fast normal	$I_{charge} = R1/R_s \times I$; see Fig. 3 $I = I_{ref}$ $I = 1/p \times 0.1 \times I_o$ (p = prescale factor)	 20 10	 – –	 100 50	 µA µA
f_{osc}	oscillator frequency		10	–	100	kHz

Note to the quick reference data

1. The –dV detection level can be adjusted by use of an external voltage regulator diode to increase the sensitivity.

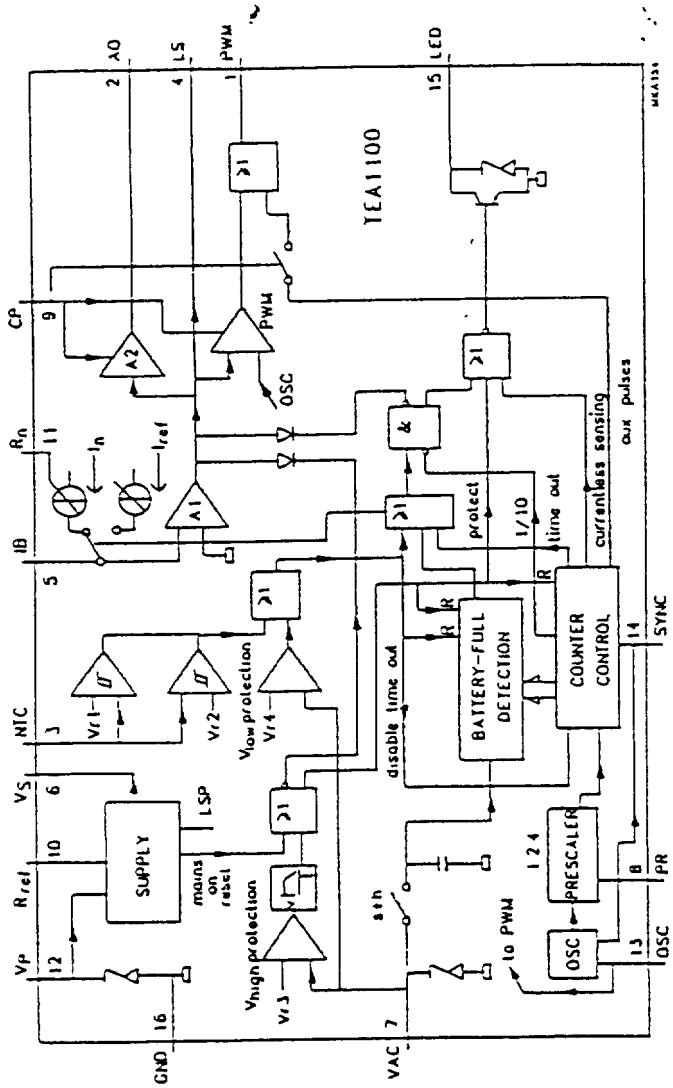


Fig 1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
PWM	1	pulse width modulator
AO	2	analog output
NTC	3	temperature sensor input
LS	4	loop stability
IB	5	charge current
V_s	6	stabilized supply voltage
VAC	7	battery voltage
PR	8	prescaler
CP	9	charge polarity
R_{ref}	10	reference resistor
R_n	11	normal charge reference resistor
V_p	12	positive supply voltage
OSC	13	oscillator input
SYNC	14	synchronization input
LED	15	LED output
GND	16	ground

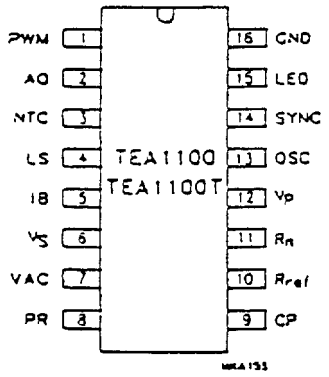


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The operation of the circuit will be explained with the aid of Fig.1 (block diagram) and Fig.3 (application diagram). The circuit is divided into several blocks which are described separately.

Supply block

The circuit needs a supply voltage on pin V_p with a value between 5.65 and 11.5 V. Above 6.4 V typ., the circuit starts up assuming that mains is connected to the system and the charge session begins. This supply can be generated by a separate winding on the transformer, as shown in Fig.3 (application diagram), in either the flyback or the forward stroke. Another possibility is rectification from the mains secondary winding (at the connection G1 and L2). Considerations for choosing the way of supplying the IC are:

- supply voltage range of 5.65 to 11.5 V under all circumstances (also during the 90% pause at normal charging, the standby current then is 1 mA typ.)
- maximum battery voltage (flyback stroke)
- minimum power delivered by the primary SMPS (normal charging)

The supply block delivers the following outputs:

- By using an external resistor R_{ref} at pin 10 (R_{ref}) a reference current is obtained which defines all external related currents (charge reference currents, oscillator).
- Externally available 4.25 V stabilized voltage source (V_s). This source is used internally for a large part of the circuit and can be used to set the NTC biasing and to supply other external circuitry. V_s is cut off in the 90% pause during normal charging.
- Low Supply voltage Protection signal (LSP). When the supply voltage is lower than 5.25 V typ., there is supply voltage enough left to switch off the power regulation and hereafter the IC current is limited to the start level of 35 µA typ.
- Mains on reset pulse resets all digital circuitry after a start or restart due to an interrupted supply (V_p).

harge current regulation

he charge current has to be ensed by means of a low-ohmic esistor in series with diode D1. The aveform on resistor R_s (see Fig.4 or a flyback converter) has the form f a negative-going ramp and after tening a negative DC voltage is otained. Across resistor R1 a ositive voltage is created by means f the current sources set by the ins R_{ref} and R_n. The error amplifier A1 references the result to ground nd via the regulation loop of the MPS, the secondary current will be egulated to a value which is defined y:

$_n \times R_s = R1 \times I_{ref}$ (fast charge) or,
$_n \times R_s = R1 \times I_n$ (normal charge)

he I_{ref} current is the fast charging eference current, the I_n current is sed for regulation after a full attery is detected. The I_{ref} current is he reference current set by R_{ref} while I_n is dependent on the resistor t pin R_n. With no resistor on pin R_n, he I_n current has a default value hich is half the I_{ref} current. By choosing the correct resistor alues R_s, R1, R_{ref} and R_n a wide ange of charge currents can be set s well as a wide range of the ratio ast charge current as a function of ormal charge current. For etermination of the normal charge urrent the 1:10 duty cycle and the rogrammable prescale factor (p) hould be taken into account (see ogic block); $I_n = 1/p \times 0.1 \times I_{ref}$. The utput of amplifier A1 is available at he loop stability pin (LS), so the ime constant of the SMPS loop can e set at the secondary side of the ystem.

NTC block

The voltage at the NTC pin is ompared with two reference oltages. When the NTC voltage is etween V_{rl} and V_{r2}, the charge current regulation is unaffected. When the NTC voltage is outside this window, the power of the SMPS is reduced to the normal charge level.
The NTC input can be used for temperature protection as shown in Fig.3 (application diagram) by using a suitable NTC resistor. To avoid switching on and off with temperature, a hysteresis is built in for both levels.

Output drivers

The SMPS regulation signal is available at different pins:

- Analog voltage output (push or pull) at AO (pin 2) to drive an opto-coupler in mains separated applications when an external resistor is connected between AO and the opto-coupler. The maximum current through the opto-coupler diode is 2 mA. The voltage gain of amplifier A2 is: $A = (V_{LS} - 1.4) \times 4$ and is typ. 12 dB. The voltage at AO can also be used to drive a PWM input of an SMPS circuit directly. During 'Inhibit SMPS' the AO output is fixed to zero charge current for currentless sensing.
- The LS voltage is compared internally with the oscillator voltage to deliver a pulse width modulated output at PWM (pin 1) to drive an output device in a DC/DC converter application via a driver stage. The PWM output is latched to prevent multi-pulsing. Moreover with the latch a kind of current mode control is possible. The maximum duty cycle is internally fixed to 78% (typ.). The 'PWM' output can be used for synchronization and duty cycle control of a primary SMPS via a pulse transformer (the SMPS inhibit and auxiliary pulses are also available at pin PWM).
- The AO and PWM outputs can be changed in polarity by programming the change polarity pin CP. The PWM output in the on-state pushes current (CP = 0) or pulls current (CP = 1). The appearance of the auxiliary pulses at pin PWM can also be programmed with CP.

The 'LED' output pin offers the following output signals:

- 10/90% signal for driving a LED when the duty cycle is too small during the 10% time. This occurs when there is a large difference between fast and normal charge currents. The LED frequency is $f_{LED} = 2^{-12} \times 1/p \times f_{osc}$
- An SMPS inhibit period (duration 10 OSC pulses) for currentless VAC sensing.
- VAC high voltage protection signals.

Battery monitor

At higher battery voltages it is advised to divide the battery voltage with a factor 5 before offering this to pin VAC (Voltage ACcumulator). It is also possible to take a tap on the chain of batteries.
The VAC voltage range has to be between 0.385 V and 3.85 V.
The VAC voltage is sampled at a low cycle frequency ($f_{cycle} = 2^{-16} \times f_{osc}$) and the analog value of VAC is digitized and stored in a register. One cycle later, the digitized value is converted back to the analog value and compared with the actual value of VAC. If the actual value is higher, then the new VAC voltage is stored in the register, otherwise no conversion is done. So the VAC top value is stored and it is possible to detect an increasing VAC indicating 'not yet full batteries' or decreasing VAC indicating that the batteries are probably fully charged.

The circuit waits until the battery voltage has dropped 1% below the top value before indicating 'full batteries'. However, by applying a voltage regulator diode in the battery voltage sense-line (see Fig.7) an increased sensitivity of the –dV detection level can be obtained, e.g. 0.5% or even a lower value.
In Fig.5 the battery voltage as function of the charging time is shown. The negative slope depends on the charge current and is approximately 3 mV/cell/K.

The switching of the SMPS can cause interference on the battery voltage and therefore it has been necessary to stop the SMPS during the inhibit time (see Fig.8). This can be done automatically via the regulation pins AO and PWM or by using the SYNC output of the logic block. The SMPS is stopped for 10 periods at the end of which sampling is done. The VAC voltage will now be sensed currentless. To avoid false decisions concerning a failing VAC voltage, VAC is digitally filtered and analog stored in a sample-and-hold circuit. This approach ensures, even at very high –dV sensitivity (<1%) accurate detection of the battery full condition. Immediately hereafter decisions and VAC digitizing takes place. The benefit of a sample-and-hold circuit is that at high frequencies the noise on the VAC voltage is filtered and the VAC manipulations like decisions and digitizing are done on the same VAC voltage available in the sample-and-hold circuit.

When a –dV is detected, the reference current I_{ref} is switched off, the normal current I_n is switched on during 10% of regulation and the outputs are high-ohmic during 90%. This 1:10 ratio in active regulation, together with the ratio in reference currents (I_n as a function of I_{ref}), ensures that the resulting charge current is low enough to be allowed to flow through the batteries for a long time to overcome the self-discharge of the batteries without causing memory effects. In case the prescale factor p is programmed, the I_n current has to be lowered with the p factor, so $I_n = 1/p \times 0.1 \times I_{ref}$.

Protections

- The circuit goes into standby (not active, low current consumption) when the supply voltage is less than 5.25 V (LSP).
- When the divided battery voltage exceeds the V_{cl} level (nominal 4.25 V) this is recognized as open or removed batteries and the output control signals terminate to stop the SMPS operation. This over-voltage sensing is digitally filtered. In above cases the 'battery full detector' and the 'counter/control' will be reset.
- When the divided battery voltage is less than V_{ss} (0.3 V), the circuit assumes short-circuited batteries, the charge current is reduced to the normal charge level. As soon as the voltage exceeds V_{ss}, the fast charging starts.
- The temperature protections are already mentioned in section NTC. In the case of short-circuited batteries or active temperature protections the 'battery full detector' is reset and the 'counter/control' is stopped.

Oscillator and control logic

The whole timing of the circuit is controlled by the oscillator.
The period time is defined by:
$T_{osc} = 0.93 \times R_{ref} \times C_{osc}$.

The counter block defines a maximum fast charge time called 'Time Out' (TO). As the charge current and the oscillator frequency (and so the TO) are both set by R_{ref}, changing one effects the other. Initially the oscillator capacitor can be chosen such that the fast charge time is half the TO time. This means that in case of a one hour (1C) charger, the TO signal occurs at 2 hours. In case of a quarter of an hour (4C) charger, the TO signal is active after half an hour. After that the circuit switches over to normal charging.

To adapt the SMPS switching frequency in the synchronized mode to the required oscillator frequency of the timing logic, the timer logic is preceded by a programmable divider. By means of the PR pin the divider ratio can be set to 1, 2 or 4 (p factor). Doing so the oscillator frequency can be increased with the factor p without changing TO.

Fast charging current:
$I_{ch} = R1/R_s \times V_{ref}/R_{ref}$
Time out:
$TO = 2^{16} \times 0.93 \times R_{ref} \times C_{osc} \times p$
Normal charging current:
$I_{ch} = R1/R_s \times 1/p \times 0.1 \times V_{ref}/R_n$

The control block determines the following timing sequences:

- VAC sampling; this takes 1 clock pulse every interval cycle.
  The power converter is switched off during VAC sampling. As there are several types of converters, there also are several control signals available at :
  - pin 'SYNC' for synchronization in analog voltage controlled primary SMPS circuits
  - pin 'PWM' for digital controlled primary SMPS and DC/DC converters
  - pin 'LED' in special applications

- Disabling –dV during 2^4 x TO (3% of TO) for proper start with flat or inverse polarized batteries. Disabling is active at each fast charge cycle.
- Maximum fast charging time (TO): the maximum timer is stopped during VAC low voltage protection and outside temperature range.
- The normal charge duty cycle is 1/p x 0.1
- Auxiliary pulses to support the supply voltage of the primary SMPS circuit via pin PWM: the pulses can be programmed on and off at an appearance rate of $f_{osc}/8$ with a duty cycle of 14%; programming is achieved by activating CP.

The timing logic and the –dV recognition circuitry are reset after each supply voltage failure and after a battery over-voltage recognition. The –dV circuit is also reset during normal charging.

The SYNC output delivers negative-going synchronization pulses which are suppressed during the sampling of the battery voltage. With these sync pulses the SMPS can be synchronized. The polarity of the sync pulses is chosen so that in case of an open SYNC pin in the synchronization mode, the power is regulated to a minimum. During the VAC sampling the absense of sync pulses causes the SMPS to stop thus minimizing interference (see Fig.8, synchronization waveforms).

During the 90% pause, only the oscillator and the control logic are operative to save current. In the pause V_p is never allowed to become less than V_{LP}. This would cause a 'mains-on-reset' and so fast charging.

Programming

With pins 'CP' (change polarity) and 'PR' (prescaler) several functions can be programmed.

By defining the current (V_{ref}/R_{CP}) at pin CP, the following functions can be activated :

1	change polarity	CP = 0, normal polarity CP = 1, changed polarity
2	no auxiliary pulses at PWM	aux = 0
3	auxiliary pulses at f/8	aux = 8

CP PIN	FUNCTIONS	
	CP	aux
open pin	0	0
10 µA	0	8
22 µA	1	0
57 µA	1	8

By defining the voltage at pin PR, the following functions can be activated :

PR PIN	FUNCTIONS
V_s	prescaler divide by 1
open pin	prescaler divide by 2
ground	prescaler divide by 4

Formulas

DESCRIPTION	SYMBOL	FORMULA	FUNCTION
timing	T_{osc}	$0.93 \times R_{ref} \times C_{osc}$	repetition
	TO	$2^{16} \times p \times T_{osc}$	duration
	$T_{disable}$	$2^4 \times TO$	duration
	$T_{LED} = T_{measure}$	$2^{12} \times p \times T_{osc}$	repetition
	$T_{LED} = T_{measure}$	$3/4 \times 2^8 \times T_{osc}$	duration
	$T_{inhibit}$	$2^{16} \times T_{osc}$	repetition
	$T_{inhibit}$	$10 \times T_{osc}$	duration
charge currents	I_{fast}	$R1/R_s \times V_{ref}/R_{ref}$	
	I_{normal}	$R1/R_s \times 1/p \times 0.1 V_{ref}/R_s$	

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

All voltages with respect to ground; positive currents flow into the IC; all pins not mentioned in the voltage list are not allowed to be voltage driven. The voltage ratings are valid provided other ratings are not violated; current ratings are valid provided the power rating is not violated.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Voltages					
V_P	positive supply voltage (pin 12)		−0.5	13.2	V
V_{LED}	LED voltage (pin 15)		−0.5	13.2	V
$V_{1,8,4,3}$	voltage at PWM (pin 1), PR (pin 8), LS (pin 4), NTC (pin 3)		−0.5	V_P	V
V_5	voltage at IB (pin 5)		−0.5	−1	V
Currents					
I_{VS}	current at V_S (pin 6)		−3	+0.01	mA
I_{LED}	current at LED (pin 15)		−	25	mA
I_{AO}	current at AO (pin 2)		−5	+5	mA
I_{PWM}	current at PWM (pin 1)		−15	+15	mA
I_{SYNC}	current at SYNC (pin 14)		−2	+2	mA
$I_{11,10,9}$	current at R_{Ω} (pin 11), R_{Ω} (pin 10), CP (pin 9)		−1	+0.01	mA
$I_{4,5,7}$	current at LS (pin 4), IB (pin 5), VAC (pin 7)		−1	+1	mA
I_P	current at V_P (pin 6)		−	15	mA
Dissipation					
P_{tot}	total power dissipation	T_{amb} = 85 °C SOT38G SOT162A	 − −	 0.6 0.3	 W W
Temperatures					
T_{amb}	operating ambient temperature		−20	+85	°C
T_j	junction temperature		−	+150	°C
T_{stg}	storage temperature		−55	+150	°C

HARACTERISTICS

$_{amb}$ = 25 °C; V_P = 10 V; R_{ref} = 33 kΩ; R_n = 68 kΩ; C_{OSC} = 1 nF; CP is open; PR connected to V_S; unless otherwise pecified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (V_P, V_S, R_{ref})						
V_P	supply voltage range		5.65	–	11.5	V
V_{PC}	clamp voltage	I_{PC} = 10 mA	11.5	–	12.8	V
V_{PS}	start voltage		6.1	6.4	6.7	V
V_{PLSP}	low supply protection level		4.85	5.25	5.65	V
V_{PLSPH}	hysterens of V_{PLSP}		0.3	0.95	–	V
I_P	supply current	outputs off	–	–	4.1	mA
I_{PP}	supply pause current	V_P = 6 V	–	–	1.71	mA
I_{PSB}	standby current	V_P = 4 V	–	35	45	µA
V_S	source voltage (stabilized)	I_S = 1 mA	4.03	4.25	4.46	V
V_{ref}	reference voltage	I_{ref} = 20 µA	1.18	1.25	1.31	V
TC_{Vref}	temperature coefficient of V_{ref}	T_{amb} = 0 to 45 °C	–	±100	±200	ppm/K
dV_{ref}/dV_P	power supply rejection ratio (PSRR) of V_{ref}	f = 100 Hz; dV_P = 2 V (peak-to-peak value); V_P = 8 V	–46	–	–	dB
ΔV_{ref}	voltage difference	dI_S = 1 mA	–	–	5	mV
I_{Rrng}	current range of R_{ref}		10	–	100	µA
Charge current regulation (IB, R_n, R_{ref})						
V_n	voltage at pin R_n	I_n = 10 µA; I_{ref} = 20 µA	1.17	1.25	1.32	V
I_n	current range at R_n		5	–	50	µA
I_{IB}/I_{ref}	input current ratio normal charging fast charging	R_n not connected V_{IB} = 0 V_{IB} = 0	 0.475 0.95	 0.5 1	 0.525 1.05	
I_{IB}/I_n	input current ratio normal charging	R_n connected	0.90	0.97	1.04	
V_{thIB}	threshold voltage at IB	T_{amb} = 25 °C T_{amb} = 0 to 45 °C	–5 –7	– –	+5 +7	mV mV
NTC Input						
V_{NTCSPH}	switching protection voltage on high temperatures		0.75	0.81	0.87	V
V_{NTCHH}	hysteresis of V_{NTCSPH}		60	90	120	mV
V_{NTCSPL}	switching protection voltage on low temperatures		2.78	3.00	3.20	V
V_{NTCHL}	hysteresis of V_{NTCSPL}		65	100	135	mV
I_{NTC}	input current	V_{NTC} = 2 V	–5	–	+5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output drivers (AO, LS, PWM, LED)						
$I_{AOsource}$	source current	V_{AO} = 3 V; CP = 0	–	–	−2	mA
I_{AOsink}	sink current	V_{AO} = 0.5 V; CP = 1	2	–	–	mA
g_m	transconductance A1	V_{ia} = 50 mV	–	300	–	µS
G_{v1}	voltage gain A1 x A2	V_{AO} = 2 V (peak-to-peak value)	–	72	–	dB
G_{v2}	voltage gain A2	V_{AO} = 2 V (peak-to-peak value)	–	12	–	dB
$I_{LSsource}$	maximum source current	V_{LS} = 2.25 V	−25	−21	−16	µA
I_{LSsink}	maximum sink current	V_{LS} = 2.25 V	16	21	25	µA
I_{PWMH}	HIGH level output current	V_{PWM} = 3 V	−18	−14	−10	mA
I_{PWML}	LOW level output current	V_{PWM} = 0.5 V	7	12	17	mA
$I_{PWMleak}$	leakage current	V_{PWM} = 4.25 V	–	0.2	10	µA
δ_{PWM}	maximum duty cycle		70	78	86	%
δ_{PWMaux}	auxiliary pulse duty cycle		12.6	14	15.4	%
V_{LEDsat}	saturation voltage	I_{LED} = 15 mA	–	–	600	mV
$I_{LEDleak}$	leakage current	V_{LED} = 10 V	–	–	5	µA
Battery monitor (VAC)						
I_{VAC}	input current	V_{VAC} = 4.25 V	–	1	–	nA
V_{VAC}	voltage range of −dV detection		0.385	–	3.85	V
dV_{VAC}/V_{VAC}	−dV detection level w.r.t. top level	V_{VAC} = 2 V	0.85	1	1.15	%
ΔV_{VAC}	resolution −dV		0.42	0.6	0.78	mV
T_{-dV}	temperature range of −dV detection		0	–	50	°C
Protections (VAC)						
V_{VACLBP}	low battery voltage protection		–	0.3	0.33	V
V_{VACHBP}	high battery voltage protection	with respect to V_p	–	0	150	mV
Oscillator, logic (OSC, SYNCH)						
V_{OSCH}	oscillator switching level HIGH		–	2.5	–	V
V_{OSCL}	oscillator switching level LOW		–	1.5	–	V
K	period time $T_{osc} = K \times R_{ref} \times C_{osc}$		0.84	0.93	1.02	
f_{OSC}	oscillator frequency range		10	–	100	kHz
V_{SYNCH}	SYNC output level HIGH	I_{SYNCH} = −0.4 mA	3.4	–	–	V
V_{SYNCL}	SYNC output level LOW	I_{SYNCL} = 0.4 mA	–	–	0.85	V

TEST AND APPLICATION INFORMATION

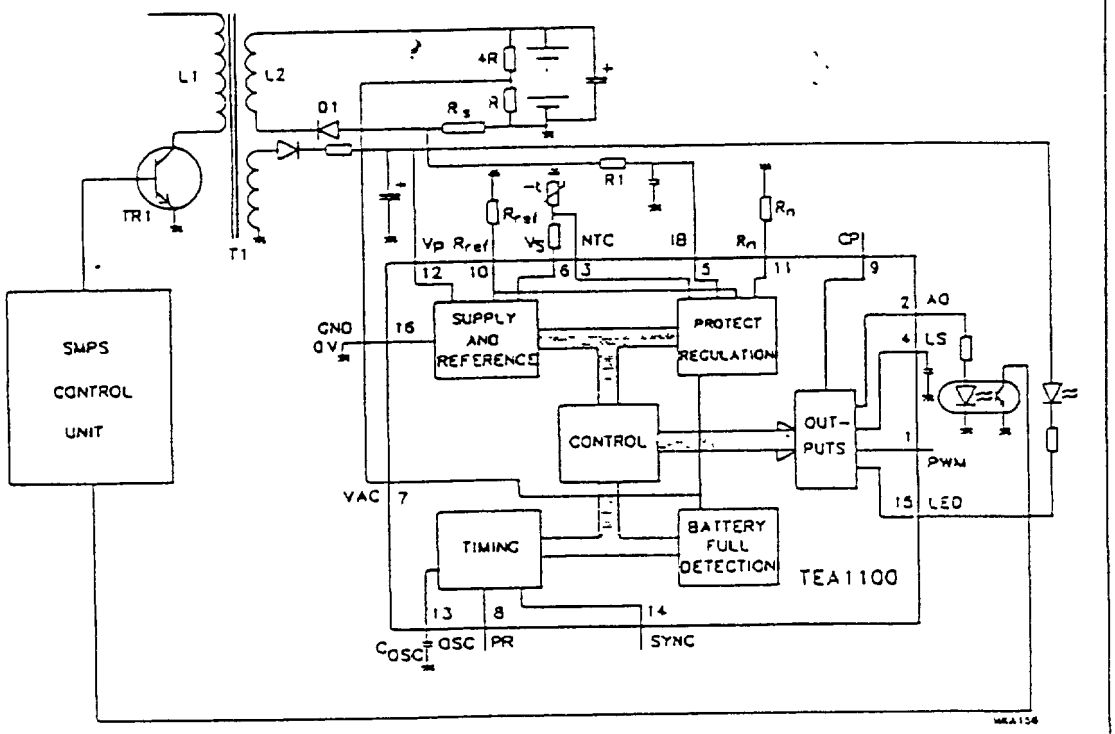


Fig.3 Application diagram.

Notes to Fig.3

1. Signaling the status of the charging session can be done by a LED-diode-resistor combination parallel to L2 (transformer T1). During the fast charging period the LED will burn continuously. During normal charging the LED will switch with the 10/90% rhythm. With mains-off the LED is off, thus not discharging the batteries. If at normal charging the duty cycle is too low during the 10% because of a very large difference between the fast charge and the normal charge levels, the LED can be driven by the LED pin.
2. With R_s = 50 mΩ and a required fast charging current level of 6 A (5C for 1.2 Ah batteries), the average current sense level is 300 mV. Power dissipation in R_s = 1.8 W.
   With a 3 kΩ resistor for R1, the required I_{sense} current is 300 mV/3 kΩ = 100 µA. For a normal charge level of 0.25C (300 mA) the voltage drop over R_s is 15 mV. Taken into account the duty cycle of 10%, the voltage drop over R1 = 150 mV. So the I_{sense} current has to be: 150 mV/3 kΩ = 50 µA (p = 1).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Programming (CP)						
I_{CP}	programming currents					
	CP = 0; aux = 0	R_{CP} = 330 kΩ	–	–	4.2	µA
	CP = 0; aux = 8	R_{CP} = 120 kΩ	9.4	10.4	11.4	µA
	CP = 1; aux = 0	R_{CP} = 56 kΩ	20.0	22.3	24.5	µA
	CP = 1; aux = 8	R_{CP} = 22 kΩ	51.1	56.8	62.5	µA

UALITY SPECIFICATION

eneral quality specification for
ntegrated circuits:
/ZW-B0/FQ-0601.

lemark: for the synchronization pin
14), the ESD positive zap voltage is
estricted to a maximum of 1000 V.

ethod to increase –dV sensitivity

he basic, direct battery sensing via resistive divider, which adapts the attery voltage within the V_{AC} range, shown in Fig.6. Detection occurs : –dV = 1% of $V_{B(max)}$.

he position of the Zener diode is hown in Fig.7. The TEA1100 now enses the voltage V_R, which is the attery voltage minus the ener-diode voltage ($V_R = V_B - V_Z$).

etection occurs at $-dV_R$ = 1% of $_{max}$. This detection corresponds ith a –dV in the battery in ccordance with:

$V_{bat} = (V_Z/V_{B(max)}) - 1$ (in %).

the Zener voltage is half the laximum battery voltage, the dV_B etection will be at –0.5%.

esign example for six-cells' attery and 5% –dV cut-off

onditions:

maximum battery voltage (1.7 V/cell) = 10.2 V

sense network current = 300 µA

maximum monitor sense voltage V_{AC} = 3.6 V (<3.85 V)

or –dV = 0.5%, a Zener voltage of bout half the battery voltage is equired; choose V_Z = 5 V. Now V_R t top level is –5.2 V and the equired divider factor (V_{AC}/V_R) is .69. R1 and R2 become 5.6 kΩ nd 12 kΩ respectively (see Figs 6 nd 7).

uring charge the battery voltage ses with a minimum rate of –8 mV er minute for 6 cells under 1 C harge. The temperature coefficient f the Zener diode and its ambient mperature change should not ause a premature full detection.

Vith the following equation the llowance of the Zener-diode mperature change can be derived:

K/minute < (0.5%($V_B - V_Z$) + (8 mV/minute)|/S_Z

At the early state of charging, V_B = 8.4 V for 6 cells; 0.5% is a safe value for 1% detection in the TEA1100 and V_Z = 5 V.

Assuming a S_Z of +0.5 mV/K (typ. 0.2 mV/K for e.g. Zener diode PLVA450A), this results in maximum 50 K/minute.

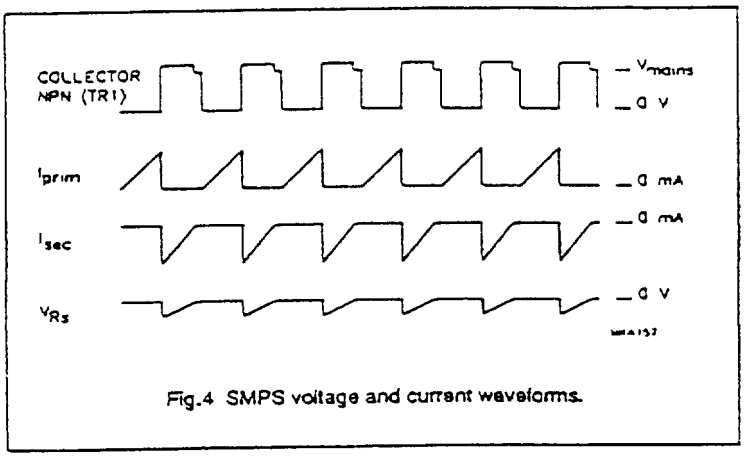


Fig.4 SMPS voltage and current waveforms.

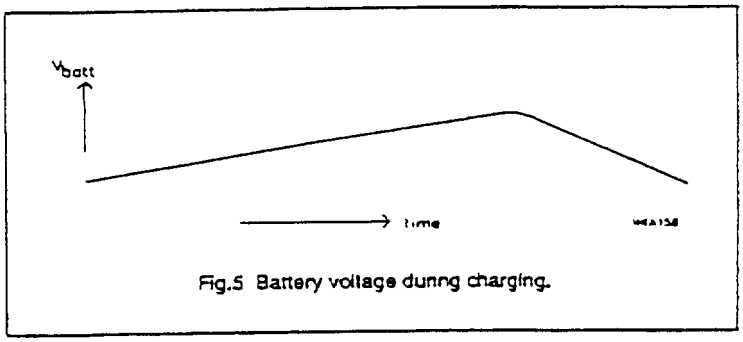


Fig.5 Battery voltage during charging.

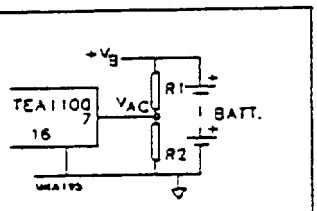


Fig.6 Basic circuit for direct battery sensing.

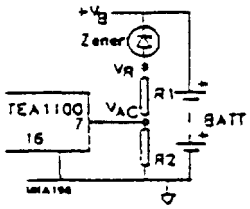


Fig.7 Basic circuit showing the use of a Zener diode.

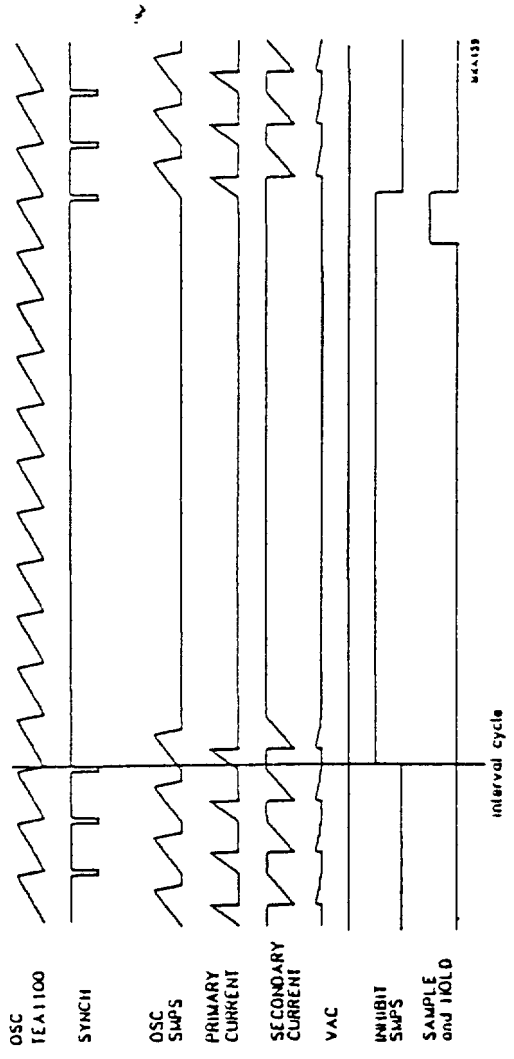
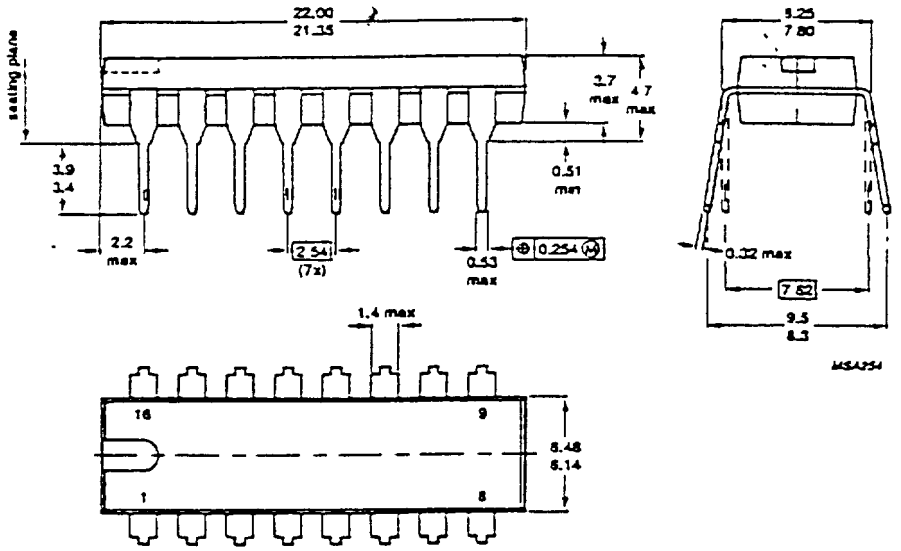


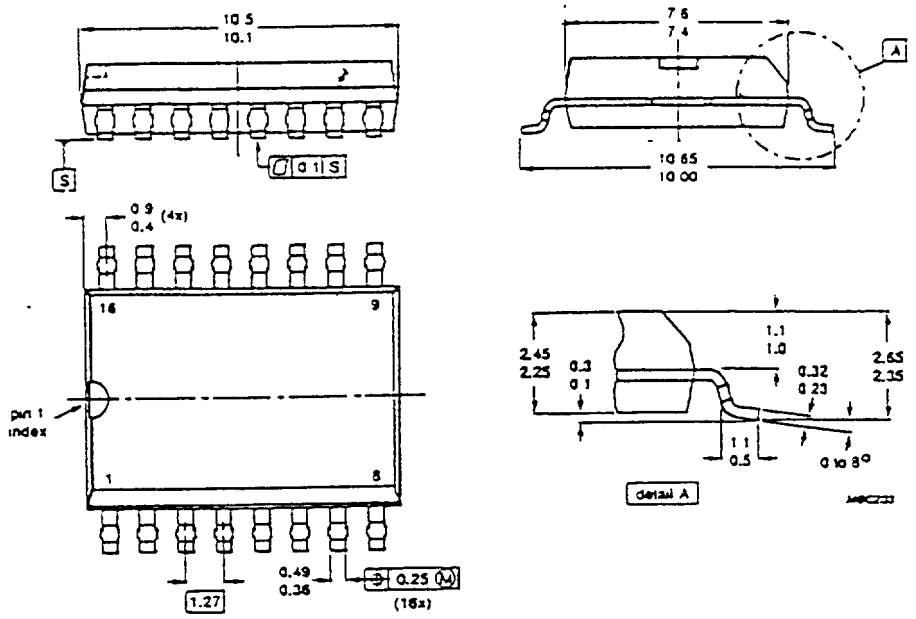
Fig.8 Synchronization waveforms.

ACKAGE OUTLINES



Dimensions in mm.

Fig.9 16-lead dual in-line; plastic (SOT38G).



Dimensions in mm.

Fig.10 16-lead mini-pack; plastic (SO16L; SOT162A).

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REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	